LMH0030 or LMH0031 Control Port Bussed Operation

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Introduction

In systems using multiple LMH0030 serializer and LMH0031 deserializer devices, it is often convenient to connect their ancillary data/control ports to a host controller using a bus network. This reduces the amount of wiring and PCB area required for this function. When designing such a network, it is necessary to understand how the devices are controlled and used in a manner similar to microprocessor peripheral devices.

LMH0030 AD Port

The LMH0030 ancillary/control data port provides read/write access to the device's control data registers. It can also accept parallel ancillary data as input. The port is controlled by three signals: ANC/$\overline{\text{CTRL}}$, RD/$\overline{\text{WR}}$ and A_{CLK}. A_{CLK} serves two distinct functions and works differently in the ANC and CTRL modes. In CTRL-Write mode, A_{CLK} loads control register addresses and data into the device. In CTRL-Read mode, A_{CLK} loads control register addresses and returns the port to address input mode after register output data has been read by the host. In ANC-Write mode, A_{CLK} strobes ancillary data into the device. There is no ANC-Read mode. A_{CLK} is the primary controlling signal affecting device control execution. Each control read or write cycle requires two A_{CLK} cycles for completion.

In the control data mode, when multiple devices are bussed, a means of selecting the particular device to be addressed is needed. Since the LMH0030 and LMH0031 do not have chip-select inputs, controlling access to the control signals provides the means of addressing a particular device on the bus network. The simplest means of controlling access to a particular device uses only A_{CLK}. This is possible since the ANC/CTRL port will not respond unless A_{CLK} is toggled when the port control address or data are valid.

LMH0031 AD Port

The ancillary/control data port of the LMH0031 operates identically to that of the LMH0030 with one exception: There is no ANC-Write mode since the device can only output ancillary data. Bussing the control port functions is the same as described previously.

Multiplexing ACLK as Chip-select

A_{CLK} may be multiplexed to function as a chip-select. The basic logic for doing this is shown in *Figure 1*. This function can be implemented in a variety of ways, of course. The logic can be discrete, a portion of an FPGA or the functions can be incorporated into a microcontroller.

To accommodate situations where it is desired to write the same data simultaneously to all of the LMH0030s or LMH0031s, the multiplexer logic can incorporate a broadcast control function as shown in *Figure 2*. This function saves time by reducing the number of cycles otherwise needed to load the devices individually. The broadcast input overrides the select inputs, S0 and S1. Naturally, this function can only be used to access and write identical information to the same control register in all devices. The broadcast function cannot be used to read simultaneously from all devices as this would cause output drive conflicts.

Multiplexing ACLK as Chip-select (Continued)

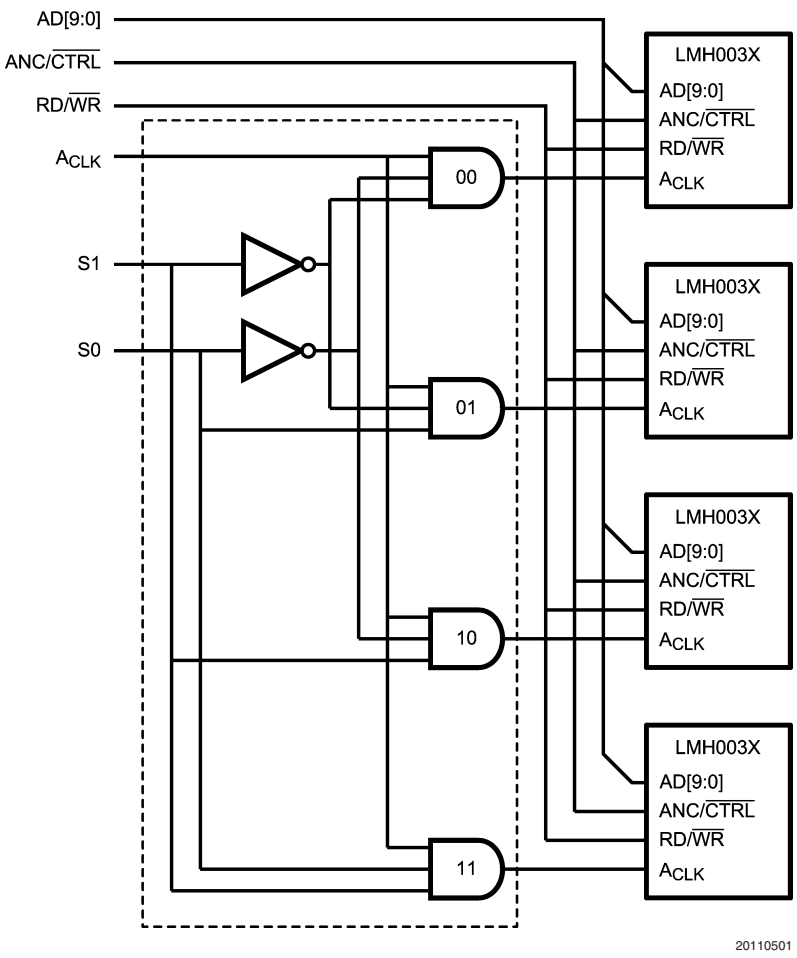

FIGURE 1. A_{CLK} Control Logic

Multiplexing ACLK as Chip-select (Continued)

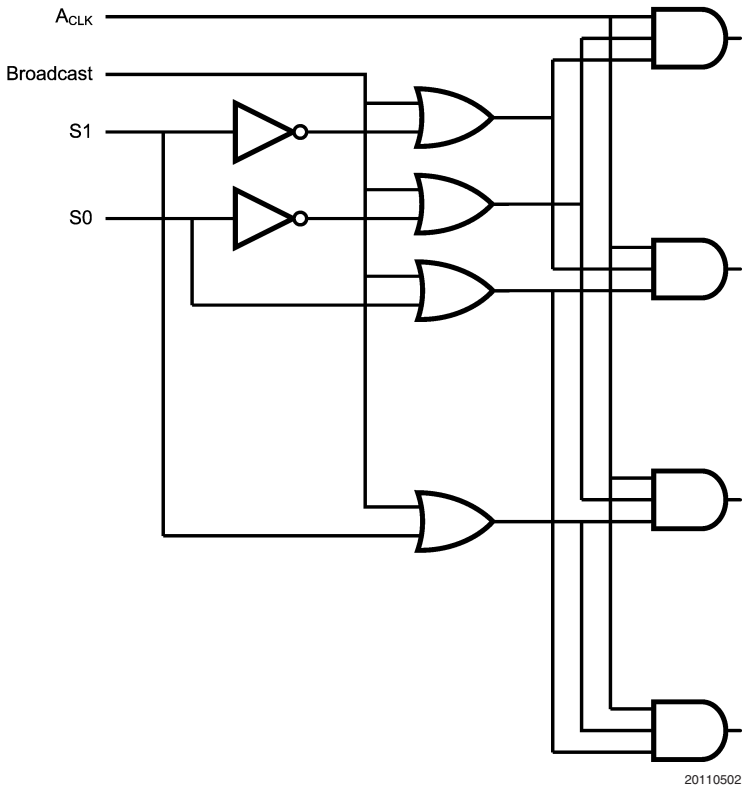

FIGURE 2. A_{CLK} Control Logic with Broadcast Mode

Write and Read Cycle Timing

However the multiplexing function is implemented, it is important to avoid decode glitches which might cause false or multiple A_{CLK} pulses or overlapping A_{CLK} cycles to more than one device. The design of the multiplexer logic must make suitable allowance to assure that the propagation of all select inputs, such as S0, S1 and BROADCAST, to the decoded outputs remains stable from the falling edge of A_{CLK} to the next rising edge which initiates the register address load operation. The select decode process must be completed before A_{CLK} is asserted. For the complete write operation, this is shown in *Figure 3*. Addition of a broadcast function places additional timing constraints on the logic which must be accommodated in the timing margin allowance. The select logic must remain stable during both the register address and the subsequent data read or write operations which comprise the complete access cycle.

Note that the setup and hold times of the AD port data with respect to the rising edge of A_{CLK} are those timing values defined in the data sheet AC Specifications of the respective device.

The write operation begins with an address load cycle. The control inputs ANC/$\overline{CTRL}$ and RD/$\overline{WR}$ are set appropriately. It is recommended that these control signals be changed coincident with the falling edge of A_{CLK}. The multiplexer should be fully stable a suitable time before the rising edge of A_{CLK} and remain stable until after the falling edge of A_{CLK} which ends the data load portion of the operation.

The read operation, *Figure 4*, begins with an address load cycle in the same manner as the write operation. The RD/$\overline{WR}$ control is set to the read mode. Once the register address is strobed into the port, the device driving the port must release the port in order for the device to drive the register's data as output. The data will appear and be driven by the port after an internal propagation delay of about 8.5ns. The port will remain in the output mode until the next rising edge of A_{CLK} releases the port and returns it to the receive mode pending the input of the next register address. Care should be taken to avoid prolonged periods of bus contention between the AD port and external drivers.

Write and Read Cycle Timing (Continued)

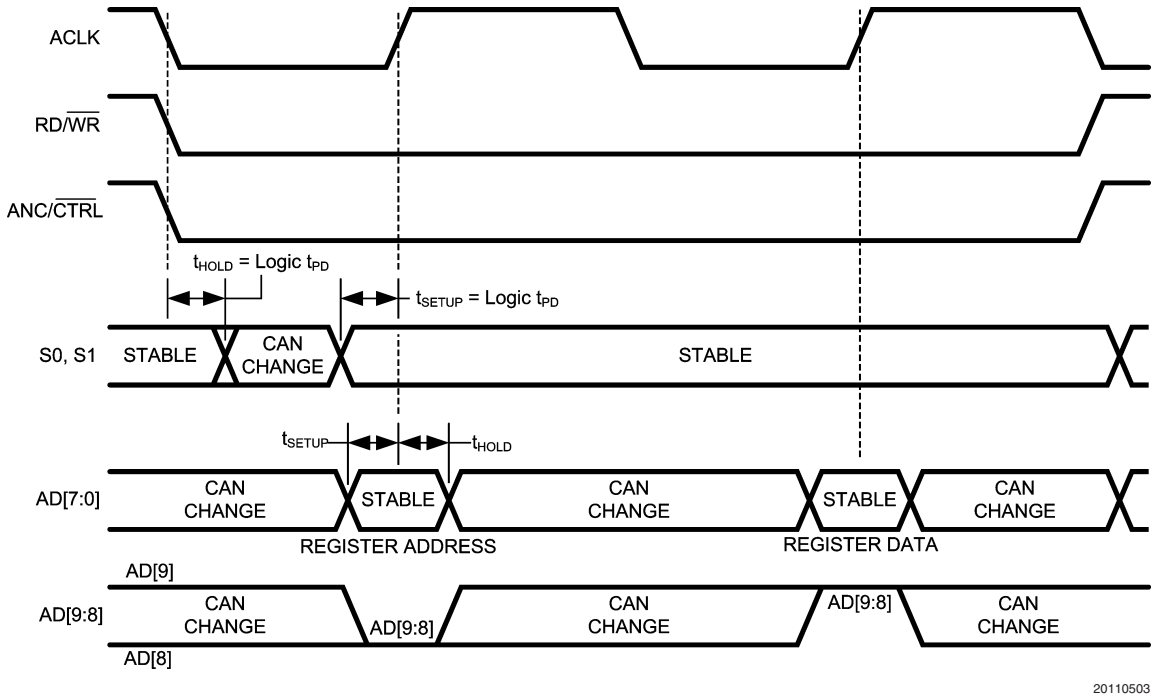

FIGURE 3. Write Cycle Timing Diagram

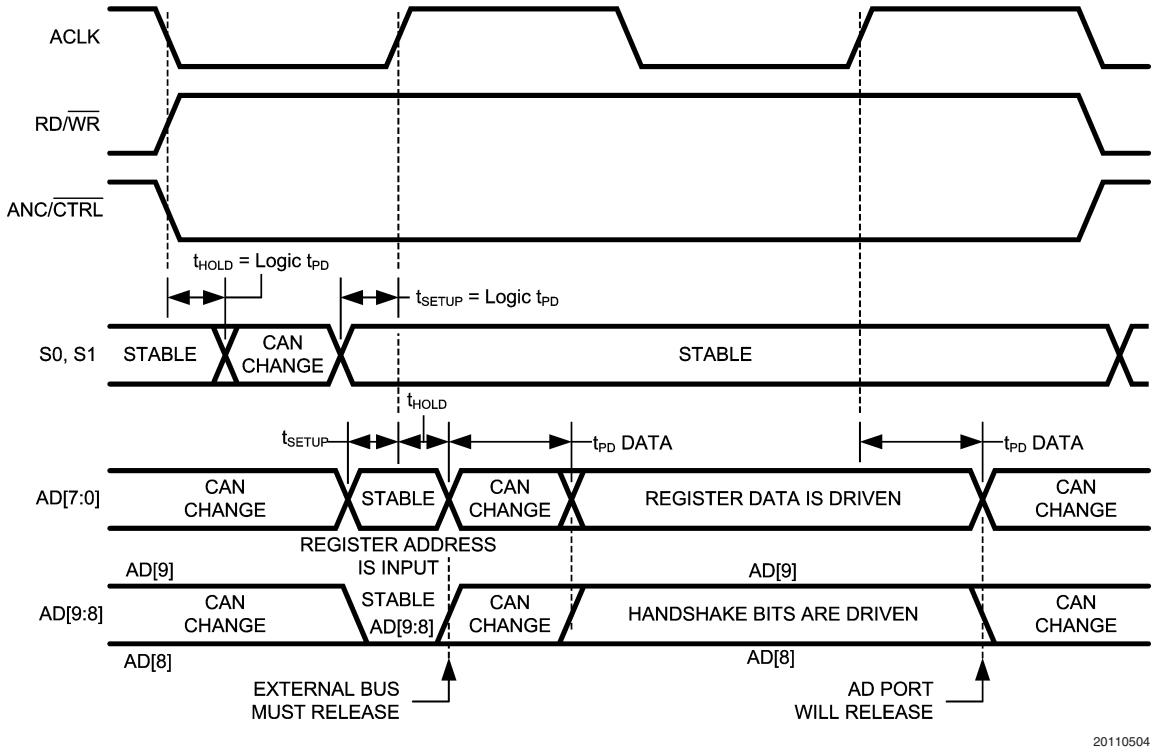

FIGURE 4. Read Cycle Timing Diagram

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