Intel NetStructure® ZT 5524 / MPCBL5524 High-Performance System Master Processor Board

Technical Product Specification

February 2006

Order Number: 273788-009

Contents

Figures

Tables

Revision History

Date	Revision	Description
February 2006	009	Added Section 5.2.3, “IDE HDD Specifications”. Nomenclature changes to add “MPCBL5524”.
February 2005	008	Modified text in Sections 2.3.7, 3.3, and A.3.2.12.
June 2003	007	Removed Build Options from document.
June 2003	006	Updated warranty and customer support information.
February 2003	005	Replaced references to BIOS document.
February 2003	004	Removed references to BIOS document.
November 2002	003	Corrected LED section, CPCI inferface information and console redirection information.
October 2002	002	Removed 800 MHz option from functional block diagram
September 2002	001	First Release of this document

Glossary 1

BMC	Baseboard Management Controller
CIC	CompactPCI Interface Controller
CICBC	CompactPCI Interface Controller B Command
CICBS	CompactPCI Interface Controller B Status
HARST	HA Reset
HCF	Host Control Function
HSPOR	Power-On Reset
IPMI	Intelligent Platform Management Interface
ISAWD1	ISA Watchdog First Stage timeout
ISAWD2	ISA Watchdog Second Stage timeout
MRST	Master Reset
NMI	
P2P	PCI-to-PCI
PCI	Peripheral Component Interconnect
PBRST	Push-button Reset
PCIRST	PCI Reset
PROM	
PWROK	Power OK
RST	Reset
RPIO	Rear Panel Input/Output
S1PBRST	Push-button Reset from the S1 PCI segment
SEL	System Event Log
SMM	System Management Mode

Introduction 2

This chapter provides a brief introduction to the Intel® NetStructure™ ZT 5524 / MPCBL5524 System Master Processor Board. Included in this chapter:

- Product definition
- List of product features
- ZT 5524 / MPCBL5524 Faceplate figure
- ZT 5524 / MPCBL5524 Functional Block Diagram and a description of each block

Unpacking, initial board configuration, and other setup information are provided in Chapter 3, "Getting Started".

2.1 Product Definition

The ZT 5524 / MPCBL5524 is a 6U, PICMG* 2.16 Version 1.0 compliant CompactPCI* processor board featuring single or dual Low Voltage Intel® Pentium® III processor(s). The ZT 5524 / MPCBL5524 supports one 64-bit CompactPCI bus at 66 MHz or 33 MHz using the Intel® 21154-BE PCI-to-PCI bridge. When the ZT 5524 / MPCBL5524 is used in conjunction with the Intel NetStructure® ZT 4901 Bridge Mezzanine board, the two cards can bridge two 64-bit CompactPCI buses at 33 MHz.

The ZT 5524 / MPCBL5524 can be used in several configurations:

- Redundant System Master
- CompactPCI-to-CompactPCI bridge
- Stand-alone processor board supporting either a maximum of seven CompactPCI peripheral cards at 33 MHz or five CompactPCI peripheral cards at 66 MHz
- Node Board in a CompactPCI Packet Switching Backplane (compliant with the CompactPCI Specification, PICMG 2.16, Version 1.0)

The Pentium III processor(s) on the ZT 5524 / MPCBL5524 provide optimum performance in uniprocessor or multiprocessor systems. The board occupies one CompactPCI slot (4HP) and comes with either one or two Pentium III processors installed. Additionally, the ZT 5524 / MPCBL5524 supports hosting hot swap peripherals in a powered system.

The on-board Baseboard Management Controller (BMC) chip from Intel monitors, controls, and performs remote diagnostics for many on- and off-board functions through six IPMI (Intelligent Platform Management Interface) compliant system management bus interfaces.

Intel's Redundant Host architecture can support redundant ZT 5524 / MPCBL5524 processor boards in a single Redundant System Slot enclosure such as the Intel NetStructure® ZT 5085 Redundant System Slot Chassis. Resource management and database information can be synchronized between the processor boards via a 100Mbps Ethernet communications channel.

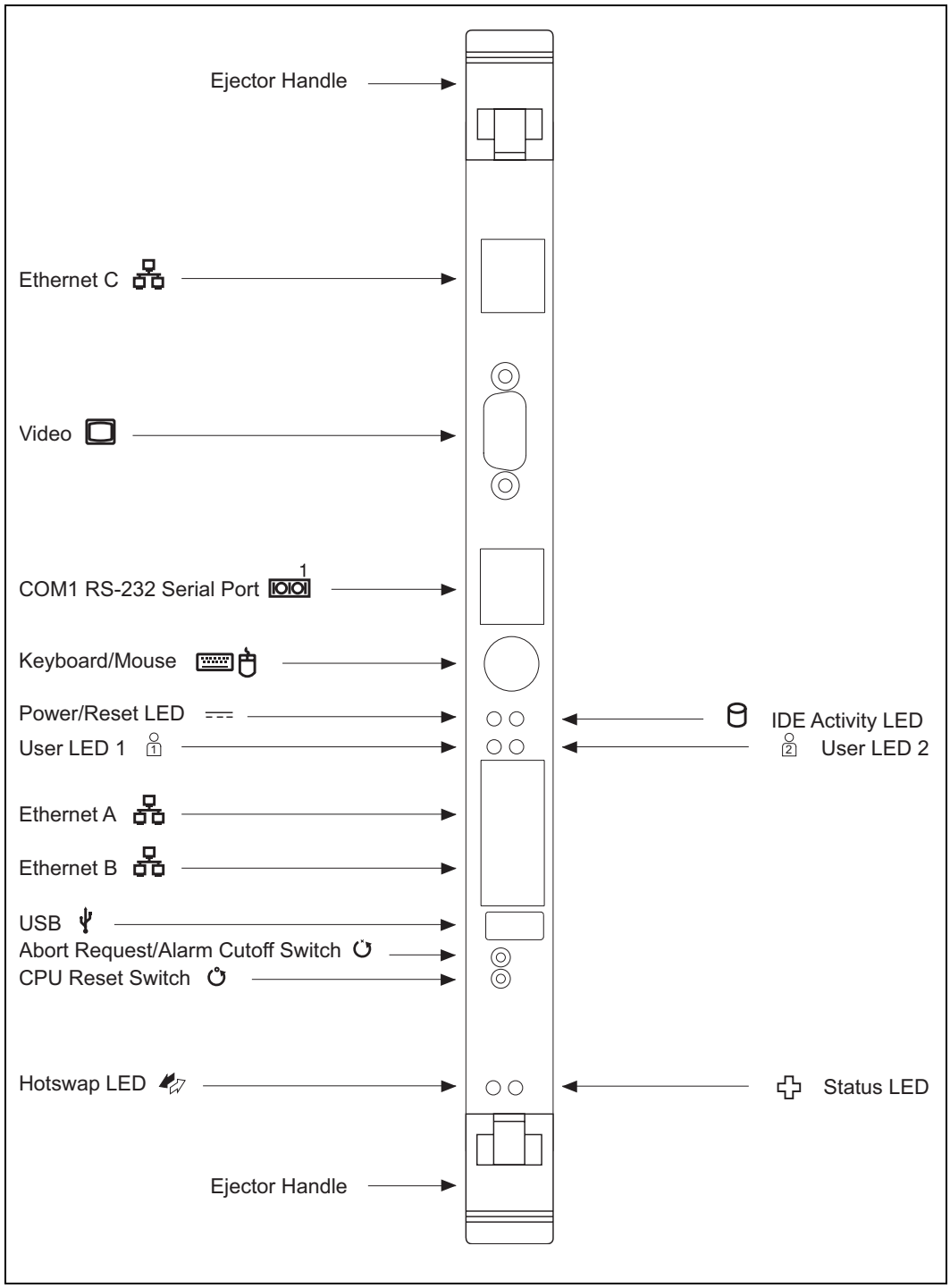
Optional ZT 4901 Bridge Mezzanine boards on both processor boards provide Redundant Host (RH) functionality, dual 2Gbit Fibre Channels, dual 64/66 PMCs, and access to a second CompactPCI bus segment.

2.2 ZT 5524 / MPCBL5524 Features

- CompactPCI System Master
- CompactPCI Specification, PICMG 2.0, Version 2.1 compliant
- CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0 compliant
- CompactPCI Specification, PICMG 2.16, Version 1.0 compliant
- Single or dual Low Voltage Intel Pentium III processors (133 MHz FSB)
- Integrated 512 KByte ECC L2 cache
- Occupies one 6U CompactPCI slot
- ServerWorks Champion LE-T* Chipset
  - ServerWorks Champion North Bridge* (CNB30LE-T)
  - ServerWorks Champion South Bridge* (CSB5)
- PCI video (Chips and Technologies 69000 HiQVideo* Accelerator with Integrated Memory), with 2 MB SDRAM
- Dual 10/100/1000 Mbit/s Ethernet interfaces
- Single 10/100 Mbit/s Ethernet interface
- Supports 64-bit PCI memory-to-memory transfers
- One 168-pin, right angle, dual inline memory module socket (Maximum Memory supported is 1GB. For other memory configurations, contact Intel Corporation).
- Intel NetStructure® Embedded BIOS (AMI core) stored in local flash memory
- Standard AT* peripherals include:
  - Two enhanced interrupt controllers (8259)
  - Three counter/timers (one 8254)
  - Real-time clock/CMOS RAM (146818)
  - Two enhanced DMA controllers (8237)
  - 8042 compatible keyboard controller
  - One primary IDE channel/one secondary IDE channel
  - Two 16C550 RS-232 serial ports
  - Floppy disk controller
  - Speaker interface (rear panel only)
  - Three USB ports
  - PC/AT keyboard/mouse controller

- Dual-stage watchdog timer
- Push-button Reset/Abort switches
- LEDs:
  - — Status (Green/Amber)
  - — Two User (Green/Amber/Off)
  - — Local IDE Disk Activity (Green/Off)
  - — Hot Swap (Blue/Off)
  - — Power/Reset (Green/Amber/Off)
  - — Ethernet C:
    - •10/100 (Off/Green)
    - •Link (Green)
    - •Activity (Flashing Green)
  - — Ethernet A and B:
    - •10/100/1000 (Off/Green/Amber)
    - •Link (Green)
    - •Activity (Flashing Green)
- Six SMBuses (Local)

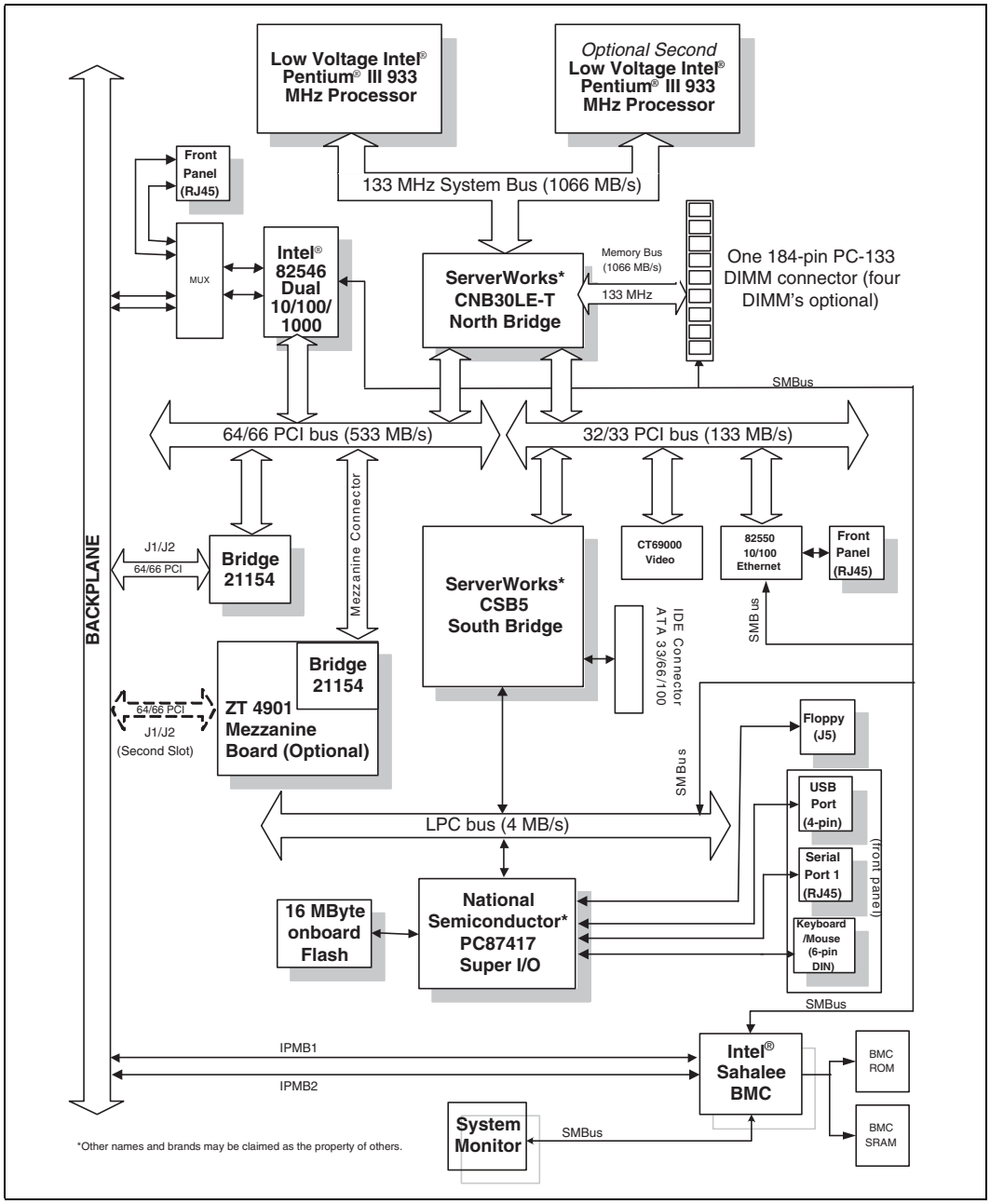
Figure 1. ZT 5524 / MPCBL5524 Faceplate



2.3 ZT 5524 / MPCBL5524 Functional Blocks

Below is a functional block diagram of the ZT 5524 / MPCBL5524. The following topics provide overviews of the functional blocks.

Figure 2. ZT 5524 / MPCBL5524 Functional Block Diagram



2.3.1 Intel® Pentium® III Processor

The ZT 5524 / MPCBL5524 features either one or two Low Voltage (LV) Intel Pentium III 512 KByte processor(s). The Pentium III processor is a small, highly integrated assembly containing an Intel Pentium processor and its immediate system-level support. The Pentium III processor includes 32 KBytes of code and data cache (L1 cache), a secondary 512 KByte cache (ECC L2 cache), and the core logic required to bridge the processor to the standard system buses. It also features a 133MHz system bus frequency.

Appendix E, "Pentium III Processor," contains a link to the datasheet for this device.

2.3.2 Chipset

The ZT 5524 / MPCBL5524 incorporates the ServerWorks* Champion* LE-T chipset. The Champion LE-T chipset consists of the ServerWorks Champion North Bridge (CNB30LE-T) and the ServerWorks Champion South Bridge (CSB5) chips.

2.3.2.1 ServerWorks* Champion North Bridge (CNB30LE-T)

The CNB30LE-T provides an optimized, integrated DRAM controller, bus-control signals, address paths, and data paths for transfers between the processor's host bus, the PCI bus, and main memory. The CNB30LE-T also features:

- Processor interface control
- Data buffering
- Power management functions
- SMBus support for desktop management functions
- Support for system management mode (SMM)
- Glueless Serial interface with CSB5

2.3.2.2 ServerWorks Champion South Bridge (CSB5)

The ZT 5524 / MPCBL5524 I/O subsystem is based on the CSB5. The CSB5 is a multifunctional PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The CSB5 South Bridge features:

- Multifunctional PCI-to-LPC Address / Data bridge
- PCI Slave, PCI Arbiter, and PCI Master
- LPC bus support and LPC Arbiter
- One 8253 Counter/Timer
- Client Management
- Support for the PCI bus at 33 MHz
- Support for PCI Rev 2.1 Specification
- Integrated dual-channel enhanced IDE interface
- Enhanced DMA controller
- Interrupt controller based on 82C59

- Power management logic
- Internal APIC Controller
- USB Interface
- SMB bus interface
- Glueless Serial interface with the CNB30LE-T
- 16-bit counters/timers based on 82C54

Appendix E, "Chipset," contains a link to more information for this device.

2.3.3 CompactPCI Bus Interface

The ZT 5524 / MPCBL5524 processor board uses the CNB30 chipset and the Intel 21154-BE PCI-PCI Bridge to support 32-bit and 64-bit CompactPCI interfaces. ZT 5524 / MPCBL5524 supports up to two 64-bit CompactPCI buses at 33 MHz in RH Mode and either 33 MHz or 66 MHz in Standard Mode.

One of the two CompactPCI buses is located on the processor board. The primary side of the bridge is connected to the CNB30s 66 MHz, 64-bit PCI bus. The secondary sides of the bridge are connected to the CompactPCI interface (backplane connectors J1 and J2, see Appendix A, "ZT 5524 / MPCBL5524 Connectors,").

The second Compact PCI bus is located on the optional ZT 4901 Mezzanine board. The primary side of this bridge is connected to the CNB30s 66 MHz, 64-bit PCI bus via a high-speed connector to maintain signal quality. The secondary side of the bridge is connected to the PCI devices on the ZT 4901 (Fibre Channel, PMC, P2P bridge) and is connected to the CompactPCI backplane through a third PCI-to-PCI bridge.

The ZT 5524 / MPCBL5524 is designed to be used as a Redundant System Master in a single or multiprocessor system, or as a stand-alone processor board in a 6U CompactPCI system. The ZT 5524 / MPCBL5524 is also compliant with the *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, Version 1.0*. The board occupies one CompactPCI slot (4HP) with one or two Pentium III Processors installed.

When used in a hot swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*, the ZT 5524 / MPCBL5524 supports hosting hot swap peripherals in a powered system. The ZT 5524 / MPCBL5524 can also function in a standard (non-hot swap) CompactPCI system. Appendix E, "Data Sheet Reference" contains links to the "CompactPCI*" Specification, the CompactPCI Packet Switching Backplane Specification, and the CompactPCI Hot Swap Specification.

For more information on Hot Swap implementation, refer to the Intel NetStructure® Hot Swap Kit Software Manual. To locate this document, see Appendix E, "User Documentation."

2.3.4 PCI-to-PCI Bridge

The ZT 5524 / MPCBL5524 features one Intel 21154-BE PCI-to-PCI bridge to support the J1/J2 CompactPCI bus. The bridge provides the isolation, arbitration, and clocks for seven CompactPCI peripheral cards at 33 MHz or five CompactPCI peripheral cards at 66 MHz, all bus masters, without the need for an external-bridge board.

Special features of the 21154-BE include:

- Support for independent primary and secondary PCI clocks
- 64-bit PCI operation
- 33 MHz or 66 MHz PCI bus operation

A link to the datasheet for this device is listed in Appendix E, “Data Sheet Reference”. See Appendix A, “ZT 5524 / MPCBL5524 Connectors” for information on ZT 5524 / MPCBL5524 CompactPCI connectors.

2.3.5 Baseboard Management Controller

The ZT 5524 / MPCBL5524 includes a Baseboard Management Controller (BMC) chip from Intel. The BMC subsystem monitors, controls, and performs remote diagnostics for many on- and off-board functions through six IPMI compliant system management bus interfaces.

The BMC monitors system sensors for system management events, such as overtemperature, out-of-range voltages, fan failures, etc., and logs any occurrences in its non-volatile System Event Log (SEL). The BMC also provides the interface to the sensors and SEL so system management software can poll and retrieve the present status of the system.

The ZT 5524 / MPCBL5524 is compliant with standard *Intelligent Platform Management Interface v1.5 Specification* functionality. Optional IPMI functionality addressed in the specification is not supported. See Appendix E, “Intelligent Platform Management Interface (IPMI)” for more information.

2.3.6 Redundant Host Operation

Intel’s High Availability architecture features two Redundant Host ZT 5524 / MPCBL5524 processor boards with ZT 4901 Bridge Mezzanine boards in a single PICMG 2.16 compliant High Availability enclosure such as the Intel NetStructure® ZT 5085 12U Redundant Host Packet Switched Platform. Resource management and database information can be synchronized between the processor boards via 100Mbps Ethernet communications channel C (available on each ZT 5524 / MPCBL5524 Faceplate at J11. For more information, see Figure 1 on page 13).

The ZT 5524 / MPCBL5524 contains one CompactPCI segment and associated control logic. The optional ZT 4901 Bridge Mezzanine board contains a second segment and its associated control logic.

PCI-to-PCI (P2P) bridges provide the interface to the two CompactPCI bus segments. The CompactPCI Interface Controller (CIC) on the host processor board controls these bridges as directed via several configurable registers. The CIC isolates the bus segments controlled by each processor board from the other processor board. Arbitration of the CompactPCI buses is provided by additional logic on the host processor board.

Note: See Appendix B, “System Registers,”for specific information.

When a fault is detected, the configuration of the appropriate register determines whether it reports a Minor, Major, or Critical fault. The register can be configured to indicate a failure due to any of the following events:

- Master Reset (MRST) from the BMC power monitor and self-reset

- Power-On Reset (HSPOR) from the Hot Swap Controller
- Power OK (PWROK) from the last stage power monitor
- PCI Reset (PCIRST) from PCI Bus 0
- HA Reset (HARST) from the redundant Host
- Push-button Reset (S1PBRST) from the S1 PCI segment
- Push-button Reset (PBRST) from the front or rear panel push-button
- CPU Initialization CPU INIT from the CSB5
- ISA Watchdog First Stage timeout (ISAWD1)
- ISA Watchdog Second Stage timeout (ISAWD2)
- BMC Watchdog
- Over Temperature
- SERR#, NMI, PERR#, ECC-Error
- Software Command
- BMC Fault

For more information about Intel's High Availability architecture and development of Redundant Host drivers, refer to the *Redundant Host Software Development Kit for Intel NetStructure CompactPCI System Master Processor Boards Software Manual*. See Appendix E, "User Documentation." for information on locating this document.

2.3.7 Memory

The ZT 5524 / MPCBL5524 includes one 168-pin, right angle, dual inline memory module (DIMM) socket allowing for memory population up to 1 GByte. The ZT 5524 / MPCBL5524 has four DIMM sockets and can support total memory of 4 GBytes. Using the serial presence detect (SPD) data structure programmed into an E2PROM on the DIMM, the ZT 5524 / MPCBL5524 BIOS can determine the SDRAM's size and speed.

The CPU board supports DIMMs that meet the following requirements:

- 168-pin, PC 133 registered DIMMs, 72-bit ECC, 3.3 V
- Single- or double-sided DIMMs
- 168-pin, registered SDRAM (with register and PLL)
- Maximum PCB height 1.2 inches
- Serial presence detect
- Gold plated contacts
- PC133 compliant
- CL3 (cas latency = 3 clocks @133 MHz)
- 8 KByte refresh (every 64ms)
- Auto- and self-refresh capable

All memory components and DIMMs used with the ZT 5524 / MPCBL5524 must comply with the following PC SDRAM specifications:

- *PC SDRAM Specification* (memory component specific)
- *PC SDRAM Registered DIMM Specification*

Note: Double-stacked DIMMs may be used only if they are within the 7.0 mm maximum thickness imposed by the 0.3 DIMM socket spacing on the processor board.

Refer to the *ZT 5524 / MPCBL5524 Compatibility Report* available on the Intel website for a complete list of compatible memory types. For more information, see Appendix E, "ZT 5524 / MPCBL5524 Product Page."

2.3.8 Flash/BIOS Recovery

The ZT 5524 / MPCBL5524 incorporates 16 MBytes of on-board, programmable, BIOS Flash memory. The BIOS resides in the first megabyte of flash. The FLASH.EXE utility allows you to install an operating system image or any executable image into the remaining 15 MBytes of flash. See the *Intel NetStructure Embedded BIOS Software Manual* for more information. See Appendix E, "User Documentation." for information on locating this document.

A second flash device is used as a BIOS recovery module. The ZT 5524 / MPCBL5524 can be configured to use either device for boot control. When booting from the BIOS recovery module, the BIOS update utility can access the onboard flash device by manipulating the system registers as described in Appendix B, "System Registers." The onboard flash is write protected on power up and reset. See Chapter 7, "BIOS Recovery," for more information.

2.3.9 Mezzanine Interface

The ZT 5524 / MPCBL5524 is available with the optional ZT 4901 mezzanine board. The ZT 4901 is a 6U mezzanine that provides Redundant Host (RH) functionality, dual Fibre Channel, dual 64/66 PMC, and access to a second CompactPCI bus segment for bridging.

Intel designed the ZT 4901 to be used as a Redundant System Master for one or two bus segments, a CompactPCI Bridge to a second CompactPCI bus segment, or as a standalone, add-on peripheral mezzanine to the ZT 5524 / MPCBL5524. The CompactPCI bus interface supports a maximum of seven CompactPCI peripheral cards at 33 MHz, or 5 peripheral slots in a 66 MHz system. See the Intel NetStructure ZT 4901 Mezzanine Expansion Card Technical Product Specification for more information. A link to this document is available in Appendix E, "User Documentation.".

The mezzanine interface is at J17 on the ZT 5524 / MPCBL5524. See Appendix A, "ZT 5524 / MPCBL5524 Connectors" for more information.

2.3.10 Power Ramp Circuitry

The ZT 5524 / MPCBL5524 features a hot swap controller with power ramp circuitry that enables the board's voltages to ramp in a controlled fashion. The power ramp circuitry eliminates any large voltage or current spikes caused by removing or inserting hot swappable boards while the system is still under power. This controlled ramping is a requirement of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*.

The ZT 5524 / MPCBL5524's hot swap controller unconditionally resets the board when it detects that the 3.3 V, 5 V, and 12 V supplies are below an acceptable operating limit. These limits are defined as 4.75 V (5 V supply), 3.0 V (3.3 V supply), and 10.0 V (+12 V supply).

Fault current sensing is also provided. If a board fault (short circuit) or over-current condition is detected, the hot swap controller automatically removes power from the ZT 5524 / MPCBL5524 components and the Status LED turns amber.

2.3.11 Reset

The ZT 5524 / MPCBL5524 provides the following reset types:

- Push-button reset
- Backplane reset input (J2 pin C17)
- Watchdog timer reset

See Appendix C, "Reset," for more information.

2.3.12 Two-Stage Watchdog Timer

The Watchdog Timer is an optional feature that monitors system operation and is programmable for one of eight different timeout periods (from 0.25 s to 256 s). It is a two-stage watchdog, meaning that it can be enabled to produce an NMI interrupt before it generates a system reset. Failure to strobe the Watchdog Timer within the programmed time period may result in an NMI interrupt, a system reset, or both.

A register bit is set if the watchdog timer caused the reset event. This Watchdog Timer is cleared on power-up, enabling system software to take appropriate action on reboot. It is not cleared on reset

See Chapter 6, "Watchdog Timer,"for more information.

2.3.13 DMA

On-board peripherals can make use of the two enhanced 8237-style DMA controllers.

DMA channel 2 is assigned to the optional floppy drive.

The ZT 5524 / MPCBL5524's DMA controllers reside in the ServerWorks CSB5 South Bridge chipset. A link to the datasheet for this device is available in Appendix E, "Chipset."

2.3.14 Interrupts

Two enhanced 8259-style interrupt controllers provide the ZT 5524 / MPCBL5524 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/timers
- Serial I/O
- Real-time clock
- Keyboard
- IDE interface
- Digital I/O
- CompactPCI backplane (21154)
- On-board PCI devices
- Floppy disk

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The ZT 5524 / MPCBL5524's interrupt controllers reside in the ServerWorks Chipset's CSB5. A link to the datasheet for this device is available in Appendix E, "Chipset."

2.3.15 Enhanced IDE Controller

The ZT 5524 / MPCBL5524 features an IDE controller that supports onboard and optional external IDE drives. ATA-66 is supported on the primary IDE channel, allowing up to 66 MBps throughput. ATA-33 is supported on the secondary IDE channel, allowing up to 33 MBps throughput.

Primary channel IDE signals are available through internal connector J19. These signals are also available at the J17 mezzanine board interface. Secondary channel IDE signals are available through rear-panel I/O connector J5. See Chapter 5, "IDE Interface," for more about the ZT 5524 / MPCBL5524's IDE support.

The ZT 5524 / MPCBL5524's IDE controller resides in the ServerWorks Chipset's CSB5. A link to the datasheet for this device is available in Appendix E, "Chipset.". Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

2.3.16 Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a common interface to slower-speed peripherals. Functions such as keyboard, serial ports, and mouse ports can be consolidated into USB, simplifying cabling requirements.

The ZT 5524 / MPCBL5524 supports booting from a USB CD-ROM or floppy device. Refer to the *ZT 5524 / MPCBL5524 Compatibility Report* available on the Intel website for a complete list of validated CD-ROM and floppy drives. A link to this website is available in the section Appendix E, "ZT 5524 / MPCBL5524 Product Page."

The ZT 5524 / MPCBL5524 supports USB v1.1. A USB port (Port 0) is directed to faceplate connector J6. Two more USB ports (Port 1 and Port 2) are directed through the ZT 5524 / MPCBL5524's RPIO connector J5.

The ZT 5524 / MPCBL5524's USB resides in the ServerWorks Chipset's CSB5 South Bridge. A link to the datasheet for this device is available in Appendix E, "Chipset."

Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

2.3.17 Counter/Timers

Three counter/timers as defined for the PC/AT* are included on the ZT 5524 / MPCBL5524. Operating modes supported by the counter/timers include:

- Interrupt on count
- Frequency divider
- Square wave generator
- Software triggered
- Hardware triggered
- One shot

The ZT 5524 / MPCBL5524's 8254-compatible counter/timer resides in the ServerWorks Chipset's CSB5. A link to the datasheet for this device is available in Appendix E, "Chipset."

Two counter/timers reside in the National Semiconductor* PC87417 I/O controller. A link to the datasheet for this device is available in Appendix E, "I/O Controller."

2.3.18 Floppy Controller

The ZT 5524 / MPCBL5524 includes a standard floppy disk controller. The floppy disk controller supports an optional external floppy drive that is compatible with an 82077 diskette drive controller and supports both PC-AT* and PS/2 modes. Floppy signals are available through the RPIO connector J5.

The ZT 5524 / MPCBL5524's floppy disk controller resides in the National Semiconductor PC87417 I/O controller. A link to the datasheet for this device is available in Appendix E, "I/O Controller." Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

Note: Floppy disks are magnetically recorded media. Avoid placing floppy disk drives near magnetic sources such as power supplies.

2.3.19 Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of battery-backed CMOS RAM in two banks that are reserved for BIOS use. Timekeeping features include a time-of-day clock and a multi-century calendar with alarm features and century rollover. The clock is accurate to ± 13 minutes/year at 25º C. The time, date, and CMOS values can be specified or returned to their defaults by using the BIOS Setup program. See Chapter 3, "Getting Started," for more information.

Note: The recommended method of accessing the date in systems with Intel processor boards is indirectly from the real time clock via the BIOS. The BIOS on Intel processor boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the real time clock during each BIOS request (INT 1Ah) to read the date and, if less than

80 (1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

A coin-cell battery located on the ZT 5524 / MPCBL5524 processor board powers the real-time clock and CMOS memory. When the ZT 5524 / MPCBL5524 is not powered externally, the battery has an estimated life of six years. When the ZT 5524 / MPCBL5524 is powered up, the 3.3 V backplane current from the power supply extends the life of the battery.

The ZT 5524 / MPCBL5524's real-time clock resides in the National Semiconductor PC87417 I/O controller.A link to the datasheet for this device is available in Appendix E, "I/O Controller."

2.3.20 Speaker Interface

For external speaker interfacing, the ZT 5524 / MPCBL5524 supports an external AT-compatible speaker through the RPIO connector J5. Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

2.3.21 Serial I/O

The ZT 5524 / MPCBL5524 provides two 16C550, PC-compatible serial ports:

Faceplate: COM1 via RJ-45 connector J9

Rear Panel: COM1 and COM2 via RPIO connector J5

Both ports are compatible with RS-232 signaling levels and supports data transfers at speeds up to 115.2 Kbits/sec with BIOS support.

The ZT 5524 / MPCBL5524's serial controller resides in the National Semiconductor PC87417 I/O controller. A link to the datasheet for this device is available in Appendix E, "I/O Controller." Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

2.3.22 Keyboard/Mouse Controller

The ZT 5524 / MPCBL5524 includes an on-board PC/AT keyboard/mouse controller. Keyboard and mouse signals are available at the faceplate via J8. A "Y" interface cable is required to use both interfaces at once. The keyboard and mouse signals are also available through the RPIO connector J5. For a diagram of the faceplate, see Figure 1, "ZT 5524 / MPCBL5524 Faceplate" on page 13.

The ZT 5524 / MPCBL5524's keyboard/mouse controller resides in the National Semiconductor PC87417 I/O controller. A link to the datasheet for this device is available in Appendix E, "I/O Controller." Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

2.3.23 PCI Video

The ZT 5524 / MPCBL5524 provides on-board video using the Chips and Technologies* 69000 HiQVideo Accelerator with Integrated Memory video device configured as a PCI device. The PCI bus supports 32 bits of data and runs at a speed of 33 MHz, giving it a theoretical bandwidth of 133 MB/s. The 69000 provides support for display resolutions up to 1024 x 768.

The 69000 incorporates 2 MB of integrated SDRAM for the graphics/video frame buffer. The integrated SDRAM memory can support up to 83 MHz operation, thus increasing the available memory bandwidth for the graphics subsystem.

VGA-compatible video signals are available at the ZT 5524 / MPCBL5524 faceplate via connector J10 and also at rear-panel I/O connector J5. For a diagram of the faceplate, see Figure 1, “ZT 5524 / MPCBL5524 Faceplate” on page 13.

A link to the datasheet for this device is available in Appendix E, “Video.” Connector locations and pinouts are documented in Appendix A, “ZT 5524 / MPCBL5524 Connectors.”

2.3.24 Ethernet Interfaces

The ZT 5524 / MPCBL5524 provides two 10/100/1000Base-T Ethernet channels (ENET A and ENET B) through the Intel® 82546 Gigabit Ethernet PCI Controller. Two RJ-45 connectors, with status LEDs to indicate the status of each channel, are available on the faceplate via connector J7. Ethernet channels A and B can be directed through the BIOS setup to the RPIO connector J3.

A third 10/100Base-T Ethernet channel (ENET C) is also available on the ZT 5524 / MPCBL5524 through the Intel® 82550 Ethernet PCI Controller. An RJ-45 connector, with status LEDs to indicate the status of ENET C, is available on the faceplate via connector J11. For a diagram of the faceplate, see Figure 1, “ZT 5524 / MPCBL5524 Faceplate” on page 13.

For more information on E4h, see Appendix B, “Ethernet/Geographic Addressing (E4h),” for more information.

Appendix E, “Ethernet,”contains links to the data sheets for the Ethernet devices used on the ZT 5524 / MPCBL5524. Connector locations and pinouts are documented in Appendix A, “ZT 5524 / MPCBL5524 Connectors.”

2.3.25 LED Indicators

The LEDs located on the faceplate are defined below. See the topic Chapter 3, “Programming the LEDS,” in Chapter 2 for software code used to program the user-defined LEDs.

Ethernet C RJ-45 LEDs

- Flashing green = activity
- Green = Link
- Off = 10 Mbps
- Green = 100 Mbps

Power/Reset

- Green = out of reset, power enabled
- Amber = active reset, power enabled
- Off = Power disabled

IDE disk activity (primary or secondary)

- Green = active
- Off = inactive

User-defined LEDs—one may be defined as clock throttle

- Green = user defined
- Amber = user defined
- Off = user defined

Ethernet A, Ethernet B RJ-45 LEDs, one per channel

- Flashing green = activity
- Green = Link
- Off = 10 Mbps
- Green = 100 Mbps
- Amber = 1000 Mbps

Hot Swap

- Blue = safe to extract board
- Off = not safe to extract board

Status

- Green = healthy
- Amber = needs service

2.3.26 Rear-Panel I/O

The ZT 5524 / MPCBL5524 transitions the following I/O signals through CompactPCI connector J5 to a rear-panel transition (RPIO) board such as the Intel NetStructure® ZT 4807 Rear-Panel Transition Board:

- Floppy
- Two serial ports (COM1 and COM2)
- USB channels 1 and 2
- Keyboard
- IDE secondary channel
- RPIO Eject
- PS/2 mouse
- Ethernet LED
- Power/Ground
- Video
- Local CPU SMBus

In addition, the ZT 5524 / MPCBL5524 transitions Ethernet A and B through CompactPCI connector J3 and Ethernet C through J5.

Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

2.4 Software

This section explains key software components.

2.4.1 BIOS

The Intel NetStructure Embedded BIOS (AMI core) is loaded in flash on board the ZT 5524 / MPCBL5524. The BIOS is user-configurable to boot an operating system from one of the following locations:

- Local flash memory
- Hard drive
- CD-ROM drive
- Floppy drive
- Network source

2.4.2 Operating Systems

The ZT 5524 / MPCBL5524 is compatible with all major PC operating systems. Intel provides additional operating system support when the ZT 5524 / MPCBL5524 is purchased in conjunction with an Intel NetStructure development system (for example, the Intel NetStructure® ZT 5087 4U General Purpose Platform). This support may include additional drivers for NetStructure products such as peripherals and flash drives. Software device drivers for the ZT 5524 / MPCBL5524 can be found on the Intel website. A link to the website can be found in Appendix E, "ZT 5524 / MPCBL5524 Product Page."

The following operating systems are supported:

- Windows* 2000*
- Windows* .NET* Enterprise
- Industry standard version of Linux*
- Comprehensive board support package (BSP) for VxWorks*. The CompactPCI VxWorks-Tornado II BSP streamlines the implementation of VxWorks on the ZT 5524 / MPCBL5524. The VxWorks Tornado development system must be purchased directly from WindRiver.
- Refer to the *ZT 5524 / MPCBL5524 Compatibility Report* available on the Intel website ZT 5524 / MPCBL5524 product page for a complete list of compatible operating systems.

2.4.3 Redundant Host

The ZT 5524 / MPCBL5524 is designed to operate as a Host in a PICMG 2.13 compliant RSS backplane. Intel's Redundant Host Software Development Kit is fully integrated with software features, including development utilities to simulate fault conditions and verify system operation. All start-up software is included and ready for development. Refer to the *Redundant Host Software Development Kit for Intel NetStructure CompactPCI System Master Processor Boards Software Manual* for more information about Intel's High Availability architecture and development of Redundant Host drivers. A link to this document is available in Appendix E, "User Documentation."

2.4.4 IPMI

Refer to the *Redundant Host Software Development Kit for Intel NetStructure CompactPCI System Master Processor Boards Software Manual* for information about IPMI and firmware support.

For more information about how to program software to interact with the IPMI firmware, refer to the *Intelligent Platform Management Interface v1.5 Specification and the Intelligent Platform Management Interface Implementer's Guide.*

2.4.5 Hot Swap

Hot swap refers to the dynamic insertion and removal of devices in a computer system without halting the system.

When used in a hot swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0*, the ZT 5524 / MPCBL5524 supports hosting hot swap peripherals in a powered system. Appendix E, "Data Sheet Reference" contains a link to the CompactPCI Hot Swap Specification.

Intel's Hot Swap Kit provides software that collaborates with the operating system to provide hot swap support for CompactPCI. For more information, refer to the *Intel NetStructure® Hot Swap Kit Software Manual.*

Getting Started 3

This chapter summarizes the information you need to make the ZT 5524 / MPCBL5524 operational. Please read it before attempting to use the board.

3.1 Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Intel. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Intel. Refer to "Warranty Information" on page 90 for assistance information.

Warning: Like all equipment that uses MOS devices, the ZT 5524 / MPCBL5524 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with your order to handle the boards.

3.2 ZT 5524 / MPCBL5524 System Requirements

The following ZT 5524 / MPCBL5524 system requirements are briefly described below:

- Backplane requirements
- Electrical and environmental requirements

3.2.1 Backplane Connectivity

The ZT 5524 / MPCBL5524 is designed for use in a CompactPCI Packet Switching Backplane (compliant with the *CompactPCI Specification, PICMG* 2.16, Version 1.0*). This requires that the backplane provide a CompactPCI bus on connectors J1 and J2 and Ethernet pins on J3. To support optional rear-panel transition (RPIO) boards, the backplane's RPIO connector (J5) must be available and have through pins to the ZT 5524 / MPCBL5524's J5 connector.

The ZT 5524 / MPCBL5524 supports universal voltage: it operates in both 3.3 V V(I/O) and 5 V V(I/O) slots.

Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

3.2.2 Electrical and Environmental Requirements

The ZT 5524 / MPCBL5524 requires a maximum of +5 VDC +5%, -3% @ 4.5 A with dual 933 MHz processors loaded, +5 VDC +5%, -3% @ 2.7 A with a single 933 MHz processor loaded, +3.3 VDC +5%, -3% @ 7 A, and +12 VDC ± 5%, -3% @ 50 mA. Electrical specifications are covered in more detail in Appendix A, "Specifications."

The ZT 5524 / MPCBL5524 is supplied with a heatsink allowing the processor to operate between 0° and approximately 45 °C ambient with a minimum of 250 LFM (1.27 meters per second) of external airflow. It is the users' responsibility to ensure that the ZT 5524 / MPCBL5524 is installed in a chassis capable of supplying adequate airflow. The maximum power dissipation of the processor is 13.2 W. External airflow **must** be provided at all times. See Appendix A, "Specifications," and Appendix B, "System Registers," for more details.

Warning: Operating the ZT 5524 / MPCBL5524 without adequate airflow will damage the processor.

The ZT 5524 / MPCBL5524 may contain materials that require regulation upon disposal. Please dispose of this product in accordance with local rules and regulations. For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance at http://www.eiae.org/.

3.3 Memory Configuration

The ZT 5524 / MPCBL5524 addresses up to 4 GBytes of memory. The address space is divided between memory local to the board and memory located on the CompactPCI bus. Any memory not reserved or occupied by a local memory device (DRAM/flash) is available to the CompactPCI bus. The DIMM socket of the ZT 5524 / MPCBL5524 can be populated with one registered, 168-pin ECC SDRAM. The socket supports 256, 512, or 1024 MByte memory modules, giving a memory size range from 256 MByte to a maximum of 1 GByte (single DIMM socket) or 4 GBytes (four DIMM sockets) of 133 MHz SDRAM memory. Refer to the *ZT 5524 / MPCBL5524 Compatibility Report*, available on the Intel website, for a complete list of compatible memory types. A link to this website is available in Appendix E, "ZT 5524 / MPCBL5524 Product Page."

Figure 3, "Memory Address Map Example" on page 30 shows example memory addressing for the ZT 5524 / MPCBL5524.

3.4 I/O Configuration

The ZT 5524 / MPCBL5524 addresses up to 64 KByte of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the CompactPCI bus. Any I/O space not occupied by a local I/O device is available for the CompactPCI bus.

The ZT 5524 / MPCBL5524 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in Table 1, "I/O Address Map" on page 31.

Figure 3. Memory Address Map Example

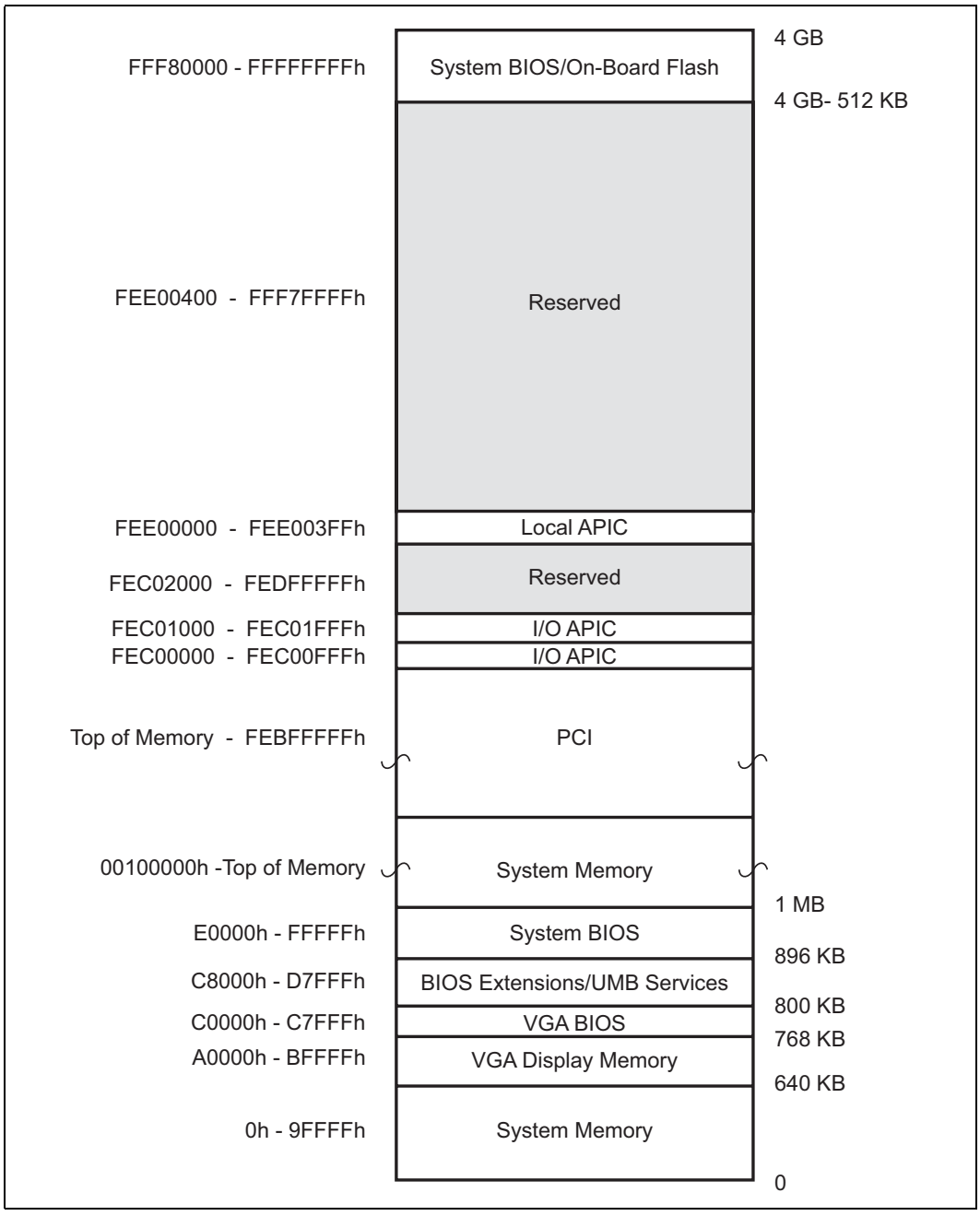


Table 1. I/O Address Map (Sheet 1 of 2)

F50-F58h	General Purpose Chipset
CD7h	Power Management Data Register
CD6h	Power Management Index Register
C6Fh	Miscellaneous Control Registers
C6Ch	ISA Wait Register
C52h	General Purpose Registers
C51h	Client Management, Security Data
C50h	Client Management, Security Index
C4Ah	Rise Time Counter Value
C49h	Address/Status Control
C14h	PCI Error Status Register
C01h	PCI IRQ Mapping Data Register
C00h	PCI IRQ Mapping Index Register
4D6h	DMA2 Extended Write Mode Register
4D1h	On-board Slave Interrupt Controller
4D0h	On-board Master Interrupt Controller
40Bh	DMA1 Extended Write Mode Register
3F6h	Primary IDE Registers
376h	Secondary IDE Registers
1F0 - 1F7h	Primary IDE Registers
170h - 177h	Secondary IDE Registers
F0h	Coprocessor
E1-E6h	ZT 5524 / MPCBL5524 System Registers
C0 - DFh	On-board Slave DMA Controller
A0 - A1h	On-board Slave Interrupt Controller
92h	Positively Decoded, Passed to ISA
81 - 8Fh	On-board DMA Page Registers
80h	ZT 5524 / MPCBL5524 System Registers
7Bh	ZT 5524 / MPCBL5524 System Registers
78 - 79h	ZT 5524 / MPCBL5524 System Registers

Table 1. I/O Address Map (Sheet 2 of 2)

70h	NMI Enable Register
61h	NMI Status Register
60h	Positively Decoded, Passed to ISA
40 - 43h	On-board Timer/Counters
20 - 21h	On-board Master Interrupt Controller
0 - 1Fh	On-board Master DMA Controller

3.4.1 Analog Video Interface

The ZT 5524 / MPCBL5524 provides access to video at the faceplate through J10, using the Chips and Technologies 69000 HiQVideo Accelerator with Integrated Memory, a 2 MB SDRAM video device. Video connector J10 is a 15-pin subminiature D connector. Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors.".

The ZT 5524 / MPCBL5524 must be used with an analog monitor. If your monitor is capable of both digital and analog modes, be sure it is set to analog.

Monitor timing specifications for supporting various display modes are provided in the *69000 HiQVideo Accelerator with Integrated Memory* data sheet. A link to the datasheet for this device is available in Appendix E, "Video."

The ZT 5524 / MPCBL5524 can be used in a wide variety of video applications. To ensure the best quality display, take into account such factors as environment, noise from surrounding equipment, video mode, distance from video source, and cabling.

The analog video signals are comprised of a horizontal and vertical sync and three color signals (red, green, and blue). The signals are driven by a RAMDAC, which is used to convert the digital video data to analog signals. The RAMDAC's analog outputs have an impedance of 75 Ω Ideally, the connection to this output should use high-quality 75 Ω shielded cable.

Note: A secondary video card accessed via the backplane is not supported in multiprocessing environments when running under Windows 2000.

3.5 Video BIOS

The video BIOS provides low-level control of the VGA controller. It is used to interpret higher-level commands and transform them into register-level instructions that the VGA controller can understand. The ZT 5524 / MPCBL5524's BIOS is fully IBM VGA and VESA compatible. The BIOS is automatically installed during system initialization and is mapped to the standard C0000 to C7FFFh VGA BIOS memory space.

3.6 Connectivity

The ZT 5524 / MPCBL5524 provides several connectors for interfacing to application-specific devices. Connector locations and pinouts are documented in Appendix A, “ZT 5524 / MPCBL5524 Connectors.”

3.7 Switches and Build Options

The ZT 5524 / MPCBL5524 provides switch configuration options for features that cannot be provided through the BIOS Setup utility (see “BIOS Configuration Overview” on page 33). Refer to “Switch Options and Locations” on page 38 for location figures and descriptions.

Several additional functional options are built into the ZT 5524 / MPCBL5524 but not implemented in the standard product.

3.8 BIOS Configuration Overview

This topic presents a brief introduction to the Intel NetStructure Embedded BIOS. For more detailed information about the BIOS and other utilities, see the *Intel NetStructure Embedded BIOS (AMI Core) Software Manual*. A link to this document is available in Appendix E, “User Documentation.”

The Intel NetStructure Embedded BIOS has many separately configurable features. These features are selected by running the built-in Setup utility. The system configuration settings are saved in a portion of the battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

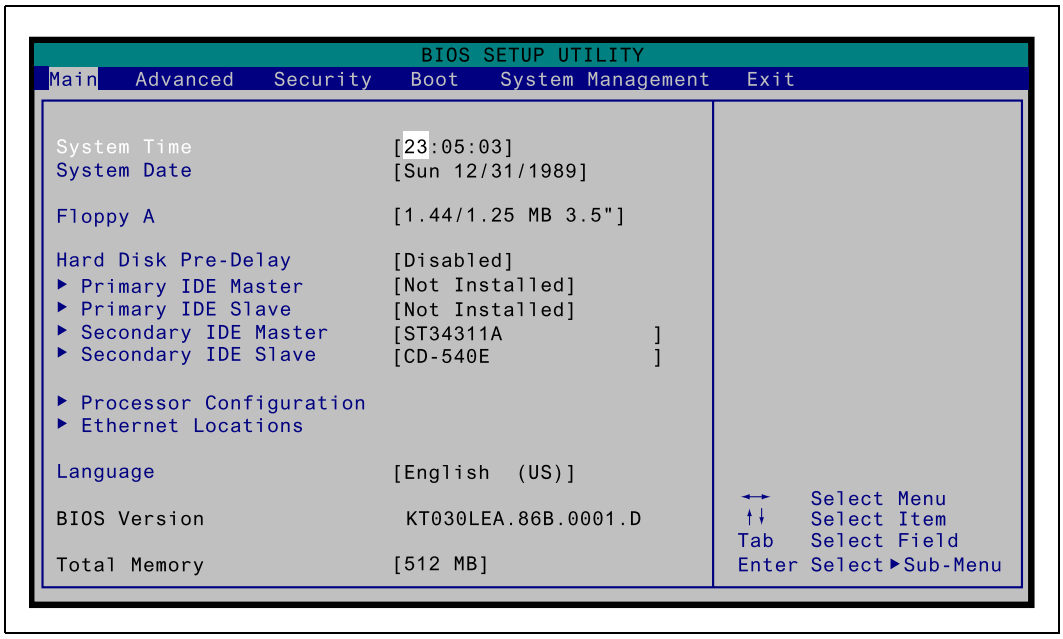
To access the Setup utility, press the **F2** key during POST test and initialization at boot time. Setup runs once the POST functions complete.

When Setup runs, an interactive configuration screen displays. See Figure 4, “Setup Screen” on page 34 for an example. Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context-sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the + or – keys to change the value of a parameter.

Items in the main portion of the screen that have a triangular mark to their left are submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press the **Enter** key.

Figure 4. Setup Screen



3.8.1 Console Redirection

Console redirection allows users to monitor the ZT 5524 / MPCBL5524's boot process and to run the ZT 5524 / MPCBL5524's Setup utility from a remote serial terminal. Connection is made directly through a serial port.

The console redirection feature is most useful in cases where it is necessary to communicate with a processor board, such as the ZT 5524 / MPCBL5524, in an embedded application without video support.

The Console Redirection option in the BIOS can be overridden by hardware switch 3-1. Console Redirection is enabled by default in the BIOS but is disabled by default by the hardware switch.

See the *Intel NetStructure Embedded BIOS (AMI Core) Software Manual* for more information about console redirection. A link to this document is available in Appendix E, "User Documentation."

3.9 Installing the Operating System

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor and to the ZT 5524 / MPCBL5524 Product Page on the Intel website (URL listed in Appendix E, “ZT 5524 / MPCBL5524 Product Page” on page 89).

To install the operating system

1. Install peripheral devices. CompactPCI devices are automatically configured by the BIOS during the boot sequence.
2. Install, configure and test any devices that will be used in the installation process. Most operating systems require initial installation on a hard drive from a floppy or CD-ROM drive.
3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any readme files or documents provided with the OS as these typically note documentation discrepancies or compatibility problems.
4. Select the appropriate boot device order in the Setup boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation floppy, select **Removable Media** as the first boot device and reboot the system with the installation floppy installed in the floppy drive.

Note: If the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive.

- In order to boot from a USB CD-ROM you must first connect the USB drive, then enter the BIOS Setup utility and move the “CD-ROM” device to the top of the boot list (or above any other bootable devices).
- To boot from a USB Floppy you must connect the floppy device to the board, then enter the BIOS Setup utility, move “Removable Devices” to the top of the boot order on the Boot screen and then move the USB floppy device to the top of the removable devices list.

5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. For specific device types and compatibility modes of Intel NetStructure product, refer to the appropriate hardware documentation (see Appendix E, “User Documentation.”).
6. When installation is complete, reboot the system and set the boot device order in the Setup boot menu.
7. The Flash Write Protect/Write Enable switch, SW4-1, must be open when installing an operating system image into flash. See Chapter 4, “SW4-1 (Flash Write Protect/Write Enable)” for more information.

3.10 Programming the LEDS

The ZT 5524 / MPCBL5524 includes two user-controlled, bi-color (amber/green), LEDs located on the connector plate (see Figure 1 on page 13). The user LEDs are software programmable through bits 0-3 of the Power/LED Control Register (Port E5h) (see Appendix B, "Video/LED Control (E5h)"). The LEDs are turned off after a power cycle or a reset.

As shown below, two bits each are used to control the state of User LEDs 0 and 1. Since bi-color LEDs are used, there are three states for each LED: green, amber, and off. Both LEDs may be turned on at the same time.

Table 2. User LED States

Bit	State			
User LED 1	**Amber**	**Green**	**Both Off**	**Both On**
Bit 2	1	0	0	1
Bit 3	0	1	0	1
User LED 2	**Amber**	**Green**	**Both Off**	**Both On**
Bit 0	1	0	0	1
Bit 1	0	1	0	1

The LED bits are in the same register as other functions. It is important not to change the state of other bits in this register when modifying the User LED status. The following code demonstrates the mechanism for modifying the bits for User LED 1:

Table 3. Code for Modifying Bits of User LED 1 (Sheet 1 of 2)

Code	Description
; set USER LED 1 ON (GREEN)	
cli	; clear interrupts
in al, E5h	; read current state
and al, F3h	; preserve other register bits
or al, 08h	; set USER LED 1 (GREEN and enabled)
out E5h, al	; output new value for register
sti	; re-enable interrupts
; set USER LED 1 ON (AMBER)	
cli	; clear interrupts
in al, E5h	; read current state
and al, F3h	; preserve other register bits
or al, 04h	; set USER LED 1 (AMBER and enabled)
out E5h, al	; output new value for register
sti	; re-enable interrupts
; set LED OFF	
cli	; clear interrupts

Table 3. Code for Modifying Bits of User LED 1 (Sheet 2 of 2)

Code	Description
in al, E5h	; read current state
and al, F3h	; set bit 1 to turn off LED
out E5h, al	; output new value for register
sti	; re-enable interrupts

Configuration 4

The ZT 5524 / MPCBL5524 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS Setup mechanism (discussed in Chapter 3, “BIOS Configuration Overview”).

Some options cannot be software controlled and are configured by opening or closing the appropriate switch. This chapter details the ZT 5524 / MPCBL5524’s switch options.

4.1 Switch Options and Locations

The ZT 5524 / MPCBL5524 contains four banks of switches located on the component side of the board (SW3-SW6). S1 and S2 are push-button switches located on the faceplate. For a diagram of the faceplate, see Figure 1, “ZT 5524 / MPCBL5524 Faceplate” on page 13.

Figure 5 on page 39 shows the ZT 5524 / MPCBL5524’s switch settings as shipped from the factory. Figure 6 on page 39 provides a blank switch layout; print this figure and use it to document your switch configuration if it differs from the factory default. This will allow you to restore the configuration if it is changed for any reason.

The table below presents the switch options by function.

Table 4. ZT 5524 / MPCBL5524 Switch Cross-Reference Table

Function	Switch
Abort Request	SW2 (push button on the faceplate)
Battery Back/Clear CMOS	SW5-1, SW5-2, SW6-2
BMC Flash Write Protect	SW4-4
Boot Source	SW4-2
Console Redirection	SW3-1
CPU Reset	SW1 (push button on the faceplate)
Drone Reset Control	SW6-3
Flash Write Protect/Write Enable	SW4-1
Master/Slave Drive Select	SW3-4
Software Configured	SW3-2, SW3-3
Video Select	SW5-3

Figure 5. Factory Default Switch Configuration

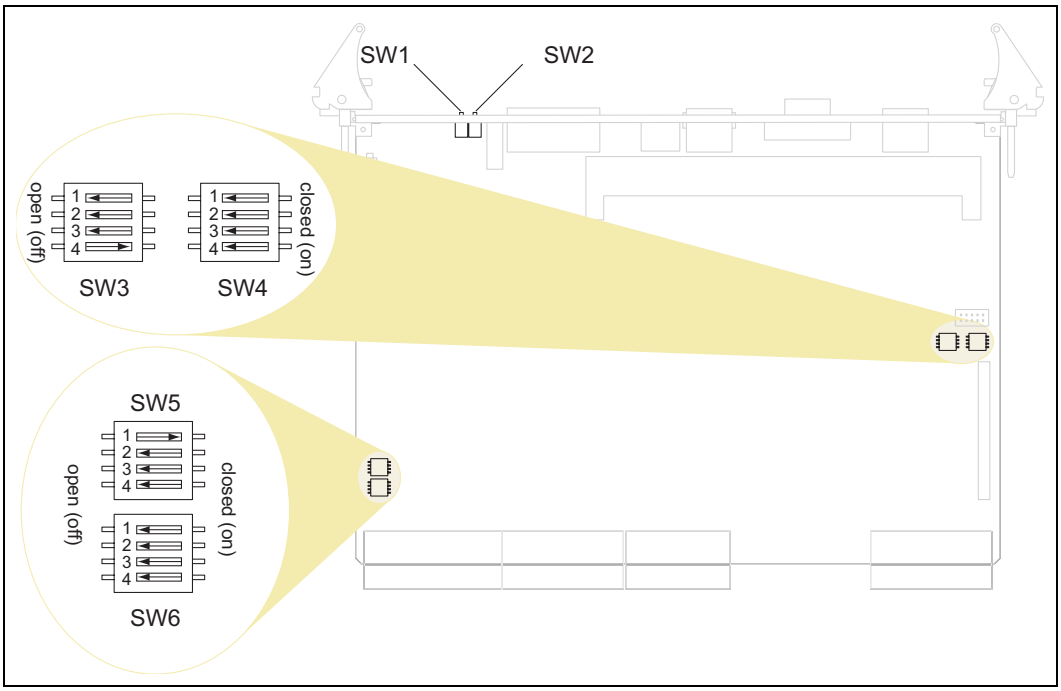
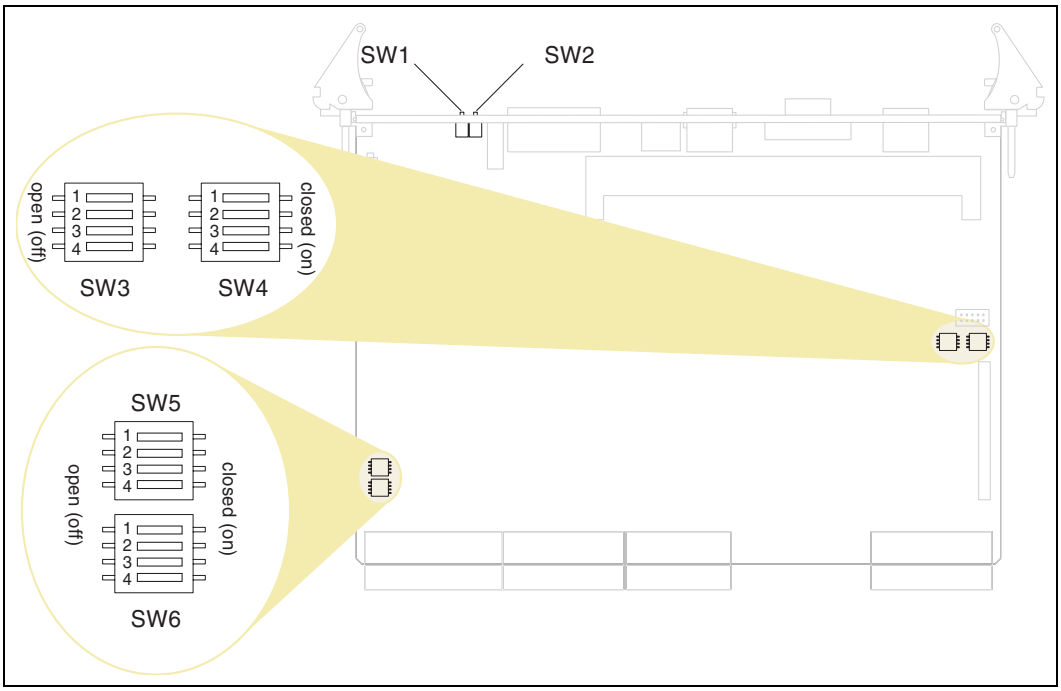


Figure 6. Customer Switch Configuration



4.2 Switch Descriptions

The following topics present the switches in numerical order and provide a detailed description of each switch. Multiple-position switches are identified in the form **SWx-N**, where **x** is the switch number and **-N** is the switch position (for example, SW3-2 means “switch number 3, position 2”).

4.2.1 SW1 (CPU Reset)

SW1 is a push button on the ZT 5524 / MPCBL5524’s faceplate. When pressed with a short pulse, SW1 issues a Reset Request to the CPU. Pressing on the switch for 2 seconds forces a hard CPU reset. For a diagram of the faceplate, see Figure 1, “ZT 5524 / MPCBL5524 Faceplate” on page 13.

4.2.2 SW2 (Abort Request)

SW2 is a push button on the ZT 5524 / MPCBL5524’s faceplate. When pressed, SW2 issues an Abort Request (NMI) to the CPU. For a diagram of the faceplate, see Figure 1, “ZT 5524 / MPCBL5524 Faceplate” on page 13.

4.2.3 SW3-1 (Console Redirection)

Close this switch to enable console redirection (see page 34). The status of this switch is monitored by the user’s software through the Switch Monitors register (Port E3h Bit 0) Console Redirection Enable bit to provide user-configurable features (see Table 39 on page 77). When open, this switch reads back a 0; when closed it reads back a 1. Factory default is open.

Table 5. SW3-1 Settings

SW3-1	Reading	Function
Open (Default)	0	Console Redirection Disabled
Closed	1	Console Redirection Enabled

4.2.4 SW3-2, SW3-3 (Software Configured)

These switches are used to provide configuration information to the user’s software. The Software Configuration bits of the Switch Monitors register (Port E3h Bits 1-2) monitors the status of SW3 segments as listed below (see Table 39 on page 77). An open switch reads back a 0; a closed switch reads back a 1. The switch segments correspond to register bits as follows:

- **SW3-2** = Bit 1
- **SW3-3** = Bit 2

4.2.5 SW3-4 (Master/Slave Drive Select)

This switch designates an IDE drive attached to onboard IDE connector J19 as a master or slave IDE device. Opening SW3-4 selects the drive as a master device. Closing SW3-4 assigns the drive as a slave device. Factory default is closed.

Table 6. SW3-4 Settings

SW3-4	Function
Open	Onboard IDE Master
Closed (Default)	Onboard IDE Slave

4.2.6 SW4-1 (Flash Write Protect/Write Enable)

Closing this switch write-protects the BIOS portion of the flash memory. Open SW4-1 when installing an operating system image (such as VxWorks) into flash or when using the FLASH.EXE utility to recover from a corrupted BIOS (see "Flash Utility Program" on page 53). The status of this switch can be read back at the Flash Write-Protect Status bit of the Switch Monitor register (Port E3h, bit 7). Factory default is open. For more information on this bit, see Table 39 on page 77.

The Flash Write Enable bit of the Flash Control register (Port 78h, bit 1) must also be properly set to write to flash (see Table 34 on page 73). Factory default is open.

Table 7. SW4-1 Settings

SW4-1	Function
Open (Default)	BIOS read/write
Closed	BIOS read only

4.2.7 SW4-2 (Boot Source)

Open this switch to boot from flash (normal operation). Close this switch to recover from a corrupted BIOS. This allows the ZT 5524 / MPCBL5524 to boot from the BIOS Recovery Module. See Chapter 7, "BIOS Recovery" for more information.

The status of this switch can be read back at the Boot Source Monitoring bit of the Switch Monitors register (Port E3h, bit 6). Factory default is open. For more information on this bit, see Table 39 on page 77.

Note: The BIOS Recovery Module Override Bit (Port 78h, bit 7) must be set to 0 for this switch to be operational.

Table 8. SW4-2 Settings

SW4-2	Function
Open (Default)	Boot from Flash
Closed	Boot from BIOS Recovery Module

4.2.8 SW4-3 (Reserved)

The function of this switch is reserved and should not be altered from its factory default setting (open).

4.2.9 SW4-4 (BMC Flash Write Protect)

This switch allows write protection of the BMC flash. Factory default is open.

Table 9. SW4-4 Settings

SW4-4	Function
Open (Default)	Normal Operation
Closed	BMC Flash Write Protected

4.2.10 SW5-1, SW5-2, SW6-2 (Battery Back/Clear CMOS)

These switches are used to control the battery backup for CMOS memory and for clearing CMOS memory. When closed, SW5-1 connects the CMOS memory to the on-board battery. To clear CMOS, open SW5-1 and close SW5-2 and SW6-2. After two seconds, return SW5-2 and SW6-2 to the open position and SW5-1 to the closed position. Factory default is SW5-1 closed, SW5-2 open, and SW6-2 open.

Caution: Closing SW5-1 and SW5-2 at the same time significantly shortens battery life. SW5-1 should be closed and SW5-2 should be open during normal operation.

Table 10. SW5-1, SW5-2, SW6-2 Settings

SW5-1	SW5-2	SW6-2	Function
Closed (Default	Open (Default)	Open (Default)	Normal operation– battery backed CMOS
Open	Closed	Closed	Battery power off, battery grounded, Clear CMOS, (return to default after clearing)

4.2.11 SW5-3 (Video Select)

This switch allows video signals to be active at both the faceplate and the rear panel I/O connector or only at the rear panel I/O connector. Open SW5-3 to activate video signals at faceplate connector J10 and at rear panel I/O connector J5. The BIOS setup then controls which connector receives video signals. Close SW5-3 to route video signals to rear panel I/O connector J5 only. If SW5-3 is closed, the BIOS can be set to route video signals to the front, but SW5-3 overrides the BIOS setting and sends video out the rear. Factory default is open.

Table 11. SW5-3 Settings

SW5-3	Function
Open (Default)	Front/Rear Video Signals Active
Closed	Rear Video Signals Active

4.2.12 SW5-4, SW6-1 (Reserved)

The functions of these switches are reserved and should not be altered from their factory default settings (open).

4.2.13 SW6-3 (Drone Reset Control)

Closing SW6-3 allows the PCI Reset signal to be ignored when the ZT 5524 / MPCBL5524 is used in Drone Mode. Factory default is open.

Table 12. SW6-3 Settings

SW6-3	Function
Open (Default)	Drone PCI Reset Enabled
Closed	Ignore PCI Reset

4.2.14 SW6-4 (Reserved)

The function of this switch is reserved and should not be altered from its factory default setting (open).

IDE Interface 5

This chapter provides an introduction to the ZT 5524 / MPCBL5524's IDE interface controller. It documents the ZT 5524 / MPCBL5524's support for local and remote IDE disk drives. The ZT 5524 / MPCBL5524 supports ATA-66 for the primary IDE channel and ATA-33 for the secondary IDE channel.

The ZT 5524 / MPCBL5524's IDE interface provides two IDE channels for interfacing with up to three IDE devices.

The IDE controller is incorporated into the ServerWorks* CSB5, which uses the PCI bus to give exceptional IDE performance. The IDE interface can sustain a maximum transfer rate of 66.6 MB per second between the IDE drive buffer and PCI.

A link to the datasheet for this device is available in Appendix E, "Chipset."

5.1 ZT 5524 / MPCBL5524 IDE Interface Features

- IBM*-AT compatible
- 32-bit, 33 MHz, high-performance PCI bus interface
- Supports PIO and Bus Master EID
- Ultra DMA/66 synchronous DMA operation
- Bus Master IDE transfers up to 66 MB/s
- Primary and secondary channels for interfacing up to four devices
- On-board IDE drive
- Individual software control for each IDE channel

5.2 Disk Drive Support

The ZT 5524 / MPCBL5524 supports either internal or external IDE drives. These configurations are described below. Connector locations and pinouts are documented in Appendix A, "ZT 5524 / MPCBL5524 Connectors."

5.2.1 Primary IDE Channel

The ZT 5524 / MPCBL5524 primary IDE channel is directed to IDE connector J19. Connector J19 is used to connect to a locally mounted 2.5 inch, low-profile hard drive.

Primary IDE signals are also routed to the J17 mezzanine board interface.

5.2.2 Secondary IDE Channel

The ZT 5524 / MPCBL5524 secondary IDE channel is routed to rear-panel I/O connector J5, providing an optional transition board (such as the ZT 4807 Rear-Panel Transition Board) signals for up to two external IDE devices.

5.2.3 IDE HDD Specifications

Disk characteristics for Logical Block Addressing (LBA) mode:

Characteristic	Value
Capacity in LBA Mode	40 GB
Number of Heads	4
Number of Cylinders (User)	35,968
Number of Sectors (User)	78,140,160
Bytes per Sector	512
Recording Method	48/50 RLL
Track Density	2.42 K tracks/mm (61,500 TPI)
Bit Density	23.30 K bits/mm (592,000 BPI)
Rotational Speed	4,200 rpm +/- 1%
Average Latency	7.14 ms
Positioning time (read and seek): Minimum (Track to Track) Average Maximum (Full)	 1.5 ms (typical) Read : 12ms (typical) 22 ms (typical)
Start time	5 sec (typical)
Interface	ATA-5 (maximum cable length: 0.46 m) (equipped with expansion function)
Data Transfer Rate To/From Media To/From Host	 18.4 to 32.5 MB/s 100 MB/s Maximum (U-DMA mode 5)
Data Buffer Size	2 MB
Physical Dimensions (Height x Width x Depth)	 9.5mm x 100.0mm x 70.0mm
Weight	99 g

Disk characteristics for Cylinder-Head-Sector (CHS) mode:

Characteristic	Value
Formatted Capacity	8.45 GB
Number of Heads	16
Number of Cylinders (User)	16,383
Number of Sectors in CHS Mode (User)	63

5.3 I/O Mapping

The I/O map for the IDE interface varies depending on the mode of operation (see Table 1, “I/O Address Map” on page 31). The default mode is *compatibility mode*, which means that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h, and interrupt IRQ15. No memory addresses are used.

Watchdog Timer 6

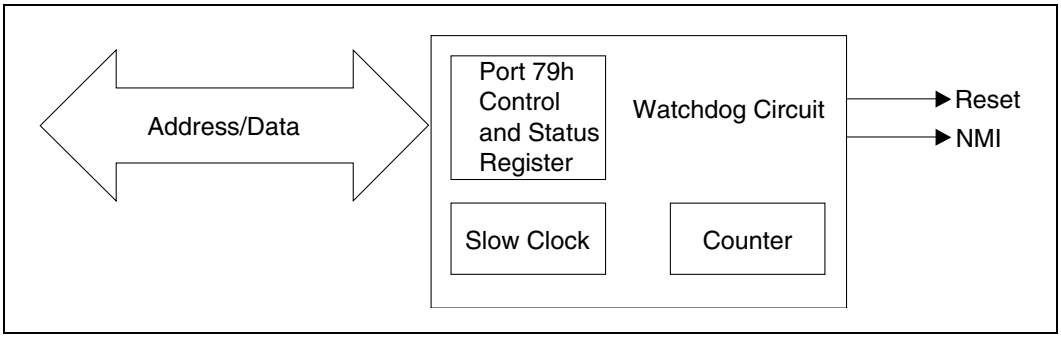
This chapter explains the operation of the ZT 5524 / MPCBL5524 Watchdog Timer. It provides an overview of watchdog operation and features, as well as sample code to help you learn how the Watchdog Timer works with applications.

6.1 Overview

The primary function of the Watchdog Timer is to monitor ZT 5524 / MPCBL5524 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are:

- Two-stage operation
- Enabled and disabled through software control
- Armed and strobed through software control

Figure 7. Watchdog Timer Architecture



The ZT 5524 / MPCBL5524's custom watchdog timer circuit is implemented in a programmable logic device. The watchdog timer contains a Control and Status register (referred to in this document as the Watchdog register, Port 79h. See Appendix B, "System Registers" for the Watchdog register description).

The register allows the BIOS or user application to determine the source of a particular reset (watchdog time-out, power-up, power out-of-range/low voltage, etc.). When the watchdog times out, it drives an NMI and RST. Watchdog NMI and RST can be independently disabled through the Watchdog register.

Eight timeout intervals are selectable from the Watchdog register, ranging from a minimum timeout period of 250 ms to a maximum timeout period of 256 seconds. The watchdog is strobed by reading the Watchdog register. This resets the timer. If the timer is not reset within the timeout interval, the watchdog timer drives an NMI followed by RST 250 ms later. The NMI gives the application 250 ms to perform essential tasks before the hardware is reset.

6.2 Power-Up Initialization

The Watchdog Timer's programmable logic is initialized only at power-up. This ensures that the NMI, RST, NMI ENABLE, and RESET ENABLE status and control bits power up to unasserted states, allowing the BIOS or user applications to determine the reset source (watchdog time-out, power-up, power out-of-range/low voltage, and so on).

6.3 Time-Out Values

The watchdog timer has its own separate slow clock source. This clock runs at a maximum frequency of 32 Hz (25 Hz nominal—because this slow clock is based on an RC oscillator, the nominal timeout period is approximately 30% longer than the minimum value). The watchdog is guaranteed to time-out in no less than the programmed minimum value.

6.4 Using the Watchdog in an Application

The following topics help you learn how to use the watchdog in an application. They describe the watchdog's reset and NMI functions and provide sample code. Watchdog reset and NMI are controlled through the watchdog's Control and Status register (referred to in this document as the Watchdog register, Port 79h). See Appendix B, "Watchdog (79h)" B for more information.

6.4.1 Watchdog Reset

An application using the reset feature:

1. Enables the watchdog reset
2. Sets the terminal count period
3. Periodically strobes the watchdog to keep it from resetting the system
4. If a strobe is missed, the watchdog assumes that an application error has occurred and resets the system hardware

6.4.1.1 Enabling the Watchdog Reset

C code for enabling the watchdog reset might look like the following:

```
#define WD_RESET_EN_BIT_SET                    0x20
void EnableWatchdogReset(void){
unsigned char WdValue;                         // Holds watchdog register values.
                                               //
WdValue = inb(WD_CSR_IO_ADDRESS);              // Read the current contents of the
                                               //watchdog register.
WdValue |= WD_RESET_EN_BIT_SET;                // Assert the enable bit in the
local
                                               //copy.
outb(WD_CSR_IO_ADDRESS,WdValue);               // Assert the enable in the watchdog
// register.
}
```

6.4.1.2 Setting the Terminal Count

The terminal count determines how long the watchdog waits for a strobe before resetting the hardware. C code for setting the terminal count might look like the following:

```
#define WD_CSR_IO_ADDRESS            0x79    // IO address of the watchdog

#define WD_T_COUNT_MASK              0x07    // Bit mask for terminal count bits.

#define WD_500MS_T_COUNT             0x01    // Terminal count values . . . .

#define WD_1S_T_COUNT                0x00    //

#define WD_250MS_T_COUNT             0x00    //

.



void SetTerminalCount(void){

Unsigned char WdValue;               // Holds watchdog register values.

                                     //

WdValue = inb(WD_CSR_IO_ADDRESS);    // Get the current contents of the watchdog
                                     // register.

WdValue &= ~ WD_T_COUNT_MASK;        // Mask out the terminal count bits.

WdValue |= WD_500MS_T_COUNT;         // Set the desired terminal count.

outb(WD_CSR_IO_ADDRESS,WdValue);     // Furnish the watchdog register with the new

                                                  // count value.

}
```

6.4.1.3 Strobing the Watchdog

Once the watchdog is enabled, it must be strobed within the terminal count period to avoid resetting the system hardware. C code to strobe the watchdog might look like the following:

```
void StrobeWatchdog(void){

inb(WD_CSR_IO_ADDRESS);              // A single read is all it takes.

}
```

6.4.2 Watchdog NMI

When enabled, an NMI precedes a watchdog reset by 250 ms. The NMI generation feature gives the application 250 ms to perform essential tasks before the hardware is reset. Before using watchdog NMI, ensure the following:

- The code for performing the essential tasks is included in an interrupt service routine (ISR)
- The ISR is chained to the existing NMI ISR
- The watchdog NMI is enabled

6.4.2.1 Chaining the ISRs

Save the original NMI ISR vector so that it can be invoked from the new watchdog NMI ISR. Alter the interrupt vector table so that the NMI ISR vector is overwritten with a vector to the watchdog ISR. C code to do this in DOS might look like the following:

```
#define NMI_INTERRUPT_VECTOR_NUMBER 2

void interrupt far (*OldNMIIsr)();

void HookWatchdogIsr(void){

//
// To be absolutely certain the interrupt table is not accessed by an NMI (This is
// quite unlikely.), the application could disable the NMI in the chipset before
// installing the new vector.
//
.
.
.
//
// Install the new ISR.
//
OldNMIIsr = getvect(IsrVector);                              // Save the old
vector.
setvect(NMI_INTERRUPT_VECTOR_NUMBER, WatchdogIsr);            // Install the new.
}
```

6.4.2.2 Enabling the Watchdog NMI

To activate the NMI feature, enable it in the Watchdog register (Port 79h). Register specifications are located in Appendix B, “Watchdog (79h).”

The code to do this might look like the following:

```
#define WD_NMI_EN_BIT_SET          0x10

void EnableWatchdogNMI(void){

  unsigned char WdValue;                          // Holds watchdog register values.

                                                  //

  WdValue = inb(WD_CSR_IO_ADDRESS);               // Read the current contents of the

                                                  //watchdog register.

  WdValue |= WD_NMI_EN_BIT_SET;                   // Assert the enable bit in the local
  copy.

  outb(WD_CSR_IO_ADDRESS,WdValue);                // Assert the enable in the watchdog

                                                  // register.

}
```

6.4.2.3 NMI Handler

Because the NMI may have originated from another source such as a RAM Error Correction Code (ECC) error, the NMI handler cannot assume that the NMI occurred due to a watchdog time out. Therefore, the NMI handler must check the Watchdog Status register before taking watchdog-related emergency action. When the NMI handler completes handling the emergency, it invokes the original NMI handler. The code to do this might look like the following:

```
#define WD_NMI_DETECT_BIT_SET0x40          // Bit that indicates a NMI occurred, set.
                                           //
void WatchdogIsr(void){                    //
                                           //
        //
                // Did the watchdog cause the NMI?
                //
        if(inb(WD_CSR_IO_ADDRESS) & WD_NMI_DETECT_BIT_SET){
                                                   //
                        TripAlarm();               // Take care of essential tasks.
                                                   //
                        TurnOffTheGas();           //
                }                                  //
                _chain_intr(OldNMIIsr);            // Invoke the originally installed ISR.
}
```

6.4.2.4 Other Watchdog NMI Uses

The watchdog NMI feature can be used independently of the watchdog reset feature. Code for checking the bit is provided in the “NMI Handler” topic above.

BIOS Recovery 7

The ZT 5524 / MPCBL5524 provides 16 MB of on-board flash memory containing the system BIOS.

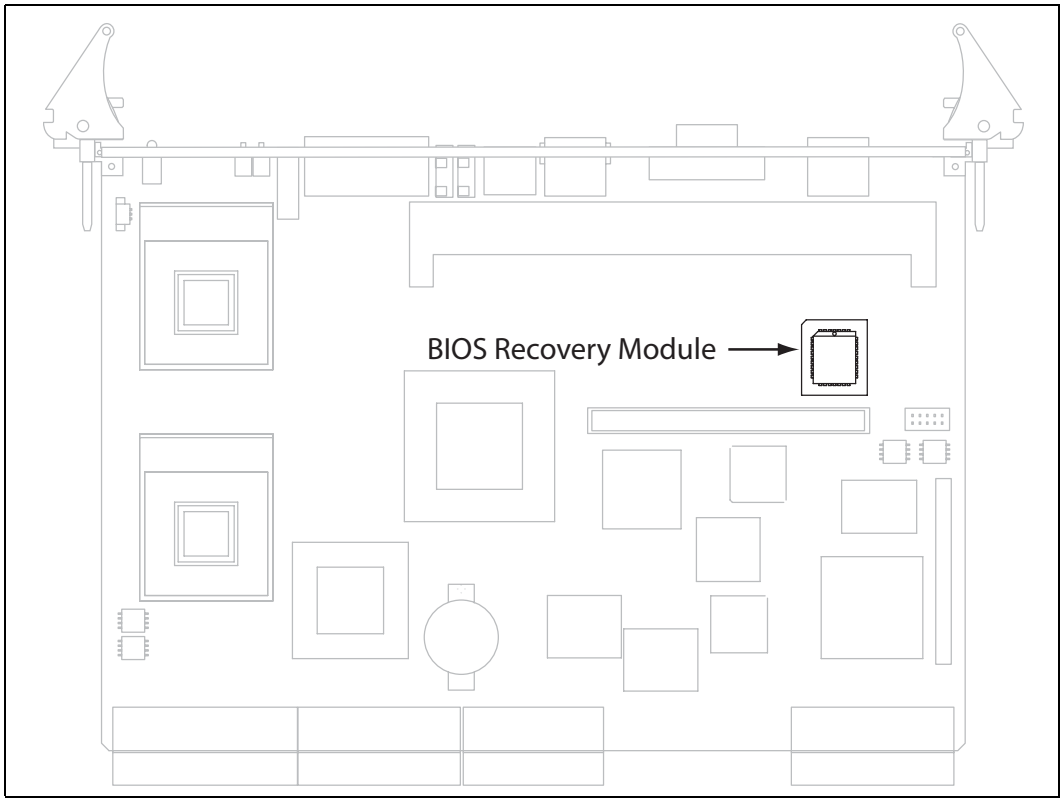
The flash device is divided into eight pages mapped into a window in extended memory (FFF80000h–FFFFFFFFh). The BIOS occupies 512 KByte in flash page 0. To reprogram the BIOS or update it if it becomes corrupted, use the BIOS Recovery Module and FLASH.EXE utility.

7.1 BIOS Recovery Module

The ZT 5524 / MPCBL5524 provides a 512 KByte EPROM programmed with a backup copy of the BIOS. If the ZT 5524 / MPCBL5524 system BIOS stored in on-board flash becomes corrupted, the ZT 5524 / MPCBL5524 can boot from this BIOS Recovery module and flash memory can be reprogrammed via the FLASH.EXE program.

The board is shipped with the BIOS Recovery module installed in a 32-pin socket (U9). If the EPROM is removed for any reason, ensure that it is correctly oriented when reinstalled. Orient the beveled corner of the BIOS Recovery module as shown in the “BIOS Recovery Socket Location” figure below.

Table 13. BIOS Recovery Socket Location



7.1.1 Forcing a Boot from the BIOS Recovery Module

To force a boot from the BIOS recovery module:

1. Remove the board from the enclosure.
2. Close switch SW4-2 to boot from the BIOS Recovery Module.
3. Make sure flash write protection is disabled (SW4-1 = open).

Note: For more information on SW4-1 and SW4-2, see "Switch Descriptions" on page 40.

4. Re-insert the board in the enclosure and apply power to the board. The system should boot.
5. See the "Flash Utility Program" on page 53 for detailed instructions on reprogramming the on-board flash with the BIOS.
6. After flashing the BIOS, turn off power, remove the board from the enclosure, and open switch SW4-2 to boot from flash.
7. If desired, enable flash write protection by closing switch SW4-1.
8. Re-insert the board in the enclosure.

7.1.2 Flash Utility Program

FLASH.EXE is a utility program that is available for download free from Intel. Run FLASH.EXE to modify or restore the BIOS in the on-board flash memory. FLASH.EXE eliminates the need for a PROM programmer and for removing boards and chips from the system. A link to FLASH.EXE is available in Appendix E, "User Documentation."

Before attempting to program the flash, make sure that switch SW4-1 (Flash Write Protect/Write Enable) is open.

To reprogram the BIOS on the ZT 5524 / MPCBL5524, use the following syntax at a DOS prompt:

```
FLASH  /b  BIOS.XXX
```

where **BIOS.XXX** is the BIOS image for the ZT 5524 / MPCBL5524. See the *Intel NetStructure Embedded BIOS (AMI Core) Software Manual* for more information on the Flash utility. A link to this document is available in Appendix E, "User Documentation."

Note: The following error is displayed the first time the ZT 5524 / MPCBL5524 is booted after its BIOS is updated: "0105: CMOS/GPNV CheckSum Bad." This error message is not a defect. When you use the BIOS update process using the flash.exe utility, the system clears CMOS to force a reload of CMOS defaults. So the CMOS checksum does not match the values within the BIOS the first time the board reboots after an update. This error message is not displayed the next time the ZT 5524 / MPCBL5524 is rebooted.

System Monitoring and Alarms 8

The ZT 5524 / MPCBL5524 performs system monitoring and alarming functions using the flexible, industry standard, Intelligent Platform Management Interface (IPMI). The ZT 5524 / MPCBL5524 comes equipped with an on-board Baseboard Management Controller (BMC) chip, IPMI and IPMB J-connector pinouts, and IPMI v1.5 firmware already installed on the board. Some of the functions available on this board through the IPMI interface include:

- Monitoring of the CPU and board temperatures with critical and non-critical alerting
- Monitoring of the voltage rails (+5 V, +/- 12 V, +3.3 V, +2.5 V, VBAT, CPU core voltages) with critical and non-critical alerting
- Remote reset and shutdown of the board
- Monitoring of ejector switches for hot swap functionality
- Intel IPMI driver and firmware provide features for hot swap
- Hot swap interaction for redundant host capabilities
- Monitoring and event recording of critical errors
- Board power up/power down by monitoring BD_SEL# lines on the CompactPCI backplane
- Dual domain capability (this refers to the ability of the BMC to act as either a BMC or as an SMC when there is already a BMC present on the IPMI bus)
- Interface to dual IPMB lines (IPMB 0 and IPMB 1)
- Monitoring and reporting of sensors from the ZT 4901 mezzanine board.

The firmware on the board is also exercised with the Intel® IPMI v1.5 Conformance Test Suite (ICTS) before shipping. This test suite is available for free at:

http://developer.intel.com

In order to take advantage of the features provided by the firmware, IPMI aware applications must be developed. Information on IPMI v1.5 is provided at:

http://www.intel.com/design/servers/ipmi/spec.htm

8.1 SMBus Address Map

The table below lists the function and address of each SMBus device used on the ZT 5524 / MPCBL5524.

Table 14. SMBus Address Map (Sheet 1 of 2)

Device	Function	I^2C Address
CSB5	Master Controller	N/A
Memory DIMM	DIMM presence and size	:50
CNB30LE	N/A	:C0

Table 14. SMBus Address Map (Sheet 2 of 2)

Gigabit Ethernet Channels A/B	N/A	Set by external TCO software
BMC SCL4	Master Controller	TBD
ADM1026	Slave	58
RPIO FRU Device	Slave	A8
Mezzanine Card FRU Device	Slave	AA
Mezzanine RPIO Card FRU Device	Slave	AC
ADM1026 Mezzanine	Slave	5A
10/100 Ethernet Controller C	Slave	84

Specifications A

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5524 / MPCBL5524. It includes illustrations of the board dimensions and connector locations, as well as connector descriptions and pinout tables.

A.1 Electrical and Environmental Specifications

The subsequent topics provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

A.1.1 ZT 5524 / MPCBL5524 Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5524 / MPCBL5524 at these maximums. See the "DC Operating Characteristics" topic in this appendix for operating conditions.

Table 15. ZT 5524 / MPCBL5524 Maximum Ratings

Item	Limit
Supply Voltage, Vcc:	5.5 V
Supply Voltage, Vcc3:	4.5 V
Supply Voltage, AUX +:	15 V
Storage Temperature:	-40° to +85° C
Non-Condensing Relative Humidity:	<95% at 40° C
Ethernet Cable Length	Channel A and B: 75 meters. Channel C: 100 fmeters

A.1.1.1 Operating Temperature

Operating temperature is processor dependent. The operating temperature range is 0° C to 45° C. The ZT 5524 / MPCBL5524 comes from the factory with an integrated heat sink for cooling the processor. The heat sink requires 250 LFM (linear feet per minute) of airflow. The maximum power dissipation of each CPU is 13.2 W.

Caution: External airflow must be provided at all times during operation to avoid damaging the CPU modules. Intel strongly recommends use of a fan tray below the card rack to supply the external airflow.

A.1.2 DC Operating Characteristics

Table 16. Power Consumption

Voltage (VDC)	Single 933 MHz, 1GB SDRAM		Dual 933 MHz, 1GB SDRAM	
	Power (W)		Power (W)	
	Typical	Max	Typical	Max
5.00 V, +5%, -3%	9	13	17	22
3.30 V, +5%, -3%	13.5	22	13.5	22
NOTE: Add 3 W for each additional 1GB Memory Module.				

A.1.3 Battery Backup Characteristics

Table 17. Battery Backup Characteristics

Item	Characteristic
Battery Voltage:	3 V
Battery Capacity:	285 mAh
Real-Time Clock Requirements:	8 µA max. (Vbat = 3 V, Vcc= 0 V)
Real-Time Clock Data Retention:	35,625 hrs/ 4.0 yrs min. (not powered), 6.0 yrs min. (with Vcc power applied 8 hrs/day)
Electrochemical Construction:	Poly carbonmonofluoride
CAUTION: The ZT 5524 / MPCBL5524 contains a lithium battery. This battery is not a field-replaceable unit. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the ZT 5524 / MPCBL5524 to Intel for battery service.	

A.2 ZT 5524 / MPCBL5524 Reliability

Board MTBF = 117936 hours (13.5 years) @ 40°C
MTTR: 3 min.

A.3 Mechanical Specifications

This section includes the following mechanical specifications for the ZT 5524 / MPCBL5524:

- Board dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)

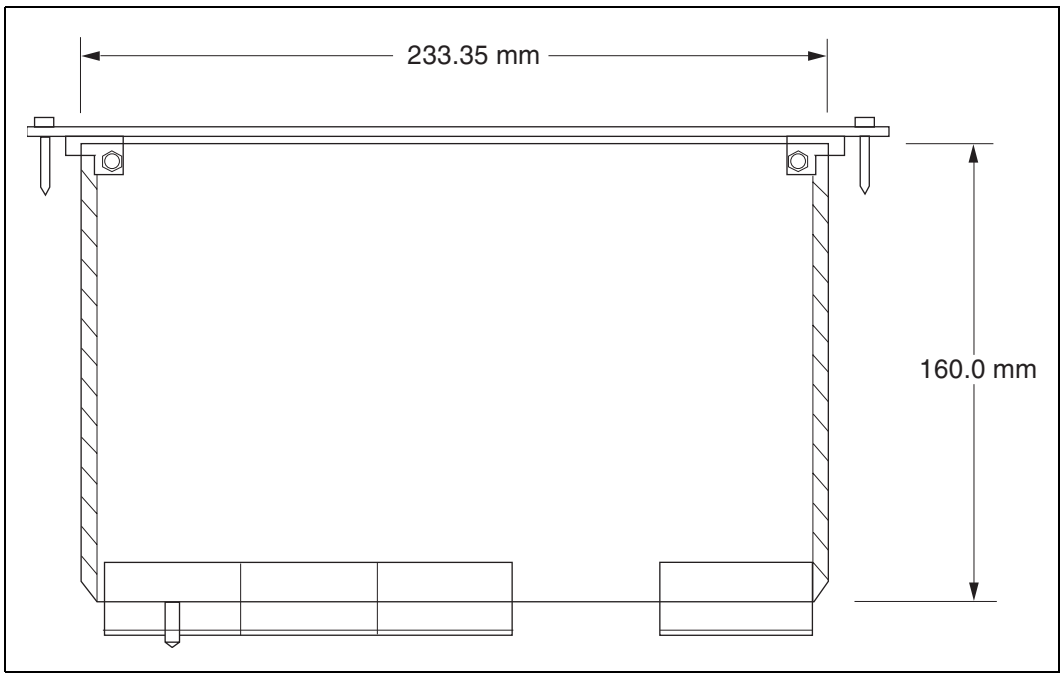
A.3.1 Board Dimensions and Weight

The ZT 5524 / MPCBL5524 meets the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters. In a CompactPCI enclosure with 0.8 inch spacing, the ZT 5524 / MPCBL5524 requires two card slots.

Mechanical dimensions are shown in Figure 8 and are outlined below.

Board Length	160 mm (6.24 in)
Board Width	233.35 mm (9.1 in)
Board Height:	34.80 mm (1.37 in) typ., measuring from the tallest secondary side component to the tallest primary side component
Board Weight:	Dual processors: .57 kg (1.25 pounds) Single processor: .50 kg (1.1 pounds)

Figure 8. ZT 5524 / MPCBL5524 Board Dimensions



A.3.2 ZT 5524 / MPCBL5524 Connectors

As shown in the Figure 9, “Connector Locations” on page 60, the ZT 5524 / MPCBL5524 includes several connectors to interface with application-specific devices. A brief description of each connector is given in the “Connector Assignments” table. A detailed description and pinout for each connector is given in the following topics.

Table 18. Connector Assignments

Connector	Function
J1, page 61	CompactPCI Bus Connector (125-pin, 2 mm x 2 mm, female)
J2, page 62	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
J3, page 63	Rear-Panel Gigabit Ethernet Connector (95-pin 2 mm x 2 mm, female)
J5, page 63	Rear-Panel User I/O Connector (110-pin, 2 mm x 2 mm, female)
J6, page 65	Universal Serial Bus Connector (4-pin, USB, Port 0)
J7, page 65	Ethernet A and B Connector (Dual RJ-45)
J8, page 66	Keyboard/Mouse Connector (6-pin DIN)
J9, page 66	COM1 Serial Port (RJ-45)
J10, page 67	Video Interface (15-pin, D-Shell)
J11, page 67	Ethernet C Connector (8-pin, RJ-45)
J12, page 67	Hot Swap Ejector Switch Connector (3-pin surface-mount)
J13, page 68	SDRAM Connector (DIMM)
J17, page 68	I/O Mezzanine Interface (190-pin female vertical)
J18, page 70	ISP Programming (10-pin female vertical)
J19, page 70	On-board EIDE Interface (50-pin female vertical)

Figure 9. Connector Locations

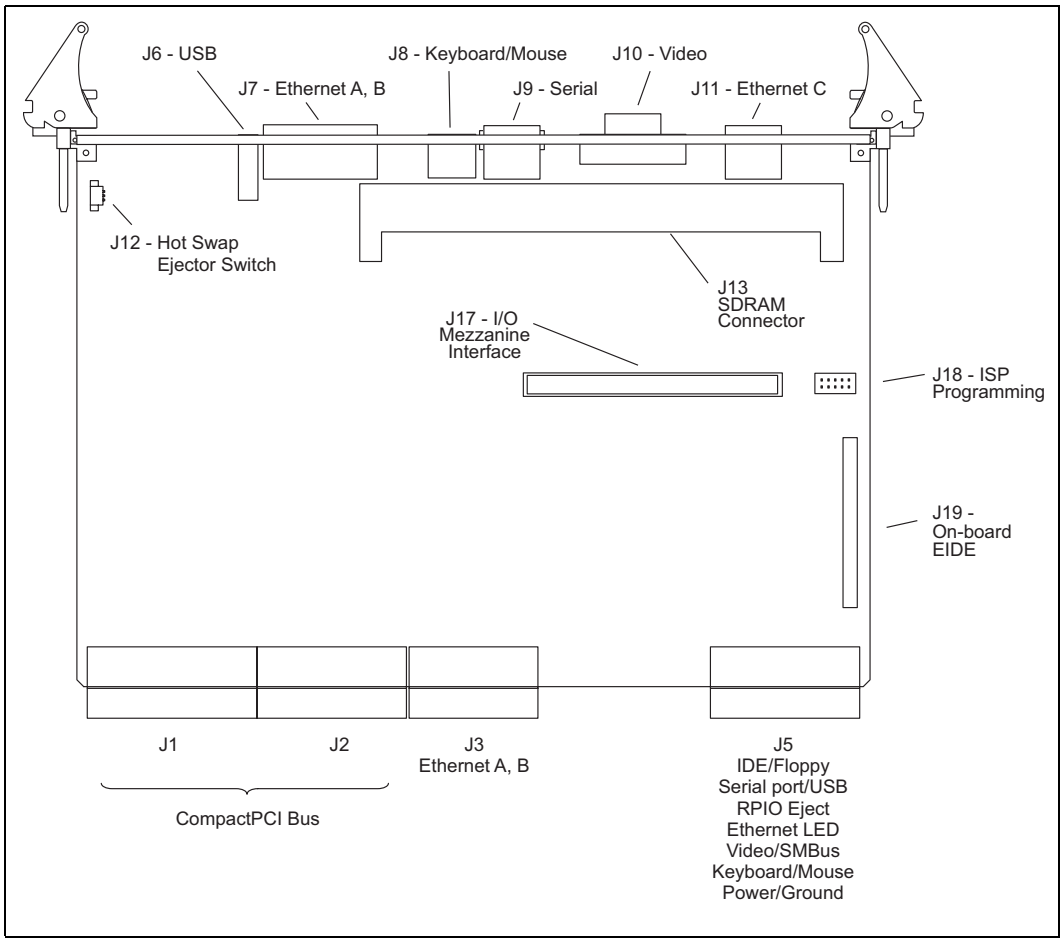
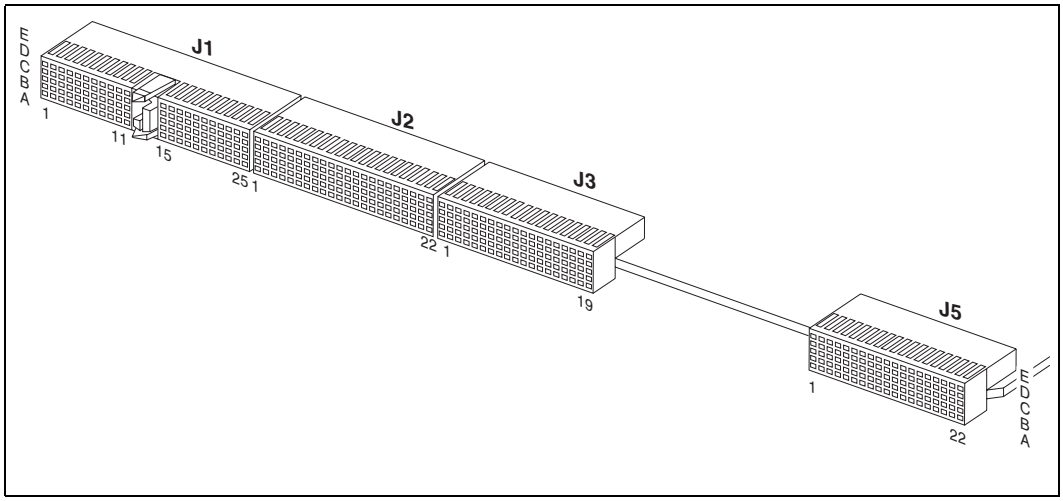


Figure 10. Backplane Connectors Pin Locations



A.3.2.1 J1 (CompactPCI Bus Connector)

J1 is a 125-pin, 2 mm x 2 mm, female 32-bit CompactPCI connector. Rows 12-14 are used for connector keying. See the "J1 CompactPCI Bus Connector Pinout" table for pin definitions and Figure 10, "Backplane Connectors Pin Locations" on page 60 for pin placement.

Table 19. J1 CompactPCI Bus Connector Pinout

Pin	A	B	C	D	E	F
25	5V	REQ64#	ENUM#	3.3V	5V	Ground
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	
23	3.3V	AD[4]	AD[3]	5V	AD[2]	
22	AD[7]	GND	3.3V	AD[6]	AD[5]	
21	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	
19	3.3V	AD[15]	AD[14]	GND	AD[13]	
18	SERR#	GND	3.3V	PAR	C/BE[1]#	
17	3.3V	NC	NC	GND	PERR#	
16	DEVSEL#	GND	V(I/O)	STOP#	NC	
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	
12-14	KEY AREA					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	Shield
10	AD[21]	GND	3.3V	AD[20]	AD[19]	
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	
6	REQ#	GND	3.3V	CLK	AD[31]	
5	NC	NC	PCI_RST#	GND	GNT#	
4	NC	HEALTHY#	V(I/O)	NC	NC	
3	INTA#	INTB#	INTC#	5V	INTD#	
2	NC	5V	NC	NC	NC	
1	5V	-12V	NC	+12V	5V	
Pin	A	B	C	D	E	F

= long pins = short pins All others = medium-length pins

NOTE: Row F GND pins are long length, as is standard for CompactPCI.

A.3.2.2 J2 (CompactPCI Bus Connector)

J2 is a 110-pin, 2 mm x 2 mm, right-angle female 64-bit CompactPCI connector. See the "J2 CompactPCI Bus Connector Pinout" table for pin definitions and Figure 10, "Backplane Connectors Pin Locations" on page 60 for pin placement.

Table 20. J2 CompactPCI Bus Connector Pinout

Pin #	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	Ground Shield
21	CLK6	NC	NC	NC	NC	
20	CLK5	NC	NC	GND	NC	
19	NC	NC	SMB DATA	SMB CLK	SMB ALERT	
18	NC	NC	NC	GND	NC	
17	NC	GND	PRST#	REQ7#	GNT6#	
16	NC	NC	DEG#	GND	NC	
15	NC	GND	FAL#	REQ5#	GNT5#	
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	
5	C/BE[5]#	64EN-	V(I/O)	C/BE[4]#	PAR64	
4	V(I/O)	NC	C/BE[7]#	GND	C/BE[6]#	
3	CLK4	GND	GNT3#	REQ4#	GNT4#	
2	CLK2	CLK3	NC	GNT2#	REQ3#	
1	CLK1	GND	REQ1#	GNT1#	REQ2#	
Pin #	A	B	C	D	E	F

A.3.2.3 J3 (Rear-Panel Gigabit Ethernet Connector)

J3 is a 95-pin, 2 mm x 2 mm, female connector providing rear-panel access to Ethernet A and Ethernet B. See the "J3 Rear-Panel Gigabit Ethernet Connector Pinout" table for pin definitions and Figure 10, "Backplane Connectors Pin Locations" on page 60 for pin placement.

Table 21. J3 Rear-Panel Gigabit Ethernet Connector Pinout

Pin #	A	B	C	D	E	F
19	NC	NC	NC	NC	NC	Ground Shield
18	LPA_DA+	LPA_DA-	GND	LPA_DC+	LPA_DC-	
17	LPA_DB+	LPA_DB-	GND	LPA_DD+	LPA_DD-	
16	LPB_DA+	LPB_DA-	GND	LPB_DC+	LPB_DC-	
15	LPB_DB+	LPB_DB-	GND	LPB_DD+	LPB_DD-	
14	RESV	RESV	RESV	RESV	RESV	
13	RESV	RESV	RESV	RESV	RESV	
12	RESV	RESV	RESV	RESV	RESV	
11	RESV	RESV	RESV	RESV	RESV	
10	RESV	RESV	RESV	RESV	RESV	
9	RESV	RESV	RESV	RESV	RESV	
8	RESV	RESV	RESV	RESV	RESV	
7	RESV	RESV	RESV	RESV	RESV	
6	RESV	RESV	RESV	RESV	RESV	
5	RESV	RESV	RESV	RESV	RESV	
4	RESV	RESV	RESV	RESV	RESV	
3	RESV	RESV	RESV	RESV	RESV	
2	RESV	RESV	RESV	RESV	RESV	
1	RESV	RESV	RESV	RESV	RESV	
Pin #	A	B	C	D	E	F

A.3.2.4 J5 (Rear-Panel User I/O Connector)

J5 is a 110-pin, 2 mm x 2 mm, female connector providing rear-panel access to the following:

- IDE
- COM port
- Ethernet LED
- Video
- Keyboard/Mouse
- Floppy
- RPIO Eject
- USB

- SMBus
- Power and Ground

See the "J5 Rear-Panel User I/O Connector Pinout" table for pin definitions and Figure 10, "Backplane Connectors Pin Locations" on page 60 for pin placement.

Table 22. J5 Rear-Panel User I/O Connector Pinout

Pin #	A	B	C	D	E	F
22	USB0+	USB0-	SW-5V	USB1+	USB1-	Ground Shield
21	SW-3.3V	GND	GND	GND	GND	
20	RED	GND	H-SYNC	GND	SMBD	
19	GND	SW-5V	GND	SW-5V	SMBC	
18	GREEN	GND	V-SYNC	GND	SMBA-	
17	GND	RESV	RPIO_PRESENT#	RESV	IPMB PWR	
16	BLUE	GND	DDCCLK	KBDAT	KBCLK	
15	GND	SW-5V	DDCDAT	MSDAT	MSCLK	
14	S1RTS	S1CTS	S1RIN	S1DTR	ENETA-LINK	
13	S1DCD	S1TXD	S1RXD	S1DSR	ENETA-ACT	
12	S2RTS	S2CTS	S2RIN	S2DTR	ENETB-LINK	
11	S2DCD	S2TXD	S2RXD	S2DSR	ENETB-ACT	
10	TRK0-	WP-	RDATA-	HDSEL-	DSKCHG-	
9	MTR1-	DIR-	STEP-	WDATA-	WGATE-	
8	DENSL	INDEX-	MTR0-	DR1-	DR0-	
7	CS1S-	CS3S-	DA1	RPELED	RPEJECT-	
6	PWRGD	SPKR	NMI-	DA0	DA2	
5	DDRQ	IORDY	DI0W-	DDACK	DIOR-	
4	DD14	DD0	IDE_ACT	DD15	DRV_IRQ	
3	DD3	DD12	DD2	DD13	DD1	
2	DD9	DD5	DD10	DD4	DD11	
1	PBRST-	DRST-	DD7	DD8	DD6	
Pin #	A	B	C	D	E	F

A.3.2.5 J6 (USB Connectors)

J6 is a 4-pin, Port 0 USB Interface connector on the ZT 5524 / MPCBL5524's faceplate. USB (Port 1) is directed out rear-panel I/O connector J5. See the "J6 USB Connector Pinout" table for pin definitions. For a diagram of the faceplate, see Figure 1, "ZT 5524 / MPCBL5524 Faceplate" on page 13.

Table 23. J6 USB Connector Pinout

Pin#	Function
1	+5 V Fused
2	DATA-
3	DATA+
4	GND

A.3.2.6 J7 (Ethernet Connectors)

J7 is a dual RJ-45 connector on the ZT 5524 / MPCBL5524's faceplate providing 10 Mbps (10Base-T), 100 Mbps (100Base-T), and 1000 Mbps (1000Base-T) protocols. Two LEDs are located inside each RJ-45 connector:

- Off indicates 10 Mbps
- Green indicates 100 Mbps
- Amber indicates 1000 Mbps
- Green indicates link
- Flashing green indicates activity

See the "J7 Ethernet Connectors Pinout" table for pin definitions.

These Ethernet signals can be directed out J3 to the backplane. See "Ethernet/Geographic Addressing (E4h)" on page 77 for more information.

Table 24. 7 Ethernet Connectors Pinout

Pin#	Function
1	MDIO0
2	MDIO0-
3	MDIO1
4	MDIO2
5	MDIO2-
6	MDIO1-
7	MDIO3
8	MDIO3-

A.3.2.7 J8 (Keyboard/Mouse Connector)

J8 is a 6-pin, right angle, DIN connector providing for standard PS/2 style keyboard and mouse device connection on the ZT 5524 / MPCBL5524's faceplate. For a diagram of the faceplate, see Figure 1, "ZT 5524 / MPCBL5524 Faceplate" on page 13.

Keyboard and mouse signals are also directed out rear-panel I/O connector J5. See the following table for pin definitions.

Table 25. J8 Keyboard and Mouse Connector Pinout

Pin#	Function
1	KBDAT
2	MSDAT
3	GND
4	Vcc (Fused)
5	KBCLK

A.3.2.8 J9 (COM1 Serial Port)

J9 is an 8-pin, RJ-45 connector providing the COM1 interface on the ZT 5524 / MPCBL5524's faceplate. COM1 interface signals are also directed out rear-panel I/O connector J5. See the following table for pin definitions.

Table 26. J9 COM1 Serial Port Pinout

Pin#	Function
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS

A.3.2.9 J10 (Video Interface)

J10 is an HD15, 15-pin, female, D-shell connector providing an interface for VGA signals on the ZT 5524 / MPCBL5524's faceplate. See the following table for pin definitions.

Table 27. J10 Video Interface Pinout

Pin#	Signal	Pin #	Signal	Pin#	Signal
1	RED	6	RGND	11	NC
2	GRN	7	GGND	12	SDA
3	BLUE	8	BGND	13	HSYNC
4	NC	9	VCC	14	VSYNC
5	DGND	10	SGND	15	SCL

A.3.2.10 J11 (Ethernet Connector)

J11 is an RJ-45 connector on the ZT 5524 / MPCBL5524's faceplate providing 10 Mbps (10Base-T) and 100 Mbps (100Base-T) protocols. Two LEDs are located inside the RJ-45 connector:

- Off indicates 10 Mbps
- Green indicates 100 Mbps
- Green indicates link
- Flashing green indicates activity

See the following table for pin definitions.

These Ethernet signals can be directed out J5 to the backplane. See "Ethernet/Geographic Addressing (E4h)" on page 77 for more information.

Table 28. J11 Ethernet Connectors Pinout

Pin#	Function
1	MD0
2	MD0-
3	MD1
4	MD2
5	MD2-
6	MD1-
7	MD3
8	MD3-

A.3.2.11 J12 (Hot Swap Ejector Switch Connector)

J12 is a 3-pin, vertical, 1.25 mm (.049 in) surface-mount connector connecting the hot swap switch to the board's lower ejector mechanism. This switch is tied to logic on the ZT 5524 / MPCBL5524 to sense a board extraction or insertion. See the following table for pin definitions.

Table 29. J12 Hot Swap Ejector Switch Connector Pinout

Pin#	Function
1	Common
2	Latched
3	Unlatched

A.3.2.12 J13 (SDRAM Connector)

J13 is a 168-pin, right angle connector that accommodates a standard 3.3 V registered dual inline memory module (DIMM) socket SDRAM module used for system memory. The ZT 5524 / MPCBL5524 has four DIMM sockets in place of the single J13 connector on the ZT 5524 / MPCBL5524.

A.3.2.13 J17 (I/O Mezzanine Interface)

J17 is a 190-pin, female, 2 mm (.079 in) center, vertical header providing an interface for the optional ZT 4901 expansion module designed to support dual CompactPCI segment RH mode. See the *ZT 4901 Technical Product Specification* for more information.

See the following table for pin definitions.

Table 30. J17 I/O Mezzanine Interface Connector Pinout (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	IPMB_PWR	51	B1_PAD13	101	B1_PAD43	151	DDP8
2	SYS_SDA	52	B1_PAD14	102	B1_PAD44	152	DDP7
3	BMC_SMBALERT-	53	B1_PAD10	103	B1_PAD41	153	SPARE_PAL1
4	SYS_SCL	54	B1_PAD12	104	B1_PAD42	154	S2_TRNSFRRQ
5	SBC_HSPOR-	55	B1_PAD9	105	B1_PAD39	155	SPARE_PAL2
6	MEZ_HSPOR-	56	B1_PAD11	106	B1_PAD40	156	S2_TRNSFRNW
7	SBC_PWROK	57	B1_CBE-0	107	B1_PAD37	157	SPARE_PAL3
8	MEZ_PWROK	58	B1_PAD8	108	B1_PAD38	158	S2_MODELCK
9	B3_INTAO-	59	B1_PAD7	109	B1_PAD35	159	NC
10	B3_INTCO-	60	B1_PAD6	110	B1_PAD36	160	S2_BUS_Q
11	B3_INTBO-	61	B1_PAD5	111	B1_PAD33	161	S2_ARB_EN
12	B3_INTD-	62	B1_PAD4	112	B1_PAD34	162	S2_ARB_LCKD
13	B1_PAD31	63	B1_PAD3	113	B1_CBE-1	163	MEZ_VIO
14	B1_PAD30	64	B1_PAD2	114	B1_PAD32	164	S2_MODE_CH-
15	B1_PAD29	65	B1_PAD1	115	S2_INTR_EN	165	GND
16	B1_PAD28	66	B1_PAD0	116	S2_SYSEN-	166	S2_BMC_XFR_RQ
17	B1_PAD27	67	MEZ_INTB-	117	BMC_PWRCTL-	167	SBC_RXP_A
18	B1_PAD26	68	MEZ_INTA-	118	S2_RSS_LTCH-	168	NC
19	B1_PAD25	69	B1_GNT-2	119	S2_PBRST-	169	SBC_RXN_A

Table 30. J17 I/O Mezzanine Interface Connector Pinout (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
20	B1_PAD24	70	B1_REQ-2	120	S2_ENUM-	170	NC
21	B1_PAD23	71	B1_GNT-3	121	MEZ_INTD-	171	GND
22	B1_PAD22	72	B1_REQ-3	122	CSEL2	172	NC
23	B1_PAD21	73	B1_M66EN	123	PDASP	173	SBC_TXP_A
24	B1_PAD20	74	B1_ACK64-	124	PDIAG	174	NC
25	IOXB_IDSEL	75	B1_REQ64-	125	DAP2	175	SBC_TXN_A
26	IOXA_IDSEL	76	B0_PCIRST-	126	D_RSTDRV-	176	NC
27	B1_PAD19	77	MEZ_PRES-	127	IRQ14	177	GND
28	B1_PAD18	78	B1_PAR64	128	DAP0	178	NC
29	MEZ_INTC-	79	B1_CBE-5	129	CS1P-	179	SBC_RXP_B
30	B1_PAD16	80	B1_CBE-4	130	DAP1	180	NC
31	B1_PAD17	81	B1_PAD63	131	CS3P-	181	SBC_RXN_B
32	B1_FRAME-	82	B1_CBE-6	132	PDACK-	182	NC
33	B1_CBE-3	83	B1_PAD61	133	PIORDY	183	GND
34	B1_STOP-	84	B1_PAD62	134	PDREQ-	184	NC
35	B1_CBE-2	85	B1_PAD59	135	PDIOW-	185	SBC_TXP_B
36	B1_TRDY-	86	B1_PAD60	136	PDIOR-	186	SBC_BYPASS_A-
37	B1_PAR	87	B1_PAD57	137	DDP15	188	IPMB_PWR3
38	B1_PERR-	88	B1_PAD58	138	DDP0	189	GND
39	B1_IRDY-	89	B1_PAD55	139	DDP14	190	SBC_BYPASS_B-
40	GND	90	B1_PAD56	140	DDP1		
41	B1_DEVSEL-	91	B1_PAD53	141	DDP13		
42	IOXCLKB	92	B1_PAD54	142	DDP2		
43	GND	93	B1_PAD51	143	DDP12		
44	GND	94	B1_PAD52	144	DDP3		
45	IOXCLKA	95	B1_PAD49	145	DDP11		
46	B1_CBE-1	96	B1_PAD50	146	DDP4		
47	GND	97	B1_PAD47	147	DDP10		
48	B1_LOCK-	98	B1_PAD48	148	DDP5		
49	B1_PAD15	99	B1_PAD45	149	DDP9		
50	B1_SERR-	100	B1_PAD46	150	DDP6		

A.3.2.14 J18 (ISP Programming Interface)

J18 is a dual-row 10-pin, female, 2 mm (.079 in) center, vertical header providing an on-board ISP interface. See the following table for pin definitions.

Table 31. J18 ISP Programming Interface

Pin	Signal Name
1	GND
2	TDO-
3	GND
4	TDI
5	GND
6	TCK
7	GND
8	MODE
9	VCC3

A.3.2.15 J19 (EIDE Interface)

J19 is a dual-row 50-pin, female, 2 mm (.079 in) center, vertical socket providing an on-board EIDE interface. See the following table for pin definitions.

Table 32. J19 EIDE Interface Pinout (Sheet 1 of 2)

Pin#	Signal
1	RST-
2	GND
3	DDP7
4	DDP8
5	DDP6
6	DDP9
7	DDP5
8	DDP10
9	DDP4
10	DDP11
11	DDP3
12	DDP12
13	DDP2
14	DDP13
15	DDP1
16	DDP14
17	DDP0
18	DDP15

Table 32. J19 EIDE Interface Pinout (Sheet 2 of 2)

Pin#	Signal
19	GND
20	NC
21	PDREQ-
22	GND
23	PDIOW-
24	GND
25	PDIOR-
26	GND
27	PDIORDY
28	CSEL
29	PDACK-
30	GND
31	IRQ14
32	IOCS16-[1]
33	DAP1
34	PDIAG
35	DAP0
36	DAP2
37	CS1P-
38	CS3P-
39	PDASP
40	CS3P-
41	VCC
42	VCC
43	GND
44	NC
NOTE: [1]IOCS16- has 10kΩ pullup to VCC3 (+3.3V)	

System Registers B

The ZT 5524 / MPCBL5524 provides several system registers to control and monitor a variety of functions on the ZT 5524 / MPCBL5524. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers: the system BIOS may be relying on the state of the bits under their control.

B.1 System Register Definitions

The system registers are accessible as follows:

Table 33. System Register Definitions

I/O Address	Register Name	Default Value	Access	Size
78h, page 72	Flash Control	0x00	R/W	8 bits
79h, page 73	Watchdog	0x00	R/W	8 bits
80h, page 75	BIOS POST Codes	0x00	WO	8 bits
E1h, page 76	ENUM, WD NMI Status, PWR Supply Status	0x00	RO	8 bits
E2h, page 76	Board ID	0x00	R/W	8 bits
E3h, page 76	Switch Monitors	0x00	RO	8 bits
E4h, page 77	Ethernet/Geographic Addressing	0x00	R/W	8 bits
E5h, page 78	Video/LED Control	0x00	R/W	8 bits
E6h, page 78	HCINDEX - Host Control Index	0x00	R/W	8 bits
E7h, page 79	HCDATA - Host Control Function Data	NA	R/W	8 bits
E8h, page 79	INT- Interrupt Status and Mask Register	04h	RO, R/W	8 bits

B.1.1 Flash Control (78h)

I/O Address	78h
Default Value	0x00
Size	8 bits
Attribute	R/W

Note: This register is reset to 00h on init or reset. The BIOS resides in page 000.

Table 34. Flash Control Bit Descriptions

Bit	Description
7	BIOS Recovery Module Override Bit This bit supersedes the Boot Source switch (SW4-2, see page 41). If the BIOS Recovery Module Override bit is set to 1, then the Boot Source switch has no affect on the boot device, and the ZT 5524 / MPCBL5524 boots from onboard flash. See Chapter 7, "BIOS Recovery," for more information. 0=SW4-2 selects boot source 1= boot from onboard flash
6	Page 2 Flash A24 (512 KByte page)
5	Page 1 Flash A23 (512 KByte page)
4	Page 0 Flash A22 (512 KByte page)
3	Reserved. These bits are reserved and should be written as logical 0s when this register is modified.
2	Device Select. This is a read/write scratch pad bit that has no effect on the ZT 5524 / MPCBL5524.
1	Flash Write Enable.
0	Reserved. These bits are reserved and should be written as logical 0s when this register is modified.

B.1.2 Watchdog (79h)

I/O Address	79h
Default Value	0x00
Size	8 bits
Attribute	R/W

Table 35. Watchdog Bit Descriptions (Sheet 1 of 2)

Bit	Description
7	**Stage 2 Monitor (Reset Monitor)** Monitors the second stage (Reset) timer status. Read Value: 0= Watchdog has not timed out since power up or since this bit was last set to 0 1= Watchdog reset timeout has occurred since power up or since this bit was last set to 0 Write Value: 0= Sets this bit to 0 1= No effect Power-Up Value: 0 A hard reset not caused by a watchdog timeout sets this bit to 0.
6	**Stage 1 Monitor (NMI Monitor)** Monitors the first stage (NMI) timer status. Read Value: 0= Watchdog has not timed out since power up or since this bit was last set to 0 1= Watchdog timed out and NMI output was asserted Write Value: 0= Sets this bit to 0 1= No effect Power-Up Value: 0 A hard reset sets this bit to 0.
5	Stage 2 Enable Enables second stage (Reset) activation on timeout. Read Value: 0= Reset activation on timeout disabled 1= Reset activation on timeout enabled Write Value: 0= Reset operation of the watchdog is not enabled. When the watchdog times out, the Stage 2 Monitor bit is not set to 1 and the Reset output is not asserted 1= Reset operation of the watchdog is enabled. When and if the watchdog times out: The Reset output asserts The Stage 2 Monitor bit is set to 1 and stays high until set to 0 by software Reset action occurs approximately 250 ms after NMI Power-Up Value: 0 Value After Timeout: 0 (doesn't re-arm) A hard reset sets this bit to 0.

Table 35. Watchdog Bit Descriptions (Sheet 2 of 2)

4	Stage 1 Enable Enables NMI activation on timeout. Read Value: 0= Disabled 1= Enable NMI activation on timeout Write Value: 0= Disable NMI operation of the watchdog. When the watchdog times out, the Stage 1 Monitor bit is not set to 1 and the NMI output is not asserted 1= Enable NMI operation of the watchdog. When and if the watchdog times out: The Stage 1 output (NMI) occurs after the period of time specified by the Terminal Count bits The Stage 1 Monitor bit is set to 1 and stays high until set to 0 by software The Stage 2 Reset occurs approximately 250 ms after Stage 1 output, allowing the system software to take action before the reset occurs Power-Up Value: 0 Post Time-Out Value: 0 A hard reset sets this bit to 0.
3	NMI or INIT steering
2:0	**Terminal Count (TermCnt2…TermCnt0)** Read Value: Reflects the value written to bits 2 through 0 Write Value: These bits determine the terminal count of the watchdog The minimum timeout period is given. The watchdog times out in no less than the minimum value. The nominal timeout period is 30% longer than the minimum: 000 = 250 ms 100 = 32 s 001 = 500 ms 101 = 64 s 010 = 1 s 110 = 128 s 011 = 8 s 111 = 256 s Power-Up Value: 000 A hard reset sets this bit to 000.

B.1.3 BIOS POST Codes (80h)

I/O Address	80h
Default Value	0x00
Size	8 bits
Attribute	WO

Table 36. BIOS POST Codes Bit Description

Bit	Description
7:0	D7-D0. These bits correspond to eight green LEDs (labeled D0 through D7) on the bottom side of the PCB. The Port 80 bits report the BIOS POST (diagnostic) codes. These LEDs may not be visible if a “hot-swap shield” is installed on the bottom side on the PCB.

B.1.4 ENUM, WD NMI Status, PWR Supply Status (E1h)

I/O Address 0xE1h

Default Value 0x00

Size 8 bits

Attribute RO

Table 37. ENUM, WD NMI Status Bit Descriptions

Bit	Description
7	WD NMI Status
6	**ENUM-.** This bit reports that a hot swappable peripheral card has been installed or removed from the system. A logical 0 means that ENUM- is not asserted on the backplane. A logical 1 means that ENUM- is asserted on the backplane.
5:0	**Reserved.** These bits are reserved and should not be modified by the user.

B.1.5 Board ID (E2h)

Address Offset E2h

Default Value 0x00

Size 8 bits

Attribute R/W

Table 38. Board ID Bit Descriptions

Bit	Description
7:4	**Reserved**. These bits are reserved and should not be modified by the user.
3:0	**Board Revision.** This port is used to read the status of cuttable traces CT8, CT18, CT19, and CT20 to determine the current board revision (Revision 0 = Fh). The user should not change these cuttable traces since these values may be used by the system BIOS. These bits should be written as logical 0s when this register is modified.

B.1.6 Switch Monitors (E3h)

Address Offset E3h

Default Value 0x80

Size 8 bits

Attribute RO

Table 39. Switch Monitors Bit Descriptions

Bit	Description
7	**Flash Write-Protect Status.** This bit corresponds to the status of Flash Write Protect/Write Enable switch SW4-1 (see page 41). A logical 0 means that the flash is write-protected by SW4-1; a logical 1 means that the flash is *not* write-protected by SW4-1.
6	**Boot Source Monitoring.** This bit allows software to monitor the boot source as selected by SW4-2 (see page 41). When SW4-2 is closed (boot from BIOS Recovery socket U42), this bit reads back a 0. When SW4-2 is open (boot from the BIOS contained in on-board flash), this bit reads back a 1.
5:3	**Reserved.** These bits are reserved and should not be modified by the user.
2:1	**Software Configuration.** These bits are used to provide configuration information to the user's software by monitoring the status of the Software Configuration switch SW3 (see page 40). An open switch reads back a 0; a closed switch reads back a 1. The bits correspond to switch segments as follows: Bit 1 = SW3-2; Bit 2 = SW3-3
0	**Console Redirection Enable:** This bit reads the status of switch SW3-1 (see page 40). A logical 0 means that SW3-1 is open and console redirection is disabled. A logical 1 means SW4-4 is closed and console redirection is enabled

B.1.7 Ethernet/Geographic Addressing (E4h)

Address Offset	E4h
Default Value	0x00
Size	8 bits
Attribute	R/W

Table 40. Ethernet/Geographic Addressing Bit Descriptions

Bit	Description
7	**Reserved**. This bit is reserved and should not be modified by the user.
6	**Ethernet B Front/Rear Select.** This bit toggles Ethernet channel 2 (Ethernet B) connection between the faceplate and the backplane. This bit can be set in the BIOS setup screen. When this bit is set to logical 0, Ethernet Channel 2 is connected to the Ethernet faceplate connector J7 (see page 65). When this bit is set to logical 1, Ethernet Channel 2 is connected to J3 (see page 63) on the rear panel.
5	**Ethernet A Front/Rear Select.** This bit toggles Ethernet channel 1 (Ethernet A) connection between the faceplate and the backplane. This bit can be set in the BIOS setup screen. When this bit is set to logical 0, Ethernet channel 1 is connected to the Ethernet faceplate connector J7. When this bit is set to logical 1, Ethernet channel 1 is connected to J3 on the rear panel.
4:0	**Geographic Addressing.** CompactPCI defines several signal additions to the PCI specification. One of these is GA[4..0], used for geographic addressing on the backplane. Geographic addressing uniquely differentiates each board based on the physical slot into which it has been inserted. Each backplane connector in a CompactPCI system has a unique encoding for GA[4..0]. See the *CompactPCI Specification, PICMG 2.0 R3.0* for more information on geographic addressing. The bits correspond to signals as follows: Bit 0 = GA0; Bit 1 = GA1; Bit 2 = GA2; Bit 3 = GA3; Bit 4 = GA4. A logical 0 indicates that the corresponding GA pin is open. A logical 1 indicates that the corresponding GA pin is low (GND).

B.1.8 Video/LED Control (E5h)

Address Offset	E5h
Default Value	0x00
Size	8 bits
Attribute	WO

Table 41. Video/LED Control Bit Descriptions

Bit	Description
7:5	Reserved. These bits are reserved and should not be modified by the user.
4	**Video Front/Rear Selection.** This bit toggles video connection between the faceplate and the backplane. This bit can be set in the BIOS setup screen. When this bit is set to logical 0, video is connected to the faceplate connector J10. When this bit is set to logical 1, video is connected to J5 on the rear panel.
3:2	**User LED 1.** These bits set the status of User LED 1. Bit 3 affects the green LED as follows: 0=off 1=on Bit 2 affects the amber LED as follows: 0=off 1=on
1:0	**User LED 2.** These bits set the status of User LED 2. Bit 1 affects the green LED as follows: 0=off 1=on Bit 0 affects the amber LED as follows: 0=off 1=on

B.1.9 HCINDEX - Host Control Index (E6h)

I/O Address	E6h
Reset	PCIRST
Default Value	0x00
Size	8 bits
Attribute	R/W

Table 42. HCINDEX Bit Descriptions

Bit	Description
7:3	**Reserved -** Reserved for future use.
2:0	**Host Control Function Data Pointer** - This register provides the address offset for the HCDATA registers. This is the number listed in the HCINDEX Offset column in the Host Control Function Register table (see page 79).

B.1.10 HCDATA - Host Control Function Data (E7h)

I/O Address	E7h
Reset	PCIRST
Default Value	NA
Size	8 bits
Attribute	R/W

Table 43. HCDATA Bit Description

Bit	Description
7:0	This register provides access to the Host Control Function Registers. The particular register accessed is determined by the offset value in the HCINDEX register.

B.1.11 INT- Interrupt Status and Mask Register (E8h)

I/O Address	E8h
Reset	PCIRST
Default Value	04h
Size	8 bits
Attribute	RO, R/W

Table 44. INT Bit Descriptions

Bit	Description	Access	Default
7:6	Reserved.	None	XX
5	**ENUM Interrupt Mask.** If this bit is set, an external interrupt will not be issued when a device on the backplane asserts ENUM.	R/W	1
4	**ENUM Interrupt Flag.** If this bit is set, an interrupt has been issued because of ENUM being asserted by a device on the backplane. Clear at the source device.	RO	0
3	**CICBS Interrupt Mask.** If set, an interrupt will not be issued because of a change in the CICBS register (HCINDEX 03h).	R/W	1
2	**CICBS Flag.** If set, a change in the CICBS register has occurred. If the Interrupt Mask is cleared, an interrupt will be asserted. Write 1 to this bit to clear.	R/W1C	0
1	**CICAS Interrupt Mask.** If set, an interrupt will not be issued because of a change in the CICAS register (HCINDEX 01h).	R/W	1
0	**CICAS Flag.** If set, a change in the CICAS register has occurred. If the Interrupt Mask is cleared, an interrupt will be asserted. Write 1 to this bit to clear.	R/W1C	0

B.2 Host Control Function Registers

For added register security, an index and data register pair is used to access the Host Control Function (HCF) Registers. Each of these registers is addressed by the value in the HCINDEX Register at I/O Address E6h. Data access is provided via the HCDATA Register.

For example, to read the data in HCC, first write XXh, to HCINDEX. Then read HCDATA. The contents of HCC are mapped into HCDATA. HCINDEX and HCDATA registers are located on page 78.

Table 45. Host Control Function Registers

HCINDEX	Register Symbol	Register Name	Default Value	Access	Size	Reset
00h		Reserved	XXh	None	8 bits	None
01h	CICAS	CompactPCI Interface Controller A Status	00h	RO, W1C	8 bits	PWROK
02h	CICAC	CompactPCI Interface Controller A Command	00h	R/W, W1	8 bits	MRST
03h	CICBS	CompactPCI Interface Controller B Status	00h	RO, W1C	8 bits	PWROK
04h	CICBC	CompactPCI Interface Controller B Command	00h	R/W, W1	8 bits	MRST
05-FFh		Reserved	XXh	None		None

B.2.1 CICAS- CompactPCI Interface Controller A Status

HCINDEX 01h

Reset Not PWROK

Default Value 0x00

Size 8 bits

Attribute RO, W1C, R/W

Table 46. CICAS Bit Descriptions

Bit	Description	Access	Default
7:6	Reserved.	None	X
5	**Segment Reset.** If set, this bus segment is being held in reset by the PCI interface device or the CIC.	RO	0
4	**CICAC Write Enable.** If set, the CICAC may be written. If cleared, the CICAC is read only.	R/W	0
3	**Segment Quiesced (Owner)**. When in owner mode, if this bit is set, the bus segment is Quiesced; the arbiter is locked and the bus is idle. **Handover Requested (Drone).** When in drone mode, if this bit is set, the bus owner has requested a handover. This bit is cleared when the handover is complete. When this bit transitions from 0 to 1, the CICAS flag in the INT register will be set.	RO	0
2	**Mode Change**. If set, the bus segment interface has changed modes. When this bit transitions from 0 to 1, the CICAS flag in the INT register will be set.	W1C	0
1	**Owner**. If set, this bus segment interface is in owner mode	RO	1: Owner 0: Drone
0	**RH**. If set, this bus segment interface is in a Redundant Host slot	RO	1: RH 0: Non-RH

B.2.2 CICAC- CompactPCI Interface Controller A Command

HCINDEX	02h
Reset	Not PWROK or MRST
Default Value	0x00
Size	8 bits
Attribute	R/W, W1

Note: Writes to this register must be made with extreme caution. In the interest of security, an unlock bit is included in the CICAS Register. That bit must be set in order to write to this register.

Table 47. CICAC Bit Descriptions

Bit	Description	Access	Default
7:6	**Reserved.** Reserved for future use.	None	X
5	**Arbiter Enable.** Read: 1 = the Arbiter is enabled 0 = the Arbiter is locked or disabled. Write: When in Drone mode, this bit is cannot be written and is cleared so that the arbiter remains locked. When in Owner mode, this bit may be written as a 1 to enable the Arbiter or as a 0 to lock the Arbiter. This bit is reset by MRST or when SYSEN# is high (inactive).	R/W	1: Owner 0: Drone
4	**Interrupts Enable.** When this bit is set, the backplane interrupts are enabled if the BIM is Owner. When in Drone mode, this bit is cannot be written. This bit is reset by MRST or when SYSEN# is high (inactive).	R/W	0
3	**Switchover Request.** When this bit is set, the CIC will request a switchover. Available to RH Owner and RH Drone. This bit cannot be written when the Mode Change bit is set. This bit is reset by MRST or by the Mode Change status bit or when RH# is low (asserted).	R/W	0
2	**Transfer Now Command.** When in RH Drone mode, if this bit is written as 1, the CIC will immediately remove ALT_SYSEN# from the bus owner. When in RH owner mode, if this bit is written as 1, the CIC will immediately assert ALT_SYSEN# to the RH. If there is an RH, this will result in a hostile takeover.	W1	0
1	**Mode Lock.** When this bit is set, the BIM is locked to whatever mode it is in. When in Owner mode, if this bit is set, the CIC will not disable the arbiter in the event of a fault. When in Drone mode, if this bit is set, the CIC will not respond to a mode change request and will not enter Owner mode, even if the Owner dies and is removed from the backplane. This condition will result in a backplane reset, however. RH Boards should have an onboard switch to preset this bit as 1 when a PCI reset occurs.	R/W	0(1)
0	**Backplane Bus Segment RESET MASK.** When this bit is 1, the PCI RST# to the backplane is masked and will not be asserted when in Owner Mode. The RST# will not be asserted in Drone Mode even if this bit is cleared.	R/W	0

B.2.3 CICBS- CompactPCI Interface Controller B Status

HCINDEX 03h

Reset Not PWROK

Default Value 0x00

Size 8 bits

Attribute RO, W1C, R/W

Table 48. CICBS Bit Descriptions

Bit	Description	Access	Default
7	**CIC B Present.** If this bit is set, there is a CIC B present.	RO	X
5	**Segment Reset.** If set, this bus segment is being held in reset by the PCI interface device or the CIC.	RO	0
4	**CICBC Write Enable.** If set, the CICBC may be written. If cleared, the CICBC is read only.	R/W	0
3	**Segment Quiesced (Owner).** When in owner mode, if this bit is set, the bus segment is Quiesced; the arbiter is locked and the bus is idle. **Handover Requested (Drone).** When in drone mode, if this bit is set, the bus owner has requested a handover. This bit is cleared when the handover is complete. When this bit transitions from 0 to 1, the CICBS flag in the INT register will be set.	RO	0
2	**Mode Change.** If set, the bus segment interface has changed modes. When this bit transitions from 0 to 1, the CICBS flag in the INT register will be set.	W1C	0
1	**Owner.** If set, this bus segment interface is in owner mode.	RO	1: Owner 0: Drone
0	**RH.** If set, this bus segment interface is in a redundant system slot.	RO -RH	1: RH 0: Non-RH

B.2.4 CICBC- CompactPCI Interface Controller B Command Register

HCINDEX 04h

Reset MRST or Not PWROK

Default Value 0x00

Size 8 bits

Attribute R/W, W1

Note: Writes to this register must be made with extreme caution. In the interest of security, an unlock bit is included in the CICBS Register. That bit must be set in order to write to this register.

Table 49. CICBC Bit Descriptions

Bit	Description	Access	Default
7:6	**Reserved.** Reserved for future use.	None	X
5	Arbiter Enable. Read: 1 = the Arbiter is enabled 0 = the Arbiter is locked or disabled Write: When in Drone mode, this bit is cannot be written and is cleared so that the arbiter remains locked. When in Owner mode, this bit may be written to a 1 to enable the Arbiter or to a 0 to lock the Arbiter. This bit is reset by MRST or when SYSEN# is high (inactive).	R/W	1: Owner 0: Drone
4	**Interrupts Enable.** When this bit is set, the backplane interrupts are enabled if the BIM is Owner. When in Drone mode, this bit is cannot be written. This bit is reset by MRST or when SYSEN# is high (inactive).	R/W	0
3	**Switchover Request.** When this bit is set, the CIC will request a switchover. Available to RH Owner and RH Drone. This bit cannot be written when the Mode Change bit is set. This bit is reset by MRST or by the Mode Change status bit or when RH# is low (asserted).	R/W	0
2	**Transfer Now Command.** When in RH Drone mode, if this bit is written to 1, the CIC will immediately remove ALT_SYSEN# from the bus owner. When in RH owner mode, if this bit is written to 1, the CIC will immediately assert ALT_SYSEN# to the RH. If there is an RH, this will result in a hostile takeover.	W1	0
1	**Mode Lock.** When this bit is set, the BIM is locked to whatever mode it is in. When in Owner mode, if this bit is set, the CIC will not disable the arbiter in the event of a fault. When in Drone mode, if this bit is set, the CIC will not respond to a mode change request and will not enter Owner mode, even if the Owner dies and is removed from the backplane. This condition will result in a backplane reset, however. RH Boards should have an onboard switch to preset this bit on when a PCI reset occurs.	R/W	0(1)
0	**Backplane Bus Segment RESET MASK.** When this bit is 1, the PCI RST# to the backplane is masked and will not be asserted when in Owner Mode. The RST# will not be asserted in Drone Mode even if this bit is cleared.	R/W	0

Reset C

This appendix discusses the various reset types and reset sources on the ZT 5524 / MPCBL5524. Because many embedded systems have different requirements for board reset functions, the incorporation of this sub-system on the ZT 5524 / MPCBL5524 has been designed to provide maximum flexibility.

C.1 Reset Types and Sources

The three reset types of the ZT 5524 / MPCBL5524 are listed below. The sources for each reset type are detailed in the following topics.

- **Backend Power Down:** The backend logic is powered off. All on-board devices are reset and PCIRST# is driven on the system backplane.
- **General Reset:** All on-board devices are reset and PCIRST# is driven on the system backplane.
- **NMI:** Non-maskable interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

C.1.1 Backend Power Down Sources

Board Extraction

When a board is extracted from an enclosure (specifically, when the short, board select pin is disengaged), the hot swap controller unconditionally removes backend power from the board and holds the ZT 5524 / MPCBL5524 in reset.

Low Voltage

When the 3.3 V, 5 V, and 12 V supply voltages are detected as below an acceptable operating limit, the Hot Swap controller unconditionally removes backend power and holds the ZT 5524 / MPCBL5524 in reset.

Overcurrent Fault

If a power fault condition (overcurrent) is detected, the BMC removes backend power and turns the Power/Reset LED indicator Amber. The ZT 5524 / MPCBL5524 is held in reset.

C.1.2 General Reset Sources

Push-Button Reset

When the System Reset button (SW1) on the faceplate is pressed, the ZT 5524 / MPCBL5524 resets itself and drives PCIRST on both CompactPCI buses. Sources for push-button reset include:

- Faceplate push-button Reset switch (SW1)
- Programmable watchdog timer

- CompactPCI bus push-button reset signal, PRST# (J2-C17)
- PBRST- (J3-A4) generated by an RPIO transition board (e.g., the ZT 4807 Rear-Panel Transition Board's push button-switch SW2

Note: For a diagram of the faceplate, see Figure 1, "ZT 5524 / MPCBL5524 Faceplate" on page 13.

C.1.3 NMI Sources

Abort Push Button (SW2)

When the Abort button (SW2) on the faceplate is pressed, it enables an NMI interrupt to the host CPU controller.

The Watchdog Timer (Port 79h)

The watchdog timer can be programmed through the Watchdog Register (Port 79h, bit 4) to generate a non-maskable interrupt if it is not strobed within a given time-out period. The Watchdog Timer is discussed in Chapter 6, the Watchdog Register specifications are on page 73.

Rear-Panel Transition Board NMI Push Button

An NMI push button may be available on the optional RPIO transition board (such as the ZT 4807 Rear-Panel Transition Board). Pressing this button causes the ZT 5524 / MPCBL5524 to generate a non-maskable interrupt.

Thermal Considerations D

This appendix describes the thermal requirements to reliably operate a ZT 5524 / MPCBL5524 processor board with a Pentium III processor.

D.1 Thermal Requirements

The maximum processor core temperature allowed by the Pentium III processors on the ZT 5524 / MPCBL5524 is 100° C.

Caution: To avoid damaging the CPU, *do not exceed the maximum processor core temperature!*

The ZT 5524 / MPCBL5524 comes from the factory with integrated heat sinks to help dissipate the heat generated by the processors. The maximum ambient air temperature required by the heat sinks to maintain core temperature below the maximum is 45° C. The maximum ambient air temperature assumes an airflow of 250 linear feet per minute past the heat sinks.

Caution: External airflow must be provided at all times during operation to avoid damaging the CPU. Intel strongly recommends use of a fan tray below the card rack to supply the external airflow.

D.2 Temperature Monitoring

Because reliable long-term operation of the ZT 5524 / MPCBL5524 depends on maintaining proper temperature, Intel strongly recommends that you verify the operating temperature of the processor (core) in your final system configuration.

The Pentium III processor incorporates an on-die thermal diode that can be used to monitor the processor's die temperature. The ZT 5524 / MPCBL5524 includes an ADM1026 device that is monitored through the BMC. This device checks the die temperature of the processor for thermal management purposes.

Data Sheet Reference E

This appendix provides links to data sheets, standards, and specifications for the technology designed into the ZT 5524 / MPCBL5524.

E.1 Chipset

The ZT 5524 / MPCBL5524 incorporates the ServerWorks* Champion LE-T chipset. The Champion LE-T chipset consists of the ServerWorks Champion North Bridge (CNB30LE-T) and the ServerWorks Champion South Bridge (CSB5) chips.

More information on the ServerWorks Champion LE-T chipset may be found on the ServerWorks website:

http://www.serverworks.com

E.2 CompactPCI*

The ZT 5524 / MPCBL5524 is compliant with the following CompactPCI specifications:

- CompactPCI Specification, PICMG 2.0, Version 2.1
- CompactPCI Hot Swap Specification, PICMG 2.1, Version 2.0
- CompactPCI Packet Switching Backplane Specification, PICMG 2.16, Version 1.0

These specifications can be purchased from PICMG* (PCI Industrial Computers Manufacturers Group). A short form specification in Adobe* Acrobat* format (PDF) is also available on PICMG's website at:

https://www.picmg.org/compactpci.stm

E.3 Ethernet

Gigabit Ethernet is implemented on the ZT 5524 / MPCBL5524 via the Intel 82546 Gigabit Ethernet PCI Controller. Refer to the *Intel 82546EB Dual Port Gigabit Ethernet Controller* data sheet for more information. The data sheet is in HTML format and available online at:

http://www.intel.com/design/network/products/lan/controllers/82546.htm

10/100Base-T Ethernet is implemented on the ZT 5524 / MPCBL5524 via the Intel 82550 Fast Ethernet Multifunction Controller. More information is available online at:

http://www.intel.com/design/network/products/lan/controllers/82550.htm

E.4 Intelligent Platform Management Interface (IPMI)

See the Intel IPMI home page for information concerning the Intelligent Platform Management Interface, including the *Intelligent Platform Management Interface v1.5 Specification* and the *Intelligent Platform Management Interface Implementer's Guide*:

http://developer.intel.com/design/servers/ipmi/spec.htm

E.5 PCI-to-PCI Bridge

For more information about the Intel 21154-BE PCI-to-PCI bridges used on the ZT 5524 / MPCBL5524 CPU, visit the Intel website addressed below.

http://developer.intel.com/design/bridge/

E.6 Pentium III Processor

For more information about the Low Power Intel Pentium III 512 KByte processor, see *Discover the New Low Voltage Pentium® III 512KByte Processor Product Overview.* This document is available online at:

http://developer.intel.com/design/pentiumiii/lvpentiumiii/prodbref/index3.htm

The data sheet is available at:

http://developer.intel.com/design/pentiumiii/datashts/273673.htm

E.7 I/O Controller

Refer to the National Semiconductor* *PC87413, PC87414, PC87416, PC87417 LPC ServerI/O for Servers and Workstations* data sheet for more information on the following ZT 5524 / MPCBL5524 functions:

- Serial port controller
- Floppy disk controller
- Mouse and keyboard controller
- Real-time clock and CMOS memory
- Counter/Timers
- Access Bus Interface to the BIOS
- Intelligent power management

The data sheet is in Adobe* Acrobat format (PDF) and available online at:

http://www.national.com/pf/PC/PC87417.html

E.8 Thermal Management

For more information about the Analog Devices* ADM1026 Complete Thermal System Management Controller, see the manufacturer's website at:

http://products.analog.com/products/info.asp?product=ADM1026

E.9 User Documentation

The latest Intel NetStructure® product information and manuals are available on the Intel NetStructure website. BIOS and driver updates are also available from this site.

http://developer.intel.com/design/network/products/cbp/linecard.htm.

E.10 Video

For more information on the Chips and Technologies* 69000 HiQVideo Accelerator with Integrated Memory, refer to the *69000 HiQVideo Accelerator with Integrated Memory* data sheet. This and other related documents are available online at:

http://www.asiliant.com/69000.htm

E.11 ZT 5524 / MPCBL5524 Product Page

See the ZT 5524 / MPCBL5524 product page for information updates and additional product information:

http://developer.intel.com/design/network/products/cbp/zt5524.htm

Warranty Information F

F.1 Intel NetStructure® Compute Boards & Platform Products Limited Warranty

Intel warrants to the original owner that the product delivered in this package will be free from defects in material and workmanship for two (2) year(s) following the latter of: (i) the date of purchase only if you register by returning the registration card as indicated thereon with proof of purchase; or (ii) the date of manufacture; or (iii) the registration date if by electronic means provided such registration occurs within 30 days from purchase. This warranty does not cover the product if it is damaged in the process of being installed. Intel recommends that you have the company from whom you purchased this product install the product.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ANY WARRANTY OF INFRINGEMENT OF ANY OTHER PARTY'S INTELLECTUAL PROPERTY RIGHTS, OR ANY WARRANTY ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

This warranty does not cover replacement of products damaged by abuse, accident, misuse, neglect, alteration, repair, disaster, improper installation or improper testing. If the product is found to be otherwise defective, Intel, at its option, will replace or repair the product at no charge except as set forth below, provided that you deliver the product along with a return material authorization (RMA) number (see below) either to the company from whom you purchased it or to Intel. If you ship the product, you must assume the risk of damage or loss in transit. You must use the original container (or the equivalent) and pay the shipping charge. Intel may replace or repair the product with either a new or reconditioned product, and the returned product becomes Intel's property. Intel warrants the repaired or replaced product to be free from defects in material and workmanship for a period of the greater of: (i) ninety (90) days from the return shipping date; or (ii) the period of time remaining on the original two (2) year warranty.

This warranty gives you specific legal rights and you may have other rights which vary from state to state. All parts or components contained in this product are covered by Intel's limited warranty for this product. The product may contain fully tested, recycled parts, warranted as if new.

F.1.1 Returning a Defective Product (RMA)

Before returning any product, contact an Intel Customer Support Group to obtain either a Direct

Return Authorization (DRA) or Return Material Authorization (RMA). Return Material

Authorizations are only available for products purchased within 30 days.

Return contact information by geography:

F.1.2 For the Americas

Return Material Authorization (RMA) credit requests e-mail address: requests.rma@intel.com

Direct Return Authorization (DRA) repair requests e-mail address: uspss.repair@intel.com

DRA on-line form: http://support.intel.com/support/motherboards/draform.htm

Intel Business Link (IBL): http://www.intel.com/ibl

Telephone No.: 1-800-INTEL4U or 480-554-4904

Office Hours: Monday - Friday 0700-1700 MST Winter / PST Summer

F.1.3 For EMEA

Return Material Authorization (RMA) e-mail address - emea.fs@intel.com

Direct Return Authorization (DRA) for repair requests e-mail address: emea.fs@intel.com

Intel Business Link (IBL): http://www.intel.com/ibl

Telephone No.: 00 44 1793 403063

Fax No.: 00 44 1793 403109

Office Hours: Monday - Friday 0900-1700 UK time

F.1.4 For APAC

RMA/DRA requests email address: apac.rma.front-end@intel.com

Telephone No.: 604-859-3111 or 604-859-3325

Fax No.: 604-859-3324

Office Hours: Monday - Friday 0800-1700 Malaysia time

Return Material Authorization (RMA) requests e-mail address: rma.center.jpss@intel.com

Telephone No.: 81-298-47-0993 or 81-298-47-5417

Fax No.: 81-298-47-4264

Direct Return Authorization (DRA) for repair requests, contact the JPSS Repair center.

E-mail address: sugiyamakx@intel.co.jp

Telephone No.: 81-298-47-8920

Fax No.: 81-298-47-5468

Office Hours: Monday - Friday 0830-1730 Japan time

If the Customer Support Group verifies that the product is defective, they will have the Direct Return Authorization/Return Material Authorization Department issue you a DRA/RMA number to place on the outer package of the product. Intel cannot accept any product without a DRA/RMA number on the package. Limitation of Liability and Remedies

INTEL SHALL HAVE NO LIABILITY FOR ANY INDIRECT OR SPECULATIVE DAMAGES (INCLUDING , WITHOUT LIMITING THE FOREGOING, CONSEQUENTIAL, INCIDENTAL AND SPECIAL DAMAGES) ARISING FROM THE USE OF OR INABILITY TO USE THIS PRODUCT, WHETHER ARISING OUT OF CONTRACT, NEGLIGENCE, TORT, OR UNDER ANY WARRANTY, OR FOR INFRINGEMENT OF ANY OTHER PARTY'S INTELLECTUAL PROPERTY RIGHTS, IRRESPECTIVE OF WHETHER INTEL HAS ADVANCE NOTICE OF THE POSSIBILITY OF ANY SUCH DAMAGES, INCLUDING, BUT NOT LIMITED TO LOSS OF USE, BUSINESS INTERRUPTIONS, AND LOSS OF PROFITS. NOTWITHSTANDING THE FOREGOING, INTEL'S TOTAL LIABILITY FOR ALL CLAIMS UNDER THIS AGREEMENT SHALL NOT EXCEED THE PRICE PAID FOR THE PRODUCT. THESE LIMITATIONS ON POTENTIAL LIABILITIES WERE AN ESSENTIAL ELEMENT IN SETTING THE PRODUCT PRICE. INTEL NEITHER ASSUMES NOR AUTHORIZES ANYONE TO ASSUME FOR IT ANY OTHER LIABILITIES.

Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitations or exclusions may not apply to you.

Customer Support G

This appendix offers technical and sales assistance information for this product, and information on returning an Intel NetStructure product for service.

G.1 Technical Support and Return for Service Assistance

For all product returns and support issues, please contact your Intel product distributor or Intel Sales Representative for specific information.

G.2 Sales Assistance

If you have a sales question, please contact your local Intel ® NetStructure™ Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at Intel's website, located at:

http://www.intel.com/network/csp/sales/

Intel Corporation
Telephone (in U.S.) 1-800-755-4444
Telephone (Outside U.S.) 1-973-993-3030

Agency Approvals H

This appendix presents agency approval and certification information for the ZT 5524 / MPCBL5524 Processor Board.

H.1 UL 1950 Certification

Underwriters Laboratories, Inc.*

Safety:	UL Safety of Information Technology Equipment, including Electrical Business Equipment IEC 950 and UL 1950 (UL file # E179737)

H.2 CE Certification

The ZT 5524 / MPCBL5524 meets the intent of *Directive 89/336/EEC* for electromagnetic compatibility and the *Low-Voltage Directive 73/23/EEC* for product safety. Compliance was demonstrated to the following specifications as listed in the *Official Journal of the European Communities*:

H.2.0.1 EN 50081-1 Emissions

FCC 15B, Class A	AC Line Conducted Emissions Test
EN55022, Class A	Radiated Radio Frequency (RF) Emissions Tests
EN55022, (1998)	Telecommunications Port Conducted Emissions Test
EN 61000-3-2 (1995)	Power Line Harmonics Test
EN61000-3-3 (1995)	Power Line Fluctuation/Flicker Test

H.2.0.2 EN 55024: 1998 Immunity

IEC 61000 4-2 (1995)	Electrostatic Discharge
IEC 61000 4-3 (1995)	RF Radiated Fields
IEC 61000 4-4 (1995)	Electrical Fast Transients/Burst
IEC 61000 4-6 (1996)	RF Common Mode

H.2.0.3 BELLCORE GR-1089-CORE

Sect. 2	Electrostatic Discharge
Sect. 3.2.2	Radiated RF Emissions
Sect. 3.2.3	AC Line Conducted Emissions
Sect. 3.3.1	RF Radiated Fields
Sect. 3.3.3	RF Common Mode

H.2.0.4 Low Voltage Directive 73/23/EEC

UL 1950/EN 60950	Safety of Information Technology Equipment, Including Electrical Business Equipment

H.3 FCC Regulatory Information

Regulatory information: Federal Communications Commission* (FCC) (USA only).

Caution: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to FCC 47 CFR Part 15, Subpart B, Class A of the FCC Rules. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Intel NetStructure system RFI and Radiated Immunity tests were conducted with a specific configuration representing an anticipated general application. Changes or modifications to peripheral devices and shielded cables not expressly approved by Intel could result in EMI interference.

FCC compliance was achieved under the following conditions:

- Shielded signal cables and a shielded power cord
- Shielded cables on all I/O ports
- Cable shields connected to earth ground via metal shell connectors
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground
- Faceplate screws properly tightened

For minimum RF emissions, it is essential that the conditions above are implemented; failure to do so could compromise the FCC compliance of the equipment containing the system.