

# CAT5112

## 32-Tap Digitally Programmable Potentiometer (DPP™) with Buffered Wiper

### Description

The CAT5112 is a single digitally programmable potentiometer (DPP™) designed as an electronic replacement for mechanical potentiometers. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5112 contains a 32-tap series resistor array connected between two terminals  $R_H$  and  $R_L$ . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper,  $R_{WB}$ . The CAT5112 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non-volatile memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5112 is accomplished with three input control pins,  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$ . The  $\overline{INC}$  input increments the wiper in the direction which is determined by the logic state of the  $U/\overline{D}$  input. The  $\overline{CS}$  input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a buffered voltage divider. For applications where the potentiometer is used as a 2-terminal variable resistor, please refer to the CAT5114. The buffered wiper of the CAT5112 is not compatible with that application.

### Features

- 32-position Linear Taper Potentiometer
- Non-volatile EEPROM Wiper Storage; Buffered Wiper
- Low Power CMOS Technology
- Single Supply Operation: 2.5 V – 6.0 V
- Increment Up/Down Serial Interface
- Resistance Values: 10 k $\Omega$ , 50 k $\Omega$  and 100 k $\Omega$
- Available in PDIP, SOIC, TSSOP and MSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper-proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions

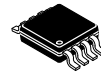


ON Semiconductor®

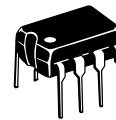
<http://onsemi.com>



SOIC-8  
V SUFFIX  
CASE 751BD



MSOP-8  
Z SUFFIX  
CASE 846AD

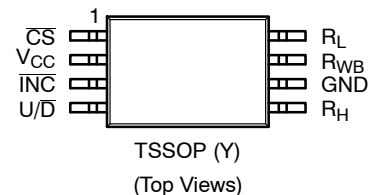
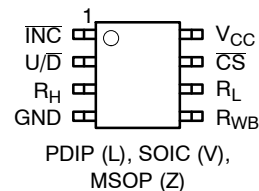


PDIP-8  
L SUFFIX  
CASE 646AA



TSSOP-8  
Y SUFFIX  
CASE 948AL

### PIN CONFIGURATIONS



### PIN FUNCTION

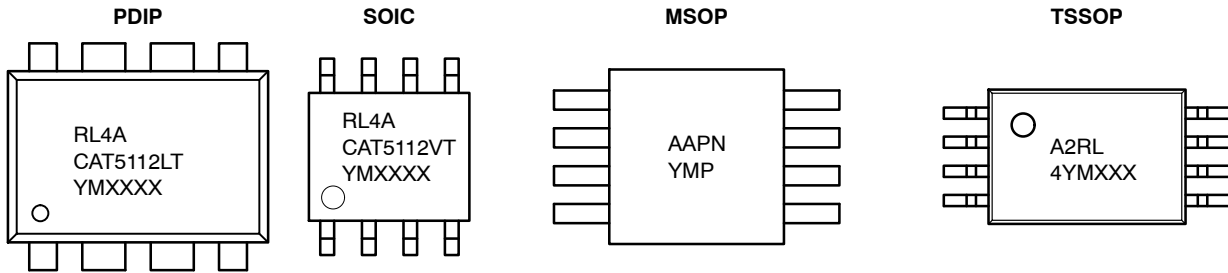
Pin Name	Function
$\overline{INC}$	Increment Control
$U/\overline{D}$	Up/Down Control
$R_H$	Potentiometer High Terminal
GND	Ground
$R_{WB}$	Buffered Wiper Terminal
$R_L$	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
$V_{CC}$	Supply Voltage

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

# CAT5112

## DEVICE MARKING INFORMATION



R = Resistance:

2 = 10 kΩ

4 = 50 kΩ

5 = 100 kΩ

L = Assembly Location

4 = Lead Finish – NiPdAu

A = Product Revision (Fixed as "A")

CAT5112L = Device Code (PDIP)

CAT5112V = Device Code (SOIC)

T = Temperature Range (Industrial)

Y = Production Year (Last Digit)

M = Production Month (1–9, A, B, C)

XXXX = Last Four Digits of Assembly Lot Number

AAPN = CAT5112ZI–10–T3

AAPP = CAT5112ZI–50–T3

Y = Production Year (Last Digit)

M = Production Month (1–9, A, B, C)

P = Product Revision

A2 = Device Code

R = Resistance:

2 = 10 kΩ

4 = 50 kΩ

5 = 100 kΩ

L = Assembly Location

4 = Lead Finish – NiPdAu

Y = Production Year (Last Digit)

M = Production Month (1–9, A, B, C)

XXX = Last Three Digits of

Assembly Lot Number

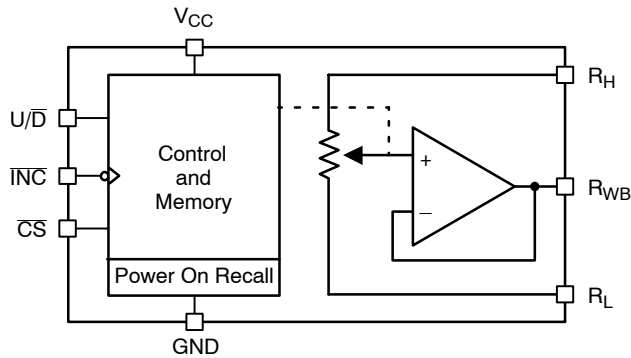


Figure 1. Functional Diagram

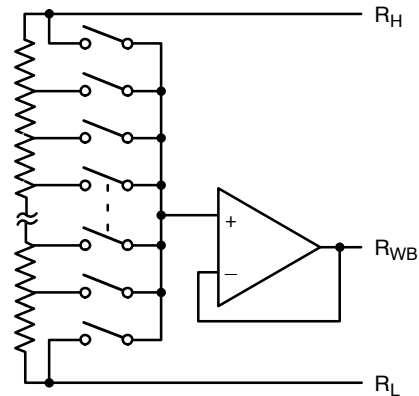


Figure 2. Electronic Potentiometer Implementation

## Pin Description

### $\overline{\text{INC}}$ : Increment Control Input

The  $\overline{\text{INC}}$  input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the  $\text{U}/\overline{\text{D}}$  input.

### $\text{U}/\overline{\text{D}}$ : Up/Down Control Input

The  $\text{U}/\overline{\text{D}}$  input controls the direction of the wiper movement. When in a high state and  $\overline{\text{CS}}$  is low, any high-to-low transition on  $\overline{\text{INC}}$  will cause the wiper to move one increment toward the  $\text{R}_\text{H}$  terminal. When in a low state and  $\overline{\text{CS}}$  is low, any high-to-low transition on  $\overline{\text{INC}}$  will cause the wiper to move one increment towards the  $\text{R}_\text{L}$  terminal.

### $\text{R}_\text{H}$ : High End Potentiometer Terminal

$\text{R}_\text{H}$  is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the  $\text{R}_\text{L}$  terminal. Voltage applied to the  $\text{R}_\text{H}$  terminal cannot exceed the supply voltage,  $\text{V}_{\text{CC}}$  or go below ground, GND.

### $\text{R}_{\text{WB}}$ : Wiper Potentiometer Terminal (Buffered)

$\text{R}_{\text{WB}}$  is the buffered wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs,  $\overline{\text{INC}}$ ,  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{CS}}$ .

### $\text{R}_\text{L}$ : Low End Potentiometer Terminal

$\text{R}_\text{L}$  is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the  $\text{R}_\text{H}$  terminal. Voltage applied to the  $\text{R}_\text{L}$  terminal cannot exceed the supply voltage,  $\text{V}_{\text{CC}}$  or go below ground, GND.  $\text{R}_\text{L}$  and  $\text{R}_\text{H}$  are electrically interchangeable.

### $\overline{\text{CS}}$ : Chip Select

The chip select input is used to activate the control input of the CAT5112 and is active low. When in a high state, activity on the  $\overline{\text{INC}}$  and  $\text{U}/\overline{\text{D}}$  inputs will not affect or change the position of the wiper.

## Device Operation

The CAT5112 operates like a digitally controlled potentiometer with  $\text{R}_\text{H}$  and  $\text{R}_\text{L}$  equivalent to the high and low terminals and  $\text{R}_{\text{WB}}$  equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points,  $\text{R}_\text{H}$  and  $\text{R}_\text{L}$ . There are 31 resistor elements connected in series between the  $\text{R}_\text{H}$  and  $\text{R}_\text{L}$  terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs,  $\overline{\text{INC}}$ ,  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{CS}}$ . These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the  $\overline{\text{INC}}$  and  $\overline{\text{CS}}$  inputs.

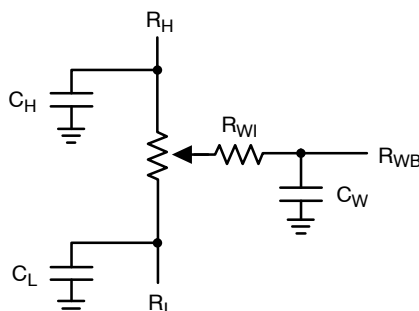
With  $\overline{\text{CS}}$  set LOW the CAT5112 is selected and will respond to the  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{INC}}$  inputs. HIGH to LOW transitions on  $\overline{\text{INC}}$  will increment or decrement the wiper (depending on the state of the  $\text{U}/\overline{\text{D}}$  input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever  $\overline{\text{CS}}$  transitions HIGH while the  $\overline{\text{INC}}$  input is also HIGH. When the CAT5112 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With  $\overline{\text{INC}}$  set low, the CAT5112 may be deselected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

# CAT5112

**Table 1. OPERATION MODES**

INC	CS	U/D	Operation
High to Low	Low	High	Wiper toward R <sub>H</sub>
High to Low	Low	Low	Wiper toward R <sub>L</sub>
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



**Figure 3. Potentiometer Equivalent Circuit**

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Supply Voltage V <sub>CC</sub> to GND	-0.5 to +7	V
Inputs CS to GND	-0.5 to V <sub>CC</sub> + 0.5	V
INC to GND	-0.5 to V <sub>CC</sub> + 0.5	V
U/D to GND	-0.5 to V <sub>CC</sub> + 0.5	V
R <sub>H</sub> to GND	-0.5 to V <sub>CC</sub> + 0.5	V
R <sub>L</sub> to GND	-0.5 to V <sub>CC</sub> + 0.5	V
R <sub>WB</sub> to GND	-0.5 to V <sub>CC</sub> + 0.5	V
Operating Ambient Temperature Commercial ('C' or Blank suffix)	0 to 70	°C
Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to +150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V <sub>ZAP</sub> (Note 1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
I <sub>LTH</sub> (Notes 1, 2)	Latch-Up	JEDEC Standard 17	100			mA
T <sub>DR</sub>	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N <sub>END</sub>	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to V<sub>CC</sub> + 1 V

# CAT5112

**Table 4. DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +2.5\text{ V}$  to  $+6\text{ V}$  unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>POWER SUPPLY</b>						
$V_{CC}$	Operating Voltage Range		2.5	–	6	V
$I_{CC1}$	Supply Current (Increment)	$V_{CC} = 6\text{ V}$ , $f = 1\text{ MHz}$ , $I_W = 0$	–	–	200	$\mu\text{A}$
		$V_{CC} = 6\text{ V}$ , $f = 250\text{ kHz}$ , $I_W = 0$	–	–	100	$\mu\text{A}$
$I_{CC2}$	Supply Current (Write)	Programming, $V_{CC} = 6\text{ V}$	–	–	1000	$\mu\text{A}$
		$V_{CC} = 3\text{ V}$	–	–	500	$\mu\text{A}$
$I_{SB1}$ (Note 4)	Supply Current (Standby)	$\overline{CS} = V_{CC} - 0.3\text{ V}$ $U/\overline{D}$ , $\overline{INC} = V_{CC} - 0.3\text{ V}$ or GND	–	75	150	$\mu\text{A}$
<b>LOGIC INPUTS</b>						
$I_{IH}$	Input Leakage Current	$V_{IN} = V_{CC}$	–	–	10	$\mu\text{A}$
$I_{IL}$	Input Leakage Current	$V_{IN} = 0\text{ V}$	–	–	-10	$\mu\text{A}$
$V_{IH1}$	TTL High Level Input Voltage	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	2	–	$V_{CC}$	V
$V_{IL1}$	TTL Low Level Input Voltage		0	–	0.8	V
$V_{IH2}$	CMOS High Level Input Voltage	$2.5\text{ V} \leq V_{CC} \leq 6\text{ V}$	$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V
$V_{IL2}$	CMOS Low Level Input Voltage		-0.3	–	$V_{CC} \times 0.2$	V
<b>POTENTIOMETER CHARACTERISTICS</b>						
$R_{POT}$	Potentiometer Resistance	-10 Device		10		k $\Omega$
		-50 Device		50		
		-00 Device		100		
	Pot. Resistance Tolerance				$\pm 20$	%
$V_{RH}$	Voltage on $R_H$ pin		0		$V_{CC}$	V
$V_{RL}$	Voltage on $R_L$ pin		0		$V_{CC}$	V
	Resolution			1		%
INL	Integral Linearity Error	$I_W \leq 2\ \mu\text{A}$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \leq 2\ \mu\text{A}$		0.25	0.5	LSB
$R_{OUT}$	Buffer Output Resistance	$0.05\ V_{CC} \leq V_{WB} \leq 0.95\ V_{CC}$ , $V_{CC} = 5\text{ V}$			1	$\Omega$
$I_{OUT}$	Buffer Output Current	$0.05\ V_{CC} \leq V_{WB} \leq 0.95\ V_{CC}$ , $V_{CC} = 5\text{ V}$			3	mA
$TC_{RPOT}$	TC of Pot Resistance			300		ppm/ $^{\circ}\text{C}$
$TC_{RATIO}$	Ratiometric TC			20		ppm/ $^{\circ}\text{C}$
$C_{RH}/C_{RL}/C_{RW}$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 k $\Omega$		1.7		MHz
$V_{WB(SWING)}$	Output Voltage Range	$I_{OUT} \leq 100\ \mu\text{A}$ , $V_{CC} = 5\text{ V}$	$0.01\ V_{CC}$		$0.99\ V_{CC}$	

3. This parameter is tested initially and after a design or process change that affects the parameter.

4. Latch-up protection is provided for stresses up to 100 mA on address and data pins from  $-1\text{ V}$  to  $V_{CC} + 1\text{ V}$

5.  $I_W$  = source or sink

6. These parameters are periodically sampled and are not 100% tested.

**Table 5. AC TEST CONDITIONS**

V <sub>CC</sub> Range	2.5 V ≤ V <sub>CC</sub> ≤ 6 V
Input Pulse Levels	0.2 V <sub>CC</sub> to 0.7 V <sub>CC</sub>
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V <sub>CC</sub>

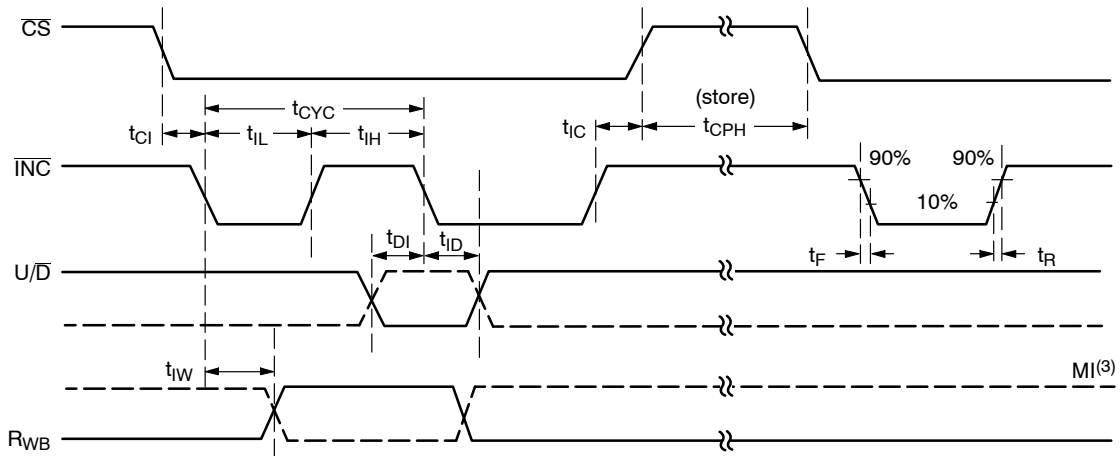
**Table 6. AC OPERATING CHARACTERISTICS** (V<sub>CC</sub> = +2.5 V to +6.0 V, V<sub>H</sub> = V<sub>CC</sub>, V<sub>L</sub> = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t <sub>CI</sub>	CS to INC Setup	100	-	-	ns
t <sub>DI</sub>	U/D to INC Setup	50	-	-	ns
t <sub>ID</sub>	U/D to INC Hold	100	-	-	ns
t <sub>IL</sub>	INC LOW Period	250	-	-	ns
t <sub>IH</sub>	INC HIGH Period	250	-	-	ns
t <sub>IC</sub>	INC Inactive to CS Inactive	1	-	-	μs
t <sub>CPH</sub>	CS Deselect Time (NO STORE)	100	-	-	ns
t <sub>CPH</sub>	CS Deselect Time (STORE)	10	-	-	ms
t <sub>IW</sub>	INC to V <sub>OUT</sub> Change	-	1	5	μs
t <sub>CYC</sub>	INC Cycle Time	1	-	-	μs
t <sub>R</sub> , t <sub>F</sub> (Note 8)	INC Input Rise and Fall Time	-	-	500	μs
t <sub>PU</sub> (Note 8)	Power-up to Wiper Stable	-	-	1	ms
t <sub>WR</sub>	Store Cycle	-	5	10	ms

7. Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.

8. This parameter is periodically sampled and not 100% tested.

9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

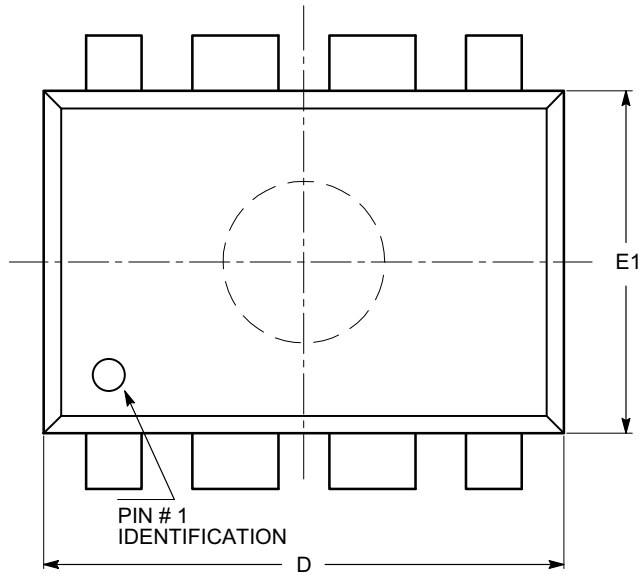


**Figure 4. A.C. Timing**

# CAT5112

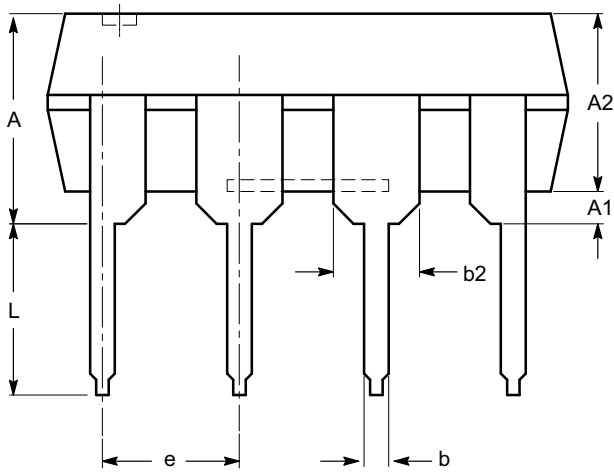
## PACKAGE DIMENSIONS

PDIP-8, 300 mils  
CASE 646AA-01  
ISSUE A

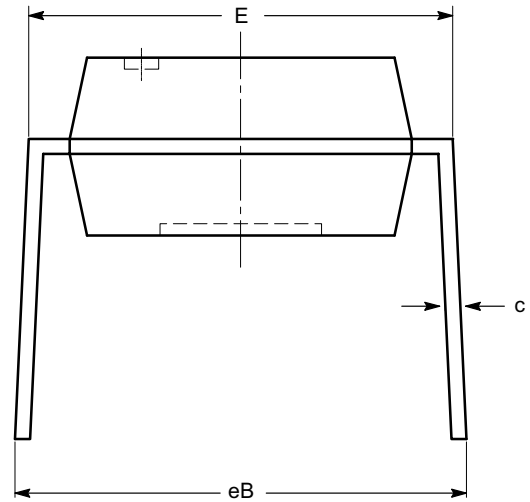


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e	2.54 BSC		
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW



END VIEW

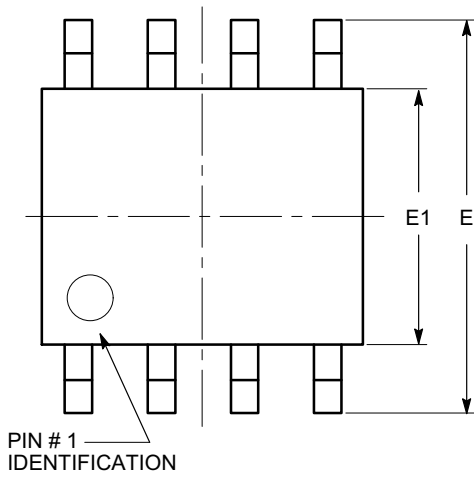
**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

# CAT5112

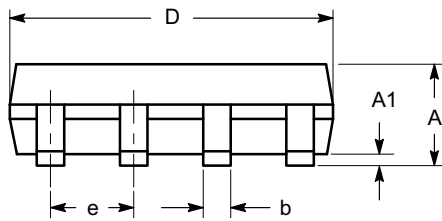
## PACKAGE DIMENSIONS

SOIC 8, 150 mils  
CASE 751BD-01  
ISSUE O

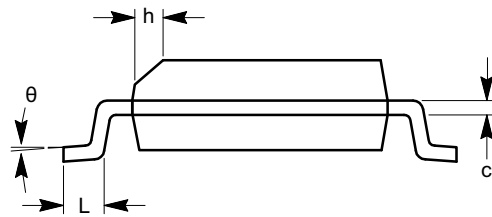


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



SIDE VIEW



END VIEW

**Notes:**

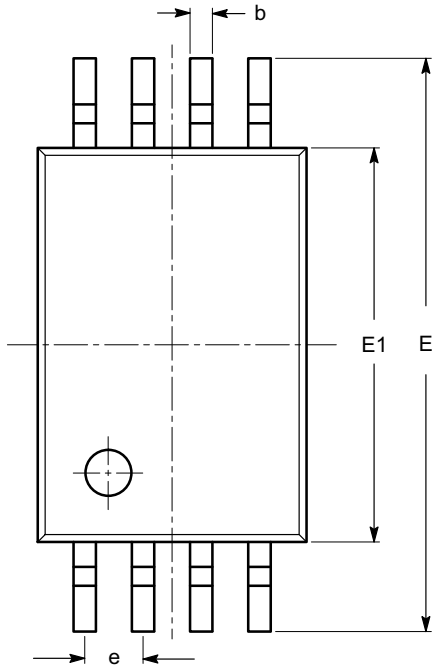
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.



# CAT5112

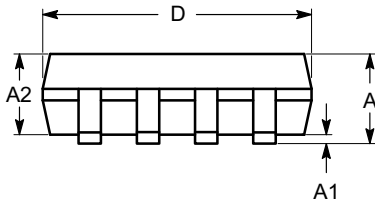
## PACKAGE DIMENSIONS

TSSOP8, 4.4x3  
CASE 948AL-01  
ISSUE O

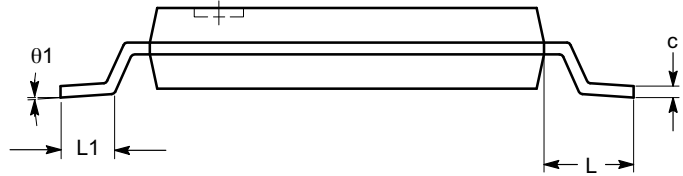


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta$	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

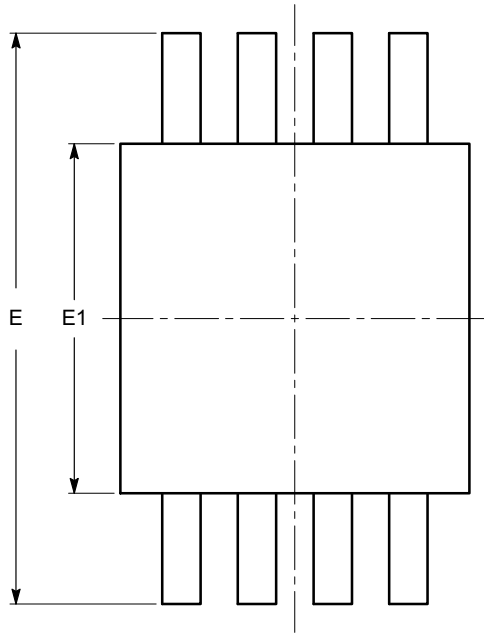
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

# CAT5112

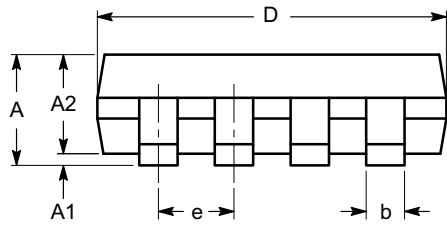
## PACKAGE DIMENSIONS

MSOP 8, 3x3  
CASE 846AD-01  
ISSUE O

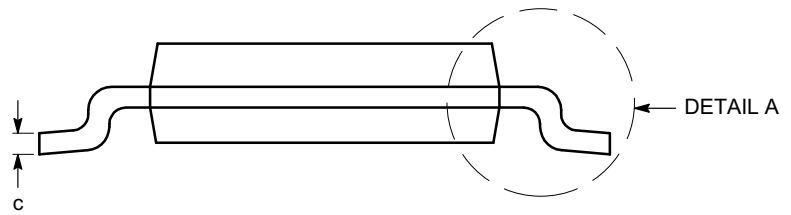


TOP VIEW

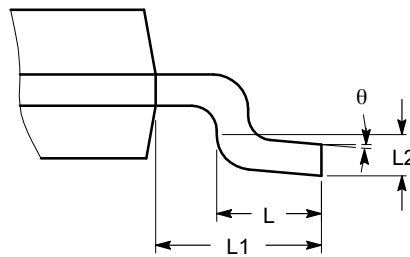
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
$\theta$	0°		6°



SIDE VIEW



END VIEW



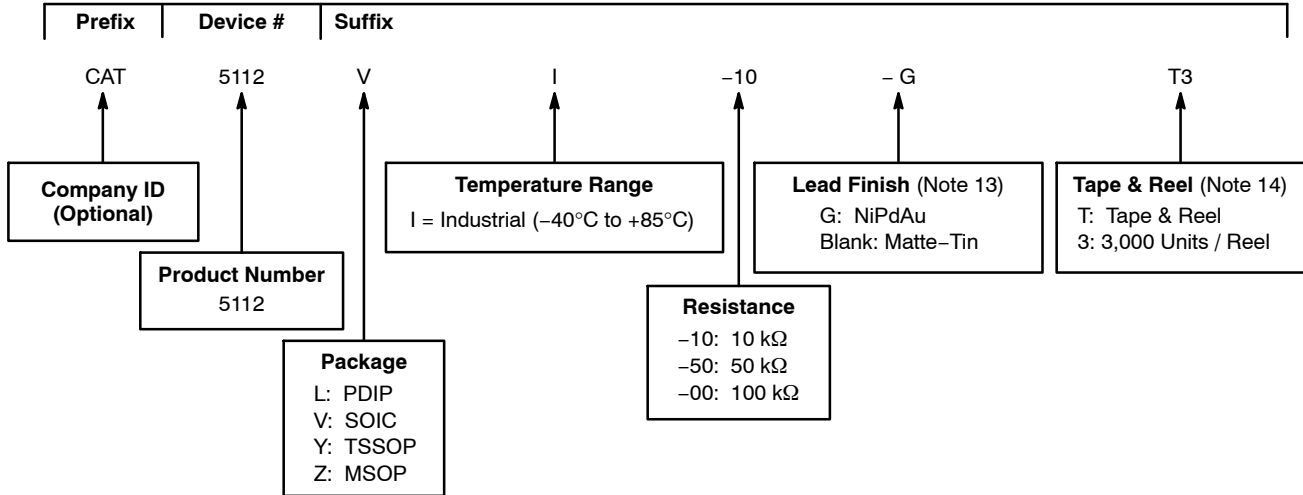
DETAIL A

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

# CAT5112

## Example of Ordering Information (Note 12)



**Table 7. ORDERING INFORMATION**

Orderable Part Number	Resistance (kΩ)	Package-Pins	Lead Finish (Note 13)
CAT5112LI-10-G	10	PDIP-8	NiPdAu
CAT5112LI-50-G	50		
CAT5112LI-00-G	100		
CAT5112VI-10-GT3	10	SOIC-8	
CAT5112VI-50-GT3	50		
CAT5112VI-00-GT3	100		
CAT5112YI-10-GT3	10	TSSOP-8	
CAT5112YI-50-GT3	50		
CAT5112YI-00-GT3	100		
CAT5112ZI-10-GT3	10	MSOP-8	
CAT5112ZI-50-GT3	50		
CAT5112ZI-00-GT3	100		

10. All packages are RoHS-compliant (Lead-free, Halogen-free).


11. The standard lead finish is NiPdAu.

12. The device used in the above example is a CAT5112VI-10-GT3 (SOIC, Industrial Temperature, 10 kΩ, NiPdAu, Tape & Reel, 3,000/Reel).

13. Contact factory for Matte-Tin finish.

14. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DPP is a trademark of Semiconductor Components Industries, LLC.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

**CAT5112/D**