

AD7470/AD7472

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V

1.75 MSPS for AD7470 (10-Bit)

1.5 MSPS for AD7472 (12-Bit)

Low Power

AD7470: 3.34 mW Typ at 1.5 MSPS with 3 V Supplies
7.97 mW Typ at 1.75 MSPS with 5 V Supplies

AD7472: 3.54 mW Typ at 1.2 MSPS with 3 V Supplies
8.7 mW Typ at 1.5 MSPS with 5 V Supplies

Wide Input Bandwidth

70 dB Typ SNR at 500 kHz Input Frequency

Flexible Power/Throughput Rate Management

No Pipeline Delays

High Speed Parallel Interface

Sleep Mode: 50 nA Typ

24-Lead SOIC and TSSOP Packages

GENERAL DESCRIPTION

The AD7470/AD7472 are 10-bit/12-bit high speed, low power, successive approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS for the 12-bit AD7472 and up to 1.75 MSPS for the 10-bit AD7470. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

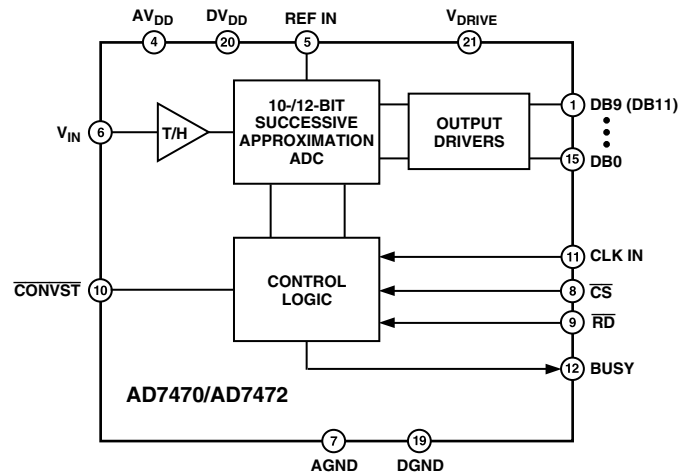
The conversion process and data acquisition are controlled using standard control inputs, allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$, and conversion is also initiated at this point. BUSY goes high at the start of conversion and goes low 531.66 ns after falling edge of $\overline{\text{CONVST}}$ (AD7472 with a clock frequency of 26 MHz) to indicate that the conversion is complete. There are no pipeline delays associated with the parts. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7470/AD7472 use advanced design techniques to achieve very low power dissipation at high throughput rates. With 3 V supplies and 1.5 MSPS throughput rates, the AD7470 typically consumes, on average, just 1.1 mA. With 5 V supplies and 1.75 MSPS, the average current consumption is typically 1.6 mA. The part also offers flexible power/throughput rate management. Operating the AD7470 with 3 V supplies and 500 kSPS throughput reduces the current consumption to 713 μA . At 5 V supplies and 500 kSPS, the part consumes 944 μA .

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FUNCTIONAL BLOCK DIAGRAM



AD7470 IS A 10-BIT PART WITH DB0 TO DB9 AS OUTPUTS.
AD7472 IS A 12-BIT PART WITH DB0 TO DB11 AS OUTPUTS.

It is also possible to operate the parts in an auto sleep mode, where the part wakes up to do a conversion and automatically enters sleep mode at the end of conversion. This method allows very low power dissipation numbers at lower throughput rates. In this mode, the AD7472 can be operated with 3 V supplies at 100 kSPS, and consume an average current of just 124 μA . At 5 V supplies and 100 kSPS, the average current consumption is 171 μA .

The analog input range for the part is 0 V to REF IN. The 2.5 V reference is applied externally to the REF IN pin. The conversion rate is determined by the externally-applied clock.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption. The AD7470 offers 1.75 MSPS throughput and the AD7472 offers 1.5 MSPS throughput rates with 4 mW power consumption.
2. Flexible Power/Throughput Rate Management. The conversion rate is determined by an externally-applied clock allowing the power to be reduced as the conversion rate is reduced. The part also features an auto sleep mode to maximize power efficiency at lower throughput rates.
3. No Pipeline Delay. The part features a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

AD7470/AD7472

AD7470—SPECIFICATIONS¹ ($V_{DD} = 2.7\text{ V to }5.25\text{ V}^2$, REF IN = 2.5 V, $f_{CLKIN} = 30\text{ MHz @ }5\text{ V and }24\text{ MHz @ }3\text{ V}$; $T_A = T_{MIN}$ to T_{MAX} ³, unless otherwise noted.)

Parameter	A Version ¹		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE	5 V	3 V		$f_S = 1.75\text{ MSPS @ }5\text{ V}$, $f_S = 1.5\text{ MSPS @ }3\text{ V}$
Signal to Noise + Distortion (SINAD)	60	60	dB min	$f_{IN} = 500\text{ kHz Sine Wave}$
Signal-to-Noise Ratio (SNR)	60	60	dB min	$f_{IN} = 100\text{ kHz Sine Wave}$
Total Harmonic Distortion (THD)	-83	-83	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
Peak Harmonic or Spurious Noise (SFDR)	-75	-75	dB max	$f_{IN} = 100\text{ kHz Sine Wave}$
Intermodulation Distortion (IMD)	-85	-85	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
Second-Order Terms	-75	-75	dB max	$f_{IN} = 100\text{ kHz Sine Wave}$
Third-Order Terms	-77	-75	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
Aperture Delay	5	5	ns typ	$f_{IN} = 100\text{ kHz Sine Wave}$
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	20	20	MHz typ	@ 3 dB
DC ACCURACY				$f_S = 1.75\text{ MSPS @ }5\text{ V}$; $f_S = 1.5\text{ MSPS @ }3\text{ V}$
Resolution	10	10	Bits	
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error	±2.5	±2.5	LSB max	
Gain Error	±1	±1	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN	0 to REF IN	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	V	±1% for Specified Performance
DC Leakage Current	±1	±1	µA max	
Input Capacitance	10/20	10/20	pF typ	Track-and-Hold Mode
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, $V_{IN} = 0\text{ V or }V_{DD}$
Input Capacitance, C_{IN}^4	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2$	$V_{DRIVE} - 0.2$	V min	$I_{SOURCE} = 200\text{ µA}$
Output Low Voltage, V_{OL}	0.4	0.4	V max	$I_{SINK} = 200\text{ µA}$
Floating-State Leakage Current	±10	±10	µA max	$V_{DD} = 2.7\text{ V to }5.25\text{ V}$
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	12	12	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time	135	135	ns min	
Throughput Rate	1.75	1.5	MSPS max	Conversion Time + Acquisition Time CLK IN of 30 MHz @ 5 V and 24 MHz @ 3 V
POWER REQUIREMENTS				
V_{DD}^5	+2.7/+5.25		V min/max	
I_{DD}^5				Digital Inputs = 0 V or DV_{DD}
Normal Mode	2.4		mA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_S = 1.75\text{ MSPS}$; Typ 2 mA
Quiescent Current	900		µA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_S = 1.75\text{ MSPS}$
Normal Mode	1.5		mA max	$V_{DD} = 2.7\text{ V to }3.3\text{ V}$; $f_S = 1.5\text{ MSPS}$; Typ 1.3 mA
Quiescent Current	800		µA max	$V_{DD} = 2.7\text{ V to }3.3\text{ V}$; $f_S = 1.5\text{ MSPS}$
Sleep Mode	1		µA max	CLK IN = 0 V or DV_{DD}
Power Dissipation ⁵				Digital Inputs = 0 V or DV_{DD}
Normal Mode	12		mW max	$V_{DD} = 5\text{ V}$
	4.5		mW max	$V_{DD} = 3\text{ V}$
Sleep Mode	5		µW max	$V_{DD} = 5\text{ V}$; CLK IN = 0 V or DV_{DD}
	3		µW max	$V_{DD} = 3\text{ V}$; CLK IN = 0 V or DV_{DD}

NOTES

¹Temperature ranges as follows: A Version: -40°C to +85°C.

²The AD7470 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 59 dB; THD (100 kHz) = -84 dB; INL ±0.8 LSB.

³The AD7470 will typically maintain A-grade performance up to 125°C, with a reduced CLK of 20 MHz @ 5 V and 16 MHz @ 3 V. Typical sleep mode current @ 125°C is 700 nA.

⁴Sample tested @ 25°C to ensure compliance.

⁵See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7472—SPECIFICATIONS¹(V_{DD} = 2.7 V to 5.25 V², REF IN = 2.5 V, A and B Versions: f_{CLKIN} = 26 MHz @ 5 V and 20 MHz @ 3 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version ¹		B Version ¹		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE	5 V	3 V	5 V	3 V		f _S = 1.5 MSPS @ 5 V, f _S = 1.2 MSPS @ 3 V
Signal to Noise + Distortion (SINAD)	69	69	69	69	dB typ	f _{IN} = 500 kHz Sine Wave
	68	68	68	68	dB min	f _{IN} = 100 kHz Sine Wave
Signal-to-Noise Ratio (SNR)	70	70	70	70	dB typ	f _{IN} = 500 kHz Sine Wave
	68	68	68	68	dB min	f _{IN} = 100 kHz Sine Wave
Total Harmonic Distortion (THD)	-83	-78	-83	-78	dB typ	f _{IN} = 500 kHz Sine Wave
	-83	-84	-83	-84	dB typ	f _{IN} = 100 kHz Sine Wave
	-75	-75	-75	-75	dB max	f _{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	-86	-81	-86	-81	dB typ	f _{IN} = 500 kHz Sine Wave
	-86	-86	-86	-86	dB typ	f _{IN} = 100 kHz Sine Wave
	-76	-76	-76	-76	dB max	f _{IN} = 100 kHz Sine Wave
Intermodulation Distortion (IMD)						
Second-Order Terms	-77	-77	-77	-77	dB typ	f _{IN} = 500 kHz Sine Wave
	-86	-86	-86	-86	dB typ	f _{IN} = 100 kHz Sine Wave
Third-Order Terms	-77	-77	-77	-77	dB typ	f _{IN} = 500 kHz Sine Wave
	-86	-86	-86	-86	dB typ	f _{IN} = 100 kHz Sine Wave
Aperture Delay	5	5	5	5	ns typ	
Aperture Jitter	15	15	15	15	ps typ	
Full Power Bandwidth	20	20	20	20	MHz typ	@ 3 dB
DC ACCURACY						f _S = 1.5 MSPS @ 5 V, f _S = 1.2 MSPS @ 3 V
Resolution	12	12	12	12	Bits	
Integral Nonlinearity	±2	±2	±1	±1	LSB max	Guaranteed No Missed Codes to 11 Bits (A Version)
Differential Nonlinearity	±1.8	±1.8	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits (B Version)
Offset Error	±10	±10	±10	±10	LSB max	
Gain Error	±2	±2	±2	±2	LSB max	
ANALOG INPUT						
Input Voltage Ranges	0 to REF IN	0 to REF IN	0 to REF IN	0 to REF IN	V	
DC Leakage Current	±1	±1	±1	±1	μA max	
Input Capacitance	33	33	33	33	pF typ	
REFERENCE INPUT						
REF IN Input Voltage Range	2.5	2.5	2.5	2.5	V	±1% for Specified Performance
DC Leakage Current	±1	±1	±1	±1	μA max	
Input Capacitance	10/20	10/20	10/20	10/20	pF typ	Track-and-Hold Mode
LOGIC INPUTS						
Input High Voltage, V _{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V _{INL}	0.4	0.4	0.4	0.4	V max	
Input Current, I _{IN}	±1	±1	±1	±1	μA max	Typically 10 nA, V _{IN} = 0 V or V _{DD}
Input Capacitance, C _{IN} ³	10	10	10	10	pF max	
LOGIC OUTPUTS						
Output High Voltage, V _{OH}	V _{DRIVE} - 0.2	V _{DRIVE} - 0.2	V _{DRIVE} - 0.2	V _{DRIVE} - 0.2	V min	I _{SOURCE} = 200 μA
Output Low Voltage, V _{OL}	0.4	0.4	0.4	0.4	V max	I _{SINK} = 200 μA
Floating-State Leakage Current	±10	±10	±10	±10	μA max	V _{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	10	10	10	pF max	
Output Coding	Straight (Natural) Binary	Straight (Natural) Binary	Straight (Natural) Binary	Straight (Natural) Binary		
CONVERSION RATE						
Conversion Time	14	14	14	14	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time	135	135	135	135	ns min	
Throughput Rate	1.5	1.2	1.5	1.2	MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS						
V _{DD}	+2.7/+5.25		+2.7/+5.25		V min/max	
I _{DD} ⁴						Digital Inputs = 0 V or DV _{DD}
Normal Mode	2.4		2.4		mA max	V _{DD} = 4.75 V to 5.25 V; Typ 2 mA; f _S = 1.5 MSPS
Quiescent Current	900		900		μA max	V _{DD} = 4.75 V to 5.25 V; f _S = 1.5 MSPS
Normal Mode	1.5		1.5		mA max	V _{DD} = 2.7 V to 3.3 V; Typ 1.3 mA; f _S = 1.2 MSPS
Quiescent Current	800		800		μA max	V _{DD} = 2.7 V to 3.3 V; f _S = 1.2 MSPS
Sleep Mode	1		1		μA max	CLK IN = 0 V or DV _{DD}
Power Dissipation ⁴						Digital Inputs = 0 V or DV _{DD}
Normal Mode	12		12		mW max	V _{DD} = 5 V
	4.5		4.5		mW max	V _{DD} = 3 V
Sleep Mode	5		5		μW max	V _{DD} = 5 V; CLK IN = 0 V or DV _{DD}
	3		3		μW max	V _{DD} = 3 V; CLK IN = 0 V or DV _{DD}

NOTES

¹Temperature ranges as follows: A and B Versions: -40°C to +85°C.²The AD7472 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 68 dB; THD (100 kHz) = -84 dB; INL ±0.8 LSB.³Sample tested @ 25°C to ensure compliance.⁴See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7470/AD7472

AD7472—SPECIFICATIONS¹ ($V_{DD} = 2.7\text{ V to }5.25\text{ V}^2$, REF IN = 2.5 V, Y Version: $f_{CLKIN} = 20\text{ MHz @ }5\text{ V}$ and $14\text{ MHz @ }3\text{ V}$; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

Parameter	Y Version ¹		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE	5 V	3 V		$f_S = 1.2\text{ MSPS @ }5\text{ V}$, $f_S = 875\text{ kSPS @ }3\text{ V}$
Signal to Noise + Distortion (SINAD)	69	69	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
	68	68	dB min	$f_{IN} = 100\text{ kHz Sine Wave}$
Signal-to-Noise Ratio (SNR)	70	70	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
	68	68	dB min	$f_{IN} = 100\text{ kHz Sine Wave}$
Total Harmonic Distortion (THD)	-83	-78	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
	-83	-84	dB typ	$f_{IN} = 100\text{ kHz Sine Wave}$
	-75	-75	dB max	$f_{IN} = 100\text{ kHz Sine Wave}$
Peak Harmonic or Spurious Noise (SFDR)	-86	-81	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
	-86	-86	dB typ	$f_{IN} = 100\text{ kHz Sine Wave}$
	-76	-76	dB max	$f_{IN} = 100\text{ kHz Sine Wave}$
Intermodulation Distortion (IMD)				
Second-Order Terms	-77	-77	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
	-86	-86	dB typ	$f_{IN} = 100\text{ kHz Sine Wave}$
Third-Order Terms	-77	-77	dB typ	$f_{IN} = 500\text{ kHz Sine Wave}$
	-86	-86	dB typ	$f_{IN} = 100\text{ kHz Sine Wave}$
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	20	20	MHz typ	@ 3 dB
DC ACCURACY				$f_S = 1.2\text{ MSPS @ }5\text{ V}$; $f_S = 875\text{ kSPS @ }3\text{ V}$
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1.8	±1.8	LSB max	Guaranteed No Missed Codes to 11 Bits
Offset Error	±10	±10	LSB max	
Gain Error	±2	±2	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN	0 to REF IN	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	V	±1% for Specified Performance
DC Leakage Current	±1	±1	µA max	
Input Capacitance	10/20	10/20	pF typ	Track-and-Hold Mode
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, $V_{IN} = 0\text{ V}$ or V_{DD}
Input Capacitance, C_{IN}^3	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2$	$V_{DRIVE} - 0.2$	V min	$I_{SOURCE} = 200\text{ µA}$
Output Low Voltage, V_{OL}	0.4	0.4	V max	$I_{SINK} = 200\text{ µA}$
Floating-State Leakage Current	±10	±10	µA max	$V_{DD} = 2.7\text{ V to }5.25\text{ V}$
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	14	14	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time	140	140	ns min	
Throughput Rate	1200	875	kSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25		V min/max	
I_{DD}^4				Digital Inputs = 0 V or DV_{DD}
Normal Mode	2.4		mA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_S = 1.2\text{ MSPS}$; Typ 2 mA
Quiescent Current	900		µA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_S = 1.2\text{ MSPS}$
Normal Mode	1.5		mA max	$V_{DD} = 2.7\text{ V to }3.3\text{ V}$; $f_S = 875\text{ kSPS}$; Typ 1.3 mA
Quiescent Current	800		µA max	$V_{DD} = 2.7\text{ V to }3.3\text{ V}$; $f_S = 875\text{ kSPS}$
Sleep Mode	2		µA max	CLK IN = 0 V or DV_{DD}
Power Dissipation ⁴				Digital Inputs = 0 V or DV_{DD}
Normal Mode	12		mW max	$V_{DD} = 5\text{ V}$
	4.5		mW max	$V_{DD} = 3\text{ V}$
Sleep Mode	10		µW max	$V_{DD} = 5\text{ V}$; CLK IN = 0 V or DV_{DD}
	6		µW max	$V_{DD} = 3\text{ V}$; CLK IN = 0 V or DV_{DD}

NOTES

¹Temperature ranges as follows: Y Version: -40°C to +125°C.

²The AD7472 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 68 dB; THD (100 kHz) = -84 dB; INL ±0.8 LSB.

³Sample tested @ 25°C to ensure compliance.

⁴See Power vs. Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS¹ ($V_{DD} = 2.7\text{ V to } 5.25\text{ V}$, REF IN = 2.5 V; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

Parameter	Limit at T_{MIN} , T_{MAX}		Unit	Description
	AD7470	AD7472		
f_{CLK}^2	10 30	10 26	kHz min MHz max	
$t_{CONVERT}$	436.42	531.66	ns min	$t_{CLK} = 1/f_{CLK\ IN}$
t_{WAKEUP}	1	1	μs max	Wake-Up Time
t_1	10	10	ns min	\overline{CONVST} Pulse Width
t_2	10 30	10 30	ns max ns max	\overline{CONVST} to \overline{BUSY} Delay, $V_{DD} = 5\text{ V}$, A and B Versions $V_{DD} = 5\text{ V}$, Y Version
t_3	0	0	ns max	$V_{DD} = 3\text{ V}$, A and B Versions $V_{DD} = 3\text{ V}$, Y Version
t_4^3	0	0	ns max	\overline{BUSY} to \overline{CS} Setup Time
t_5	20	20	ns min	\overline{CS} to \overline{RD} Setup Time
t_6^3	15	15	ns min	\overline{RD} Pulse Width
t_7^4	8	8	ns max	Data Access Time After Falling Edge of \overline{RD}
t_8	0	0	ns max	Bus Relinquish Time After Rising Edge of \overline{RD}
t_9	135	135	ns max	\overline{CS} to \overline{RD} Hold Time
		140	ns max	Acquisition Time
		100	ns min	A and B Versions Y Version
t_{10}	100	100	ns min	Quiet Time

NOTES

¹Sample tested at 25°C to ensure compliance. All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Figure 1.

²Mark/Space ratio for the CLK inputs is 40/60 to 60/40. First CLK pulse should be 10 ns min from falling edge of \overline{CONVST} .

³Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

⁴ t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7 , quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

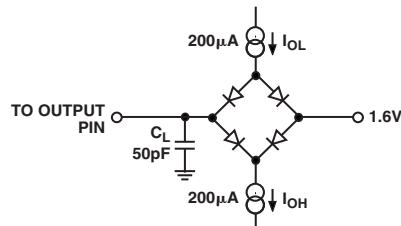


Figure 1. Load Circuit for Digital Output Timing Specifications

AD7470/AD7472

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted.)

AV _{DD} to AGND/DGND	−0.3 V to +7 V
DV _{DD} to AGND/DGND	−0.3 V to +7 V
V _{DRIVE} to AGND/DGND	−0.3 V to +7 V
AV _{DD} to DV _{DD}	−0.3 V to +0.3 V
V _{DRIVE} to DV _{DD}	−0.3 V to DV _{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV _{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV _{DD} + 0.3 V
REF IN to AGND	−0.3 V to AV _{DD} + 0.3 V
Input Current to Any Pin Except Supplies ²	±10 mA
Operating Temperature Range	
Commercial (A and B Versions)	−40°C to +85°C
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Junction Temperature	150°C
θ _{JA} Thermal Impedance	75°C/W (SOIC)
	115°C/W (TSSOP)
θ _{JC} Thermal Impedance	25°C/W (SOIC)
	35°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1.5 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Resolution (Bits)	Package Options ¹	Package Description
AD7470ARU	−40°C to +85°C	10	RU-24	TSSOP
AD7470ARU-REEL	−40°C to +85°C	10	RU-24	TSSOP
AD7470ARU-REEL7	−40°C to +85°C	10	RU-24	TSSOP
AD7472AR	−40°C to +85°C	12	R-24	SOIC
AD7472AR-REEL	−40°C to +85°C	12	R-24	SOIC
AD7472AR-REEL7	−40°C to +85°C	12	R-24	SOIC
AD7472ARU	−40°C to +85°C	12	RU-24	TSSOP
AD7472ARU-REEL	−40°C to +85°C	12	RU-24	TSSOP
AD7472ARU-REEL7	−40°C to +85°C	12	RU-24	TSSOP
AD7472BR	−40°C to +85°C	12	R-24	SOIC
AD7472BR-REEL	−40°C to +85°C	12	R-24	SOIC
AD7472BRU	−40°C to +85°C	12	RU-24	TSSOP
AD7472BRU-REEL	−40°C to +85°C	12	RU-24	TSSOP
AD7472BRU-REEL7	−40°C to +85°C	12	RU-24	TSSOP
AD7472YR	−40°C to +125°C	12	R-24	SOIC
AD7472YR-REEL	−40°C to +125°C	12	R-24	SOIC
AD7472YRU	−40°C to +125°C	12	RU-24	TSSOP
AD7472YRU-REEL	−40°C to +125°C	12	RU-24	TSSOP
AD7472YRU-REEL7	−40°C to +125°C	12	RU-24	TSSOP
EVAL-AD7470CB ²				Evaluation Board
EVAL-AD7472CB ²				Evaluation Board
EVAL CONTROL BRD ³				Controller Board

NOTES

¹R = SOIC; RU = TSSOP.

²This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

³This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, you need to order the specific ADC evaluation board, for example, EVAL-AD7472CB, the EVAL CONTROL BRD2, and a 12 V ac transformer. See the relevant evaluation board application note for more information.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7470/AD7472 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

