

1.75 MSPS, 4 mW 10-Bit/12-Bit Parallel ADCs

FEATURES Specified for V_{DD} of 2.7 V to 5.25 V 1.75 MSPS for AD7470 (10-Bit) 1.5 MSPS for AD7472 (12-Bit) Low Power AD7470: 3.34 mW Typ at 1.5 MSPS with 3 V Supplies 7.97 mW Typ at 1.75 MSPS with 5 V Supplies AD7472: 3.54 mW Typ at 1.2 MSPS with 3 V Supplies 8.7 mW Typ at 1.5 MSPS with 5 V Supplies Wide Input Bandwidth 70 dB Typ SNR at 500 kHz Input Frequency Flexible Power/Throughput Rate Management **No Pipeline Delays High Speed Parallel Interface** Sleep Mode: 50 nA Typ 24-Lead SOIC and TSSOP Packages

GENERAL DESCRIPTION

The AD7470/AD7472 are 10-bit/12-bit high speed, low power, successive approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS for the 12-bit AD7472 and up to 1.75 MSPS for the 10-bit AD7470. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using standard control inputs, allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$, and conversion is also initiated at this point. BUSY goes high at the start of conversion and goes low 531.66 ns after falling edge of $\overline{\text{CONVST}}$ (AD7472 with a clock frequency of 26 MHz) to indicate that the conversion is complete. There are no pipeline delays associated with the parts. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7470/AD7472 use advanced design techniques to achieve very low power dissipation at high throughput rates. With 3 V supplies and 1.5 MSPS throughput rates, the AD7470 typically consumes, on average, just 1.1 mA. With 5 V supplies and 1.75 MSPS, the average current consumption is typically 1.6 mA. The part also offers flexible power/throughput rate management. Operating the AD7470 with 3 V supplies and 500 kSPS throughput reduces the current consumption to 713 μ A. At 5 V supplies and 500 kSPS, the part consumes 944 μ A.

AD7470/AD7472

FUNCTIONAL BLOCK DIAGRAM



It is also possible to operate the parts in an auto sleep mode, where the part wakes up to do a conversion and automatically enters sleep mode at the end of conversion. This method allows very low power dissipation numbers at lower throughput rates. In this mode, the AD7472 can be operated with 3 V supplies at 100 kSPS, and consume an average current of just 124 μ A. At 5 V supplies and 100 kSPS, the average current consumption is 171 μ A.

The analog input range for the part is 0 V to REF IN. The 2.5 V reference is applied externally to the REF IN pin. The conversion rate is determined by the externally-applied clock.

PRODUCT HIGHLIGHTS

- 1. High Throughput with Low Power Consumption. The AD7470 offers 1.75 MSPS throughput and the AD7472 offers 1.5 MSPS throughput rates with 4 mW power consumption.
- 2. Flexible Power/Throughput Rate Management. The conversion rate is determined by an externally-applied clock allowing the power to be reduced as the conversion rate is reduced. The part also features an auto sleep mode to maximize power efficiency at lower throughput rates.
- 3. No Pipeline Delay. The part features a standard successive approximation ADC with accurate control of the sampling instant via a CONVST input and once off conversion control.

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AD7470/AD7472

$\label{eq:AD7470-SPECIFICATIONS} \begin{array}{l} (V_{DD} = 2.7 \ V \ to \ 5.25 \ V^2, \ \text{REF IN} = 2.5 \ V, \ f_{CLKIN} \\ T_A = T_{MIN} \ to \ T_{MAX}{}^3, \ unless \ otherwise \ noted.) \end{array} \\ \end{array}$

Parameter	A Versio	n ¹	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE Signal to Noise + Distortion (SINAD)	5 V 60 60	3 V 60 60	dB min dB min	$f_{S} = 1.75$ MSPS @ 5 V, $f_{S} = 1.5$ MSPS @ 3 V $f_{IN} = 500$ kHz Sine Wave $f_{IN} = 100$ kHz Sine Wave
Signal-to-Noise Ratio (SNR) Total Harmonic Distortion (THD)	60 60 -83	60 60 -83	dB min dB min dB typ	$ f_{IN} = 500 \text{ kHz Sine Wave} $ $ f_{IN} = 100 \text{ kHz Sine Wave} $ $ f_{IN} = 500 \text{ kHz Sine Wave} $
Peak Harmonic or Spurious Noise (SFDR)	-75 -85 -75	75 85 75	dB max dB typ dB max	$f_{IN} = 100 \text{ kHz}$ Sine Wave $f_{IN} = 500 \text{ kHz}$ Sine Wave $f_{N} = 100 \text{ kHz}$ Sine Wave
Intermodulation Distortion (IMD) Second-Order Terms	-79 -75	-75 -75	dB typ dB max	$f_{IN} = 500 \text{ kHz}$ Sine Wave $f_{NN} = 100 \text{ kHz}$ Sine Wave
Third-Order Terms	-77 -75	-75 -75 5	dB typ dB max	$f_{IN} = 500 \text{ kHz}$ Sine Wave $f_{IN} = 100 \text{ kHz}$ Sine Wave
Aperture Jetay Aperture Jitter Full Power Bandwidth	15 20	15 20	ps typ MHz typ	@ 3 dB
DC ACCURACY Resolution Integral Nonlinearity Differential Nonlinearity Offset Error Gain Error	$10 \\ \pm 1 \\ \pm 0.9 \\ \pm 2.5 \\ \pm 1$	$ \begin{array}{c} 10 \\ \pm 1 \\ \pm 0.9 \\ \pm 2.5 \\ \pm 1 \end{array} $	Bits LSB max LSB max LSB max LSB max	$f_S = 1.75$ MSPS @ 5 V; $f_S = 1.5$ MSPS @ 3 V Guaranteed No Missed Codes to 10 Bits
ANALOG INPUT Input Voltage Ranges DC Leakage Current Input Capacitance	0 to REF IN ±1 33	0 to REF IN ±1 33	V μA max pF typ	
REFERENCE INPUT REF IN Input Voltage Range DC Leakage Current Input Capacitance	2.5 ±1 10/20	2.5 ±1 10/20	V μA max pF typ	±1% for Specified Performance Track-and-Hold Mode
$\begin{array}{c} \hline \text{LOGIC INPUTS} \\ \text{Input High Voltage, } V_{\text{INH}} \\ \text{Input Low Voltage, } V_{\text{INL}} \\ \text{Input Current, } I_{\text{IN}} \\ \text{Input Capacitance, } C_{\text{IN}}{}^{4} \end{array}$	$2.4 \\ 0.4 \\ \pm 1 \\ 10$	$2.4 \\ 0.4 \\ \pm 1 \\ 10$	V min V max μA max pF max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
LOGIC OUTPUTS Output High Voltage, V _{OH} Output Low Voltage, V _{OL} Floating-State Leakage Current Floating-State Output Capacitance Output Coding	$V_{DRIVE} - 0.2$ 0.4 ± 10 10 Straight (Natu	$V_{DRIVE} - 0.2$ 0.4 ± 10 10 ural) Binary	V min V max μA max pF max	$I_{SOURCE} = 200 \ \mu A$ $I_{SINK} = 200 \ \mu A$ $V_{DD} = 2.7 \ V \text{ to } 5.25 \ V$
CONVERSION RATE Conversion Time Track-and-Hold Acquisition Time Throughput Rate	12 135 1.75	12 135 1.5	CLK IN Cycles (max) ns min MSPS max	Conversion Time + Acquisition Time CLK IN of 30 MHz @ 5 V and 24 MHz @ 3 V
$\begin{array}{c} \mbox{POWER REQUIREMENTS} \\ V_{DD} \\ I_{DD}{}^5 \\ \mbox{Normal Mode} \\ \mbox{Quiescent Current} \\ \mbox{Normal Mode} \\ \mbox{Quiescent Current} \\ \mbox{Sleep Mode} \\ \mbox{Sleep Mode} \\ \mbox{Sleep Mode} \end{array}$	+2.7/+5.25 2.4 900 1.5 800 1 1 12 4.5 5 3		V min/max mA max µA max mA max µA max µA max mW max µW max µW max	Digital Inputs = 0 V or DV_{DD} V_{DD} = 4.75 V to 5.25 V; f_{S} = 1.75 MSPS; Typ 2 mA V_{DD} = 4.75 V to 5.25 V; f_{S} = 1.75 MSPS V_{DD} = 2.7 V to 3.3 V; f_{S} = 1.5 MSPS; Typ 1.3 mA V_{DD} = 2.7 V to 3.3 V; f_{S} = 1.5 MSPS CLK IN = 0 V or DV_{DD} Digital Inputs = 0 V or DV_{DD} V_{DD} = 5 V V_{DD} = 3 V V_{DD} = 3 V; CLK IN = 0 V or DV_{DD} V_{DD} = 3 V; CLK IN = 0 V or DV_{DD}

NOTES

¹Temperature ranges as follows: A Version: -40°C to +85°C.

²The AD7470 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 59 dB; THD (100 kHz) = -84 dB; INL ±0.8 LSB.

³The AD7470 will typically maintain A-grade performance up to 125°C, with a reduced CLK of 20 MHz @ 5 V and 16 MHz @ 3 V. Typical sleep mode current @ 125°C is 700 nA. ⁴Sample tested @ 25°C to ensure compliance. ⁵See Power vs. Throughput Rate section.

AD7472–SPECIFICATIONS¹

 $(V_{DD}=2.7~V~to~5.25~V^2,~REF~IN=2.5~V,~A~and~B~Versions:~f_{CLKIN}=26~MHz~@~5~V~and~20~MHz~@~3~V,~T_A=T_{MIN}~to~T_{MAX},~unless otherwise noted.)$

Parameter	A Version ¹ B Version ¹		n ¹	Unit	Test Conditions/Comments	
DYNAMIC PERFORMANCE Signal to Noise + Distortion (SINAD) Signal-to-Noise Ratio (SNR) Total Harmonic Distortion (THD)	5 V 69 68 70 68 -83 -83	3 V 69 68 70 68 -78 -84	5 V 69 68 70 68 -83 -83	3 V 69 68 70 68 -78 -84	dB typ dB min dB typ dB min dB typ dB typ	$\begin{array}{l} f_{S} = 1.5 \; MSPS @.5 \; V, \; f_{S} = 1.2 \; MSPS @.3 \; V \\ f_{IN} = 500 \; kHz \; Sine \; Wave \\ f_{IN} = 100 \; kHz \; Sine \; Wave \\ f_{IN} = 500 \; kHz \; Sine \; Wave \\ f_{IN} = 100 \; kHz \; Sine \; Wave \\ f_{IN} = 500 \; kHz \; Sine \; Wave \\ f_{IN} = 500 \; kHz \; Sine \; Wave \\ f_{IN} = 100 \; kHz \; Sine \; Wave \\ \end{array}$
Peak Harmonic or Spurious Noise (SFDR)	-75 -86 -86 -76	-75 -81 -86 -76	-75 -86 -86 -76	-75 -81 -86 -76	dB max dB typ dB typ dB max	$ \begin{split} f_{IN} &= 100 \text{ kHz Sine Wave} \\ f_{IN} &= 500 \text{ kHz Sine Wave} \\ f_{IN} &= 100 \text{ kHz Sine Wave} \\ f_{IN} &= 100 \text{ kHz Sine Wave} \end{split} $
Intermodulation Distortion (IMD) Second-Order Terms Third-Order Terms Aperture Delay	-77 -86 -77 -86 5	77 86 77 86 5	-77 -86 -77 -86 5	-77 -86 -77 -86 5	dB typ dB typ dB typ dB typ ns typ	$\begin{array}{l} f_{\rm IN} = 500 \ \rm kHz \ \rm Sine \ Wave \\ f_{\rm IN} = 100 \ \rm kHz \ \rm Sine \ Wave \\ f_{\rm IN} = 500 \ \rm kHz \ \rm Sine \ Wave \\ f_{\rm IN} = 100 \ \rm kHz \ \rm Sine \ Wave \\ \end{array}$
Aperture Jitter Full Power Bandwidth	15 20	15 20	15 20	15 20	ps typ MHz typ	@ 3 dB
DC ACCURACY Resolution Integral Nonlinearity	12 ±2	12 ±2	12 ±1	12 ±1	Bits LSB max	$f_S = 1.5 \text{ MSPS } @ 5 \text{ V}, f_S = 1.2 \text{ MSPS } @ 3 \text{ V}$ Guaranteed No Missed Codes to 11 Bits (A Version)
Differential Nonlinearity Offset Error Gain Error	± 1.8 ± 10 ± 2	± 1.8 ± 10 ± 2	±0.9 ±10 +2	± 0.9 ± 10 ± 2	LSB max LSB max	(B Version)
ANALOG INPUT Input Voltage Ranges DC Leakage Current Input Capacitance	0 to REF IN ±1 33	0 to REF IN ±1 33	0 to REF IN ±1 33	0 to REF IN ±1 33	V μA max pF typ	
REFERENCE INPUT REF IN Input Voltage Range DC Leakage Current Input Capacitance	2.5 ±1 10/20	2.5 ±1 10/20	2.5 ±1 10/20	2.5 ±1 10/20	V μA max pF typ	±1% for Specified Performance Track-and-Hold Mode
$\begin{array}{c} \mbox{LOGIC INPUTS} \\ \mbox{Input High Voltage, } V_{\rm INH} \\ \mbox{Input Low Voltage, } V_{\rm INL} \\ \mbox{Input Current, } I_{\rm IN} \\ \mbox{Input Capacitance, } C_{\rm IN}^{-3} \end{array}$	2.4 0.4 ±1 10	$2.4 \\ 0.4 \\ \pm 1 \\ 10$	$2.4 \\ 0.4 \\ \pm 1 \\ 10$	2.4 0.4 ±1 10	V min V max μA max pF max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
LOGIC OUTPUTS Output High Voltage, V _{OH} Output Low Voltage, V _{OL} Floating-State Leakage Current Floating-State Output Capacitance Output Coding	$V_{DRIVE} - 0.2$ 0.4 ± 10 10 Straight (Nat	$V_{DRIVE} - 0.2$ 0.4 ±10 10 ural) Binary	$V_{DRIVE} - 0.2$ 0.4 ± 10 10 Straight (Nat	$V_{DRIVE} - 0.2$ 0.4 ± 10 10 ural) Binary	V min V max μA max pF max	$I_{SOURCE} = 200 \ \mu A$ $I_{SINK} = 200 \ \mu A$ $V_{DD} = 2.7 \ V \ to \ 5.25 \ V$
CONVERSION RATE Conversion Time	14	14	14	14	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time Throughput Rate	135 1.5	135 1.2	135 1.5	135 1.2	ns min MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS V _{DD} I _{DD} ⁴ Normal Mode Quiescent Current Normal Mode Quiescent Current Sleep Mode Power Dissipation ⁴ Normal Mode Sleep Mode	+2.7/+5.25 2.4 900 1.5 800 1 12 4.5 5 3		+2.7/+5.25 2.4 900 1.5 800 1 12 4.5 5 3		V min/max mA max μA max μA max μA max μA max mW max μW max μW max μW max	

NOTES

¹Temperature ranges as follows: A and B Versions: -40°C to +85°C.

²The AD7472 functionally works at 2.35 V. Typical specifications @ 25° C for SNR (100 kHz) = 68 dB; THD (100 kHz) = -84 dB; INL ±0.8 LSB.

³Sample tested @ 25°C to ensure compliance.

⁴See Power vs. Throughput Rate section.

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AD7470/AD7472

$\label{eq:AD7472} AD7472 - SPECIFICATIONS^{1} \ \ \ \ (V_{DD} = 2.7 \ V \ to \ 5.25 \ V^{2}, \ REF \ IN = 2.5 \ V, Y \ Version: \ f_{CLKIN} = 20 \ MHz \ @ 5 \ V \ and \ 14 \ MHz \ @ 3 \ V; \ T_{A} = T_{MIN} \ to \ T_{MAX}, \ unless \ otherwise \ noted.)$

$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Parameter	Y Version	n ¹	Unit	Test Conditions/Comments
	DYNAMIC PERFORMANCE	5 V	3 V		$f_{e} = 1.2 \text{ MSPS } @ 5 \text{ V}, f_{e} = 875 \text{ kSPS } @ 3 \text{ V}$
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Signal to Noise + Distortion (SINAD)	69	69	dB typ	$f_{\rm DV} = 500 \text{ kHz}$ Sine Wave
		68	68	dB min	$f_{IN} = 100 \text{ kHz}$ Sine Wave
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Signal-to-Noise Ratio (SNR)	70	70	dB typ	$f_{IN} = 500 \text{ kHz}$ Sine Wave
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	<u> </u>	68	68	dB min	$f_{IN} = 100 \text{ kHz}$ Sine Wave
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Total Harmonic Distortion (THD)	-83	-78	dB typ	$f_{IN} = 500 \text{ kHz}$ Sine Wave
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		-83	-84	dB typ	f_{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR) -86 -86 -86 dB typ $f_{15} = 500$ HHz Sine Wave Intermodulation Distortion (IMD) -76 -76 dB typ $f_{15} = 100$ HHz Sine Wave Second-Order Terms -76 -77 dB typ $f_{15} = 100$ HHz Sine Wave Third-Order Terms -76 -77 dB typ $f_{15} = 500$ HHz Sine Wave Aperture Ditter -76 -77 dB typ $f_{15} = 500$ HHz Sine Wave Aperture Ditter 15 15 ps typ $f_{16} = 500$ HHz Sine Wave Poll Power Bandwidth 20 20 MHz typ @ 3 dB DC ACCURACY Resolution 12 12 ISB max Guaranteed No Missed Codes to 11 Bits Inferentia Nonlinearity ± 1.8 1.5B max Guaranteed No Missed Codes to 11 Bits Guaranteed No Missed Codes to 11 Bits Offsec Error ± 1.4 ± 1.8 I.5B max Guaranteed No Missed Codes to 11 Bits DC Lackage Current ± 1 ± 1 μ Max Track-and-Hold Mode IOGIC INPUTS μ μ Max Typically 10 nA, $V_{DN} = 0$ V or V_{DD} Input Capacitance		-75	-75	dB max	f _{IN} = 100 kHz Sine Wave
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Peak Harmonic or Spurious Noise (SFDR)	-86	-81	dB typ	f_{IN} = 500 kHz Sine Wave
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		-86	-86	dB typ	$f_{IN} = 100 \text{ kHz}$ Sine Wave
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		-76	-76	dB max	$f_{IN} = 100 \text{ kHz Sine Wave}$
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Intermodulation Distortion (IMD)			10	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Second-Order Terms	-77	-77	dB typ	$f_{\rm IN} = 500 \text{ kHz Sine Wave}$
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Third Order Torms	-80	-80	dB typ	$I_{\rm IN} = 100 \text{ kHz}$ Sine Wave f = 500 kHz Sine Wave
Aperture Delay Aperture Jitter Toul Yover Bandwidth Tou 20 Tou 20 Tou Mitz typ Insp ps typ Insp (g) 3 dB DC ACCURACY Resolution 12 12 12 Iss ps typ (g) 3 dB DC ACCURACY Resolution 12 12 Iss ps typ (g) 3 dB DC ACCURACY Resolution 12 12 Iss ps typ (g) 3 dB Differential Nonlinearity Differential Nonlinearity ±1.8 ±1.8 Iss ps typ (g) 3 dB Office Error ±1.8 ±1.8 Iss max (g) arranteed No Missed Codes to 11 Bits Office Error ±1.8 ±1.8 Iss max (g) arranteed No Missed Codes to 11 Bits DC Lackage Current ±1 ±1 ph max (g) arranteed No Missed Codes to 11 Bits REFIENCE INPUT REFIENCE INPUT (g) arranteed No Missed Codes to 11 Dits (g) arranteed No Mode Input Capacitance 10/20 10/20 (g) arranteed No Missed Codes to 11 Bits Input Capacitance 10/20 10/20 (g) arranteed No Missed Codes to 11 Bits Input Capacitance 10/20 10/20 (g) arranteed No Missed C	Third-Order Terms	-11	-11	dB typ	$I_{\rm IN} = 500 \text{ kHz}$ Sine wave
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Aperture Delay	-80	-80	ub typ	$I_{\rm IN} = 100$ kHz Sille wave
Ind Def Def <thdef< th=""> <thdef< th=""> <thdef< th=""></thdef<></thdef<></thdef<>	Aperture litter	15	15	ns typ	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Full Power Bandwidth	20	20	MHz typ	@ 3 dB
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		20	20	initiz typ	$f = 1.0 \text{ MODS} \oplus 5 \text{ M/f} = 975 \text{ LODS} \oplus 2 \text{ M}$
Responsibility 12 12 12 12 13 14 14 15 max Guaranteed No Missed Codes to 11 Bits Differential Nonlinearity 11.8 ±1.8 LSB max LSB max Guaranteed No Missed Codes to 11 Bits Offset Error ±10 ±10 LSB max Guaranteed No Missed Codes to 11 Bits MALOG INPUT Input Capacitance 0 to REF IN 0 to REF IN V V DC Leakage Current ±1 ±1 µ/max pf typ Track-and-Hold Mode IDQUE Consequence 10/20 10/20 pF typ Track-and-Hold Mode IOGIC INPUTS 0.4 0.4 V min timput Capacitance 10/20 10/20 Track-and-Hold Mode IOGIC OUTPUTS 0.4 0.4 V max Typically 10 nA, V _{IN} = 0 V or V _{DD} Pf max Input Capacitance 0.4 0.4 V max Typically 10 nA, V _{IN} = 0 V or V _{DD} Input Capacitance 0.4 0.4 V max Typically 10 nA, V _{IN} = 0 V or V _{DD} Input Capacitance 0.4 0.4 V max Typically 10 nA, V _{IN} = 0 V or V _{DD} Input Capacit	DUACCURACY	10	10	Dite	$I_{S} = 1.2 \text{ MSPS} (a) 5 \text{ V}; I_{S} = 875 \text{ KSPS} (a) 3 \text{ V}$
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Resolution	12	12	DIIS LSD more	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Differential Nonlinearity	±2 +1 9	±2 +1.9	LSB max	Guarantood No Missod Codes to 11 Pits
Olise Liftor $\pm 10^{\circ}$ ± 1	Offect Error	± 1.0 ± 10	± 1.0 ± 10	LSD max	Guaranteed No Missed Codes to 11 Bits
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Gain Error	$^{\pm 10}_{\pm 2}$	$\pm 10 + 2$	LSD max	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		12	12	LOD IIIdx	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	ANALOG INPUT			*7	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	DC Lashage Connect	0 to REF IN	0 to KEF IN	V	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Canagitance	±1 22	±1 22	pF tup	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				prityp	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	REFERENCE INPUT	a =	0.5	**	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	REF IN Input Voltage Range	2.5	2.5	V	$\pm 1\%$ for Specified Performance
Input Capacitance10/2010/20pr typTrack-and-Hold ModeLOGIC INPUTS	DC Leakage Current	±1 10/20	±1 10/20	μA max	Treate and Hald Made
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		10/20	10/20	рг тур	I rack-and-Hold Mode
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	LOGIC INPUTS				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input High Voltage, V _{INH}	2.4	2.4	V min	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Low Voltage, V _{INL}	0.4	0.4	V max	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Current, I _{IN}	±1	±1	μA max	Typically 10 nA, $V_{IN} = 0$ V or V_{DD}
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Capacitance, C _{IN} ⁵	10	10	pF max	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	LOGIC OUTPUTS				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Output High Voltage, V _{OH}	$V_{DRIVE} - 0.2$	$V_{DRIVE} - 0.2$	V min	$I_{SOURCE} = 200 \mu A$
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Output Low Voltage, V _{OL}	0.4	0.4	V max	$I_{SINK} = 200 \mu A$
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Floating-State Leakage Current	±10	±10	µA max	$V_{DD} = 2.7 \text{ V to } 5.25 \text{ V}$
Output CodingStraight (Natural) BinaryCONVERSION RATE Conversion Time1414Track-and-Hold Acquisition Time140140Throughput Rate1200875POWER REQUIREMENTS VDD $+2.7/+5.25$ V min/maxVormal Mode Quiescent Current2.4mA maxNormal Mode Quiescent Current1.5mA maxQuiescent Current Sleep Mode800 μA maxVormal Mode Quiescent Current2Power Dissipation ⁴ Normal Mode12Power Dissipation ⁴ Normal Mode12Power Dissipation ⁴ Normal Mode12Normal Mode Quiescent Current10Power Dissipation ⁴ Normal Mode10Power Dissipation ⁴ Normal Mode12Normal Mode12Normal Mode10UP Normal Mode10UP Norma	Floating-State Output Capacitance	10 Sturiality (Natur	10 1) Dimension	pF max	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		Straight (Natt	Iral) billary		
Conversion Time1414CLK IN Cycles (max) ns minTrack-and-Hold Acquisition Time140140ns minThroughput Rate1200875kSPS maxConversion Time + Acquisition TimePOWER REQUIREMENTS V_{DD} $+2.7/+5.25$ V min/maxDigital Inputs = 0 V or DV_{DD}Normal Mode2.4mA max $V_{DD} = 4.75 V to 5.25 V; f_S = 1.2 MSPS; Typ 2 mA$ Quiescent Current900 $\mu A max$ $V_{DD} = 4.75 V to 5.25 V; f_S = 1.2 MSPS; Typ 2 mA$ Quiescent Current900 $\mu A max$ $V_{DD} = 2.7 V to 3.3 V; f_S = 875 kSPS; Typ 1.3 mA$ Quiescent Current800 $\mu A max$ $V_{DD} = 2.7 V to 3.3 V; f_S = 875 kSPS; Typ 1.3 mA$ Quiescent Current800 $\mu A max$ $V_{DD} = 2.7 V to 3.3 V; f_S = 875 kSPSSleep Mode12\mu M maxV_{DD} = 5 VNormal Mode12mW maxV_{DD} = 3 VSleep Mode10\mu W maxV_{DD} = 3 V; CLK IN = 0 V or DV_{DD}\phi10\mu W maxV_{DD} = 3 V; CLK IN = 0 V or DV_{DD}$	CONVERSION RATE				
Track-and-Hold Acquisition 1 time140140ns minThroughput Rate1200875kSPS maxConversion Time + Acquisition TimePOWER REQUIREMENTS V_{DD} $+2.7/+5.25$ V min/maxDigital Inputs = 0 V or DV_{DD} N_{DD}^4 P_{DD}^4 Digital Inputs = 0 V or DV_{DD}Digital Inputs = 0 V or DV_{DD}Normal Mode2.4mA max $V_{DD} = 4.75 V$ to 5.25 V; $f_S = 1.2 MSPS$; Typ 2 mAQuiescent Current900 μA max $V_{DD} = 2.7 V$ to 3.3 V; $f_S = 875 kSPS$; Typ 1.3 mAQuiescent Current800 μA max $V_{DD} = 2.7 V$ to 3.3 V; $f_S = 875 kSPS$; Typ 1.3 mASleep Mode2 μA max $V_{DD} = 5.7 V$ to 7.0 DV_{DD}Normal Mode12mW max $V_{DD} = 5 V$ Normal Mode10 μW max $V_{DD} = 5 V$; CLK IN = 0 V or DV_{DD}Normal Mode10 μW max $V_{DD} = 3 V$; CLK IN = 0 V or DV_{DD}	Conversion Time	14	14	CLK IN Cycles (max)	
Informing the field of the	Track-and-Hold Acquisition Time	140	140	ns min	Conversion Time I Acquisition Time
POWER REQUIREMENTS V_{DD} I_{DD}^4 +2.7/+5.25V min/maxDigital Inputs = 0 V or DV_{DD} $D_{DD} = 4.75 V to 5.25 V; f_s = 1.2 MSPS; Typ 2 mAQ_{DD} expression of the second se$		1200	615	KSF 5 IIIax	Conversion Time + Acquisition Time
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	POWER REQUIREMENTS				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V _{DD}	+2.7/+5.25		V min/max	
Normal Mode2.4mA max $V_{DD} = 4.75$ V to 5.25 V; $f_S = 1.2$ MSPS; $1yp 2$ mAQuiescent Current900 μA max $V_{DD} = 4.75$ V to 5.25 V; $f_S = 1.2$ MSPS; $1yp 2$ mANormal Mode1.5mA max $V_{DD} = 2.7$ V to 5.25 V; $f_S = 1.2$ MSPSQuiescent Current800 μA max $V_{DD} = 2.7$ V to 3.3 V; $f_S = 875$ kSPS; $Typ 1.3$ mASleep Mode2 μA max $V_{DD} = 2.7$ V to 3.3 V; $f_S = 875$ kSPSPower Dissipation ⁴ Digital Inputs = 0 V or DV_{DD}Normal Mode12mW max $V_{DD} = 5$ VSleep Mode10 μW max $V_{DD} = 5$ V; CLK IN = 0 V or DV_{DD}6 μW max $V_{DD} = 3$ V; CLK IN = 0 V or DV_{DD}					Digital Inputs = $0 \text{ V or } DV_{DD}$
Quiescent Current900 $\mu A \max$ $V_{DD} = 4.75 V \text{ to } 5.25 V; I_S = 1.2 \text{ MSPS}$ Normal Mode1.5mA max $V_{DD} = 2.7 V \text{ to } 3.3 V; I_S = 875 \text{ kSPS}; Typ 1.3 mA}$ Quiescent Current800 $\mu A \max$ $V_{DD} = 2.7 V \text{ to } 3.3 V; I_S = 875 \text{ kSPS}$ Sleep Mode2 $\mu A \max$ $V_{DD} = 2.7 V \text{ to } 3.3 V; I_S = 875 \text{ kSPS}$ Normal Mode12 $\mu A \max$ Digital Inputs = 0 V or DV_{DD}Normal Mode12mW max $V_{DD} = 5 V$ Sleep Mode10 $\mu W \max$ $V_{DD} = 5 V; CLK IN = 0 V or DV_{DD}$ 6 $\mu W \max$ $V_{DD} = 3 V; CLK IN = 0 V or DV_{DD}$	Normal Mode	2.4		mA max	$V_{DD} = 4.75$ V to 5.25 V; $I_S = 1.2$ MSPS; Typ 2 mA
Normal Mode1.5mA max $V_{DD} = 2.7$ V to 3.3 V; $f_S = 875$ kSPS; 1yp 1.3 mAQuiescent Current800 μA max $V_{DD} = 2.7$ V to 3.3 V; $f_S = 875$ kSPSSleep Mode2 μA maxCLK IN = 0 V or DV_{DD}Power Dissipation ⁴ Digital Inputs = 0 V or DV_{DD}Normal Mode12mW max $V_{DD} = 5$ VSleep Mode10 μW max $V_{DD} = 5$ V; CLK IN = 0 V or DV_{DD}6 μW max $V_{DD} = 3$ V; CLK IN = 0 V or DV_{DD}	Quiescent Current	900		μA max	$V_{DD} = 4.75 V \text{ to } 5.25 V; I_S = 1.2 \text{ MSPS}$
Quescent currentoutput $\mu A \max$ $V_{DD} = 2.7 \text{ V to } 3.5 \text{ V; } \text{ Is} = 875 \text{ KSPS}$ Sleep Mode2 $\mu A \max$ CLK IN = 0 V or DV_{DD} Power Dissipation ⁴ 12mW max $V_{DD} = 5 \text{ V}$ Normal Mode12mW max $V_{DD} = 5 \text{ V}$ Sleep Mode10 $\mu W \max$ $V_{DD} = 3 \text{ V}$ 6 $\mu W \max$ $V_{DD} = 3 \text{ V}$; CLK IN = 0 V or DV_{DD}	Normal Mode	1.5		IIIA max	$v_{DD} - 2.1 v to 2.2 v; t_s = 8/5 \text{ KSPS; 1yp 1.3 mA}$
Sheep Mode2 $\mu X \max$ CLR IN - 0 V or DV_{DD} Power Dissipation ⁴ Digital Inputs = 0 V or DV_{DD} Normal Mode12Normal Mode4.5Sleep Mode10 $\mu W \max$ $V_{DD} = 3 V$ $\mu W \max$ $V_{DD} = 3 V$; CLK IN = 0 V or DV_{DD} ϕ ϕ ϕ ψ	Quiescent Current Sleep Mode	200		μA max	$v_{DD} - 2.1 v to 2.2 v; t_s = 8/2 kSPS$ CLK IN = 0 V or DV
Normal Mode12mW max $V_{DD} = 5 V$ Normal Mode4.5mW max $V_{DD} = 3 V$ Sleep Mode10 μW max $V_{DD} = 5 V$; CLK IN = 0 V or DV_{DD}6 μW max $V_{DD} = 3 V$; CLK IN = 0 V or DV_{DD}	Bower Dissipation ⁴			µri max	Digital Inputs = $0 \text{ V or } D \text{ V}_{DD}$
NOTES12IIW max $V_{DD} = 3 V$ 4.5 mW max $V_{DD} = 3 V$ 10 μW max $V_{DD} = 5 V$; CLK IN = 0 V or DV_{DD} 6 μW max $V_{DD} = 3 V$; CLK IN = 0 V or DV_{DD}	Normal Mode	12		mW may	$V_{\rm DD} = 5 V$
Sleep Mode $ \begin{array}{c} $	Inolillal Mode	4.5		mW may	$v_{DD} = 3 v$ $V_{DD} = 3 V$
$\frac{10}{6}$ $\frac{\mu W \ \text{max}}{\mu W \ \text{max}}$ $\frac{V_{\text{DD}} = 3 \ \text{V}; \ \text{CLK IN} = 0 \ \text{V or } \text{DV}_{\text{DD}}}{V_{\text{DD}}}$	Sleep Mode	10		IIW max	$V_{DD} = 5 V$: CLK IN = 0 V or DV_{DD}
	Steep mode	6		uW max	$V_{DD} = 3 \text{ V}; \text{ CLK IN} = 0 \text{ V or } DV_{DD}$
	NOTES				

¹Temperature ranges as follows: Y Version: -40°C to +125°C.

²The AD7472 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 68 dB; THD (100 kHz) = -84 dB; INL ±0.8 LSB.

³Sample tested @ 25°C to ensure compliance.

⁴See Power vs. Throughput Rate section.

TIMING SPECIFICATIONS¹ ($V_{DD} = 2.7 \text{ V to } 5.25 \text{ V}$, REF IN = 2.5 V; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

	Limit at T _{MIN} , T _{MAX}				
Parameter	AD7470	AD7472	Unit	Description	
f _{CLK} ²	10	10	kHz min		
	30	26	MHz max		
t _{CONVERT}	436.42	531.66	ns min	$t_{CLK} = 1/f_{CLK IN}$	
t _{WAKEUP}	1	1	µs max	Wake-Up Time	
t ₁	10	10	ns min	CONVST Pulse Width	
t ₂				$\overline{\text{CONVST}}$ to BUSY Delay,	
	10	10	ns max	V_{DD} = 5 V, A and B Versions	
		15	ns max	V_{DD} = 5 V, Y Version	
	30	30	ns max	V_{DD} = 3 V, A and B Versions	
		35	ns max	V_{DD} = 3 V, Y Version	
t ₃	0	0	ns max	BUSY to $\overline{\text{CS}}$ Setup Time	
t_4^3	0	0	ns max	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time	
t ₅	20	20	ns min	RD Pulse Width	
t_{6}^{3}	15	15	ns min	Data Access Time After Falling Edge of \overline{RD}	
t_7^4	8	8	ns max	Bus Relinquish Time After Rising Edge of RD	
t ₈	0	0	ns max	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	
t9				Acquisition Time	
	135	135	ns max	A and B Versions	
		140	ns max	Y Version	
t ₁₀	100	100	ns min	Quiet Time	

NOTES

¹Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Figure 1.

²Mark/Space ratio for the CLK inputs is 40/60 to 60/40. First CLK pulse should be 10 ns min from falling edge of $\overline{\text{CONVST}}$.

³Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

 4 t₇ is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated

 t_7 is derived non-the incastred time taken by the data outputs to change 0.5 v when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7 , quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.



Figure 1. Load Circuit for Digital Output Timing Specifications

AD7470/AD7472

ABSOLUTE MAXIMUM RATINGS¹

 $(T_A = 25^{\circ}C \text{ unless otherwise noted.})$

AV_{DD} to $AGND/DGND$
DV_{DD} to AGND/DGND
V_{DRIVE} to AGND/DGND
AV_{DD} to DV_{DD}
V_{DRIVE} to DV_{DD} $\ \ldots \ -0.3 \ V$ to DV_{DD} + 0.3 V
AGND to DGND $\hdotspace{-0.3}$ V to +0.3 V
Analog Input Voltage to AGND \ldots -0.3 V to AV _{DD} + 0.3 V
Digital Input Voltage to DGND \dots -0.3 V to DV _{DD} + 0.3 V
REF IN to AGND \ldots
Input Current to Any Pin Except Supplies ² $\pm 10 \text{ mA}$
Operating Temperature Range
Commercial (A and B Versions)40°C to +85°C
Industrial (Y Version)40°C to +125°C
Storage Temperature Range –65°C to +150°C

Junction Temperature 150°C
θ_{JA} Thermal Impedance
$\theta_{\rm IC}$ Thermal Impedance
Lead Temperature, Soldering
Vapor Phase (60 sec) 215°C
Infrared (15 sec) 220°C
ESD

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Transient currents of up to 100 mA will not cause SCR latch-up.

Model	Temperature Range	Resolution (Bits)	Package Options ¹	Package Description
AD7470ARU	-40°C to +85°C	10	RU-24	TSSOP
AD7470ARU-REEL	-40°C to +85°C	10	RU-24	TSSOP
AD7470ARU-REEL7	-40°C to +85°C	10	RU-24	TSSOP
AD7472AR	-40°C to +85°C	12	R-24	SOIC
AD7472AR-REEL	-40°C to +85°C	12	R-24	SOIC
AD7472AR-REEL7	-40°C to +85°C	12	R-24	SOIC
AD7472ARU	-40°C to +85°C	12	RU-24	TSSOP
AD7472ARU-REEL	-40°C to +85°C	12	RU-24	TSSOP
AD7472ARU-REEL7	-40°C to +85°C	12	RU-24	TSSOP
AD7472BR	-40°C to +85°C	12	R-24	SOIC
AD7472BR-REEL	-40°C to +85°C	12	R-24	SOIC
AD7472BRU	-40°C to +85°C	12	RU-24	TSSOP
AD7472BRU-REEL	-40°C to +85°C	12	RU-24	TSSOP
AD7472BRU-REEL7	-40°C to +85°C	12	RU-24	TSSOP
AD7472YR	-40°C to +125°C	12	R-24	SOIC
AD7472YR-REEL	-40°C to +125°C	12	R-24	SOIC
AD7472YRU	-40°C to +125°C	12	RU-24	TSSOP
AD7472YRU-REEL	-40°C to +125°C	12	RU-24	TSSOP
AD7472YRU-REEL7	-40°C to +125°C	12	RU-24	TSSOP
EVAL-AD7470CB ²				Evaluation Board
EVAL-AD7472CB ²				Evaluation Board
EVAL CONTROL BRD2 ³				Controller Board

ORDERING GUIDE

NOTES

 ${}^{1}R = SOIC; RU = TSSOP.$

²This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
³This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, you need to order the specific ADC evaluation board, for example, EVAL-AD7472CB, the EVAL CONTROL BRD2, and a 12 V ac transformer. See the relevant evaluation board application note for more information.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7470/AD7472 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

