AD8306 Evaluation Board

EVAL-AD8306EB

BOARD DESCRIPTION

The AD8306 evaluation board has been carefully laid out and tested to demonstrate the specified high speed performance of the device. Figure 1 shows the schematic of the evaluation board. For ordering information, please refer to the Ordering Guide. Links, switches, and component settings for different setups are described in Table I.

ORDERING GUIDE

Model	Package Description
AD8306-EVAL	Evaluation Board

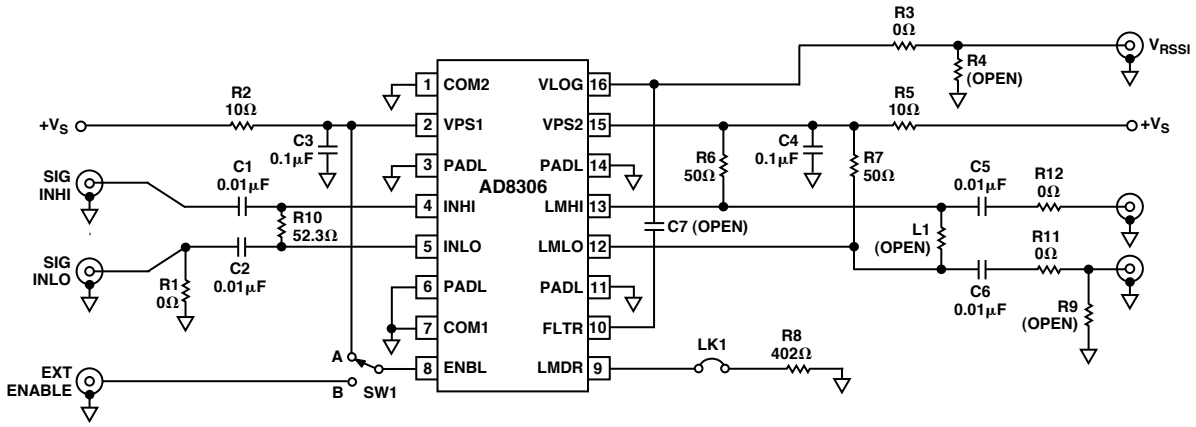

Figure 1. Evaluation Board Schematic

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the EVAL-AD8306EB features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

REV. 0

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Table I. Evaluation Board Setup Options

Component	Function	Default Condition
SW1	Device Enable. When in Position A, the ENBL pin is connected to $+V_S$ and the AD8306 is in normal operating mode. In Position B, the ENBL pin is connected to an SMA connector labeled Ext Enable. A signal can be applied to this connector to enable/disable the AD8306.	SW1 = A
R1	This pad is used to ac-couple INLO to ground for single-ended input drive. To drive the AD8306 differentially, R1 should be removed.	R1 = 0 Ω
R/L, C1, C2	Input Interface. The 52.3 Ω resistor in position R10, along with C1 and C2, create a high-pass input filter whose corner frequency (640 kHz) is equal to $1/(2\pi RC)$, where C = (C1)/2 and R is the parallel combination of 52.3 Ω and the AD8306's input impedance of 1000 Ω. Alternatively, the 52.3 Ω resistor can be replaced by an inductor to form an input matching network. See the Input Matching Network section in the AD8306 data sheet for more details.	R10 = 52.3 Ω C1 = C2 = 0.01 µF
R3/R4	Slope Adjust. A simple slope adjustment can be implemented by adding a resistive divider at the VLOG output. R3 and R4, whose sum should be about 1 kΩ and never less than 40 Ω (see specs), set the slope according to the equation: $Slope = 20\ mV/dB \times R4/(R3 + R4)$.	R3 = 0 Ω R4 = ∞
L1, C5, C6	Limiter Output Coupling. C5 and C6 ac-couple the limiter's differential outputs. By adjusting these values and installing an inductor in L1, an output matching network can be implemented. To convert the limiter's differential output to single-ended, R11 and R12 (nominally 0 Ω) can be replaced with a surface mount balun such as the ETC1-1-13 (Macom). The balun can be grounded by soldering a 0 Ω into Position R9 (nominally open).	L1 = Open C5 = 0.01 µF C6 = 0.01 µF R9 = Open R10 = R11 = 0 Ω
R8, LK1	Limiter Output Current. With LK1 installed, R8 enables and sets the limiter output current. The limiter's output current is set according to the equation ($I_{OUT} = 400\ mV/R8$). The limiter current can be as high as 10 mA (R8 = 40 Ω). To disable the limiter (recommended if the limiter is not being used), LK1 should be removed.	LK1 Installed. R8 = 402 Ω R6, R7 (Limited Load Resistors) = 50 Ω
C7	RSSI Bandwidth Adjust. The addition of C7 (farads) will lower the RSSI bandwidth of the VLOG output according to the equation: $f_{CORNER}\ (Hz) = 12.7 \times 10^{-6}/(C7 + 3.5 \times 10^{-12})$.	C7 = Open

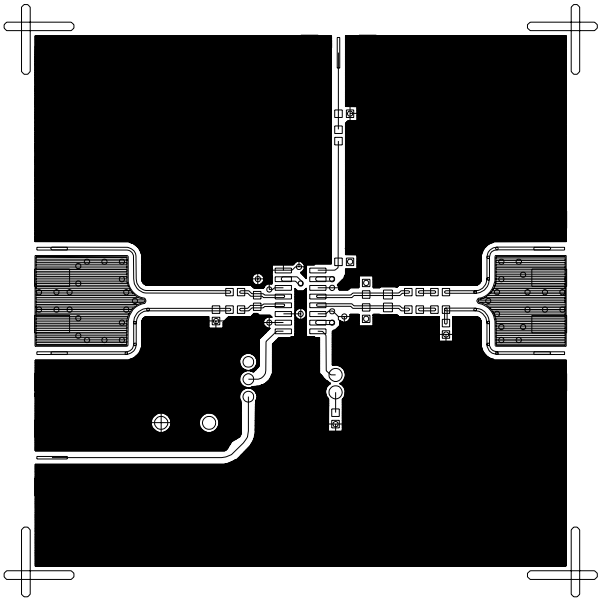

Figure 2. Layout of Signal Layer

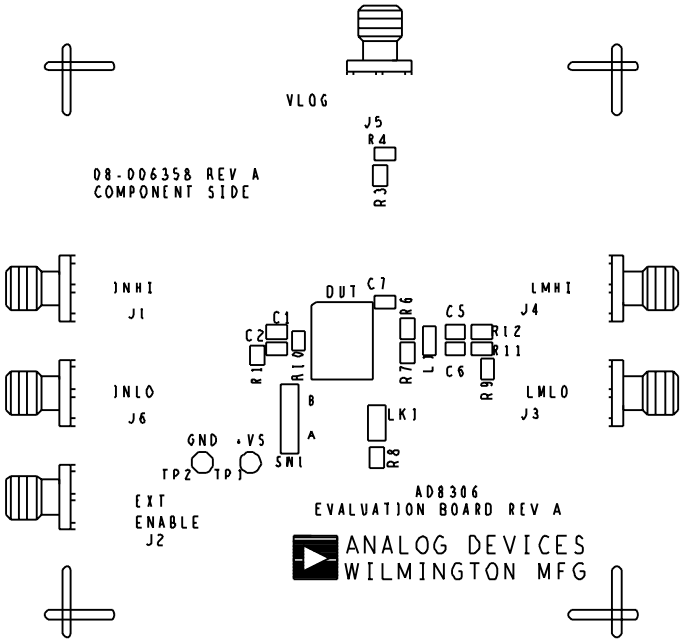

Figure 4. Signal Layer Silkscreen

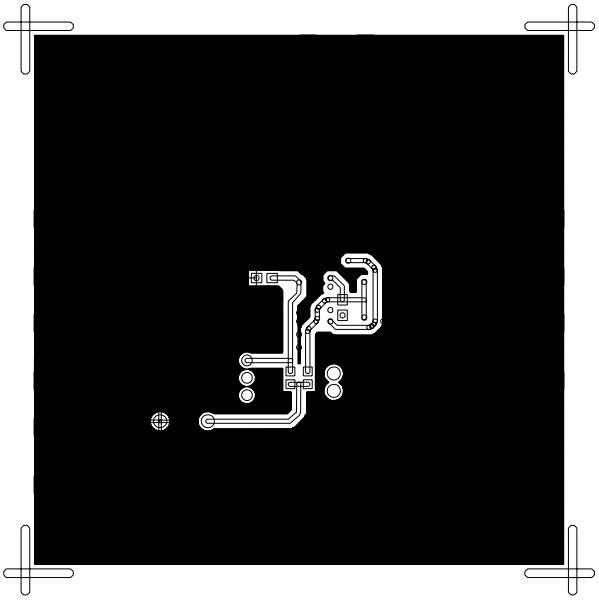

Figure 3. Layout of Power Layer

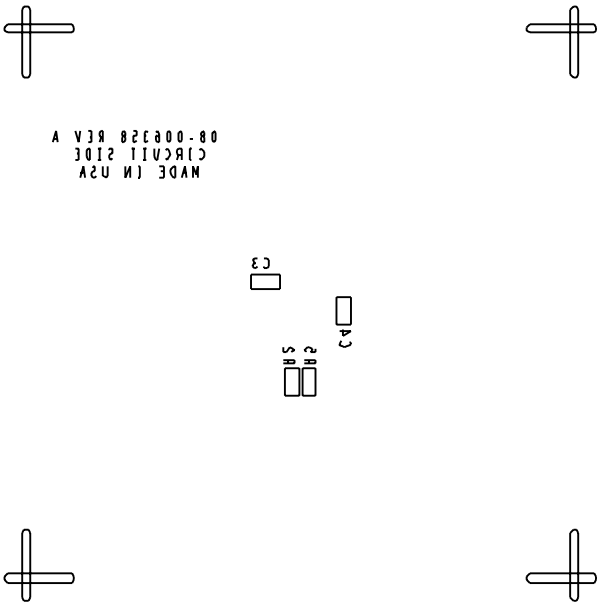

Figure 5. Power Layer Silkscreen

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