ANALOG DEVICES

Evaluation Board Documentation
ADE7752 Energy metering IC

Preliminary Technical Data

EVAL-ADE7752EB

FEATURES
Evaluation Board can be used to implement a fully functional Three-Phase Energy Meter (Watt-Hour Meter).
Easy connection of various external transducers via screw terminals.
Easy modification of signal conditioning components using PCB sockets.
LED indicators on logic outputs CF, NEGP and IRQ.
Optically isolated data output connection to PC parallel port.
Optically isolated frequency output (CF) to BNC.
External Reference option available for on-chip reference evaluation.

GENERAL DESCRIPTION
The ADE7752 is high accuracy electrical active power measurement IC for three-phase applications with a pulse output. This output is intended to be used for calibration purposes. The ADE7752 incorporates ADCs, reference circuitry, and all the signal processing required to perform active power and energy measurement.

The ADE7752 supplies average real power information on the low frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter. The evaluation board provides screw connectors for easy connection to an external counter. The NEGP logic output goes high when negative active power is detected on any of the three phases input. This causes an LED on the evaluation board to switch on.

The ADE7752 evaluation board and this documentation, together with the ADE7752 data sheet provides a complete evaluation platform for the ADE7752.

The evaluation board has been designed so that the ADE7752 can be evaluated in the end application, i.e., Watt-Hour Meter. Using the appropriate transducers on the current channel (e.g., CT) the evaluation board can be connected to a test bench or high voltage (240V rms) test circuit. On-board resistor dividers networks provide the attenuation for the line voltages. This application note also describes how the current transducers should be connected for the best performance. The evaluation board requires two external 5V power supplies (one is required for isolation purposes) and the appropriate current transducers.

FUNCTIONAL BLOCK DIAGRAM
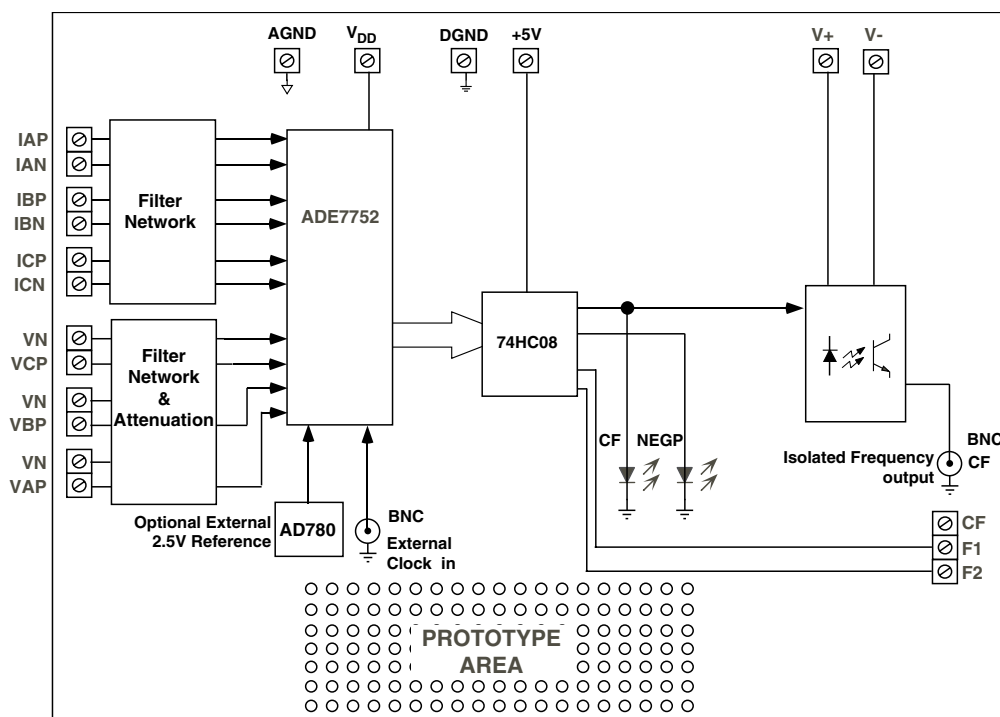
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ANALOG INPUTS (P4, P5, P6, P7, P8 AND P11)

Voltage and current signals are connected at the screw terminals P4-P6 and P7-P8 and P11 respectively. All analog input signals are filtered using the on-board anti-alias filters before being presented to the analog inputs of the ADE7752. The default component values which are shipped with the evaluation board are the recommended values to be used with the ADE7752. The user can easily change these components, however this is not recommended unless the user is familiar with sigma-delta converters and also the criteria used for selecting the component values for the analog input filters - *See ADE7752 datasheet*.

Current sense inputs (P4, P5 and P6)

P4, P5 and P6 are two-way connection blocks which allow ADE7752's current inputs of phase A, B and C respectively to be connected to current transducers. Figure 1 shows the connector P4 and the filtering network which is provided on the evaluation board.

The resistors SH1A, SH2A, SH1B, SH2B, SH1C and SH2C are by default not populated. They are intended to be used as burden resistors when CTs are used as the current transducers—*see using a CT as a the current transducer*.

The RC networks R9/C5, R7/C8, R15/C9, R13/C12, R21/C13, R19/C16 are used to provide phase compensation when a Current Transformer is being used as the current transducer with the ADE7752—see using a Current Transformer as the current transducer. These RC networks are easily disabled by placing JP4, JP1, JP10, JP7, JP16 & JP13 and removing C5, C8, C9, C12, C13 and C16 (socketed).

The RC networks R10/C6, R8/C7, R16/C10, R14/C11, R22/C14 and R20/C15 are the anti-alias filters which are required by the on-chip ADCs. The default corner frequency for these LPFs (Low Pass Filters) is selected as 4.8kHz (1kΩ & 33nF). These filters can easily be adjusted by replacing the components on the evaluation board. However before adjusting the component values the user should first review the ADE7752 datasheet.
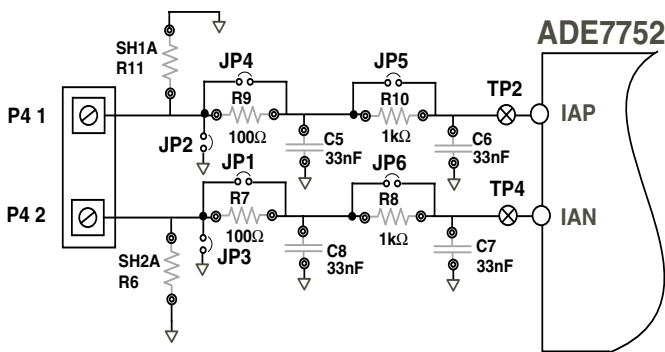

Figure 1 — Current Channel on the ADE7752 evaluation board

Using a CT as the current transducer

Figure 2 shows how a CT can be used as a current transducer in one phase of a 3-phase 4-wire distribution system (Phase A). In a three phase distribution system Phase A, Phase B and Phase C are nominally 120° phase difference to each other. Each phase usually requires a connection of this type for current sensing.
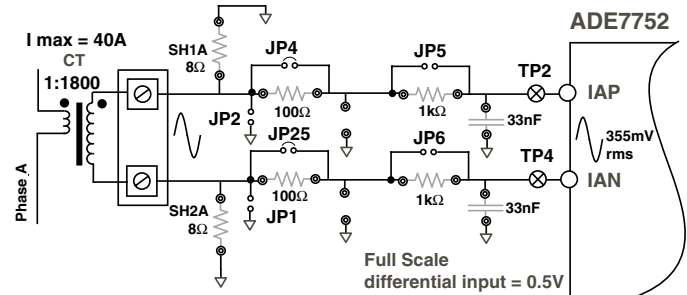

Figure 2 — CT connection to Current Channel

The CT secondary current is converted to a voltage by using a burden resistance across the secondary winding outputs. Care should be taken when using a CT as the current transducer. If the secondary is left open, i.e., no burden is connected, a large voltage could be present at the secondary outputs. This can cause an electrical shock hazard and potentially damage electronic components.

Warning!
Using a CT without a burden resistor can lead to electrical shock.

The anti-alias filters should be enabled by opening jumpers JP5, JP6, JP11, JP12, JP17 and JP18—see Figure 2.

Most CTs will have an associated phase shift of between 0.1° and 1° at 50Hz/60Hz. This phase shift or phase error can lead to significant energy measurement errors, especially at low power factors. However this phase error can be corrected by adding some capacitors in parallel to C6 and C7.

The maximum analog input range on the Current channel of the ADE7752 is 0.5V peak.

Voltage sense inputs

The voltage inputs connections on the ADE7752 evaluation board can be directly connected to the line voltage sources. The line voltages are attenuated using a simple resistor divider network before it is presented to the ADE7752. The attenuation network on the voltage channels is designed such that the corner frequency (3dB frequency) of the network matches that of the RC (anti-aliasing) filters on the current channels inputs. This is important, because if they do not match there will be large errors at low power factors. Figure 3 below shows how the attenuation network may be used with trim pot.

The trim pot allows the signals on the voltage channels to be scaled so as to calibrate the frequency on CF to some given constant, e.g., 1600 imp/kWhr. This is especially appropriate when calibrating the ADE7752. Some examples are given later. Because of the relatively large signal on this channel and the small dynamic range requirement, the voltage channels can be configured in a single-ended configuration. Figure 3 shows a typical connection for the line voltage when using the trim pot for calibration. In this case, R47, R44 and R43 should be changed to 500Ω to assure the same cut-off frequency of the anti-aliasing filter as for the current channel.
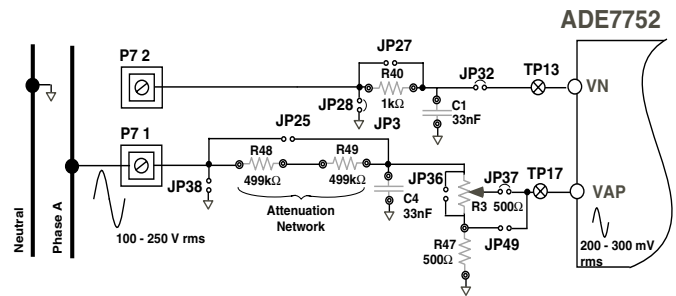

Figure 3 — Phase A Voltage Channel attenuation network using Trim pot

The maximum signal level permissible at VAP, VBP and VCP is 0.5V peak for the ADE7752. Although the ADE7752 analog inputs can withstand ±6V without risk of permanent damage, the signal range should not exceed ±0.5V with respect to AGND for the ADE7752 for specified operation.

Note that the analog input VN is connected to AGND via the anti-alias filter R40/C1 using JP28. Jumper JP27 should be left open.

ADE7752 EVALUATION BOARD SET UP

Configuration

The ADE7752 evaluation board can be configured for the different mode of operation of the ADE7752. The connection of the 2 positions jumpers (Px) are described as Right or Left. This is defined when one looks at the board with the label EVAL-ADE7752 at the front bottom left.

TABLE I : Configuration of ADE7752

JUMPER	Left	Right	DESCRIPTION
P3	$\overline{ABS}$ = High	$\overline{ABS}$ = Low	Left position: Pin 17 is connected to a pull up resistor Right position: Pin17 is connected to a pull down resistor
P12	S1=High	S1=Low	Left position: Pin 22 is connected to a pull up resistor Right position: Pin22 is connected to a pull down resistor
P14	S0=Low	S0=High	Left position: Pin21 is connected to a pull down resistor Right position: Pin 21 is connected to a pull up resistor
P16	SCF=Low	SCF=High	Left position: Pin18 is connected to a pull down resistor Right position: Pin 18 is connected to a pull up resistor

Other jumpers are present on the ADE7752 evaluation board. Their actions are described in the following table.

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TABLE II : JUMPER SETTINGS

JUMPER	OPTION	DESCRIPTION
JP1-JP7-JP13	Closed	This will short out R7, R13 and R19 respectively. The effect is to disable the phase compensation filter on the analog inputs IAN, IBN and ICN respectively. Default Closed.
JP2-JP8-JP14	Closed	This will connect the analog input IAP, IBP and ICP respectively to ground. Default Open.
JP3-JP9-JP15	Closed	This will connect the analog input IAN, IBN and ICN respectively to ground. Default Open.
JP4-JP10-JP16	Closed	This will short out R9, R15 and R21 respectively. The effect is to disable the phase compensation filter (for shunts) on the analog inputs IAN, IBN and ICN respectively. Default Closed.
JP5-JP11-JP17	Closed	This will short out R10, R16 and R22 respectively. The effect is to disable the anti-alias filter on the analog inputs IAP, IBP and ICP respectively. Default Open.
	Open	Enable the anti-alias filter on IAP, IBP and ICP respectively.
JP6-JP12-JP18	Closed	This will short out R8, R14 and R20 respectively. The effect is to disable the anti-alias filter on the analog inputs IAN, IBN and ICN respectively. Default Open.
	Open	Enable the anti-alias filter on IAN, IBN and ICN respectively.
JP19	Closed	This will connect the Analog and Digital ground planes of the PCB. Default Closed.
JP20	Closed	This will connect an external reference 2.5V (AD780) to the ADE7752
	Open	This will enable the ADE7752 on-chip reference.
JP21	Closed	This connects the VDD and +5V (buffers) supply for the evaluation board together. Default Closed.
JP23-JP24-JP25	Closed	This will short the attenuation network on the voltage channels. Default Open
JP26	Closed	This will connect the optical isolator ground to the evaluation board ground (DGND). If full isolation between the evaluation board and PC is required, this jumper should be left open
JP27	Closed	This will short out R40. The effect is to disable the anti-alias filter on the analog input VN. Default Open
JP28	Closed	This will connect the analog input VN to ground. Default Closed.
JP29-JP35-JP38	Closed	This will connect the analog inputs VAP, VBP and VCP to ground respectively. Default Open
JP30-JP33-JP36	Closed	This will short out trim pots R1, R2 and R3 respectively. Default closed.
JP31-JP34-JP37 JP47-JP48-JP49	Closed	This will short out disconnect Analog input VAP, VBP and VCP respectively from the ADE7752. Default Closed
JP32	Closed	This will short out disconnect Analog input VN from the ADE7752. Default Closed
JP43	A	This connects the buffered logic output CF to BNC J3 connector via an optical isolator.
	B	This connects the buffered logic output CF to the LED CR2.

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SETTING UP THE EVALUATION BOARD AS AN ENERGY METER

Figure 5 shows a typical set up for the ADE7752 evaluation board. In this example a kWh meter for a 4 wire, three phase distribution system is shown. Current Transformers are used to sense phases' current and are connected as shown in Figure 5. For a more detailed description on how to use a CT as a current transducer see the *Current Sense Inputs* section of this documentation. The line voltage is connected directly to the evaluation board as shown. Note JP23, JP24 and JP25 should be left open to ensure that the attenuation networks are not bypassed. Also note the use of two power supplies.

The second power supply is used to power the optical isolation. With JP26 left open, this will ensure that there is no electrical connection between the high voltage test circuit and the frequencies outputs. The power supplies should have floating voltage outputs.

Setting up the evaluation board for the ADE7752

The configuration of the jumpers on the ADE7752 evaluation board for operation with the ADE7752 are detailed in Figure 5. The selection of the outputs frequencies of CF, F1 and F2 is done by configuring SCF, S1 and S0 with jumpers P16, P12 and P14 respectively. The mode of summation of the three active energies (arithmetic sum or sum of the absolute values) can also be selected on the evaluation board with Jumper P3. Table III details the action of each jumper.

TABLE III : ADE7752 frequency setting

Signal	State	Jumper position
SCF	1	P16 - RIGHT
	0	P16 - LEFT
S1	1	P12 - LEFT
	0	P12 - RIGHT
S0	1	P14 - RIGHT
	0	P14 - LEFT
$\overline{ABS}$	1	P3 - LEFT arithmetic sum
	0	P3 - RIGHT Sum of absolute values

If CTs have a turn ration of 1:1800, the burden resistance of the CTs can be placed on the evaluation board at SH1A, SH2A, SH1B, SH2B, SH1C and SH2C.

The meter is intended to be used with a line - neutral voltage of 220 V and a maximum current per phase of 40 A. The frequency outputs F1 and F2 can be used to drive a mechanical counter. These outputs will be calibrated to provide 100imp/kWhr. The logic output CF can be used for calibration purposes and is shown connected to a frequency counter via the opto-isolator in Figure 5.

At maximum current (40 A) the power seen by the meter will be 26.4 kW. This will produce a frequency of 0.733 Hz on the logic outputs F1 and F2 when these outputs are calibrated to 100 imp/kWhr (100 imp/hr = 0.0277 Hz, 0.02777 x 26.4 = 0.733 Hz). From Table III in the ADE7752 datasheet, the closest frequency to 0.733 Hz in the half scale ac inputs column is for F1-5 = 4.77 Hz. Therefore this frequency is selected by setting S0 = 1 and S1 = 0. The choice of CF frequencies in this mode (see Table IV of the ADE7752 datasheet are 16 times F1 or 160 times F1. For this example 16 times F1 is selected by setting SCF = 1.

Since the voltage on the current inputs (IAP/IAN, IBP/IBN and ICP/ICN) are fixed, the only possible way of calibrating (adjusting) the output frequency on F1 and F2 is by varying the voltage on the voltage channels. This is carried out by varying the attenuation of the line voltage using the trim pots.

First we can calculate the voltage required on the voltage channels in order to calibrate the frequency on F1 and F2 to 100 imp/kWhr. The ADE7752 datasheet gives the equation which relates the voltage on the current channels and voltage channels to the output frequency on F1 and F2.

$$Freq = \frac{6.82 \times (V_{AN} \times I_A + V_{BN} \times I_B + V_{CN} \times I_C) \times F_{1-5}}{V_{REF}^2} \quad (1)$$

With a burden resistor of 7.6 Ω, the current channels' levels for 5 A is 5 A / 1800 X 2 X 7.6 = 0.042 V rms. The output frequency at 5A on F1 and F2 should be 0.02777 Hz (100 imp/kWhr) x 3.3 (3 x 220 V x 5 A) = 0.0917Hz.

From Equation 1 the voltage on voltage channels should be set to 139.8 mV rms. The attenuation network as shown in Figure 3 is used to attenuate 220 V to 139.8 mV.

R41 = R42 = R45 = R46 = R48 = R49 =786 kΩ,

R43= R44 = R47 = R10 = R8 = R14 = R16 = R20 = R22 = 500Ω

and trim pots = 500 Ω.

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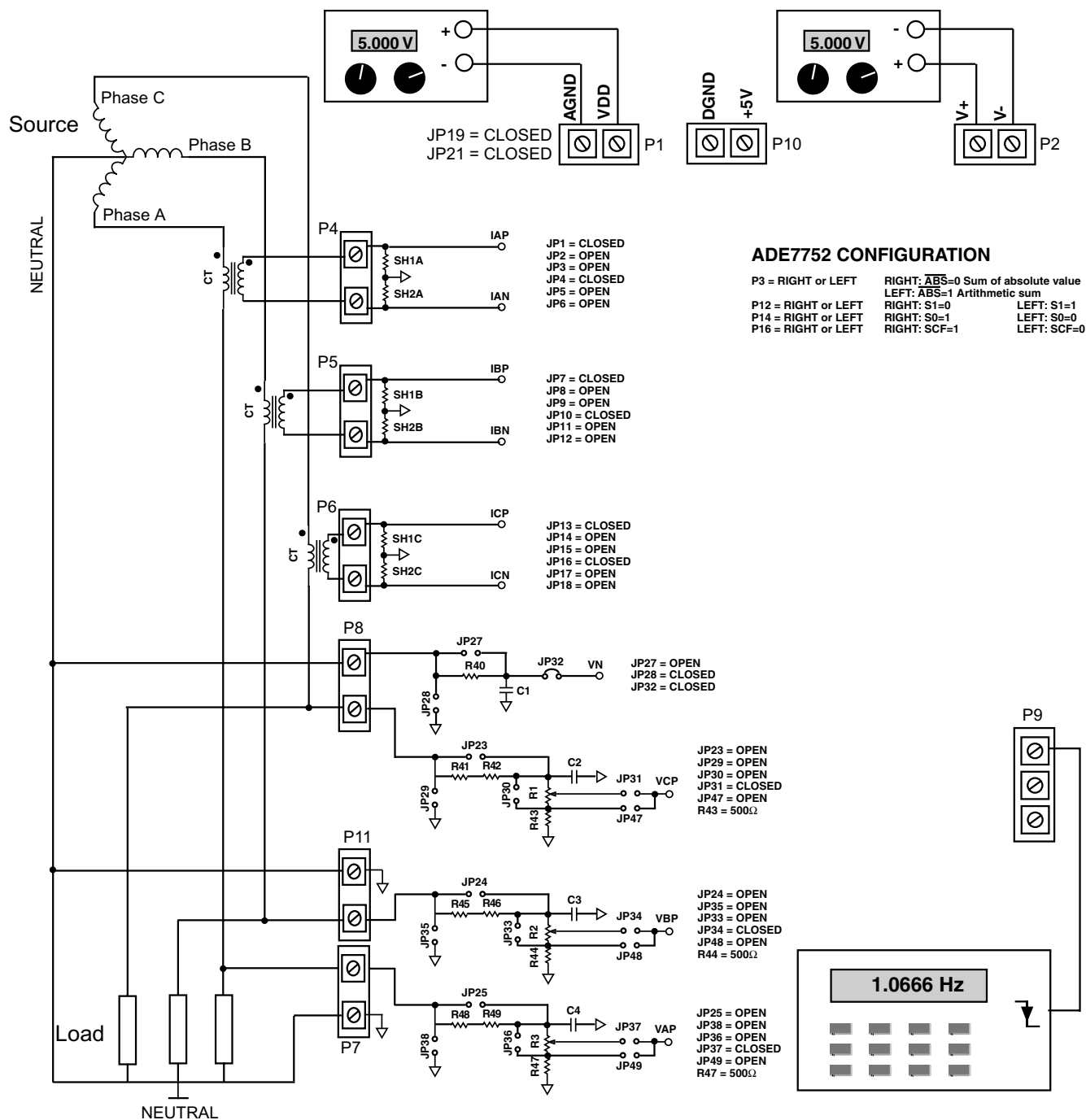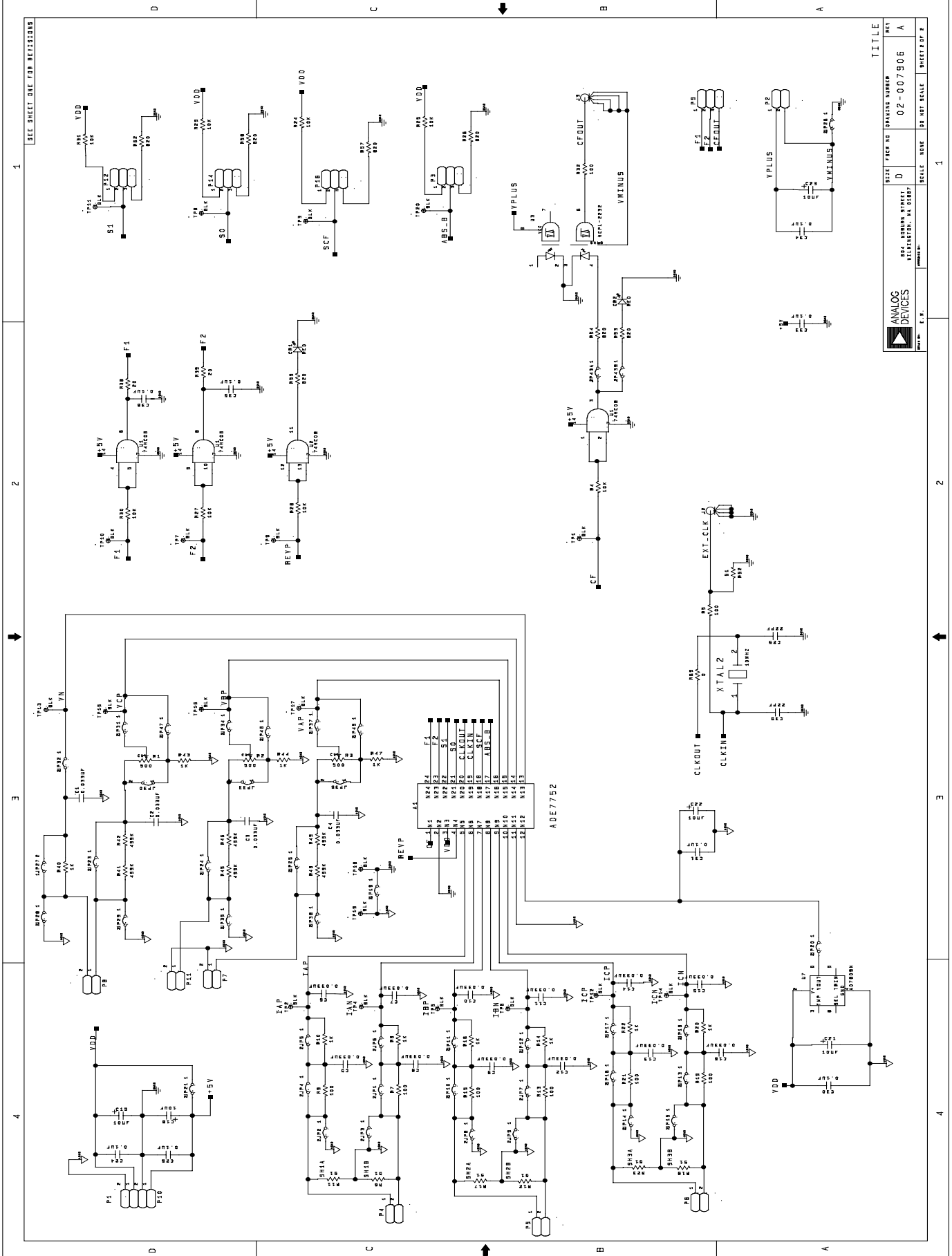*Figure 5 - Typical set up for the ADE7752 evaluation board*

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Evaluation board BOM

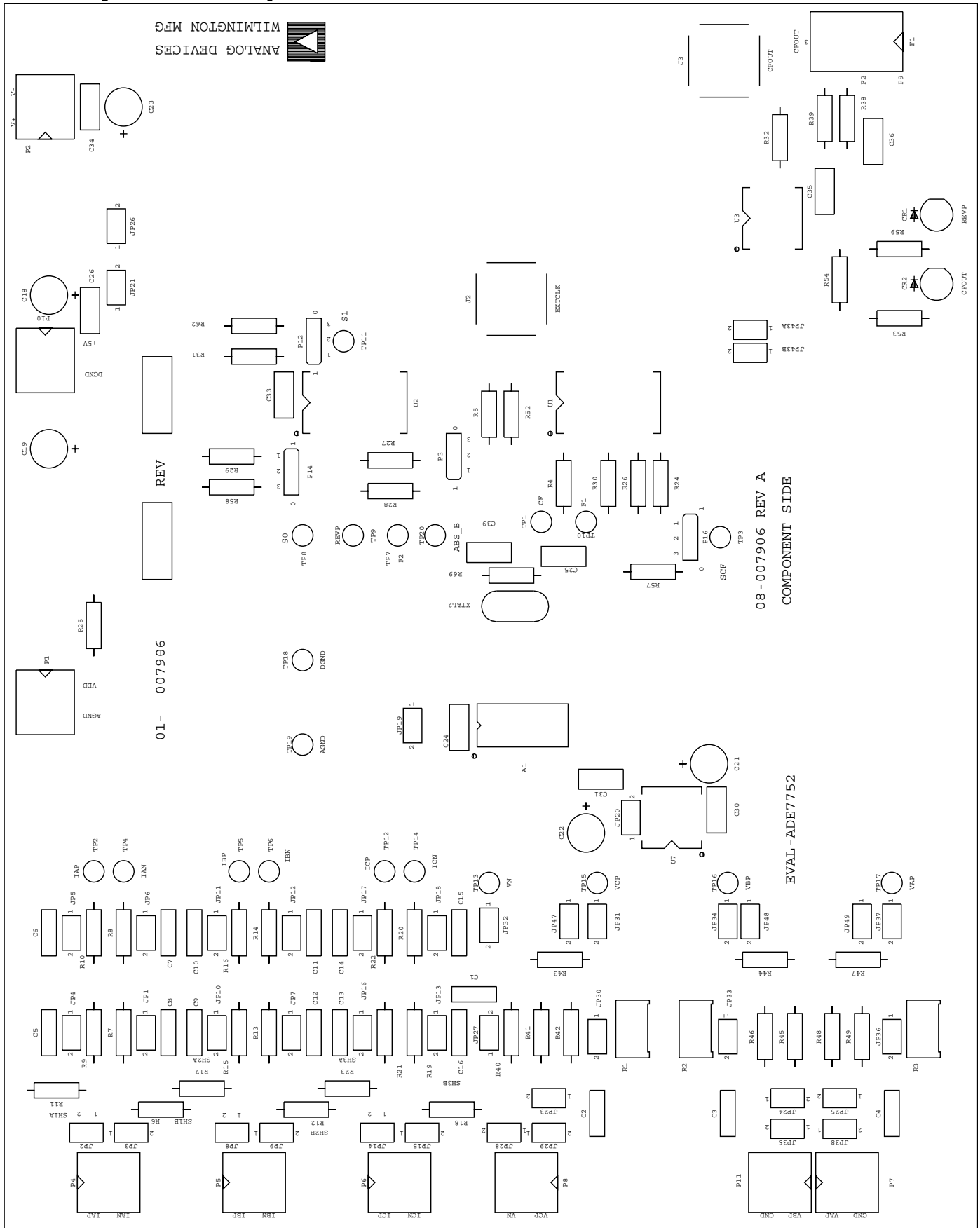| Designator	Value	Description
R1-R3	500Ω, 10%, 1/2W	Trim pot Resistor, 25 turns. BOURNS Part No. 3299W-501
R4, R24-25, R27-R31	10kΩ, 5%, ¼W	Resistor, no special requirements
R5, R7, R9, R13, R15, R19, R21, R32		100Ω, 5%, ¼W Resistor, no special requirements
R6, R11-12, R17-18, R23, R52	51Ω, 5%, ¼W	Not placed unless external clock is being used
R8, R10, R14, R16, R20, R22, R40, R43-44, R47	1kΩ, 0.1%, ¼W	±15 ppm/°C Resistor, good tolerance, used as part of the analog filter network. These resistors are not soldered, but are plugged into PCB pin sockets for easy modification by the customer. Low drift WELWYN RC55 Series, FARNELL part no. 339-179
R25	10Ω, 5%, ¼W	Resistor, no special requirements
R38-39	20Ω, 5%, ¼W	Resistor, no special requirements
R41-42, R45-46, R48-49	499kΩ, 0.1%, ¼W	Pin socketed, ±15 ppm/°C Low drift, WELWYN RC55 Series. Farnell part no. 338-484
R26,R53-54, R57-59,R62	820Ω, 5%, ¼W	Resistor, no special requirements
R69	0Ω, 10%, ¼W	
C1-16	33nF, 10%, 50 volt	X7R Capacitor, part of the filter network. These resistors are not soldered, but are plugged into PCB mount sockets for easy modification by the customer. SR15 series AVX-KYOCERNA, FARNELL part no. 108-948C5,
C17	220pF	PANASONIC ECQ-P1H221JZ
C18-19, C21-23	10uF, Tantalium	Power supply decoupling capacitors, 10%, 16V
C25, C39	22pF, ceramic	Gate oscillator load capacitors, FARNELL part no. 108-927
C24, C26,C30-31,C33-36	100nF, 25V	Power supply decoupling capacitors, 10%, X7R type, AVX-KYOCERNA, FARNELL part no. 108-950
CR1-2	LED	Low current, Red, FARNELL part no. 637-087
J2-3	BNC connector	Straight square, 1.3mm holes, 10.2mm x 10.2mm FARNELL part no. 149-453
JP1-21, JP23-38, JP47-49	2 Pin header	2-Pin, 0.025 Sq., 0.01 Ctrs, Compnt Corp., CSS-02-02
JP43A-B	2 Pin header x 2	2-Pin, 0.025 Sq., 0.01 Ctrs, Compnt Corp., CSS-02-02U1
P3, P12, P14, P16	3 Pin header x 2	2-Pin, 0.025 Sq., 0.01 Ctrs, Compnt Corp., CSS-02-02U1
A1	ADE7752	Supplied by Analog Devices Inc.
U1-2	74HC08	Quad CMOS AND gates
U3	HCPL2232	HP Optical Isolator
U7	AD780	2.5V reference, Supplied by Analog Devices Inc.
XTAL	10 MHz	Quartz Crystal, HC-49(US)
P1-2, P4-8, P10-11	screw terminal	15A, 2.5mm cable screw terminal sockets. WEILAND part no. 25.161.0253
P9	screw terminal	15A, 2.5mm cable screw terminal sockets. WEILAND 25.161.0353

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Evaluation board schematic (rev.A)

PCB layout - Component Placement

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PCB layout - Component Side

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PCB layout - Solder Side