

16Mx16
SDRAM 54CSP
(VDD/VDDQ 3.0V/3.0V or 3.3V/3.3V)

Revision 1.4

December 2002

4M x 16Bit x 4 Banks Synchronous DRAM in 54CSP

FEATURES

- 3.0V & 3.3V power supply.
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
 - CAS latency (1 & 2 & 3).
 - Burst length (1, 2, 4, 8 & Full page).
 - Burst type (Sequential & Interleave).
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- DQM for masking
- Auto refresh.
- 64ms refresh period (8K cycle).
- Commercial Temperature Operation (-25°C ~ 70°C).
Extended Temperature Operation (-25°C ~ 85°C).
Industrial Temperature Operation (-40°C ~ 85°C).
- 54balls CSP (-RXXX - Pb, -BXXX - Pb Free)

GENERAL DESCRIPTION

The K4S561633C is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 4,196,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S561633C-R(B)L/N/P75	133MHz(CL=3) 105MHz(CL=2)	LVCMOS	54 CSP Pb (Pb Free)
K4S561633C-R(B)L/N/P1H	105MHz(CL=2)		
K4S561633C-R(B)L/N/P1L	105MHz(CL=3)*1		

-R(B)L ; Low Power, Operating Temp : -25°C ~ 70°C.

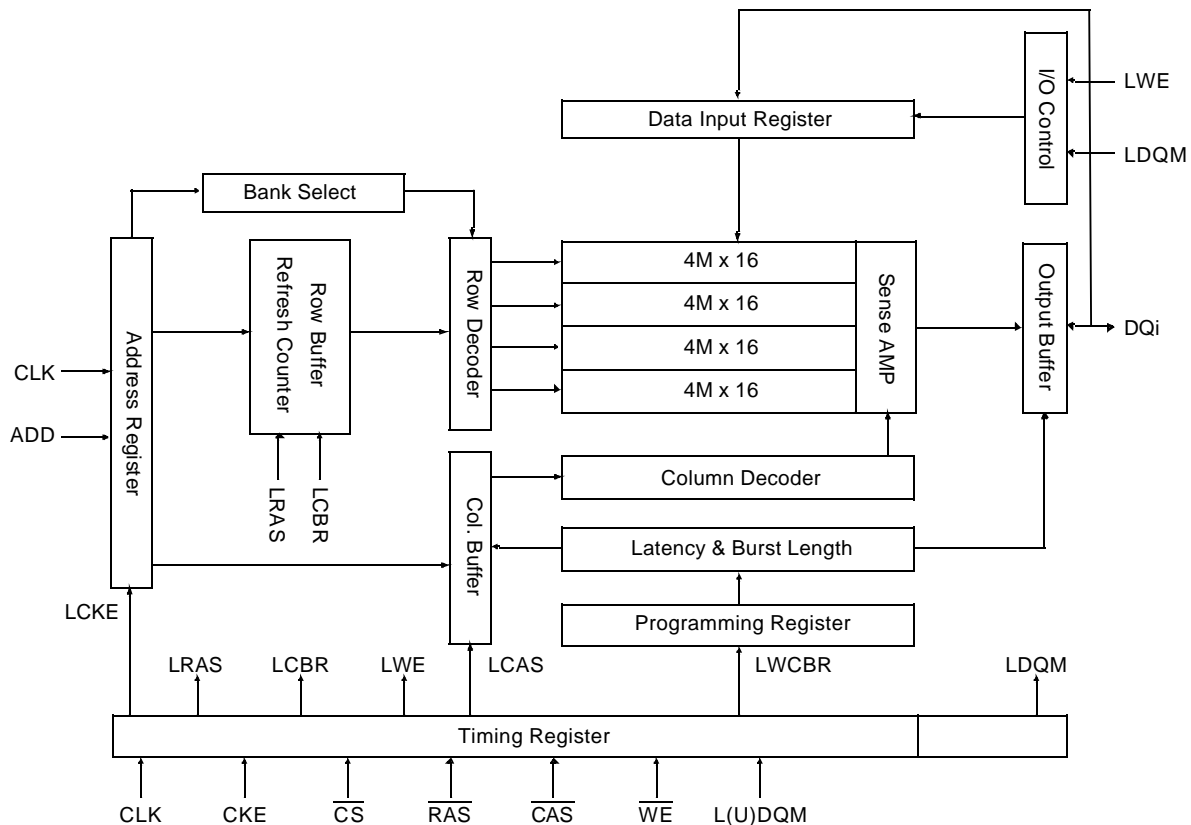
-R(B)N ; Low Power, Operating Temp : -25°C ~ 85°C.

-R(B)P : Low Power, Operating Temp : -40°C ~ 85°C.

Note :

1. In case of 40MHz Frequency, CL1 can be supported.

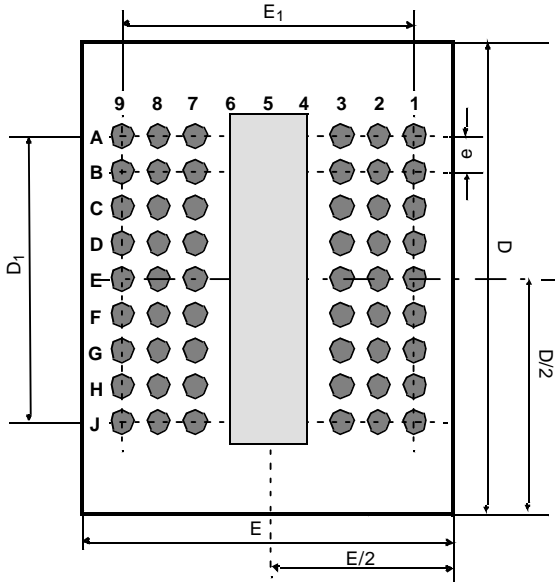
FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

Package Dimension and Pin Configuration

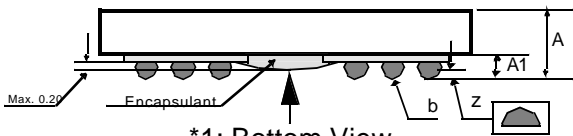
< Bottom View *1 >



< Top View *2 >

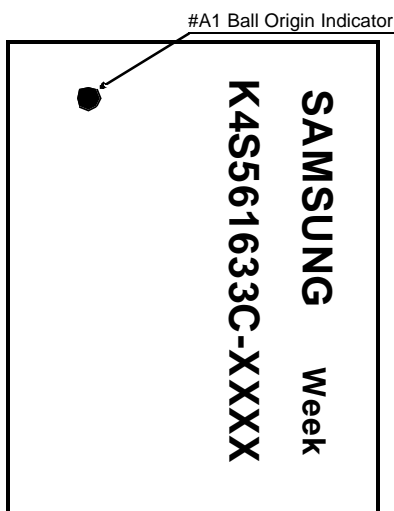
54Ball(6x9) CSP						
	1	2	3	7	8	9
A	V _{SS}	DQ15	V _{SSQ}	V _{DDQ}	DQ0	V _{DD}
B	DQ14	DQ13	V _{DDQ}	V _{SSQ}	DQ2	DQ1
C	DQ12	DQ11	V _{SSQ}	V _{DDQ}	DQ4	DQ3
D	DQ10	DQ9	V _{DDQ}	V _{SSQ}	DQ6	DQ5
E	DQ8	NC	V _{SS}	V _{DD}	LDQM	DQ7
F	UDQM	CLK	CKE	$\overline{\text{CAS}}$	$\overline{\text{RAS}}$	$\overline{\text{WE}}$
G	A12	A11	A9	BA0	BA1	$\overline{\text{CS}}$
H	A8	A7	A6	A0	A1	A10
J	V _{SS}	A5	A4	A3	A2	V _{DD}

*2: Top View



*1: Bottom View

< Top View *2 >



Pin Name	Pin Function
CLK	System Clock
$\overline{\text{CS}}$	Chip Select
CKE	Clock Enable
A ₀ ~ A ₁₂	Address
BA ₀ ~ BA ₁	Bank Select Address
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
L(U)DQM	Data Input/Output Mask
DQ ₀ ~ 15	Data Input/Output
V _{DD} /V _{SS}	Power Supply/Ground
V _{DDQ} /V _{SSQ}	Data Output Power/Ground

[Unit:mm]

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
A ₁	0.30	0.35	0.40
E	-	8.10	-
E ₁	-	6.40	-
D	-	15.10	-
D ₁	-	6.40	-
e	-	0.80	-
b	0.40	0.45	0.50
z	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Notes :

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = Commercial, Extended, Industrial Temperature)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	2.7	3.0	3.6	V	
	V _{DDQ}	2.7	3.0	3.6	V	
Input logic high voltage	V _{IH}	2.2	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.5	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes:

1. V_{IH} (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.

4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.0V & 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	2.0	4.0	pF	
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, DQM	C _{IN}	2.0	4.0	pF	
Address	C _{ADD}	2.0	4.0	pF	
DQ ₀ ~ DQ ₁₅	C _{OUT}	3.5	6.0	pF	

DC CHARACTERISTICS

Recommended operating conditions(Voltage referenced to $V_{SS} = 0V$, T_A =Commercial, Extended, Industrial Temperature)

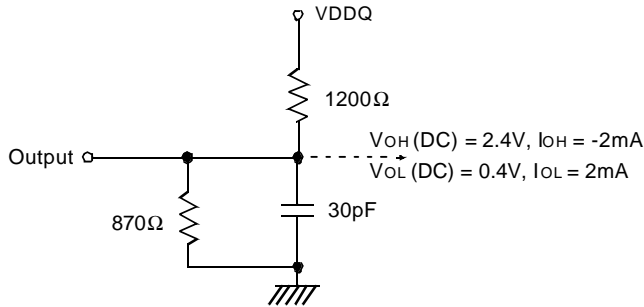
Parameter	Symbol	Test Condition	Version			Unit	Note
			-75	-1H	-1L		
Operating Current (One Bank Active)	I _{CC1}	Burst length = 1 $t_{RC} \geq t_{RC(min)}$ $I_O = 0$ mA	90	85	85	mA	1
Precharge Standby Current in power-down mode	I _{CC2P}	CKE $\leq V_{IL(max)}$, $t_{CC} = 10ns$	0.5			mA	
	I _{CC2PS}	CKE & CLK $\leq V_{IL(max)}$, $t_{CC} = \infty$	0.5				
Precharge Standby Current in non power-down mode	I _{CC2N}	CKE $\geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10ns$ Input signals are changed one time during 20ns	15			mA	
	I _{CC2NS}	CKE $\geq V_{IH(min)}$, CLK $\leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	10				
Active Standby Current in power-down mode	I _{CC3P}	CKE $\leq V_{IL(max)}$, $t_{CC} = 10ns$	6			mA	
	I _{CC3PS}	CKE & CLK $\leq V_{IL(max)}$, $t_{CC} = \infty$	6				
Active Standby Current in non power-down mode (One Bank Active)	I _{CC3N}	CKE $\geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10ns$ Input signals are changed one time during 20ns	25			mA	
	I _{CC3NS}	CKE $\geq V_{IH(min)}$, CLK $\leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	25				
Operating Current (Burst Mode)	I _{CC4}	$I_O = 0$ mA Page burst 4Banks Activated $t_{CCD} = 2CLKs$	130	130	105	mA	1
Refresh Current	I _{CC5}	$t_{RC} \geq t_{RC(min)}$	185	185	165	mA	2
Self Refresh Current	I _{CC6}	CKE $\leq 0.2V$	-R(B)L	800		uA	3
			-R(B)N				4
			-R(B)P				

Notes :

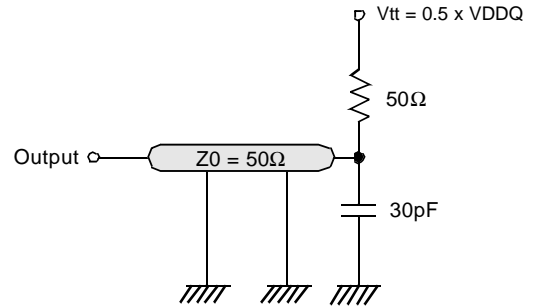
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S561633C-R(B)L**
4. K4S561633C-R(B)N**
5. K4S561633C-R(B)P**
6. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS($V_{DD} = 2.7V \sim 3.6V$, $T_A = \text{Commercial, Extended, Industrial Temperature}$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4 / 0.4	V
Input timing measurement reference level	$0.5 \times V_{DDQ}$	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	$0.5 \times V_{DDQ}$	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		- 75	-1H	-1L		
Row active to row active delay	$t_{RRD}(\text{min})$	15	19	19	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	$t_{RCD}(\text{min})$	19	19	24	ns	1
Row precharge time	$t_{RP}(\text{min})$	19	19	24	ns	1
Row active time	$t_{RAS}(\text{min})$	45	50	60	ns	1
	$t_{RAS}(\text{max})$	100			us	
Row cycle time	$t_{RC}(\text{min})$	65	70	84	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2			CLK	2,3
Last data in to Active delay	$t_{DAL}(\text{min})$	$t_{RDL} + t_{RP}$			-	3
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1			CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1			CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1			CLK	4
Number of valid output data	CAS latency=3	2			ea	5
	CAS latency=2	1				
	CAS latency=1	-	0			

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum $t_{RDL}=2\text{CLK}$ and $t_{DAL}=(t_{RDL} + t_{RP})$ is required to complete both of last data write command(t_{RDL}) and precharge command(t_{RP}). $t_{RDL}=1\text{CLK}$ can be supported only in the case under 100MHz with manual precharge mode.
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	9.5	1000	9.5	1000	ns	1
	CAS latency=2		9.5		9.5		12			
	CAS latency=1		-		-		25			
CLK to valid output delay	CAS latency=3	tsac		5.4		7		7	ns	1,2
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		
Output data hold time	CAS latency=3	toH	2.5		2.5		2.5		ns	2
	CAS latency=2		2.5		2.5		2.5			
	CAS latency=1		-		-		2.5			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	2.0		2.5		2.5		ns	3
Input hold time		tSH	1.0		1.5		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		7		7	ns	
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		

Notes :

- Parameters depend on programmed CAS latency.
- If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
- Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Note :

- Samsung are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in samsung electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.



SIMPLIFIED TRUTH TABLE (V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	DQM	BA _{0,1}	A _{10/AP}	A _{11, A12, A9 ~ A0}	Note
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh	H	H	L	L	L	H	X	X	X		3
			L									3
	Self Refresh	Entry	L	H	H	H	H	X	X	X		3
		Exit		H	X	X	X					3
Bank Active & Row Addr.		H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable	H	X	L	H	L	H	X	V	L	Column Address (A ₀ ~ A ₈)	4
	Auto Precharge Enable									H		4, 5
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	X	V	L	Column Address (A ₀ ~ A ₈)	4
	Auto Precharge Enable									H		4, 5
Burst Stop		H	X	L	H	H	L	X	X			6
Precharge	Bank Selection	H	X	L	L	H	L	X	V	L	X	
	All Banks								X	H		
Clock Suspend or Active Power Down	Entry	H	L	H	X	X	X	X	X	X		
				L	V	V	V					
	Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X	X	X		
				L	H	H	H					
	Exit	L	H	H	X	X	X	X	X	X		
				L	V	V	V					
DQM		H	X	H	X	X	X	X	V	X		7
No Operation Command		H	X	H	X	X	X	X	X	X		
				L	H	H	H					

Notes :

- OP Code : Operand Code
A₀ ~ A₁₂ & BA₀ ~ BA₁ : Program keys. (@MRS)
- MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are the same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
- BA₀ ~ BA₁ : Bank select addresses.
If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.
If BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.
If BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.
If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.
If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ are ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

