V386

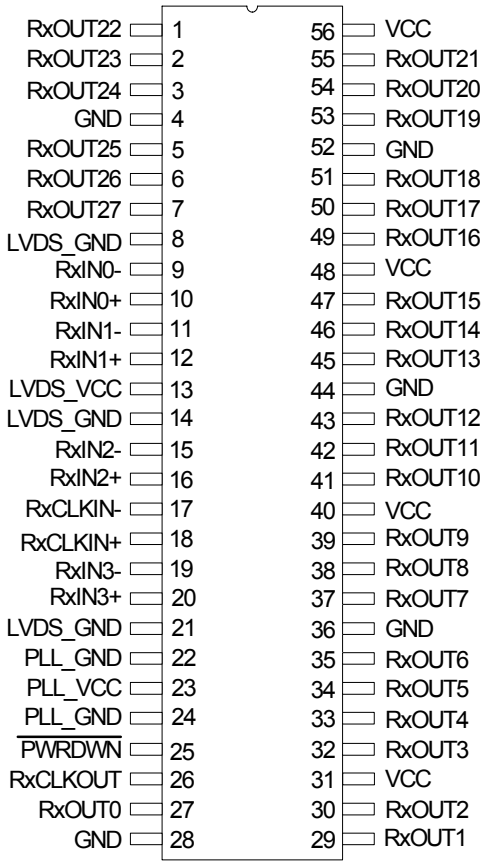
8-BIT LVDS RECEIVER FOR VIDEO

General Description

The V386 is an ideal LVDS receiver that converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data with bandwidth up to 2.38 Gbps throughput or 297.5 Mbytes per second.

This chip is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces through very low-swing LVDS signals.

Pin Assignments

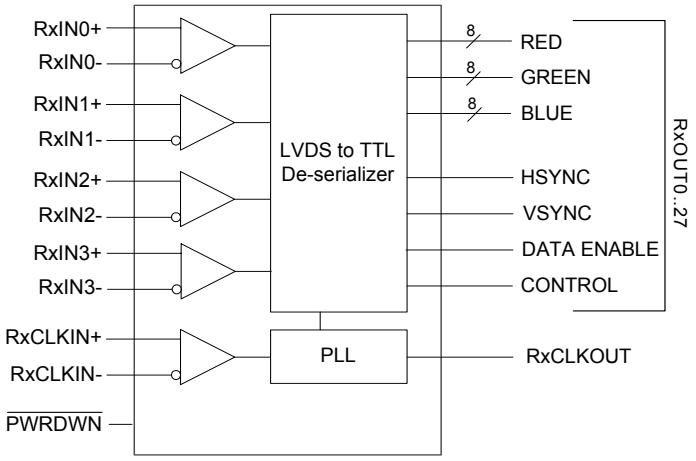


56-pin TSSOP
V386

Features

- Converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data
- Fully spread spectrum compatible
- Wide clock frequency range from 15 MHz to 85 MHz
- Supports VGA, SVGA, XGA, and SXGA
- LVDS voltage swing of 350 mV for low EMI
- On-chip PLL requires no external components
- Low-power CMOS design
- Falling edge clock triggered outputs
- Power-down control function
- Compatible with TIA/EIA-644 LVDS standards
- Packaged in a 56-pin TSSOP (Pb free available)
- Pin and function compatible with the National DS90CF386, THine THC63LVDF84, TI SN65LVDS94

Block Diagram



V386

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Pin Descriptions

Pin	Pin name	Type	Description
1	RxOUT22	OUT	Data outputs on pins (RxOUT0..27)
2	RxOUT23	OUT	Data outputs on pins (RxOUT0..27)
3	RxOUT24	OUT	Data outputs on pins (RxOUT0..27)
4	GND	Ground	Digital ground
5	RxOUT25	OUT	Data outputs on pins (RxOUT0..27)
6	RxOUT26	OUT	Data outputs on pins (RxOUT0..27)
7	RxOUT27	OUT	Data outputs on pins (RxOUT0..27)
8	LVDS_GND	Ground	Analog ground
9	RxIN0-	LVDS IN	LVDS input (-)
10	RxIN0+	LVDS IN	LVDS input (+)
11	RxIN1-	LVDS IN	LVDS input (-)
12	RxIN1+	LVDS IN	LVDS input (+)
13	LVDS_VCC	Power	Analog power
14	LVDS_GND	Ground	Analog ground
15	RxIN2-	LVDS IN	LVDS input (-)
16	RxIN2+	LVDS IN	LVDS input (+)
17	RxCLKIN-	LVDS IN	LVDS input (-)
18	RxCLKIN+	LVDS IN	LVDS input (+)
19	RxIN3-	LVDS IN	LVDS input (-)
20	RxIN3+	LVDS IN	LVDS input (+)
21	LVDS_GND	Ground	Analog ground
22	PLL_GND	Ground	PLL ground
23	PLL_VCC	Power	PLL power
24	PLL_GND	Ground	PLL ground
25	$\overline{\text{PWRDWN}}$	IN	Power-down control input. H: Normal L: Power down, all ouputs are pulled low.
26	RxCLKOUT	OUT	Clock output
27	RxOUT0	OUT	Data outputs on pins (RxOUT0..27)
28	GND	Ground	Digital ground
29	RxOUT1	OUT	Data outputs on pins (RxOUT0..27)
30	RxOUT2	OUT	Data outputs on pins (RxOUT0..27)
31	VCC	Power	Digital power
32	RxOUT3	OUT	Data outputs on pins (RxOUT0..27)
33	RxOUT4	OUT	Data outputs on pins (RxOUT0..27)

Pin	Pin name	Type	Description
34	RxOUT5	OUT	Data outputs on pins (RxOUT0..27)
35	RxOUT6	OUT	Data outputs on pins (RxOUT0..27)
36	GND	Ground	Digital ground
37	RxOUT7	OUT	Data outputs on pins (RxOUT0..27)
38	RxOUT8	OUT	Data outputs on pins (RxOUT0..27)
39	RxOUT9	OUT	Data outputs on pins (RxOUT0..27)
40	VCC	Power	Digital power
41	RxOUT10	OUT	Data outputs on pins (RxOUT0..27)
42	RxOUT11	OUT	Data outputs on pins (RxOUT0..27)
43	RxOUT12	OUT	Data outputs on pins (RxOUT0..27)
44	GND	Ground	Digital ground
45	RxOUT13	OUT	Data outputs on pins (RxOUT0..27)
46	RxOUT14	OUT	Data outputs on pins (RxOUT0..27)
47	RxOUT15	OUT	Data outputs on pins (RxOUT0..27)
48	VCC	Power	Digital power
49	RxOUT16	OUT	Data outputs on pins (RxOUT0..27)
50	RxOUT17	OUT	Data outputs on pins (RxOUT0..27)
51	RxOUT18	OUT	Data outputs on pins (RxOUT0..27)
52	GND	Ground	Digital ground
53	RxOUT19	OUT	Data outputs on pins (RxOUT0..27)
54	RxOUT20	OUT	Data outputs on pins (RxOUT0..27)
55	RxOUT21	OUT	Data outputs on pins (RxOUT0..27)
56	VCC	Power	Digital power

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V386. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VCC	-0.3 V to +4 V
CMOS/TTL Output Voltage	-0.3 V to (VCC+0.3 V)
LVDS Receiver Input Voltage	-0.3 V to (VCC+0.3 V)
Ambient Operating Temperature	-10 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature (10 seconds max.)	260°C
Maximum Package Power	1.61 W (V386)
Package Derating	12.4 mW/°C above +25°C
	15 mW/°C above +25°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Ta)	-10	25	70	°C
3.3 V Supply Voltage (VCC)	3	3.3	3.6	V
Receiver Input Range (V_{IN})	0		2.4	V
Supply Noise Voltage (V_N)			100	mVpp

Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature -10 to 70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS/TTL DC Specifications						
Input High Voltage	V_{IH}		2.0		VCC	V
Input Low Voltage	V_{IL}		GND		0.8	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.7	3.3	VCC	V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA		0.06	0.3	V
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA		-0.79	-1.5	V
Input Current	I_{IN}	VCC			±15	µA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
		0V			±10	
Output Short Circuit Current	I_{OS}	V_{OUT} = 0V			-60	mA
LVDS Receiver DC Specifications						
Differential Input High Threshold	V_{TH}	V_{CM} = +1.2 V			+100	mV
Differential Input Low Threshold	V_{TL}		-100			mV
Input Current	I_{IN}	V_{IN} = +2.4 V, VCC = 3.6 V			±10	µA
		V_{IN} = 0V, VCC = 3.6 V			±15	µA
Receiver Supply Current						
Receiver Supply Current (worst case)	I_{CCRW}	C_L = 8 pF, f = 65 MHz, worst case pattern			220	mA
		C_L = 8 pF, f = 85 MHz, worst case pattern			240	mA
Receiver Supply Current (16 Grayscale)	I_{CCRG}	C_L= 8 pF, f = 65 MHz, 16 Grayscale pattern			125	mA
		C_L= 8 pF, f = 85 MHz, 16 Grayscale pattern			140	mA
Receiver Supply Current (Power Down)	I_{CCRZ}	Power_Down = Low, Receiver outputs stay low during Power-down mode		140	400	µA
Receiver Switching Characteristics						
CMOS/TTL Low-to-High Transition Time	CLHT	20% to 80% VCC, C_L= 8 pF		2	3.5	ns
CMOS/TTL High-to-Low Transition Time	CHLT	80% to 20% VCC, C_L= 8 pF		1.8	3.5	ns
CLKOUT period	RCOP		11.76	T	66.67	ns
CLKOUT High Time	RCOH	f = 85 MHz	4.5	5	7	ns
CLKOUT Low Time	RCOL	f = 85 MHz	4	5	6.5	ns
Data Setup to CLKOUT	RSRC	f = 85 MHz	2.0			ns
Data Hold to CLKOUT	RHRC	f = 85 MHz	3.5			ns
RCK+/- to CLKOUT Delay	RCCD	25°C / 3.3 V	8	14	20	ns
Receiver PLL Setup Time	RPLLS				10	ms
Receiver Power Down Delay	RPDD				1	µs
Receiver Input Strobe Position for Bit0	RSPos0	f = 85 MHz, T = 11.76 ns	0.49	0.84	1.19	ns
Receiver Input Strobe Position for Bit1	RSPos1	f = 85 MHz, T = 11.76 ns	2.17	2.52	2.87	ns
Receiver Input Strobe Position for Bit2	RSPos2	f = 85 MHz, T = 11.76 ns	3.85	4.2	4.55	ns
Receiver Input Strobe Position for Bit3	RSPos3	f = 85 MHz, T = 11.76 ns	5.53	5.88	6.23	ns
Receiver Input Strobe Position for Bit4	RSPos4	f = 85 MHz, T = 11.76 ns	7.21	7.56	7.91	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Receiver Input Strobe Position for Bit5	RSPos5	f = 85 MHz, T = 11.76 ns	8.89	9.24	9.59	ns
Receiver Input Strobe Position for Bit6	RSPos6	f = 85 MHz, T = 11.76 ns	10.57	10.92	11.27	ns
RxIn Skew Margin (see note and Figure 8)	Rskm	f = 85 MHz, T = 11.76 ns	300			ps
		f = 65 MHz, T = 15.38 ns	500			ps

Note: The skew margins mean the maximum timing tolerance between the clock and data channel when the receiver still works well. This margin takes into account the receiver input setup and hold time, and internal clock jitter (i.e., internal data sampling window - RSPos). This margin allows for LVDS transmitter pulse position, interconnect skew, inter-symbol interference and intrinsic channel mismatch which will cause the skew between clock (RC+ and RCK-) and data (RX[n]+ and RX[n]- ; n =0, 1, 2, 3) channels.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		84		°C/W
	θ_{JA}	1 m/s air flow		76		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			50		°C/W

Timing Diagrams

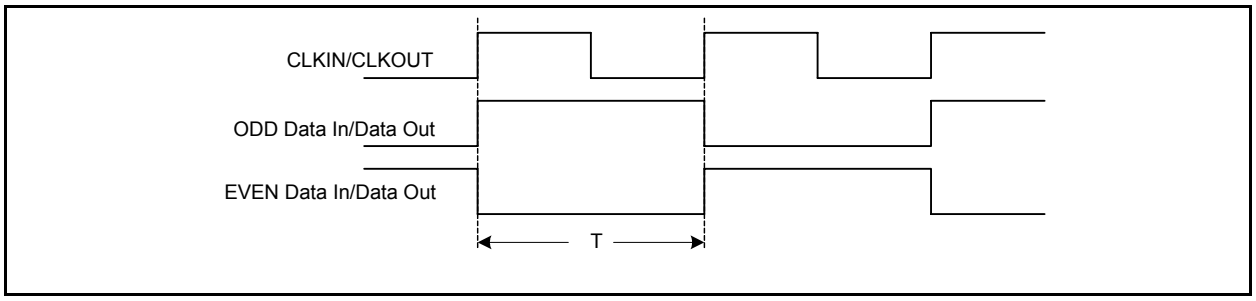


Figure 1a. “Worst Case” Test Pattern

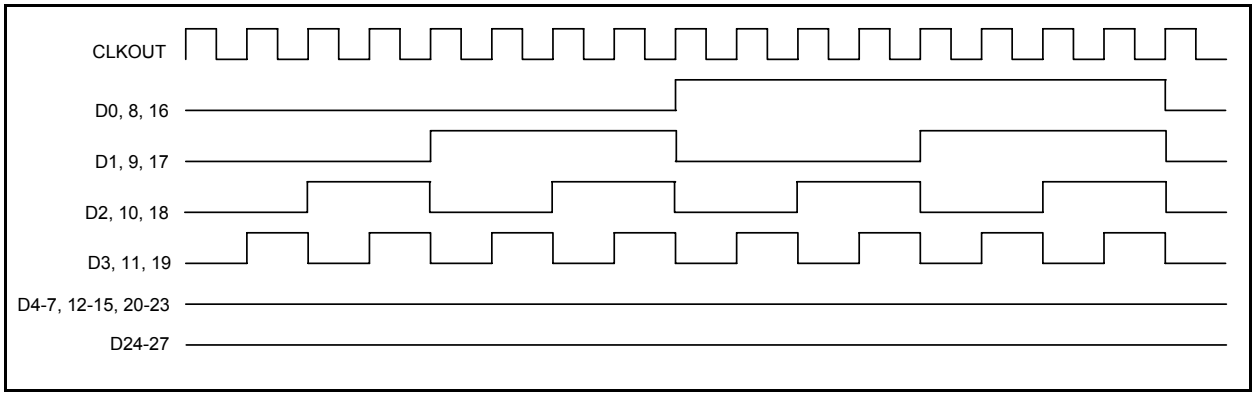


Figure 1b. 16-Grayscale Test-Pattern Waveforms

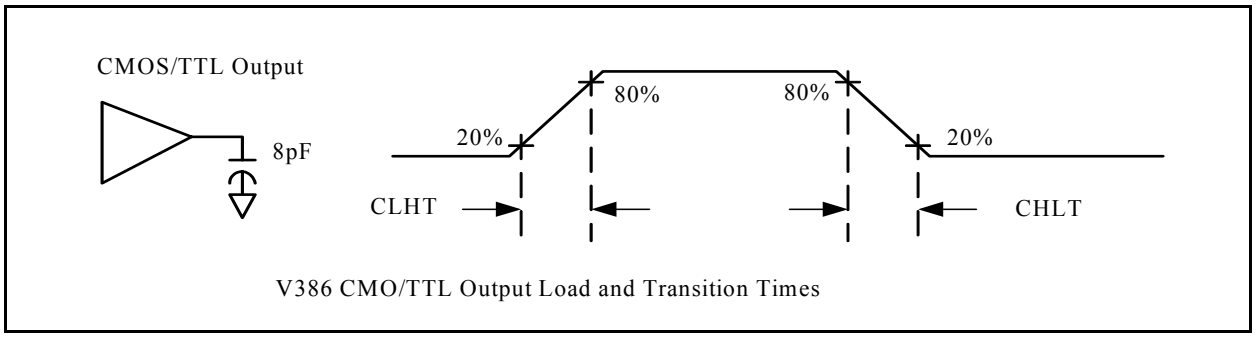


Figure 2. V386 CMOS/TTL Output Load and Transition Time

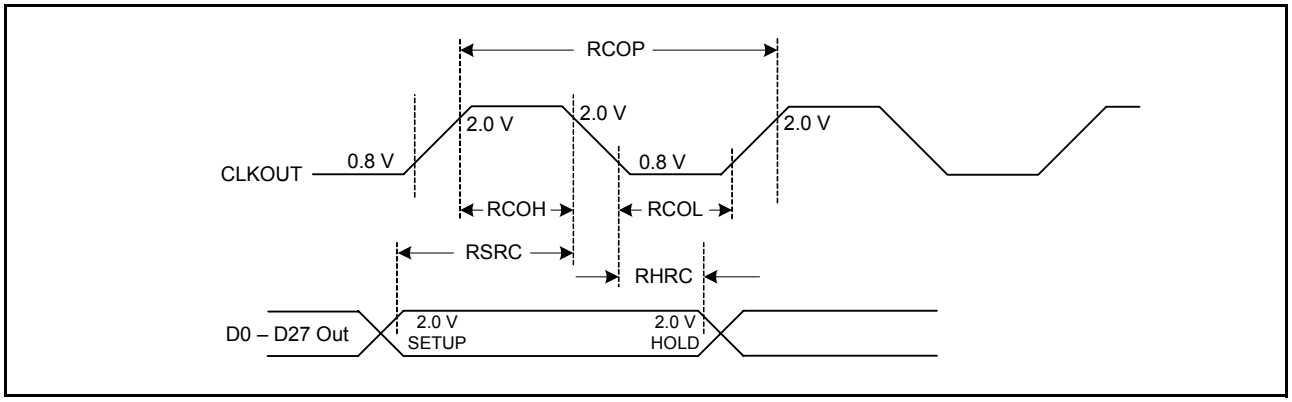


Figure 3. V386 SETUP/HOLD and High/Low Times

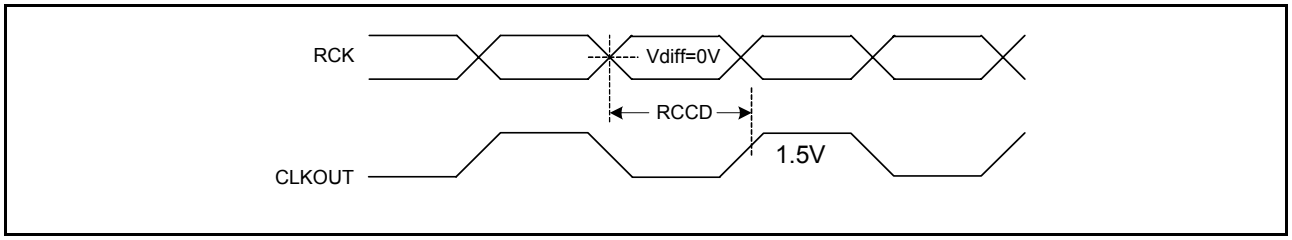


Figure 4. V386 Clock In to Clock Out Delay

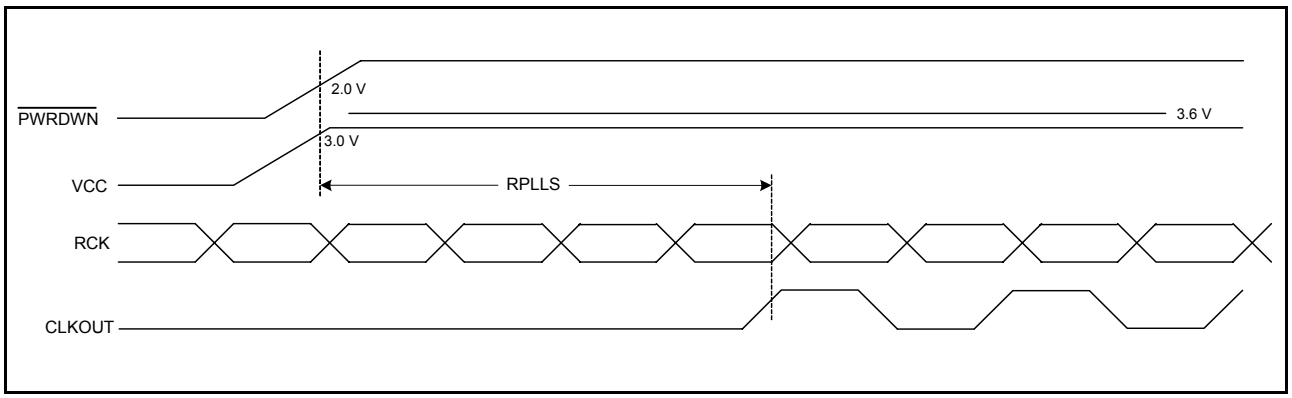


Figure 5. V386 Phase Lock Loop Set Time

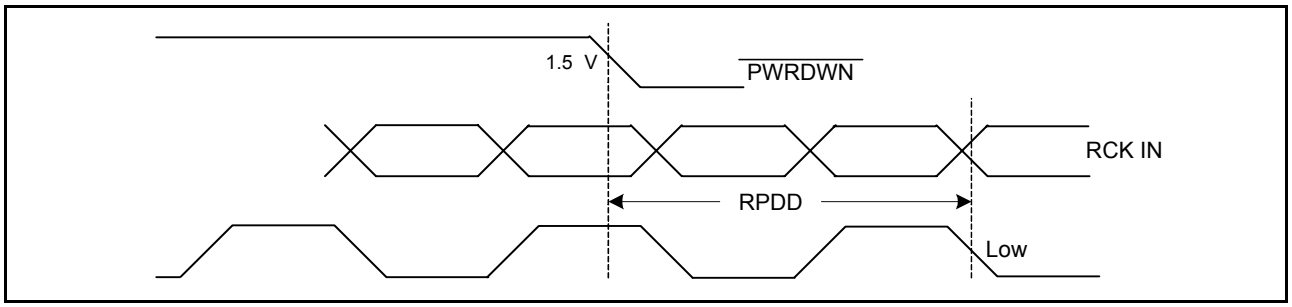


Figure 6. V386 Power Down Delay

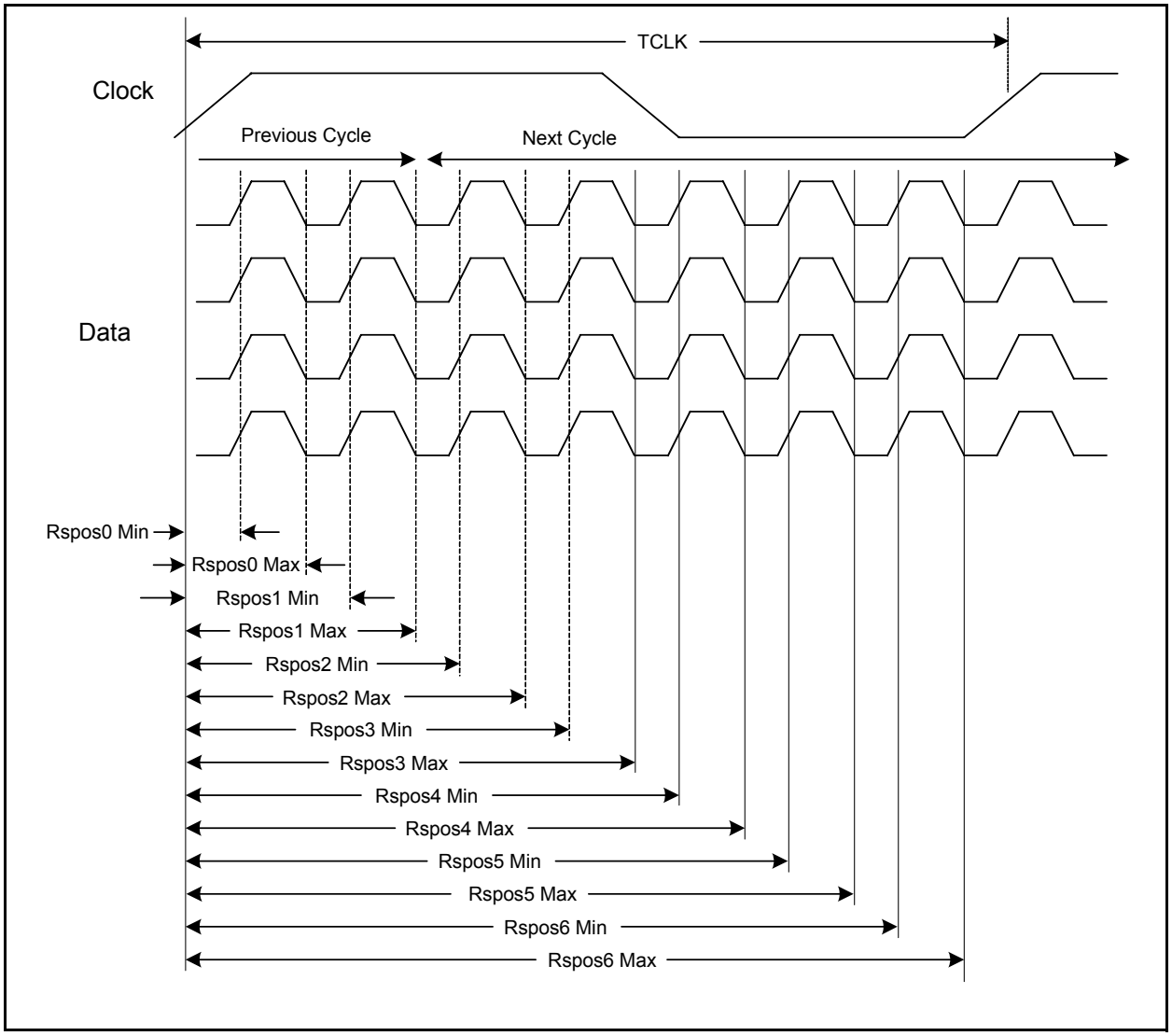


Figure 7. V386 LVDS Input Strobe Position

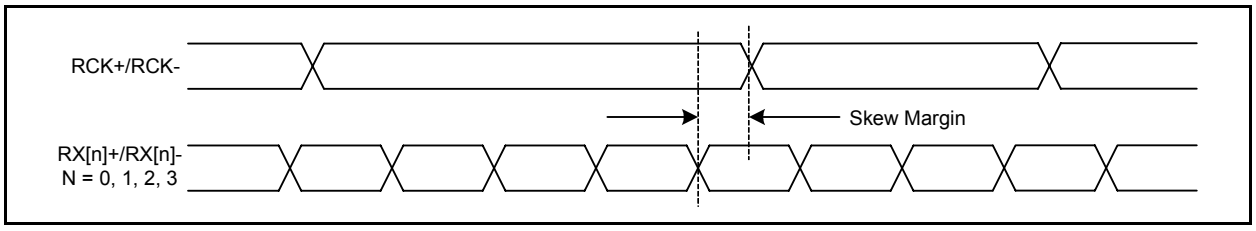
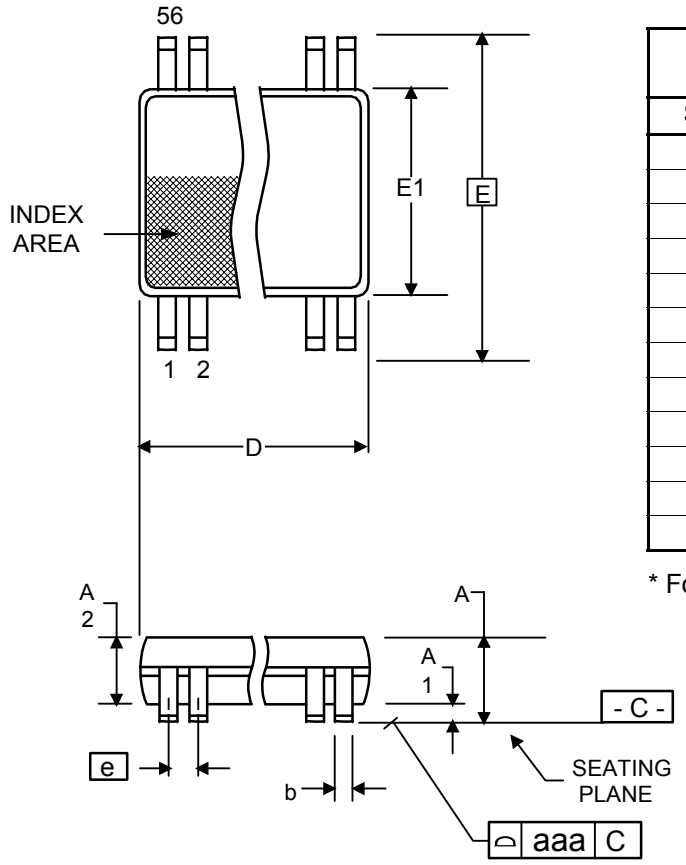


Figure 8. Receiver Input Skew Margin

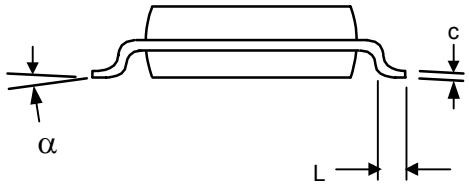
Package Outline and Package Dimensions (56-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.17	0.27	0.007	0.011
C	0.09	0.20	0.0035	0.008
D	13.90	14.10	0.547	0.555
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	0.236	0.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	0.018	0.030
a	0°	8°	0°	8°
aaa	—	0.10	—	0.004

* For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
V386GLF	V386GLF	Tubes	56-pin TSSOP	-10 to +70°C
V386GLFT	V386GLF	Tape and Reel	56-pin TSSOP	-10 to +70°C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.