National Semiconductor

September 10, 2010

LM22672

1A SIMPLE SWITCHER®, Step-Down Voltage Regulator with Features

General Description

The LM22672 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 1A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance N-channel MOSFET. The series consists of a fixed 5V output and an adjustable version.

The SIMPLE SWITCHER® concept provides for an easy to use complete design using a minimum number of external components and National's WEBENCH® design tool. National's WEBENCH® tool includes features such as external component calculation, electrical simulation, thermal simulation, and Build-It boards for easy design-in. The switching clock frequency is provided by an internal fixed frequency oscillator which operates at 500 kHz. The switching frequency can also be adjusted with an external resistor or synchronized to an external clock up to 1MHz. It is also possible to self-synchronize multiple regulators to share the same switching frequency. The LM22672 series also has built in thermal shutdown, current limiting and an enable control input that can power down the regulator to a low 25 µA quiescent current standby condition. An adjustable soft-start feature is provided by selecting an appropriate external soft-start capacitor.

Features

- Wide input voltage range: 4.5V to 42V
- Internally compensated voltage mode control
- Stable with low ESR ceramic capacitors
- 200 mΩ N-channel MOSFET
- Output voltage options:
  - -ADJ (outputs as low as 1.285V)
  - -5.0 (output fixed to 5V)
- ±1.5% feedback reference accuracy
- Switching frequency of 500 kHz, adjustable between 200 kHz and 1 MHz
- -40°C to 125°C operating junction temperature range
- Precision enable pin
- Integrated boot diode
- Adjustable soft-start
- Fully WEBENCH® enabled
- Step-down and inverting buck-boost applications

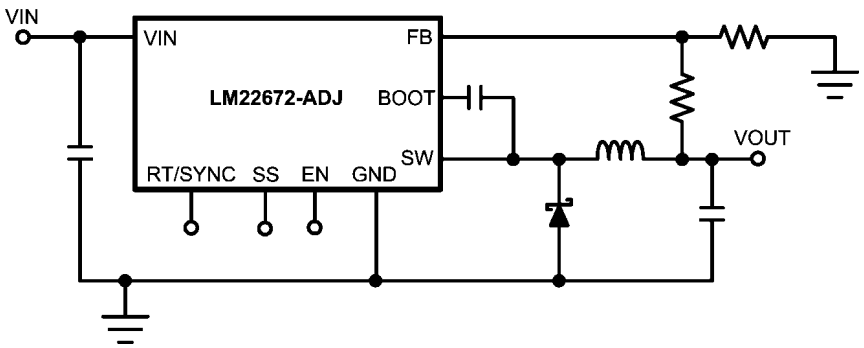
Package

- PSOP-8 (Exposed Pad)

Applications

- Industrial Control
- Telecom and Datacom Systems
- Embedded Systems
- Automotive Telematics and Body Electronics
- Conversions from Standard 24V, 12V and 5V Input Rails

Simplified Application Schematic



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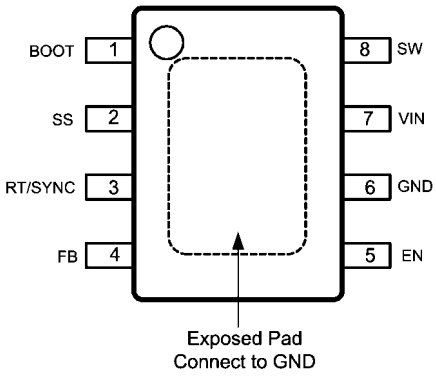
Connection Diagram



8-Lead Plastic PSOP-8 Package
NS Package Number MRA08B

Ordering Information

Output Voltage	Order Number	Package Type	NSC Package Drawing	Supplied As
ADJ	LM22672MR-ADJ	PSOP-8 Exposed Pad	MRA08B	95 Units in Rails
ADJ	LM22672MRE-ADJ			250 Units in Tape and Reel
ADJ	LM22672MRX-ADJ			2500 Units in Tape and Reel
5.0	LM22672MR-5.0			95 Units in Rails
5.0	LM22672MRE-5.0			250 Units in Tape and Reel
5.0	LM22672MRX-5.0			2500 Units in Tape and Reel

Pin Descriptions

Pin	Name	Description	Application Information
1	BOOT	Bootstrap input	Provides the gate voltage for the high side NFET.
2	SS	Soft-start pin	An external capacitor and an internal 50 µA current source set the time constant for the rise of the error amplifier reference. Pin can be left floating and internal soft-start will be default.
3	RT/SYNC	Oscillator frequency adjust pin or frequency synchronization	A resistor connected from this pin to GND adjusts the oscillator frequency. This pin can also accept an input for synchronization from an external clock. Pin can be left floating and internal setting will be default to 500 kHz.
4	FB	Feedback pin	Inverting input to the internal voltage error amplifier.
5	EN	Precision enable pin	When pulled low regulator turns off.
6	GND	System ground	Provide good capacitive decoupling between VIN and this pin.
7	VIN	Source input voltage	Input to the regulator. Operates from 4.5V to 42V.
8	SW	Switch pin	Attaches to the switch node.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN to GND	43V
EN Pin Voltage	-0.5V to 6V
SS, RT/SYNC Pin Voltage	-0.5V to 7V
SW to GND (*Note 2*)	-5V to V_{IN}
BOOT Pin Voltage	V_{SW} + 7V
FB Pin Voltage	-0.5V to 7V
Power Dissipation	Internally Limited
Junction Temperature	150°C
Soldering Information	
Infrared (5 sec.)	260°C
ESD Rating (*Note 3*)	
Human Body Model	±2 kV
Storage Temperature Range	-65°C to +150°C

Operating Ratings (*Note 1*)

Supply Voltage (V_{IN})	4.5V to 42V
Junction Temperature Range	-40°C to +125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_A = T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise specified: V_{IN} = 12V.

Symbol	Parameter	Conditions	Min (*Note 5*)	Typ (*Note 4*)	Max (*Note 5*)	Units
LM22672-5.0						
V_{FB}	Feedback Voltage	V_{IN} = 8V to 42V	4.925/**4.9**	5.0	5.075/**5.1**	V
LM22672-ADJ						
V_{FB}	Feedback Voltage	V_{IN} = 4.7V to 42V	1.266/**1.259**	1.285	1.304/**1.311**	V
All Output Voltage Versions						
I_Q	Quiescent Current	V_{FB} = 5V		3.4	**6**	mA
I_{STDBY}	Standby Quiescent Current	EN Pin = 0V		25	40	µA
I_{CL}	Current Limit		1.3/**1.2**	1.5	1.7/**1.8**	A
I_L	Output Leakage Current	V_{IN} = 42V, EN Pin = 0V, V_{SW} = 0V		0.2	2	µA
		V_{SW} = -1V		0.1	3	µA
$R_{DS(ON)}$	Switch On-Resistance			0.2	0.24/**0.32**	Ω
f_O	Oscillator Frequency		**400**	500	**600**	kHz
T_{OFFMIN}	Minimum Off-time		**100**	200	**300**	ns
T_{ONMIN}	Minimum On-time			100		ns
I_{BIAS}	Feedback Bias Current	V_{FB} = 1.3V (ADJ Version Only)		230		nA
V_{EN}	Enable Threshold Voltage	Falling	**1.3**	1.6	**1.9**	V
V_{ENHYST}	Enable Voltage Threshold Hysteresis			0.6		V
I_{EN}	Enable Input Current	EN Input = 0V		6		µA
F_{SYNC}	Synchronization Frequency	V_{SYNC} = 3.5V, 50% duty-cycle		1		MHz
V_{SYNC}	Synchronization Threshold Voltage			1.75		V
I_{SS}	Soft-Start Current		**30**	50	**70**	µA
T_{SD}	Thermal Shutdown Threshold			150		°C
θ_{JA}	Thermal Resistance	MR Package, Junction to ambient temperature resistance (*Note 6*)		60		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.

Note 2: The absolute maximum specification of the 'SW to GND' applies to DC voltage. An extended negative voltage limit of -10V applies to a pulse of up to 50 ns.

Note 3: ESD was applied using the human body model, a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 4: Typical values represent most likely parametric norms at the conditions specified and are not guaranteed.

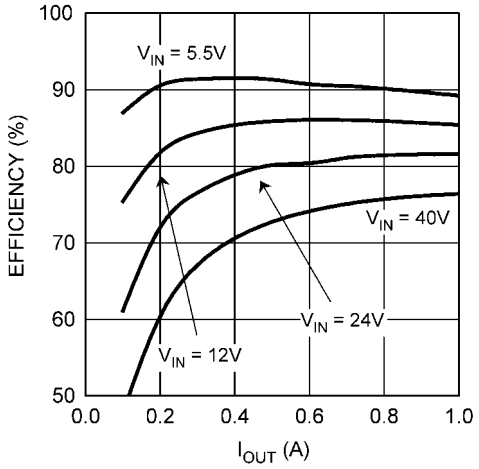
Note 5: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 6: The value of θ_{JA} for the PSOP-8 exposed pad (MR) package of 60°C/W is valid if package is mounted to 1 square inch of copper. The θ_{JA} value can range from 42 to 115°C/W depending on the amount of PCB copper dedicated to heat transfer.

Typical Performance Characteristics

Unless otherwise specified the following conditions apply: Vin = 12V, T_J = 25°C.

Efficiency vs I_{OUT} and V_{IN}
V_{OUT} = 3.3V



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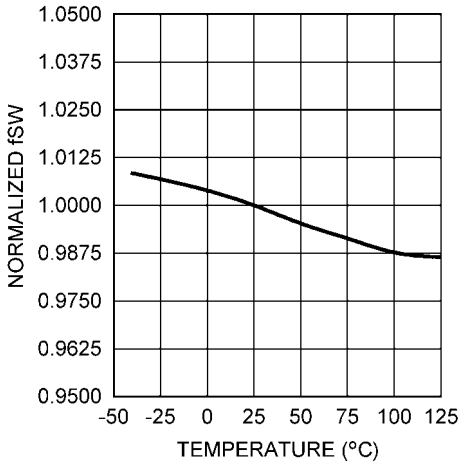
Normalized Switching Frequency vs Temperature



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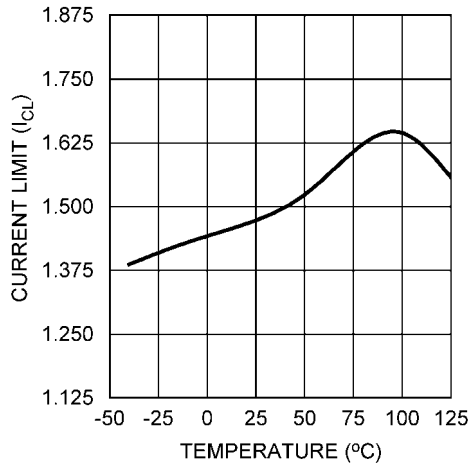
Current Limit vs Temperature



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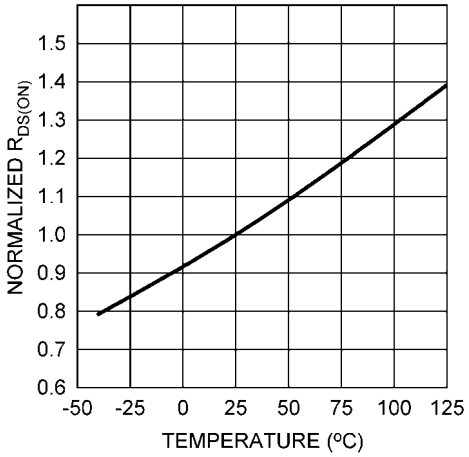
Normalized $R_{DS(ON)}$ vs Temperature



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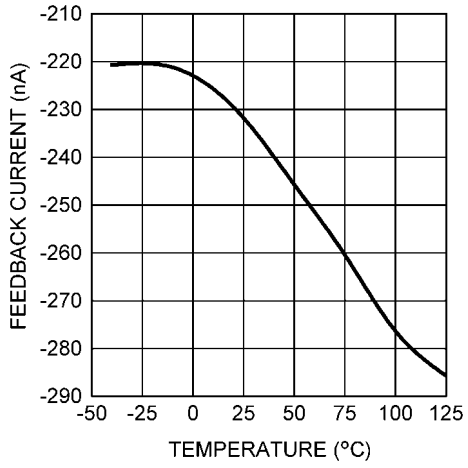
Feedback Bias Current vs Temperature



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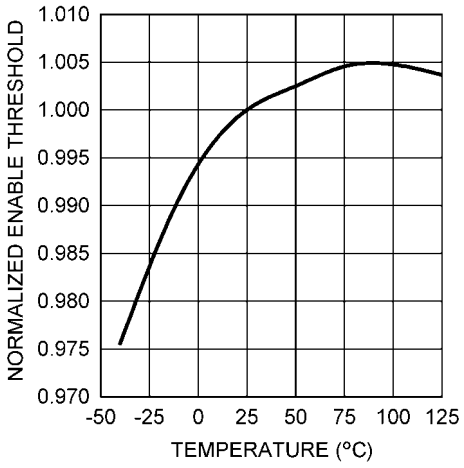
Normalized Enable Threshold Voltage vs Temperature



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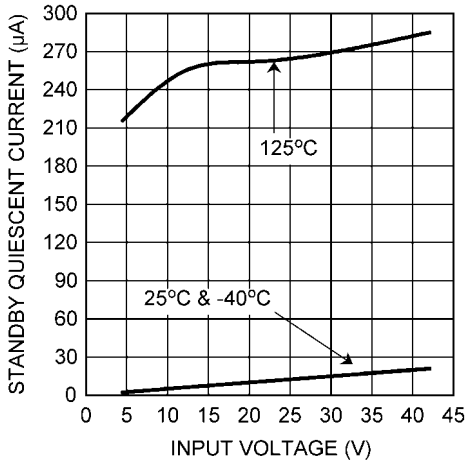
Standby Quiescent Current vs Input Voltage



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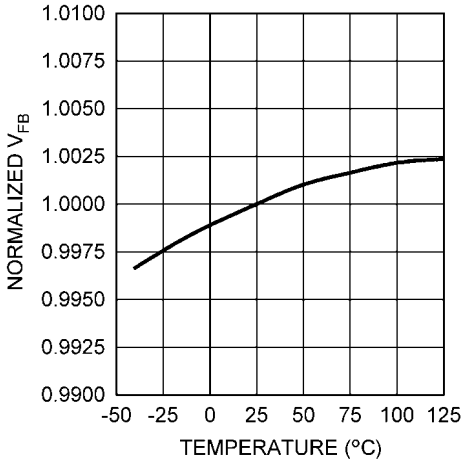
Normalized Feedback Voltage vs Temperature



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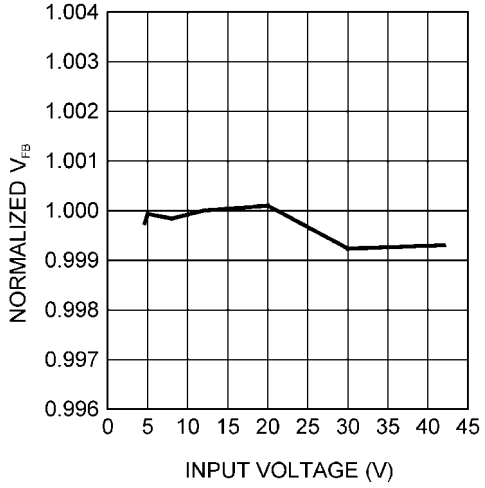
Normalized Feedback Voltage vs Input Voltage



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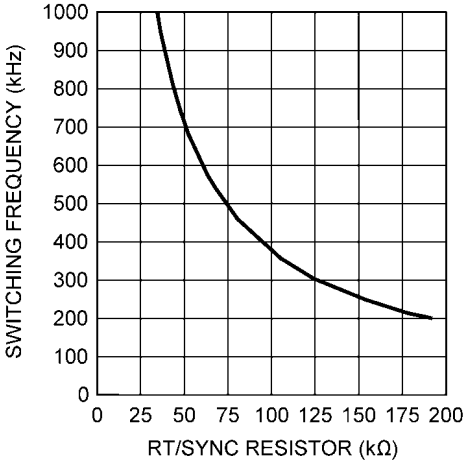
Switching Frequency vs RT/SYNC Resistor



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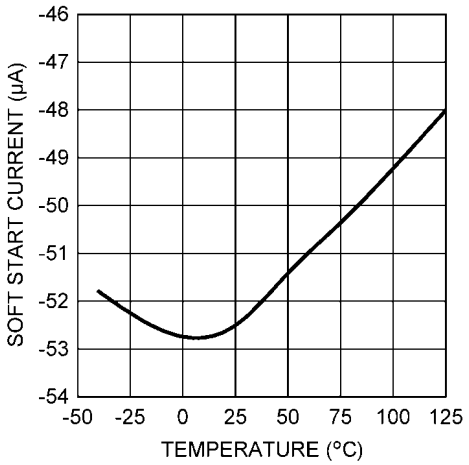
Soft-start Current vs Temperature



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Typical Application Circuit and Block Diagram

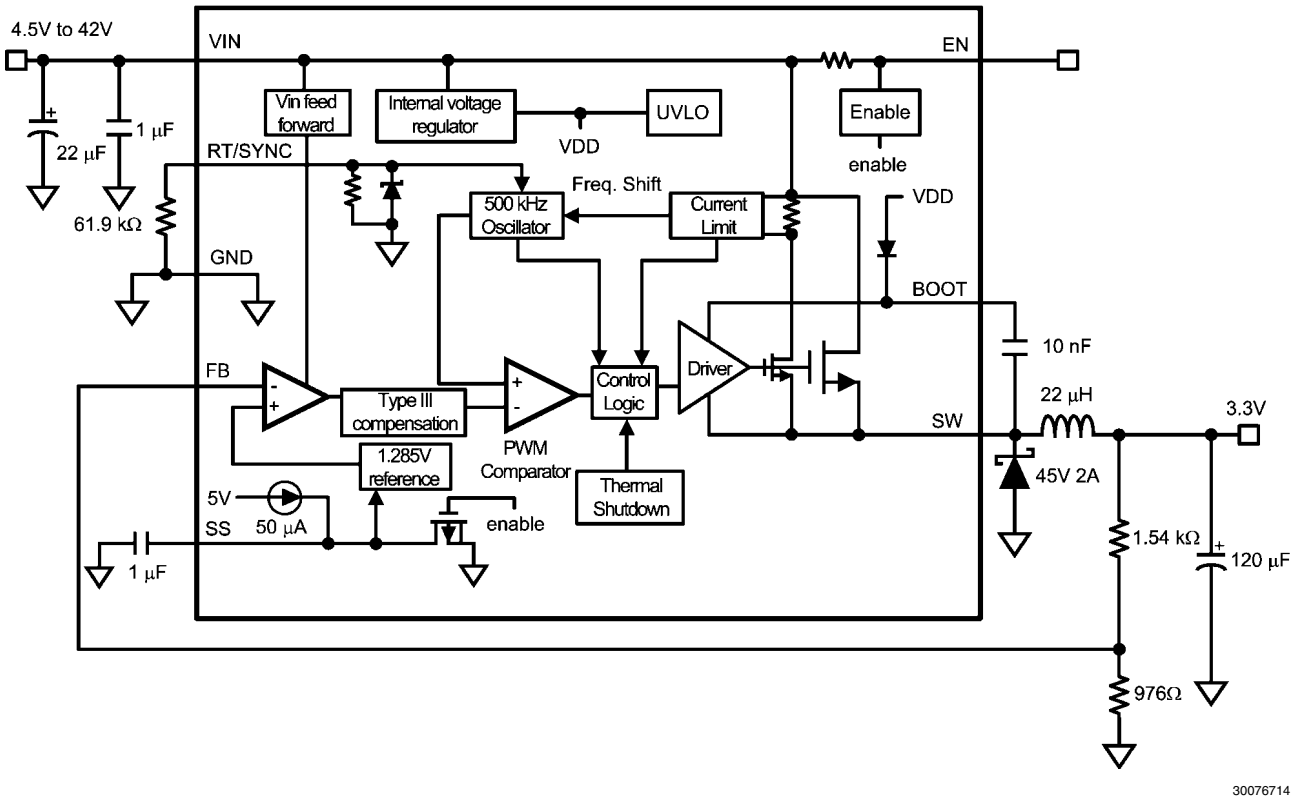


FIGURE 1. 3.3V V_{OUT}, 1A at 600 kHz

Detailed Operating Description

The LM22672 switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 42V N-Channel switch with an output current capability of 1A. The regulator control method is based on voltage mode control with input voltage feed forward. The loop compensation is integrated into the LM22672 so that no external compensation components need to be selected or utilized. Voltage mode control offers short minimum on-times allowing short duty-cycles necessary in high input voltage applications. The operating frequency is fixed at 500 kHz to allow for small external components while avoiding excessive switching losses. The switching frequency can be adjusted with an external resistor from 200 kHz to 1 MHz or it can be synchronized to an external clock up to 1 MHz. The output voltage can be set as low as 1.285V with the -ADJ device. Fault protection features include current limiting, thermal shutdown and remote shutdown capability. The device is available in the PSOP-8 package featuring an exposed pad to aid thermal dissipation.

The functional block diagram with typical application of the LM22672 are shown in *Figure 1*.

The internal compensation of the -ADJ option of the LM22672 is optimized for output voltages up to 5V. If an output voltage of 5V or higher is needed, the -5.0 fixed output voltage option with an additional external resistive feedback voltage divider may also be used.

Precision Enable

The precision enable pin (EN) can be used to shut down the power supply. Connecting this pin to ground or to a voltage less than typical 1.6V will completely turn off the regulator. The current drain from the input supply when off is typically 25 µA with 12V input voltage. The power consumed during this off state is mostly defined by an internal 2 MΩ resistor to VIN. The enable pin has an internal pull-up current source of approximately 6 µA. When driving the enable pin, the high voltage level for the on condition should not exceed the 6V absolute maximum limit. When enable control is not required, the EN pin should be left floating. The precision feature enables simple sequencing of multiple power supplies with a resistor divider from another power supply.

The EN pin can also be used as an external UVLO to disable the part when input voltage falls below a lower boundary of operation. This is often used to prevent excessive battery discharge. It can also be used to prevent early turn-on as Vin is rising which can cause undesirable on-off toggling if Vin droops below 4.5V during startup. Using EN as en external UVLO is also recommended to prevent abnormal device operation in applications where the input voltage falls below the minimum operating voltage of 4.5V, during power down for example.

Maximum Duty-Cycle / Dropout Voltage

The typical maximum duty-cycle is 90% at 500 kHz switching frequency. This corresponds to a typical minimum off-time of 200 ns. When operating at switching frequencies higher than 500 kHz, the 200 ns minimum off-time results in a lower maximum duty-cycle limit than 90%. This forced off-time is important to provide enough time for the Cboot capacitor to charge during each cycle.

The lowest input voltage required to maintain operation is:

$$V_{IN} = \frac{V_{OUT} + V_D}{1 - (T_{OFFMIN} \times F)} - V_D + V_Q$$

Where V_D is the forward voltage drop across the re-circulating Schottky diode and V_Q is the voltage drop across the internal power N-FET of the LM22672. The $R_{DS(ON)}$ of the FET is specified in the electrical characteristics section of this datasheet to calculate V_Q according to the FET current. F is the switching frequency.

Minimum Duty-Cycle

Besides a minimum off-time, there is also a minimum on-time which will take effect when the output voltage is adjusted very low and the input voltage is very high. Should the operation require an on-time shorter than minimum, individual switching pulses will be skipped.

Pulse skipping is a normal mode of operation which appears as a decrease in switching frequency. It has no effect on operation or regulation except for an increase in output ripple voltage. The pulse skipping function is required to maintain proper regulation and overcurrent protection under the full range of operating conditions.

The specified typical minimum on time of 100 ns is based on the blanking time during current limit operation. During normal operation, the minimum on-time will also include the effect of propagation delay. Assume approximately 150 ns as a typical operating minimum on time.

$$D = \frac{V_{OUT}}{V_{IN}} = T_{ON} \times F$$

where D is the duty-cycle.

Current Limit

When the power switch turns on, the slight capacitance loading of the Schottky diode, D1, causes a leading-edge current spike with an extended ringing period. This spike can cause the current limit comparator to trip prematurely. A leading edge blanking time (T_{BLK}) of 100 ns (typical) is used to avoid sampling the spike.

When the switch current reaches the current limit threshold the switch is immediately turned off. If T_{ON} is larger than the minimum (100 ns typical) the switcher will hold the output current flat at the set current limit value. But if T_{ON} is at or decreases to the minimum T_{ON} (100 ns typical) the switching frequency decreases to 1/5 the typical frequency. This effectively causes the output current to fold back to a lower and safe value. When the current limit condition is removed the switching frequency is restored to nominal. This 5X frequency fold back will result in a lower duty cycle pulse of the power switch to minimize the overall fault condition power dissipation.

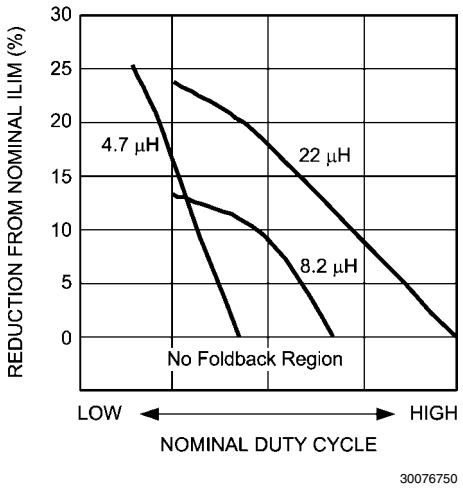


FIGURE 2. Output Current in Foldback vs. Nominal Duty Cycle

The percentage of output current limit fold back is affected by duty cycle, inductance, and switching frequency. See *Figure 2* for details.

The current limit will only protect the inductor from a runaway condition if the LM22672 is operating in its safe operating area. A runaway condition of the inductor is potentially catastrophic to the application. For every design, the safe operating area needs to be calculated. Factors in determining the safe operating area are the switching frequency, input voltage, output voltage, minimum on-time and feedback voltage during an over current condition.

As a first pass check, if the following equation holds true, a given design is considered in a safe operating area and the current limit will protect the circuit:

$$V_{IN} \times T_{BLK} \times F < V_{OUT} \times 0.724$$

If the equation above does not hold true, the following secondary equation will need to hold true to be in safe operating area:

$$(V_{IN} - V_{OUT}) \times T_{BLK} < (V_{OUT} + V_D) \times \left(\frac{1}{F}\right) - T_{BLK}$$

If both equations do not hold true, a particular design will not have an effective current limit function which might damage the circuit during startup, over current conditions, or steady state over current and short circuit condition. Oftentimes a reduction of the maximum input voltage or reduction of the switching frequency will bring a design into the safe operating area.

When synchronized to an external sync pulse, the LM22672 will not fold back the switching frequency in an over current condition.

Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The soft-start can be adjusted by selecting an external soft-start capacitor. An internal 50 µA current source charges up the external soft-start capacitor. The generated voltage is the voltage the internal reference limits. If no external soft-start capacitor is used, there is an internal soft-start feature with 500 µs (typical) start-up time. Recommended soft-start capacitor values are between 100 nF to 1 µF.

Switching Frequency Setting and Synchronization

There are three different modes for the RT/SYNC pin. It can be left floating for a 500 kHz switching frequency.

A resistor from the RT/SYNC pin to ground can be used to adjust the switching frequency between 200 kHz and 1 MHz. An external synchronization pulse can be applied to the RT/SYNC pin for switching frequencies up to 1 MHz. The LM22672 internally sets the RT/SYNC mode during start up.

Many applications are limited to lower switching frequencies due to minimum on-time and minimum off-time requirements as well as increased switching losses at switching frequencies higher than 500 kHz. In case of synchronizing to an external sync pulse, the clock pulse must be in a valid low or high state when the LM22672 starts up and can be applied after device regulation. The internal oscillator will synchronize to the external sync pulse rising edge. If the external sync pulse is disconnected the LM22672 switching frequency will return to default 500 kHz (typ.).

When operating at frequencies above 500 kHz, external components such as the inductor and the output capacitors cannot be reduced dramatically. This is due to the fixed internal compensation and stability requirements. Running the LM22672 at frequencies higher than 500 kHz is intended for applications with EMI or beat frequency concerns. The flexibility of increasing the switching frequency above 500 kHz can be used to operate outside a critical signal frequency band of an application. This can also be used to set multiple switchers in an application to the same frequency to reduce beat frequencies and simplify filtering.

See the current limit section of this datasheet for information about the safe operating area. When synchronizing to an external synchronization pulse, the LM22672 will not fold back the switching frequency in an over current condition.

The typical curve below shows adjusted switching frequencies with different frequency set resistors from the RT/SYNC pin to ground.

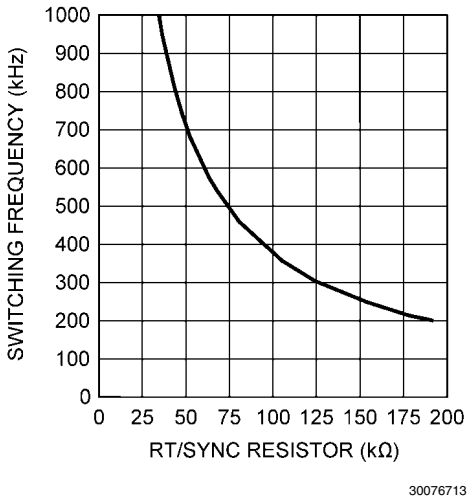


FIGURE 3. Switching Frequency vs RT/SYNC Resistor

Self Synchronize

It is also possible to self-synchronize multiple LM22672 regulators to share the same switching frequency. This can be done by attaching the RT/SYNC pins together and putting a 1 kΩ resistor to ground. The diagram in *Figure 4* illustrates this setup. The two regulators will be clocked at the same frequency but slightly phase shifted according to the minimum off-time of the regulator with the fastest running oscillator. The slight phase shift helps to reduce the stress on the input capacitors of the power supply.

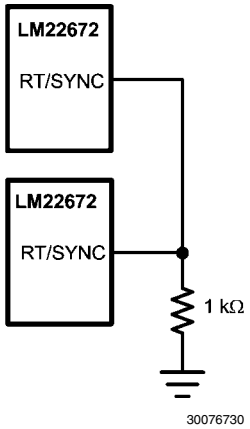


FIGURE 4. Self Synchronizing Setup

Boot Pin

The LM22672 integrates an N-Channel FET switch and associated floating high voltage level shift / gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.01 µF ceramic capacitor connected with short traces between the BOOT pin and the SW pin is recommended to effectively drive the internal FET switch. During the off-time of the switch, the SW voltage is approximately -0.5V and the external bootstrap capacitor is charged from the internal supply through the internal bootstrap diode. When operating with a high PWM duty-cycle, the buck switch will be forced off each cycle to ensure that the bootstrap capacitor is recharged. See the maximum duty-cycle section for more details.

Thermal Protection

Internal Thermal Shutdown circuitry protects the LM22672 in the event the maximum junction temperature is exceeded. When activated, typically at 150°C, the regulator is forced into a low power reset state. There is a typical hysteresis of 15 degrees.

Internal Compensation

The LM22672 has internal compensation designed for a stable loop with a wide range of external power stage components.

Insuring stability of a design with a specific power stage (inductor and output capacitor) can be tricky. The LM22672 stability can be verified over varying loads and input and output voltages using WEBENCH® Designer online circuit simulation tool at www.national.com. A quick start spreadsheet can also be downloaded from the online product folder.

The internal compensation of the -ADJ option of the LM22672 is optimized for output voltages below 5V. If an output voltage of 5V or higher is needed, the -5.0 option with an additional external resistor divider may also be used.

The typical location of the internal compensation poles and zeros as well as the DC gain is given in *Table 1*. The LM22672 has internal type III compensation allowing for the use of most output capacitors including ceramics.

This information can be used to calculate the transfer function from the FB pin to the internal compensation node (input to the PWM comparator in the block diagram).

TABLE 1.

Corners	Frequency
Pole 1	150 kHz
Pole 2	250 kHz
Pole 3	100 Hz
Zero 1	1.5 kHz
Zero 2	15 kHz
DC gain	37.5 dB

For the power stage transfer function the standard voltage mode formulas for the double pole and the ESR zero apply:

$$f_{DP} = \frac{1}{2\pi \sqrt{L \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The peak ramp level of the oscillator signal feeding into the PWM comparator is $V_{IN}/10$ which equals a gain of 20dB of this modulator stage of the IC. The -5.0 fixed output voltage option has twice the gain of the compensation transfer function compared to the -ADJ option which is 43.5dB instead of 37.5dB.

Generally, calculation as well as simulation can only aid in selecting good power stage components. A good design practice is to test for stability with load transient tests or loop measurement tests. Application note AN-1889 shows how to easily perform a loop transfer function measurement with only an oscilloscope and a function generator.

Application Information

EXTERNAL COMPONENTS

The following design procedures can be used to design a non-synchronous buck converter with the LM22672.

Inductor

The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltage. To keep the application in continuous current conduction mode (CCM), the maximum ripple current, I_{RIPPLE} , should be less than twice the minimum load current.

The general rule of keeping the inductor current peak-to-peak ripple around 30% of the nominal output current is a good compromise between excessive output voltage ripple and excessive component size and cost. Using this value of ripple current, the value of inductor, L, is calculated using the following formula:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{I_{RIPPLE} \times F \times V_{IN(MAX)}}$$

where F is the switching frequency which is 500 kHz without an external frequency set resistor or external sync signal applied to the RT/SYNC pin. If the switching frequency is set higher than 500kHz, the inductance value may not be reduced accordingly due to stability requirements. The internal compensation is optimized for circuits with a 500 kHz switching frequency. See the internal compensation section for more details. This procedure provides a guide to select the value of the inductor L. The nearest standard value will then be used in the circuit.

Increasing the inductance will generally slow down the transient response but reduce the output voltage ripple amplitude. Reducing the inductance will generally improve the transient response but increase the output voltage ripple.

The inductor must be rated for the peak current, I_{PK+}, to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. Under an overload condition as well as during load transients, the peak current is limited to 1.5A typical (1.8A maximum). This requires that the inductor be selected such that it can run at the maximum current limit and not only the steady state current.

Depending on inductor manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30% at 20°C. In typical designs the inductor will run at higher temperatures. If the inductor is not rated for enough current, it might saturate and due to the propagation delay of the current limit circuitry, the power supply may get damaged.

Input Capacitor

Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during on-time. When the switch turns on, the current into the VIN pin steps to the peak value, then drops to zero at turn-off. The average current into VIN during switch on-time is the load current. The input capacitance should be selected for RMS current, I_{RMS}, and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

Quality ceramic capacitors with a low ESR should be selected for the input filter. To allow for capacitor tolerances and voltage effects, multiple capacitors may be used in parallel. If step input voltage transients are expected near the maximum rating of the LM22672, a careful evaluation of ringing and possible voltage spikes at the VIN pin should be completed. An additional damping network or input voltage clamp may be required in these cases.

Usually putting a higher ESR electrolytic input capacitor in parallel to the low ESR bypass capacitor will help to reduce excessive voltages during a line transient and will also move the resonance frequency of the input filter away from the regulator bandwidth.

Output Capacitor

The output capacitor can limit the output ripple voltage and provide a source of charge for transient loading conditions. Multiple capacitors can be placed in parallel. Very low ESR capacitors such as ceramic capacitors reduce the output ripple voltage and noise spikes, while higher value capacitors in parallel provide large bulk capacitance for transient loading and unloading. Therefore, a combination of parallel capacitors, a single low ESR SP or Poscap capacitor, or a high value of ceramic capacitor provides the best overall performance. Output capacitor selection depends on application conditions as well as ripple and transient requirements. Typically a value of at least 100 µF is recommended. An approximation for the output voltage ripple is:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \left(\frac{1}{8 \times F \times C_{OUT}} \right) \right)$$

In applications with Vout less than 3.3V, where input voltage may fall below the operating minimum of 4.5V, it is critical that low ESR output capacitors are selected. This will limit potential output voltage overshoots as the input voltage falls below device normal operation range.

If the switching frequency is set higher than 500 kHz, the capacitance value may not be reduced accordingly due to stability requirements. The internal compensation is optimized for circuits with a 500 kHz switching frequency. See the internal compensation section for more details.

Cboot Capacitor

The bootstrap capacitor between the BOOT pin and the SW pin supplies the gate current to turn on the N-channel MOSFET. The recommended value of this capacitor is 10 nF and should be a good quality, low ESR ceramic capacitor.

It is possible to put a small resistor in series with the Cboot capacitor to slow down the turn-on transition time of the internal N-channel MOSFET. Resistors in the range of 10Ω to 50Ω can slow down the transition time. This can reduce EMI of a switched mode power supply circuit. Using such a series resistor is not recommended for every design since it will increase the switching losses of the application and makes thermal considerations more challenging.

Resistor Divider

For the -5.0 option no resistor divider is required for 5V output voltage. The output voltage should be directly connected to the FB pin. Output voltages above 5V can use the -5.0 option with a resistor divider as an alternative to the -ADJ option. This may offer improved loop bandwidth in some applications. See the Internal Compensation section for more details.

For the -ADJ option no resistor divider is required for 1.285V output voltage. The output voltage should be directly connected to the FB pin. Other output voltages can use the -ADJ option with a resistor divider.

The resistor values can be determined by the following equations:

-ADJ option:

$$R1 = \frac{R2}{\frac{V_{OUT}}{V_{FB}} - 1}$$

-5.0 option:

$$R1 = \frac{R2 \times V_{FB}}{(R2 \times 500\ \mu A) + V_{OUT} - V_{FB}}$$

Where V_{FB} = 1.285V typical for the -ADJ option and 5V for the -5.0 option

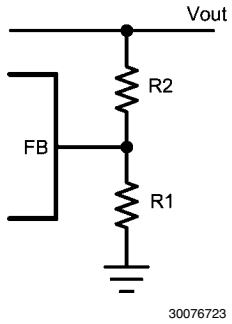


FIGURE 5. Resistive Feedback Divider

A maximum value of 10 kΩ is recommended for the sum of R1 and R2 to keep high output voltage accuracy for the –ADJ option. A maximum of 2 kΩ is recommended for the -5.0 output voltage option. For the 5V fixed output voltage option, the total internal divider resistance is typically 9.93 kΩ.

At loads less than 5 mA, the boot capacitor will not hold enough charge to power the internal high side driver. The output voltage may droop until the boot capacitor is recharged. Selecting a total feedback resistance to be below 3 kΩ will provide some minimal load and can keep the output voltage from collapsing in such low load conditions.

Catch Diode

A Schottky type re-circulating diode is required for all LM22672 applications. Ultra-fast diodes which are not Schottky diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low forward voltage drop of Schottky diodes are particularly important diode characteristics for high input voltage and low output voltage applications common to the LM22672. The reverse recovery characteristic determines how long the current surge lasts each cycle when the N-channel MOSFET is turned on. The reverse recovery characteristics of Schottky diodes minimizes the peak instantaneous power in the switch occurring during turn-on for each cycle. The resulting switching losses are significantly reduced when using a Schottky diode. The reverse breakdown rating should be selected for the maximum V_{IN}, plus some safety margin. A rule of thumb is to select a diode with the reverse voltage rating of 1.3 times the maximum input voltage.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. 'Rated' current for diodes varies widely from various manufacturers. The worst case is to assume a short circuit load condition. In this case the diode will carry the output current almost continuously. For the LM22672 this current can be as high as 1.5A (typical). Assuming a worst case 1V drop across the diode, the maximum diode power dissipation can be as high as 1.5W.

Circuit Board Layout

Board layout is critical for switching power supplies. First, the ground plane area must be sufficient for thermal dissipation purposes. Second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted L di/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI) and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The most important layout rule is to keep the AC current loops as small as possible. *Figure 6* shows the current flow of a buck converter. The top schematic shows a dotted line which represents the current flow during the FET switch on-state. The middle schematic shows the current flow during the FET switch off-state.

The bottom schematic shows the currents referred to as AC currents. These AC currents are the most critical since current is changing in very short time periods. The dotted lines of the bottom schematic are the traces to keep as short as possible. This will also yield a small loop area reducing the loop inductance. To avoid functional problems due to layout, review the PCB layout example. Best results are achieved if the placement of the LM22672, the bypass capacitor, the Schottky diode and the inductor are placed as shown in the example. It is also recommended to use 2oz copper boards or thicker to help thermal dissipation and to reduce the parasitic inductances of board traces.

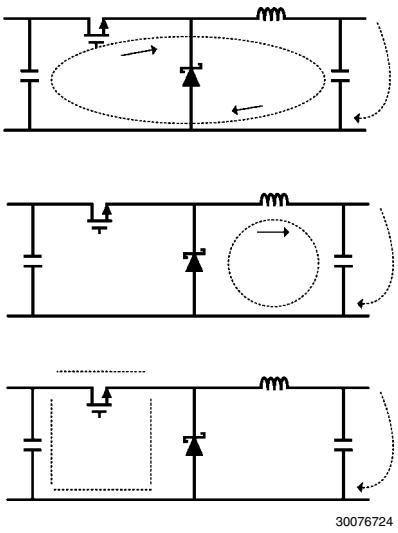


FIGURE 6. Current Flow in a Buck Application

Thermal Considerations

The two highest power dissipating components are the re-circulating diode and the LM22672 regulator IC. The easiest method to determine the power dissipation within the LM22672 is to measure the total conversion losses (Pin – Pout) then subtract the power losses in the Schottky diode and output inductor. An approximation for the Schottky diode loss is:

$$P = (1 - D) \times I_{OUT} \times V_D$$

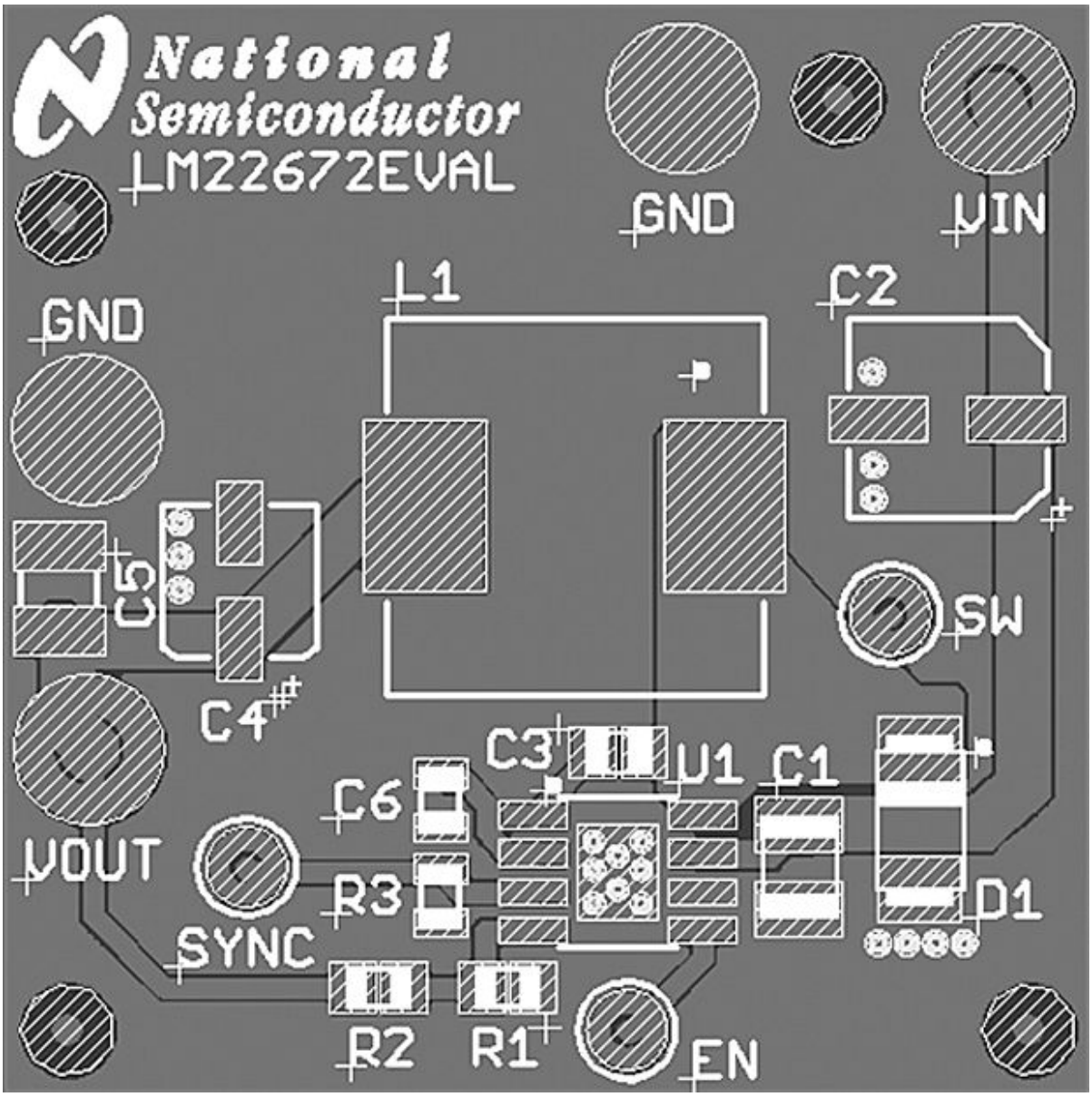
An approximation for the output inductor power is:

$$P = I_{OUT}^2 \times R \times 1.1,$$

where R is the DC resistance of the inductor and the 1.1 factor is an approximation for the AC losses. The regulator has an exposed thermal pad to aid power dissipation. Adding several vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will aid the power dissipation of the diode. The most significant variables that affect the power dissipated by the LM22672 are the output current, input voltage and operating frequency. The power dissipated while operating near

the maximum output current and maximum input voltage can be appreciable. The junction-to-ambient thermal resistance of the LM22672 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM22672 PSOP-8 package is specified in the electrical characteristics table under the applicable conditions.

PCB Layout Example



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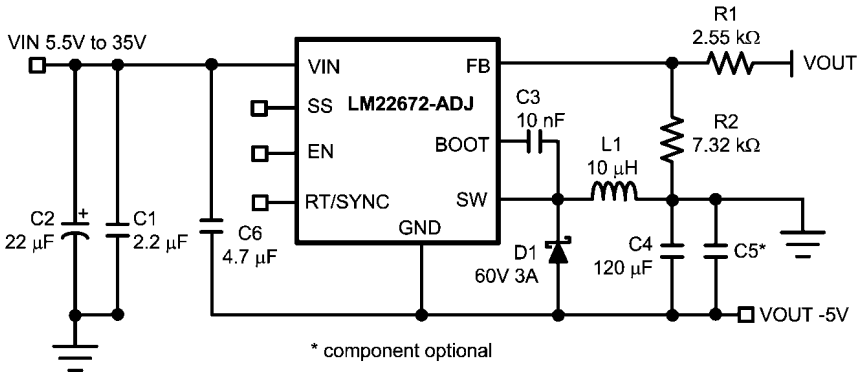
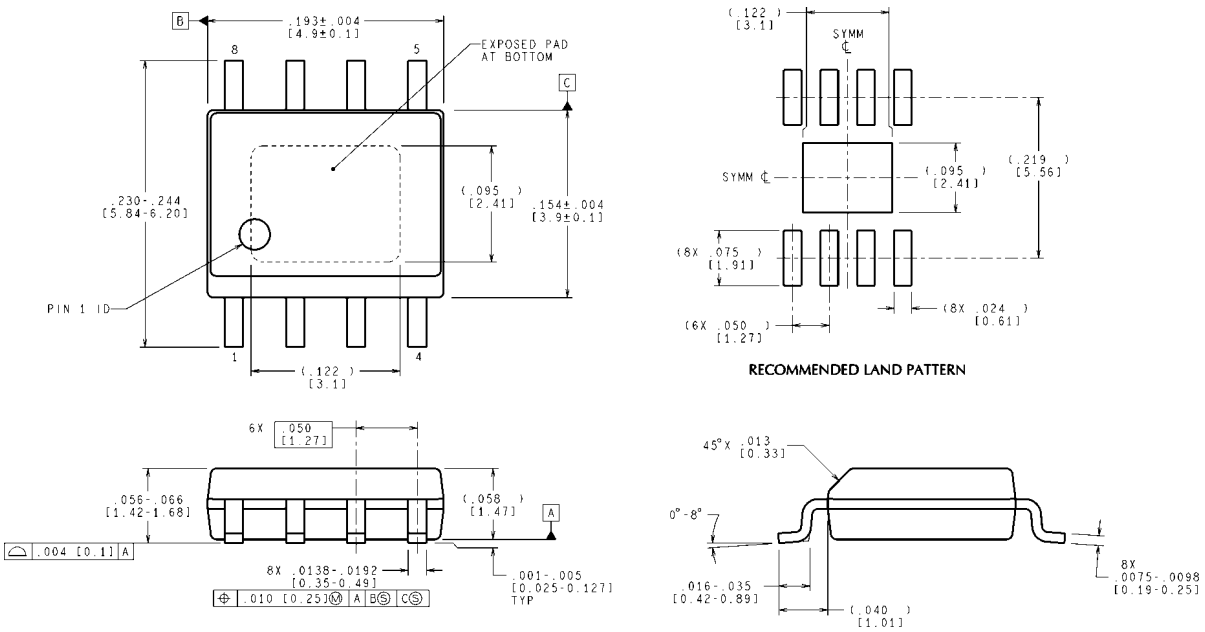
Schematic for Buck/Boost (Inverting) Application

See AN-1888 for more information on the inverting (buck-boost) application generating a negative output voltage from a positive input voltage.



Physical Dimensions inches (millimeters) unless otherwise noted



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8-Lead Plastic PSOP-8 Package
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Notes

Notes

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