High Voltage Ring Generator IC

Features

- 220V maximum operating voltage
- Integrated high voltage transistors
- Up to 70 V_{RMS} ring signal
- Adjustable AC and DC output voltage level
- Adjustable ring signal start phase angle
- Pulse by pulse output over current protection
- 5 REN output capability
- External MOSFETs enhance output rating to 20 REN

Applications

- Stand alone high voltage ring generator
- Set-top/street box ring generator
- Pair gain ring generator
- Wireless local loops
- Fibre in the loop/to the curb
- Coax cable loop

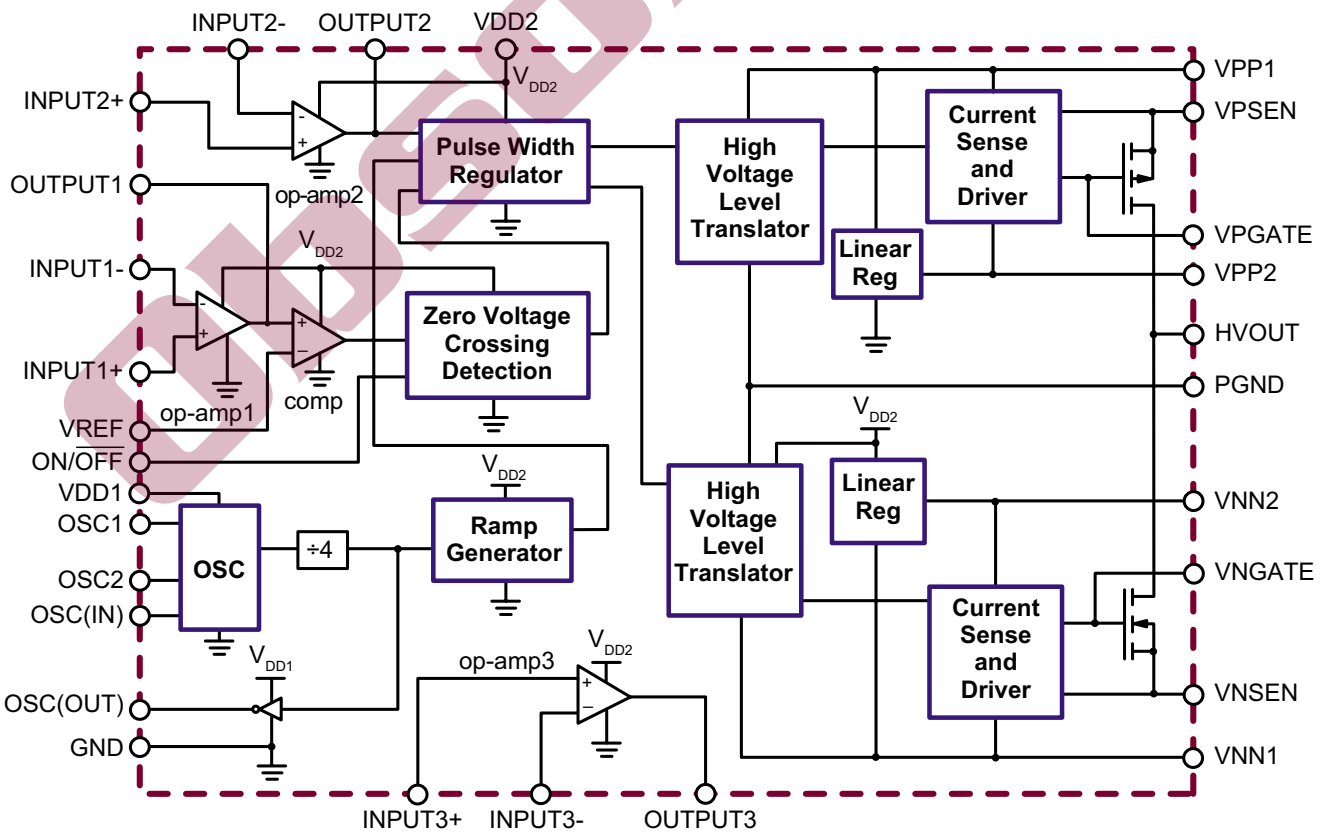
General Description

The Supertex HV441 is a monolithic integrated circuit capable of generating up to a 70V_{RMS} sine wave output at frequencies of 15 to 60Hz with a load of 5 North American RENs. Its output rating can be enhanced to 20 North American RENs with the addition of two Supertex MOSFETs: one N-Channel MOSFET, the TN2524N8, and one P-Channel MOSFET, the TP2522N8. The high voltage outputs have pulse by pulse over-current protection set by two external sense resistors.

The HV441 generates a low voltage reference sine wave by using external passive components. An external sine wave signal can be used if desired. The HV441 amplifies the reference sine wave signal by pulse width modulating the high voltage output at a nominal frequency of 100KHz. An error amplifier compares the output sine wave with the reference sine wave and adjusts the pulse width accordingly. Both the amplitude of the output sinewave and the DC offset voltage are adjustable.

For detailed circuit and application information, please refer to application note AN-H35.

Functional Block Diagram



Ordering Information

Device	44-Lead PLCC *10.30x7.50mm body* *2.65mm height (max)* *1.27mm pitch*
HV441	HV441PJ-G

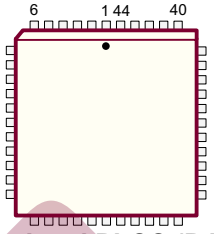
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{PP1} - V_{NN1}, power supply voltage	+240V
V_{PP1}, positive high supply voltage	+120V
V_{PP2}, positive gate supply voltage	+120V
V_{NN1}, negative high voltage	-170V
V_{NN2}, negative gate voltage	-170V
V_{DD1}, low voltage logic supply	+7.5V
V_{DD2}, low voltage analog/logic supply	+18V
Storage temperature	-65°C to +150°C
Power dissipation	1200mW

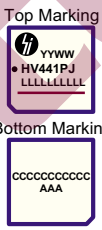
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



44-Lead PLCC (PJ)
(top view)

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
———— = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PLCC (PJ)

Electrical Characteristics *(over operating supply voltage unless otherwise specified. T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PP1}	High voltage positive supply	15	-	110	V	T_A = -40°C to +85°C
V_{PP2}	Positive charge pump output	V_{PP1}-8.0	-	V_{PP1}-19		
V_{NN1}	High voltage negative supply	V_{PP1}-220	-	-110		
V_{NN2}	Negative charge pump output	V_{PP1}+5.2	-	V_{NN1}+10.5		
V_{DD1}	Low voltage supply	3.0	-	5.5		
V_{DD2}	Low voltage supply	10.8	-	13.5		
I_{PP1Q}	V_{PP1} quiescent current	-	250	400	µA	T_A = -40°C to +85°C
I_{NN1Q}	V_{NN1} quiescent current	-	250	500		
I_{PP1}	V_{PP1} operating current	-	-	0.8	mA	HV_{OUT} switching at 100KHz, V_{PP1} = +60V, V_{NN1} = -160V, T_A = -40°C to +85°C
I_{NN1}	V_{NN1} operating current	-	-	1.0		
I_{DD1Q}	V_{DD1} quiescent current	-	-	10	µA	---
I_{DD2Q}	V_{DD2} quiescent current	-	-	4.0	mA	---

High Voltage Output

R_{SOURCE}	V_{OUT}P source resistance	-	55	-	Ω	I_{OUT} = 100mA
R_{SINK}	V_{OUT}P sink resistance	-	55	-	Ω	I_{OUT} = -100mA

Electrical Characteristics *(cont.)* *(over operating supply voltage unless otherwise specified. T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
DC_P	Max P-channel duty cycle	92	-	-	%	V_{PP1} = +60V, V_{NN1} = -160V
DC_N	Max N-channel duty cycle	94	-	-		
$t_{D(ON)}$	HV_{OUT} delay time	-	150	-	ns	---
t_{RISE}	HV_{OUT} rise time	-	-	50	ns	---
$t_{D(OFF)}$	HV_{OUT} delay time	-	200	-	ns	---
t_{FALL}	HV_{OUT} fall time	-	-	50	ns	---
V_{PSEN}	HV_{OUT} current source sense voltage	V_{PP1} -0.75	V_{PP1} -1.00	V_{PP1} -1.25	V	---
		V_{PP1} -0.67	-	V_{PP1} -1.31		T_A = -40°C to +85°C
V_{NSEN}	HV_{OUT} current sink sense voltage	V_{NN1} +0.75	V_{NN1} +1.00	V_{NN1} +1.25	V	---
		V_{NN1} +0.65	-	V_{NN1} +1.33		T_A = -40°C to +85°C
t_{SHORTP}	HV_{OUT} off time when current source sense is activated	-	-	100	ns	---
t_{SHORTN}	HV_{OUT} off time when current sink sense is activated	-	-	100	ns	---

Operational Amplifier 1, 2, and 3

V_{OS}	Input offset voltage	-	-	5.0	mV	---
I_{IN}	Input bias current	-	-	500	nA	---
V_{IN}	Input voltage range	1.0	-	V_{DD2} -1	V	---
V_{OUT}	Output voltage swing	0.5	-	V_{DD2} -1	V	---
I_{SOURCE}	Output source current	-	-	3.0	mA	---
I_{SINK}	Output sink current	-	-	-2.75	mA	---
A_O	DC open loop gain	70	85	-	dB	---
BW	Bandwidth	100	-	-	KHz	---
SR	Output slew rate	0.3	-	-	V/µs	---

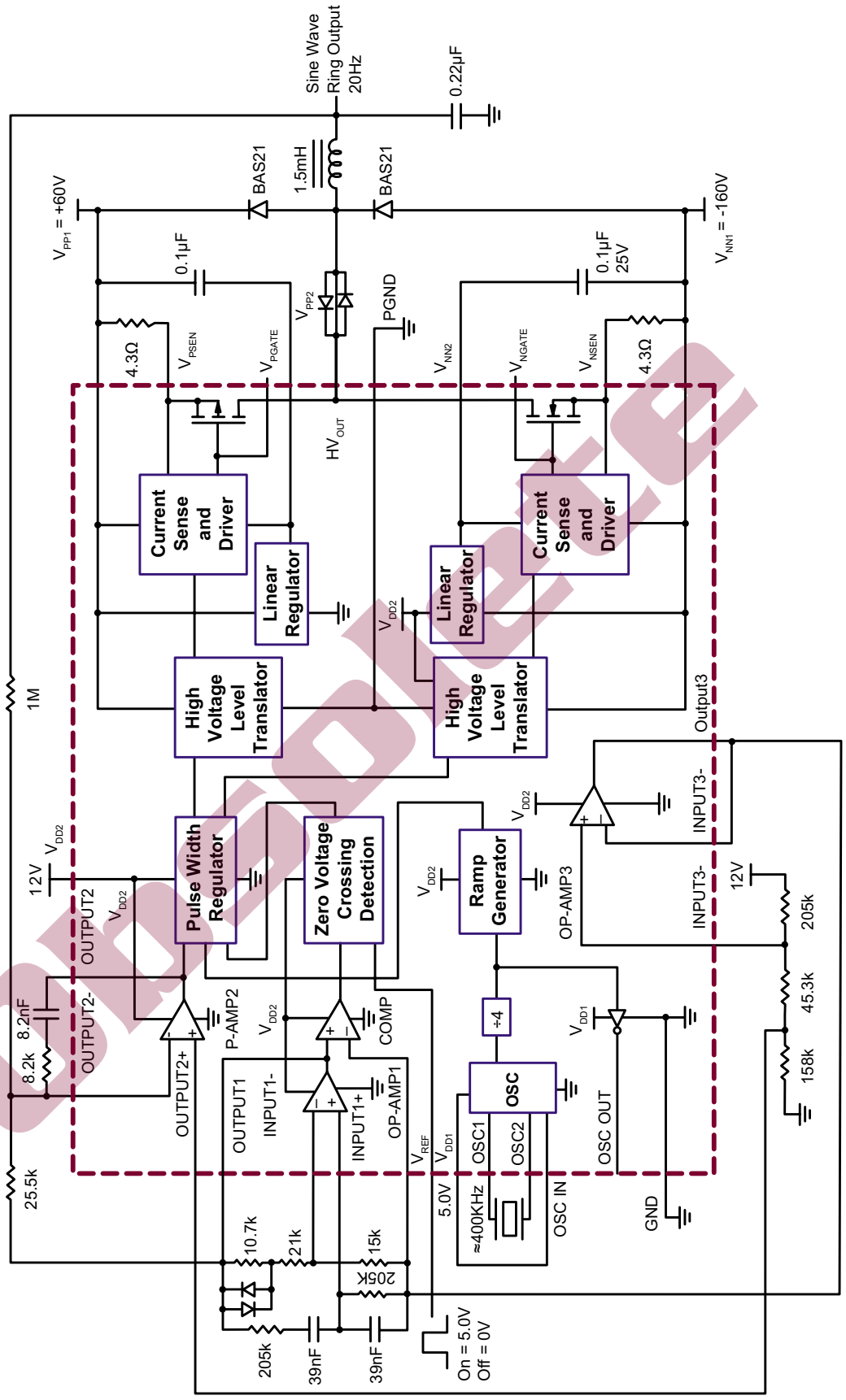
Comparator

V_{OS}	Input offset voltage	-	-	4.0	mV	---
I_{IN}	Input bias current	-	-	500	nA	---
V_{IN}	Input voltage range	-	-	V_{DD2} -2.0	V	---
A_V	Voltage gain	80	-	-	dB	---
t_{RES}	Response time	-	80	-	ns	---

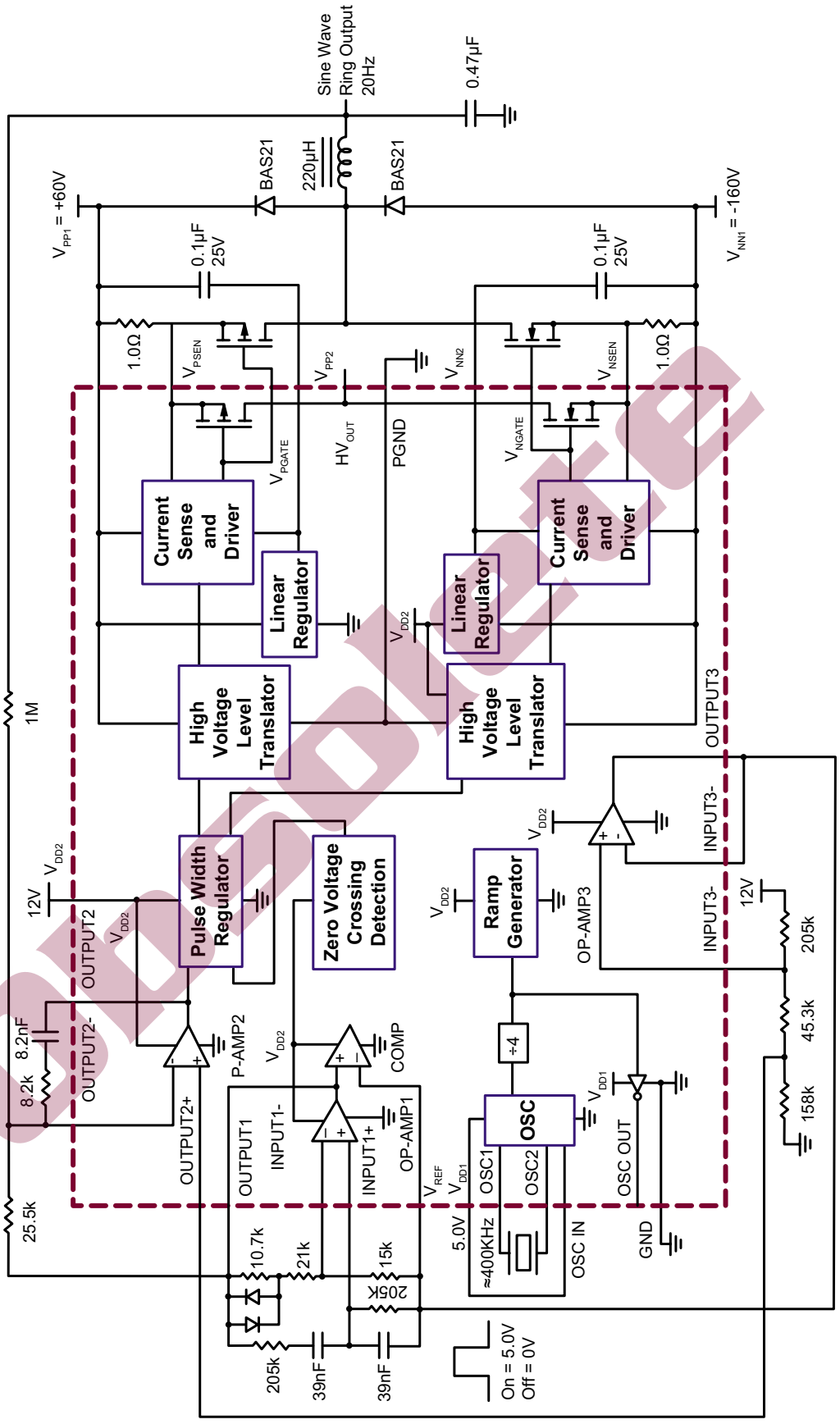
Oscillator

V_{OSC1}	Input voltage range for OSC1	0	-	V_{DD2}	V	---
V_{OSC2}	Input voltage range for OSC2	0	-	V_{DD2}	V	---
$V_{OSC(IN)}$	Input voltage range for OSC IN	0	-	V_{DD1}	V	---
$V_{OSC(OUT)}$	Input voltage range for OSC OUT	-	-	V_{DD1}	V	---
$f_{OSC(OUT)}$	Output frequency of OSC OUT	-	-	120	KHz	f_{OSC1} = 480KHz

Typical 5 REN Application Circuit



Typical 20 REN Application Circuit



Pin Description

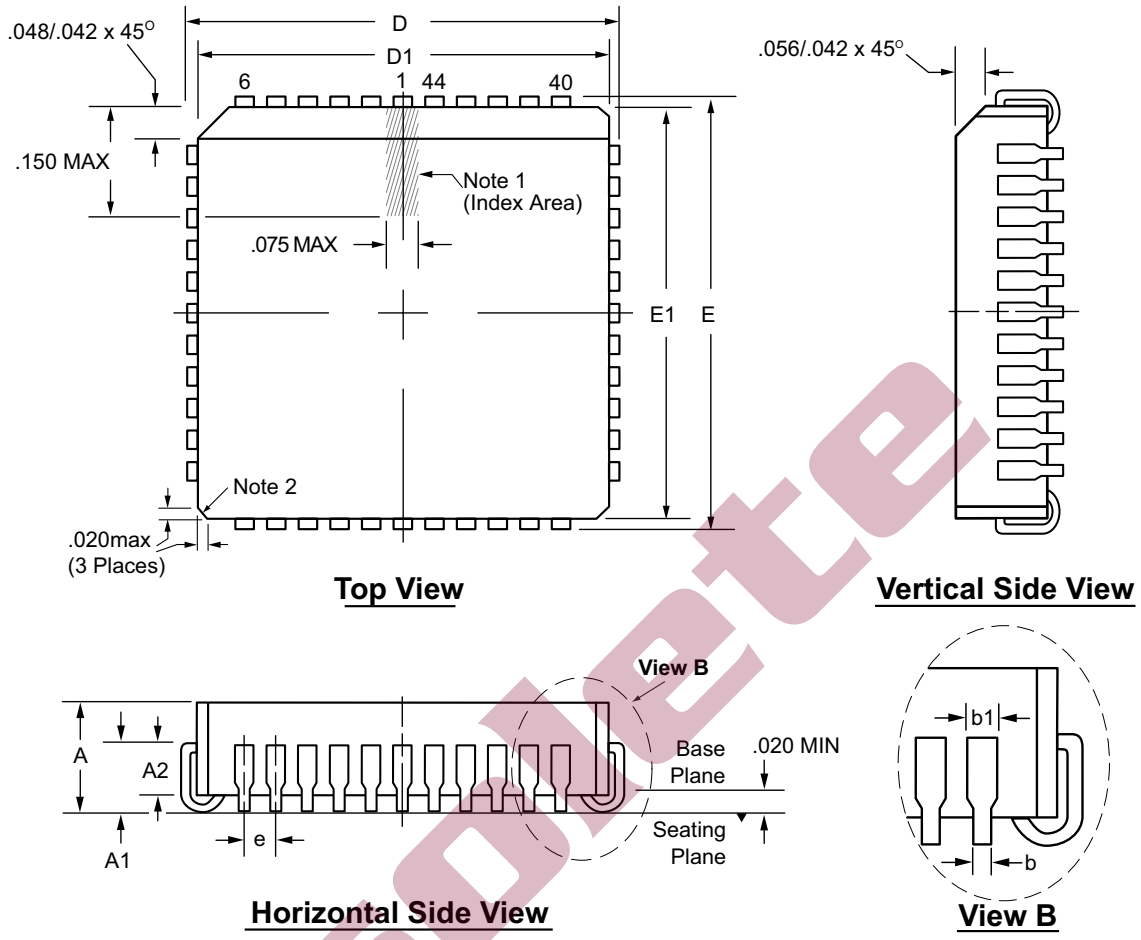
Pin	Name	Description
1	N/C	No connect.
2		
3		
4	VREF	External input reference voltage for zero crossing detection.
5	N/C	No connect.
6	VDD2	+12V supply for analog/logic circuit.
7	N/C	No connect.
8	VDD1	+3.3V to 5.0V supply for input and output logic.
9	OSC1	Input 1 for external resonator. Connect to GND when not in use.
10	OSC2	Input 2 for external resonator. Leave floating when not in use.
11	OSC(IN)	External oscillator input. Zero to VDD1 input signal. Connect to VDD1 when not in use.
12	OSC(OUT)	Oscillator output; 1/4 frequency of external resonator. 50% duty cycle.
13	ON/OFF	Enables/Disables HVOUT.
14	N/C	No connect.
15		
16		
17	VNN1	Negative high voltage supply.
18	N/C	No connect.
19	VNN2	Negative gate voltage supply. Generated by an internal linear regulator.
20	NGATE	Gate drive for external N-channel MOSFET.
21	VNSEN	Pulse by pulse over current sensing for internal N-Channel MOSFET.
22	N/C	No connect.
23	HVOUT	High voltage output. Voltage swings from VPP1 to VNN1.
24	N/C	No connect.
25	VPSEN	Pulse by pulse over current sensing for internal P-Channel MOSFET.
26	PGATE	Gate drive for external P-channel MOSFET.
27	VPP2	Positive gate voltage supply. Generated by an internal linear regulator.
28	N/C	No connect.
29	VPP1	Positive high voltage supply.
30	N/C	No connect.
31		
32		
33	PGND	High voltage power ground.
34	GND	Low voltage ground.
35	OUTPUT2	Output of OP-AMP 2.

Pin Description *(cont.)*

Pin	Name	Description
36	INPUT2-	Inverting input of OP-AMP 2.
37	INPUT2+	Noninverting input of OP-AMP 2.
38	OUTPUT1	Output of OP-AMP 1.
39	INPUT1-	Inverting input of OP-AMP 1.
40	INPUT1+	Noninverting input of OP-AMPp 1.
41	OUTPUT3	Output of OP-AMP 3.
42	INPUT3-	Inverting input of OP-AMP 3.
43	INPUT3+	Noninverting input of OP-AMP 3.
44	N/C	No connect.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656	

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version E041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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