PC-66 SYNCHRONOUS DRAM SMALL OUTLINE DIMM

64415ASWM4G05TWE 144 Pin 4Mx64 SDRAM SODIMM
(Formerly 64415ASWM4G05TC)
Unbuffered, 4k Refresh, 3.3V with SPD

General Description

The module is a 4Mx64 bit, 5 chip, 144 Pin SODIMM module consisting of (4) 1Mx16x4 (TSOP) SDRAM and (1) 256x8 EEPROM for serial presence detect. The module conforms to PC-66 specifications, is unbuffered, and has byte data masks.

Features

- JEDEC-Standard 144-pin Small Outline Dual Inline Memory Module (SODIMM)
- Non-buffered
- Based on 4Mx16 SDRAM Components
- Power Supply: 3.3V ± 0.3V
- 64ms, 4096-cycle refresh
- Serial Presence Detect (SPD)
- LVTTL Compatible Inputs and Outputs
- One External Bank
- Four Internal Banks
- Pure Power and Ground Planes
- Gold PCB connector

Pin Assignment

Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
1	Vss	37	DQ8	73	NC	109	A9
2	Vss	38	DQ40	74	CK1	110	BA1
3	DQ0	39	DQ9	75	Vss	111	A10/AP
4	DQ32	40	DQ41	76	Vss	112	A11
5	DQ1	41	DQ10	77	NC	113	Vcc
6	DQ33	42	DQ42	78	NC	114	Vcc
7	DQ2	43	DQ11	79	NC	115	DQMB2
8	DQ34	44	DQ43	80	NC	116	DQMB6
9	DQ3	45	Vcc	81	Vcc	117	DQMB3
10	DQ35	46	Vcc	82	Vcc	118	DQMB7
11	Vcc	47	DQ12	83	DQ16	119	Vss
12	Vcc	48	DQ44	84	DQ48	120	Vss
13	DQ4	49	DQ13	85	DQ17	121	DQ24
14	DQ36	50	DQ45	86	DQ49	122	DQ56
15	DQ5	51	DQ14	87	DQ18	123	DQ25
16	DQ37	52	DQ46	88	DQ50	124	DQ57
17	DQ6	53	DQ15	89	DQ19	125	DQ26
18	DQ38	54	DQ47	90	DQ51	126	DQ58
19	DQ7	55	Vss	91	Vss	127	DQ27
20	DQ39	56	Vss	92	Vss	128	DQ59
21	Vss	57	NC	93	DQ20	129	Vcc
22	Vss	58	NC	94	DQ52	130	Vcc
23	DQMB0	59	NC	95	DQ21	131	DQ28
24	DQMB4	60	NC	96	DQ53	132	DQ60
25	DQMB1	61	CK0	97	DQ22	133	DQ29
26	DQMB5	62	CKE0	98	DQ54	134	DQ61
27	Vcc	63	Vcc	99	DQ23	135	DQ30
28	Vcc	64	Vcc	100	DQ55	136	DQ62
29	A0	65	RAS*	101	Vcc	137	DQ31
30	A3	66	CAS*	102	Vcc	138	DQ63
31	A1	67	WE*	103	A6	139	Vss
32	A4	68	CKE1	104	A7	140	Vss
33	A2	69	S0*	105	A8	141	SDA
34	A5	70	NC	106	BA0	142	SCL
35	Vss	71	S1*	107	Vss	143	Vcc
36	Vss	72	NC	108	Vss	144	Vcc

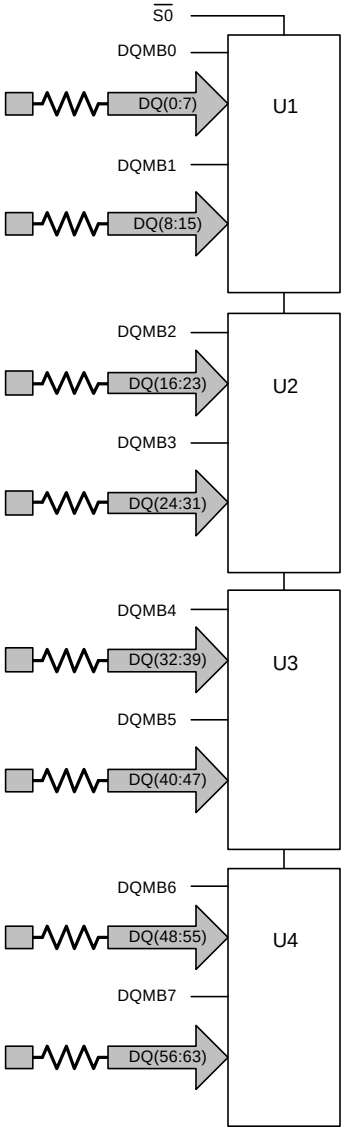
* Active Low

Valid Part Numbers

Part Number	Bus Speed	CAS Latency
64415ASWM4G05TWE	66Mhz	CL2

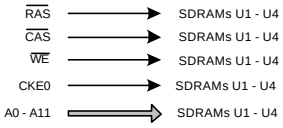
Block Diagram

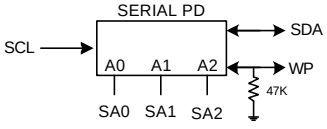
X64 SDRAM SODIMM, 1BANK with X16 SDRAMs



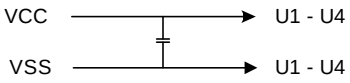
*CLOCK WIRING	
CLOCK INPUT	SDRAM
*CK0	4 SDRAM
*CK1	TERMINATION
*CK2	TERMINATION
*CK3	TERMINATION

*** wire per Clock loading Table/Wiring diagrams.**





Bypass:
Four 0.22uF capacitor per SDRAMs device.



Pin Descriptions

Pin	Name	Function
CLK#	System Clock	All input signals are sampled on the rising edge of clock.
S#	Chip Select	Enables and disables the command decoder. All commands are disabled when S# is high.
CKE	Clock Enable	Masks system clock to freeze current operation on the next clock cycle, also provides access to standby mode (see truth table).
A#	Address Lines	Input lines for Row/Column address.
BA#	Bank Select Lines	Selects the internal bank to be accessed during a row or column address latch.
RAS	Row Address Strobe	Latches the row address on the rising edge of clock when asserted.
CAS	Column Address Strobe	Latches the column address on the rising edge of clock when asserted.
WE	Write Enable	Enables write operation and row Precharge.
DQMB0-DQMB7	Data Masks	Provides a byte mask for write operations and a byte enable for read operations.
DQ0-DQ63	Data Lines	Data input/output lines.
Vdd	Power Supply	Power Supply 3.3V±0.3V
Vss	Ground	Ground
SDA, SCL	SPD Data/Clock Lines	Serial Presence Detect (SPD) EEPROM bus lines. This line provides bi-directional data transfer over an I^2C bus.
NC	No Connection	Line is not connected in DIMM.

Byte #	Function	Hex MS-LS	Description
0	Define # of bytes written into EEPROM	**80**	128
1	Total # of bytes of SPD memory device	**08**	256
2	Fundamental memory type (EDO, SDRAM...)	**04**	SDRAM
3	# of row addresses	**0C**	12
4	# of column addresses	**08**	8
5	# of module rows	**01**	1
6	Data width...	**40**	64
7	...Data width continued	**00**	00
8	Voltage interface	**01**	LVTTL
9	SDRAM cycle time	**A0**	10ns
10	SDRAM access from clock	**80**	8ns
11	DIMM configuration type (non-parity, ECC…)	**00**	non-parity
12	Refresh rate/type	**80**	Normal/Self
13	Primary SDRAM width	**10**	16
14	Error checking SDRAM width	**00**	0
15	Minimum clock delay back to back random column address	**01**	1
16	Burst lengths supported	**8F**	page/8/4/2/1
17	# of banks on each SDRAM device	**04**	4
18	CAS# latencies supported	**06**	3/2
19	CS# latency	**01**	CS latency=0
20	Write latency	**01**	WE latency=0
21	SDRAM module attributes	**00**	Unbuffered
22	SDRAM device attributes: general	**0E**	Write1/Read burst/Precharge
23	Min SDRAM cycle time at CL X-1	**90**	9ns
24	SDRAM access from clock at CL X-1	**80**	8ns
25	Min SDRAM cycle time at CL X-2	**00**	00
26	Max SDRAM access from clock at CL X-2	**00**	00
27	Min row Precharge time	**1A**	26ns
28	Min row active to row active	**14**	20ns
29	Min RAS to CAS delay	**1A**	26ns
30	Minimum RAS pulse width	**32**	50ns
31	Density of each row on module	**08**	32M
32-61	Superset information (may be used in future)	**00**	00
62	SPD data revision code	**12**	1.2
63	Checksum for bytes 0-62	**XX**	XX
64-125	Manufacturer's infomation	**00**	Not written
126	Intel specification frequency	**66**	66Mhz
127	Intel specification CAS# latency support	**06**	CAS latency 2
128-255	Unused storage locations	**00**	Not written

NOTE: 1. x = Variable Data.

Simplified Truth Table

Command			CKEn-1	CKEn	S*	RAS*	CAS*	WE*	DQM	BA0,1	A10/AP	A11 A9-A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP Code			1
Refresh	Auto refresh		H	H	L	L	L	H	X	X			
		Entry		L									
	Self Refresh	Exit	L	H	H	X	X	X	X	X			
					L	H	H	H					
Bank active & row address			H	X	L	L	H	H	X	V	Row Address		
Read & column address	Auto Precharge disable		H	X	L	H	L	H	X	V	L	Column addr (A0-A7)	2
	Auto Precharge enable										H		
Write & column address	Auto Precharge disable		H	X	L	H	L	L	X	V	L	Column addr (A0-A7)	2
	Auto Precharge enable										H		
Burst stop			H	X	L	H	H	L	X	X			
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend Mode or active power down		Entry	H	L	X	X	X	X	X	X			
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			3
No operation command			H	X	L	H	H	H	X	X			

(V=Valid, X=don't care, H=Logic High, L=Logic Low)

Notes:

1. MRS can be issued only in idle state.
2. A burst read or write with auto Precharge cannot be interrupted. New commands can be issued t_{RP} after the end of the burst.
3. DQM sampled on positive clock edge results in Hi-Z within 2 cycles, however data is immediately invalid and should be ignored.

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V_{in}	-1.0 to 4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	Pt	3.2832	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{st}	-55 to +125	°C

NOTE: Permanent damage may occur if absolute maximum ratings are exceeded.
Device should be operated within recommended operating conditions only.

DC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units	Note
Supply voltage	Vss	0	0	0	V	
Supply voltage	Vcc	3.0	3.3	3.6	V	
Input high voltage	Vih	2.0	-	Vcc+0.3	V	1
Input low voltage	Vil	-	-	0.8	V	2
Output high voltage	Voh	2.4	-	-	V	Ioh=-2mA
Output low voltage	Vol	-	-	0.4	V	Iol=2mA

DC Current Consumption (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	PC-66	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC(min)}$, I_O= 0 mA	456	mA	4
Precharge standby current in power down mode	I_{CC2P}	CKE0 ≤ V_{IL} (max), t_{CK} = min	9.6	mA	5
	I_{CC2PS}	CKE0,CKE1 ≤ V_{IL} (max), t_{CK} = ∞	9.6		
Precharge standby current in non-power down mode	I_{CC2N}	CKE0,CKE1 ≥ V_{IH} (min), t_{CK} = min, S0*-S3*= V_{IH} (min) Input signals are changed once during 2 clock cycles	168		5
	I_{CC2NS}	CKE0,CKE1 ≥ V_{IH} (min), CK0 ≤ V_{IL} (max), t_{CK} = ∞ Input signals are stable	168	mA	
Active standby current in non-power down mode	I_{CC3N}	CKE0 ≥ V_{IH} (min), t_{CK} = min, S0*-S3*= V_{IH} (min) Input signals are changed once during 2 clock cycles	168	mA	5
	I_{CC3NS}	CKE0 ≥ V_{IH} (min), CK0 ≤ V_{IL} (max), t_{CK} = ∞ Input signals are stable	168		
Burst Operating Current	I_{CC4}	I_O = 0 mA, Page Burst, multiple banks active, t_{CCD} = 2CLK	576	mA	4
Refresh Current	I_{CC5}	t_{CK} = min , $t_{RC} \geq t_{RC(min)}$	912	mA	
Self Refresh Current	I_{CC6}	CKE0 ≤ 0.2 V	4	mA	5

CL : CAS Latency

Capacitance (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	Typ	Max	Units	Note
Input capacitance (Am, BA0,CKEm)	C_{I1}	-	15.2	pF	
Input capacitance (DQMBm)	C_{I2}	-	3.8	pF	
Input capacitance (CAS*, RAS*, WE*)	C_{I3}	-	15.2	pF	
Input capacitance (CKm)	C_{I4}	-	25	pF	
Input capacitance (SDA,SCL,SAm)		-	10	pF	
Input/Output capacitance (DQm,CBm)	$C_{I/O}$	-	6	pF	

AC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	PC-66		Units	Note
		Min	Max		
CLK Cycle time (CL =3)	t_{CK}	10	1000	ns	6,7
CLK Cycle time (CL =2)	t_{CK}	15	1000	ns	6,7
CLK Cycle time (CL =1)	t_{CK}	30	1000	ns	6,7
CLK to valid output delay (CL =3)	t_{AC}	-	8	ns	6,7
CLK to valid output delay (CL =2)	t_{AC}	-	12	ns	6.7
CLK to valid output delay (CL =1)	t_{AC}	-	27	ns	6.7
Output data hold time	t_{OH}	3	-	ns	7
Output valid to High-Z	t_{HZ}	3	-	ns	7
CLK high pulse width	t_{CH}	3	-	ns	7
CLK low pulse width	t_{CL}	3	-	ns	7
Command setup time	t_{CMS}	3	-	ns	7
Address setup time	t_{AS}	3	-	ns	7
Clock enable setup time	t_{CKS}	3	-	ns	7
Data input setup time	t_{DS}	3	-	ns	7
Command hold time	t_{CMH}	1	-	ns	7
Address hold time	t_{AH}	1	-	ns	7
Clock enable hold time	t_{CKH}	1	-	ns	7
Data input hold time	t_{DH}	1	-	ns	7
Power down exit setup time	t_{PDE}	1	-	ns	7,8
CLK to output in Low-Z	t_{LZ}	1	-	ns	7
Row active to Row active delay	$t_{RRD\ (min)}$	20	-	ns	6
RAS* to CAS* delay	$t_{RCD\ (min)}$	20	-	ns	6
Row Precharge time	$t_{RP\ (min)}$	20	-	ns	6
Row active time	$t_{RAS\ (min)}$	50	-	ns	6
Row active time	$t_{RAS\ (max)}$	8	-	us	
Row cycle time	$t_{RC\ (min)}$	70	-	ns	6
Mode Register set to Active Delay	$t_{RSC\ (min)}$	30	-	ns	

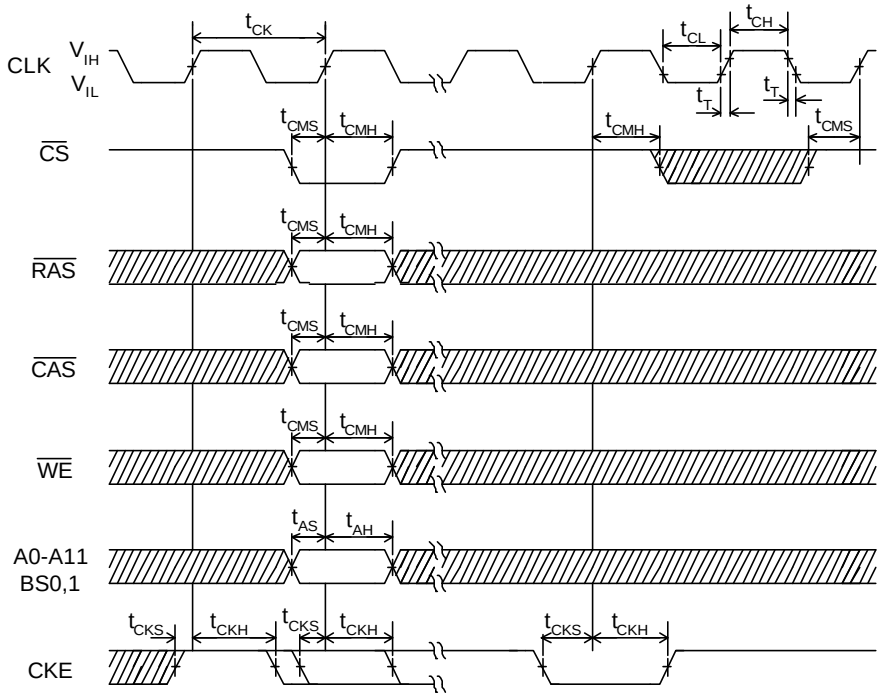
CL : CAS Latency

Notes:

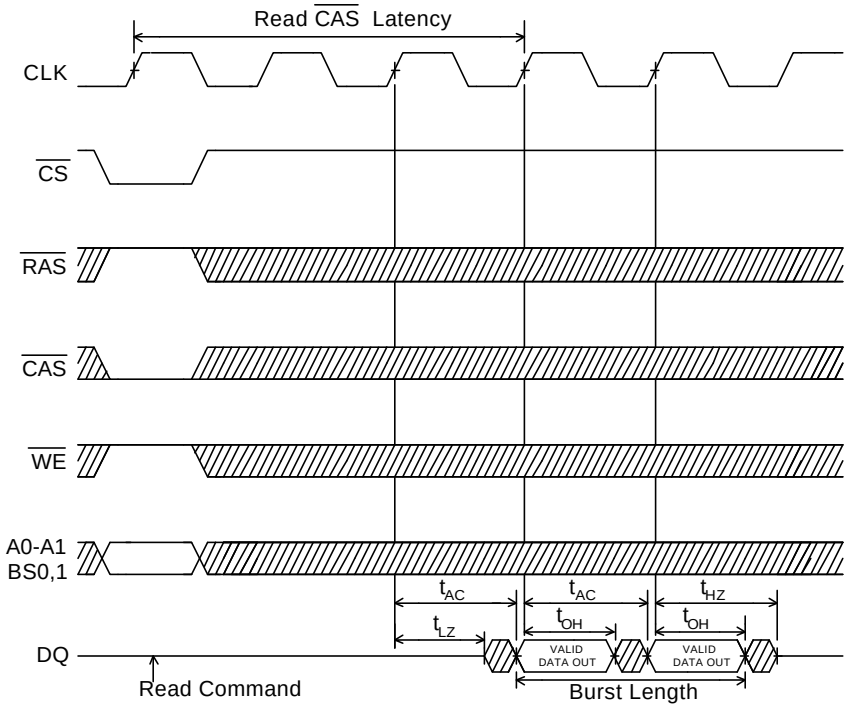
1. Overshoot: $Vih_{(MAX)}$ = Vdd + 2.0V for ≤3ns
2. Undershoot: $Vil_{(MIN)}$ = Vss – 2.0V for ≤3ns
3. Typical peak current consumption.
4. Measured with outputs open.
5. Assumes minimum column address update cycle: t_{CCD} (min).
6. Parameters depend on programmed CAS Latency.
7. Assumed input rise and fall time=1ns.
8. A time of t_{PDE} has to elapse after asserting CKE to resume normal operation when exiting power down mode.

Timings listed are for discrete SDRAM components.

Command Input Timing

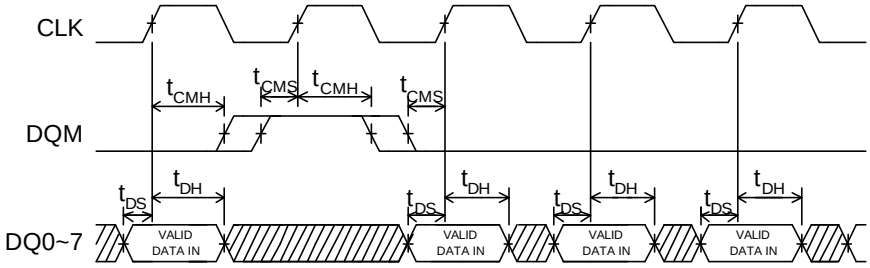


Read Timing

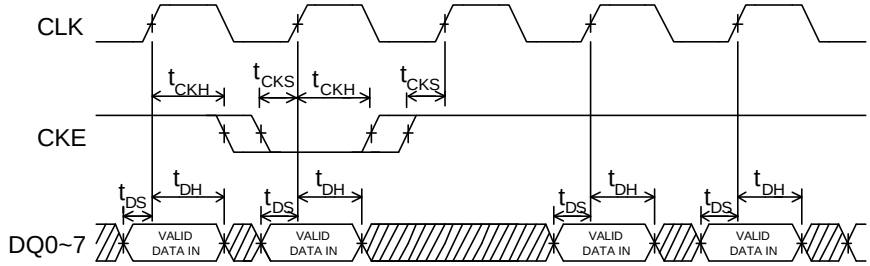


Control Timing of Input Data

(Word Mask)

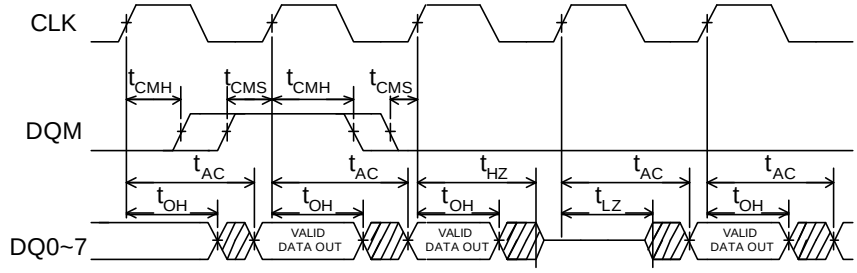


(Clock Mask)

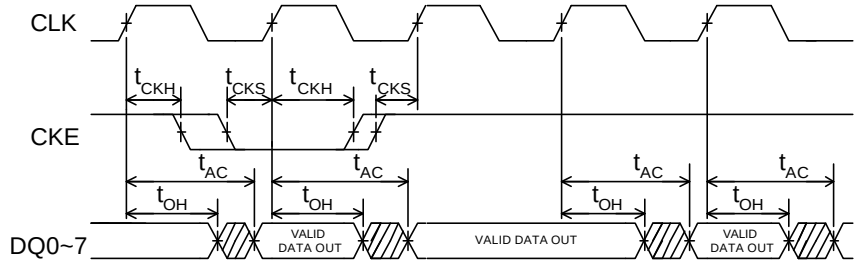


Control Timing of Output Data

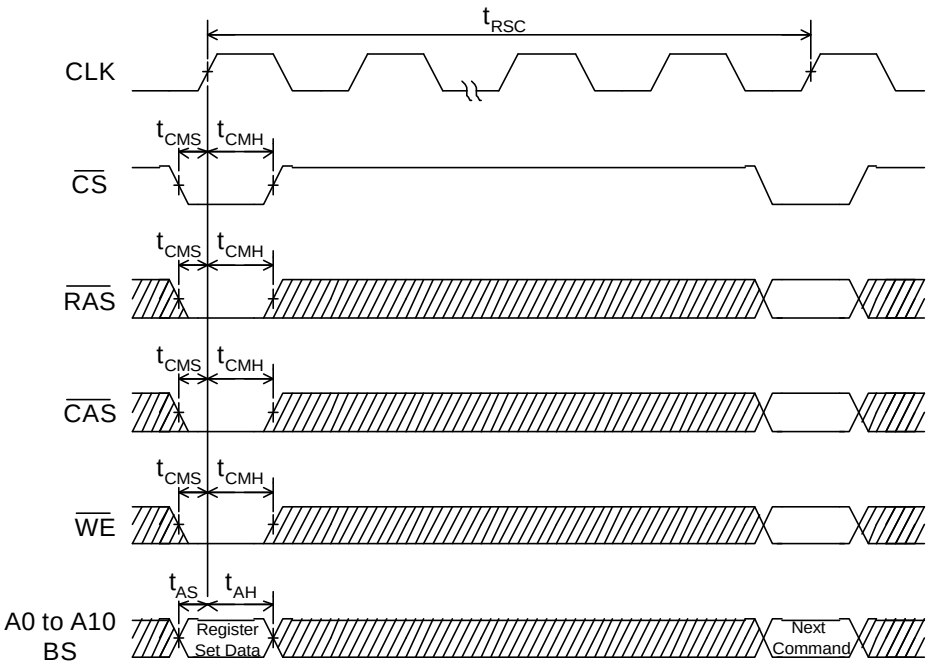
(Output Enable)



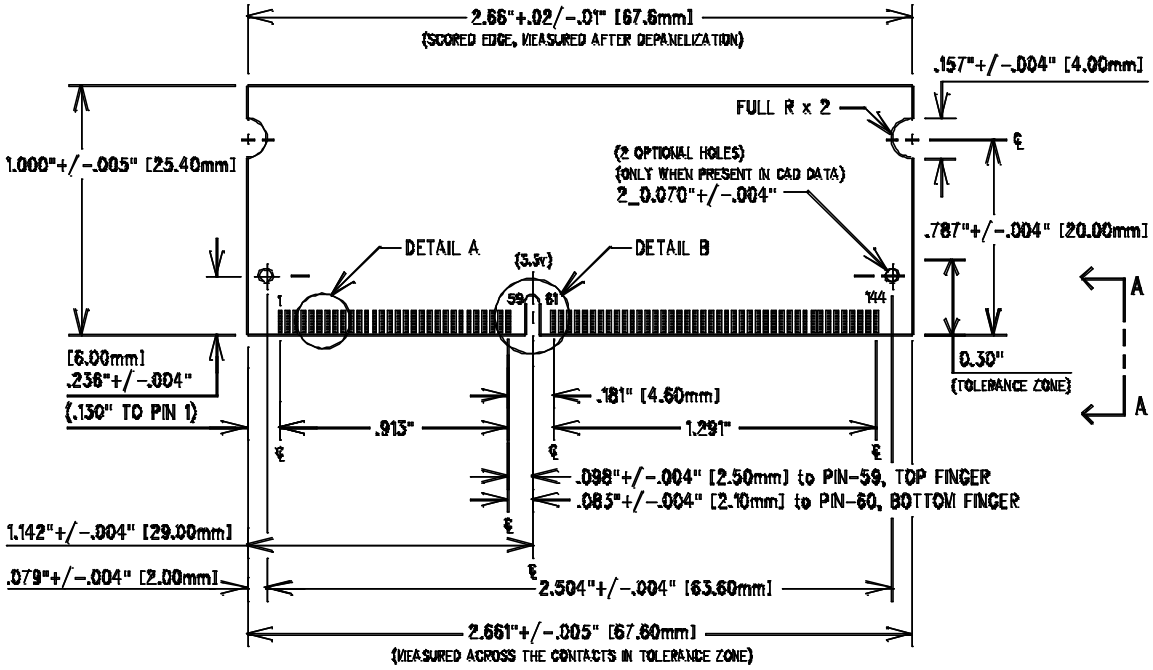
(Clock Mask)

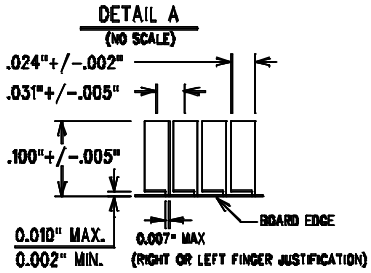


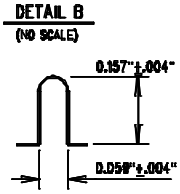
Mode Register Set Cycle

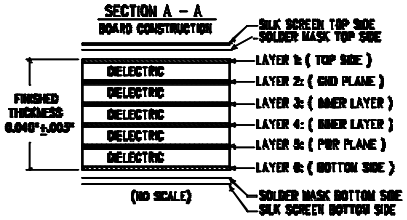


OUTLINE DRAWING









SIDE VIEW