HD-4702

CMOS Programmable Bit Rate Generator

DS Datasheets, Related Docs & Simulations	■ Description	Key Features	PT Parametric Data	● Application Diagrams	⊞ Related Devices

Ordering Information

Pb Available in RoHS/PbFree

Buy direct from Intersil	Check distributor inventory		Request samples		

Part No.	Design-In Status	Temp.	Package	MSL	Price US $ Pb
5962-9051801MEA	Active	Mil		N/A	30.99
HD3-4702-9	Active	Ind	16 Ld PDIP	N/A	6.77
HD3-4702-9Z	Active	Ind	16 Ld PDIP	N/A	6.77 ✔

The price listed is the manufacturer's suggested retail price for quantities between 100 and 999 units. However, prices in today's market are fluid and may change without notice.

MSL = Moisture Sensitivity Level - per IPC/JEDEC J-STD-020
SMD = Standard Microcircuit Drawing

■ Description

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency. The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q0, Q1, Q2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

The four rate select inputs (S0 -S3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD -4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD". The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD -4702, which is easily achieved with a single 5 -position switch.

The HD-4702 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the ECP input goes low. When ECP is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Clock Modes and Initialization below.

Key Features

- HD-4702 Provides 13 Commonly Used Bit Rates
- Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)
- Low Power Dissipation
- Conforms to EIA RS-404
- One HD-4702 Controls up to Eight Transmission Channels
- Initialization Circuit Facilitates Diagnostic Fault Isolation
- On-Chip Input Pull -Up Circuit

Related Documentation

DS Datasheet(s):
- CMOS Programmable Bit Rate Generator

TH Technical Homepage:
- Digital ICs

PT Parametric Data

Features	Low Power Dissipation Conforms to EIA RS-404 One HD-4702 Controls up to Eight Transmission Channels Initialization Circuit Facilitates Diagnostic Fault Isolation On-Chip Input Pull -Up Circuit
Data Frame Length	N/A
Data Rate	N/A

● Application Block Diagrams

- Avionics

⊞ Related Devices

PT Parametric Table

HD-15530	CMOS Manchester Encoder-Decoder
HD-15531	CMOS Manchester Encoder-Decoder
HD-6408	CMOS Asynchronous Serial Manchester Adapter (ASMA)
HD-6409	CMOS Manchester Encoder-Decoder
HS-3182	ARINC 429 Bus Interface Line Driver Circuit
HS-3282	CMOS ARINC Bus Interface Circuit

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