3.3V LVDS High-Speed Differential Line Driver and Receiver

Features

- Signaling Rates >660 Mbps (330 MHz)
- Single 3.3V Power Supply Design
- Driver:
  — ±350mV Differential Swing into a 100-ohm load
  — Propogation Delay of 1.5ns Typ.
  — Low Voltage TTL (LVTTL) Inputs are 5V Tolerant
- Receiver:
  — Accepts ±50mV (min.) Differential Swing with up to 2.0V ground potential difference
  — Propagation Delay of 3.3ns Typ.
  — Low Voltage TTL (LVTTL) Outputs
  — Open, Short, and Terminated Fail Safe
- Industrial Temperature Operating Range: –40°C to 85°C
- Meets or Exceeds IEEE 1596.3 SCI Standard
- Meets or Exceeds ANSI/TIA/EIA-644 LVDS Standard
- Bus-Terminal ESD exceeds 12kV
- Packaging (Pb-free & Green available):
  — 8-pin SOIC or MSOP

Description

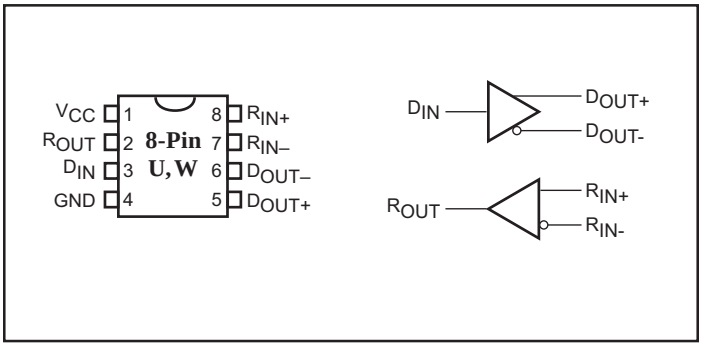
The PI90LV179is a differential line driver and receiver (transceiver) that is compliant with the IEEE 1596.3 SCI and ANSI/TIA/EIA-644 LVDS standards. This device uses low-voltage differential signaling (LVDS) to achieve data rates in excess of 660 Mbps while being less susceptible to noise than single-ended transmission.

The driver translates a low-voltage TTL/CMOS input into a low-voltage (350mV typical) differential output signal. The receiver translates a differential 350mV input signal to a 3V CMOS output level.

Applications

Applications include point-to-point and multidrop baseband data transmission over a controlled impedance media of approximately 100 ohms. These include intra-system connections via printed circuit board traces or cables, hubs and routers for data communications; PBXs, switches, repeaters and base stations for telecommunications and other applications such as digital cameras, printers and copiers.

PI90LV179



Function Tables

PI90LV179 Receiver

Inputs	Output
$V_{ID} = V_{RIN+} - V_{RIN-}$	R_{OUT}
$V_{ID} \geq 50mV$	H
$-50mV < V_{ID} < 50mV$	?
$V_{ID} \leq -50mV$	L
open	H

PI90LV179 Driver

Input	Output	
D_{IN}	D_{OUT+}	D_{OUT-}
L	L	H
H	H	L
open	L	H

Notes:
H = High Level, L = Low Level, ? = Indeterminate,
Z = High-Impedance, X = Don't Care

Pin Descriptions

Name	Description
D_{IN}	TTL/CMOS driver input pins
$D_{OUT}+$	Non-inverting driver output pins
$D_{OUT}+$	Inverting driver output pins
R_{OUT}	TTL/CMOS receiver output pins
$R_{IN}+$	Non-inverting receiver input pins
R_{IN-}	Inverting receiver input pins
V_{ID}	Input Differential Signal Voltage
GND	Ground pin
V_{CC}	Positive power supply pin, +3.3V ±10%

Absolute Maximum Ratings

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Driver
Input Voltage (D_{IN}) ..... –0.3V to (Vcc + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-}) ..... –0.3V to +3.9V
Short Circuit Duration (D_{OUT+}, D_{OUT-}) ..... Continuous
Receiver
Input Voltage (R_{IN+}, R_{IN-}) ..... –0.3V to +3.9V)
Output Voltage (R_{OUT}) ..... –0.3V to (V_{CC} + 0.3V)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range Soldering (4s) ..... +260°C
Maximum Junction Temperature ..... +150°C
ESD Rating ..... >12kV

Recommended Operating Conditions

	Min.	Typ.	Max.	Units
Supply Voltage (V_{CC})	3	3.3	3.6	V
High Level Input Voltage, V_{IH}	2			
Low Level Input Voltage, V_{IL}			0.8	
Magnitude of Differential Input Voltage V_{ID}	0.1		0.6	
Common-mode Input Voltage, V_{IC} (Fig 5)	$\|V_{ID}\|/2$		$2.4 - \|V_{ID}\|/2$	
			$V_{CC} - 0.8$	
Operating Free Air Temperature T_A	–40		85	°C

Electrical Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter	Test Condition	Min.	Typ.†	Max.	Units
I_{CC}* Supply Current	No receiver load, Driver R_L = 100 ohms		8.0	10.8	mA

†All typical values are at 25°C with a 3.3V supply
*I_{CC} measured with all TTL input. $V_{IN} = V_{CC}$ or GND.

Electrical Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter			Test Conditions	Min.	Typ.	Max.	Units
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		R_L = 100 ohms See Figures 1 and 2	247	390	470	mV
$\Delta\lvert V_{OD} \rvert$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125	1.25	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	
I_{IH}	High-level input current	D_{IN}	V_{IH} = 5V		2	20	µA
I_{IL}	Low-level input current	D_{IN}	V_{IL} = 0.8V		2	10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0V		–6	–9	mA
			V_{OD} = 0V		–8	–11	
I_{OZ}	High-impedance output current		V_{OD} = 600mV			±1	µA
			V_O - 0V or V_{CC}			±1	
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0V, V_O = 3.6V			±1	
C_{IN}	Input capacitance				7		pF

Receiver Electrical Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold	See Figures 5 & Table 1			50	mV
V_{ITH-}	Negative-going differential input voltage threshold		–50			
V_{OH}	High-level output voltage	I_{OH} = –8mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA			0.4	V
I_I	Input current (R_{IN+} or R_{IN-})	V_I = 0	–2	–11	–20	µA
		V_I = 2.4V	–1.2	–3		
$I_{I\ (OFF)}$	Power-off input current (R_{IN+} or R_{IN-})	V_{CC} = 0			±20	
I_H	High-level input current (enables)	V_{IH} = 2V			±10	
I_L	Low-level input current (enables)	V_{IL} = 0.8V			±10	
I_{OZ}	High-impedance output current	V_O = 0 or 5V			±10	
C_I	Input capacitance			5		pF

†All typical values are at 25°C with a 3.3V supply

Driver Switching Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Conditions	Min.	Typ.†	Max.	Units
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 ohms C_L = 10pF See Figure 2		1.9	2.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.9	2.5	
t_r	Differential output signal rise time			0.6	1.1	
t_f	Differential output signal fall time			0.6	1.1	
$t_{sk(p)}$	Pulse skew (t_{PHL} - t_{PLH})			270		ps
$t_{sk(pp)}$	Part-part-part skew**				0.9	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 7		2.7	4	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			1.8	4	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.0	4	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			3.0	4	

† All typical values are at 25°C with a 3.3V supply.
** $t_{sk(pp)}$: magnitude of difference in propagation delay times between any specific terminals of two devices (all things being equal).

Receiver Switching Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Conditions	Min.	Typ.†	Max.	Units
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10pF See Figure 6		2.0	3.1	ns
t_{PHL}	Propagation delay time, lhigh-to-low-level output			2.2	3.1	
$t_{sk(pp)}$**	Part-part-part skew**				1.3	
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)			300	500	ps
t_r	Output signal rise time			0.9	1.5	
t_f	Output signal fall time			1.0	1.8	
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 7		1.5	3.1	ns
t_{PZL}	Propagation delay time, low-level-to-low-impedance output			4.0	6.0	
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output			2.5	3.5	
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output			6.0	7.6	

†All typical values are at 25°C with a 3.3V supply
**$t_{sk(pp)}$: magnitude of difference in propagation delay times between any specific terminals of two devices (all things being equal)

Parameter Measurement Information

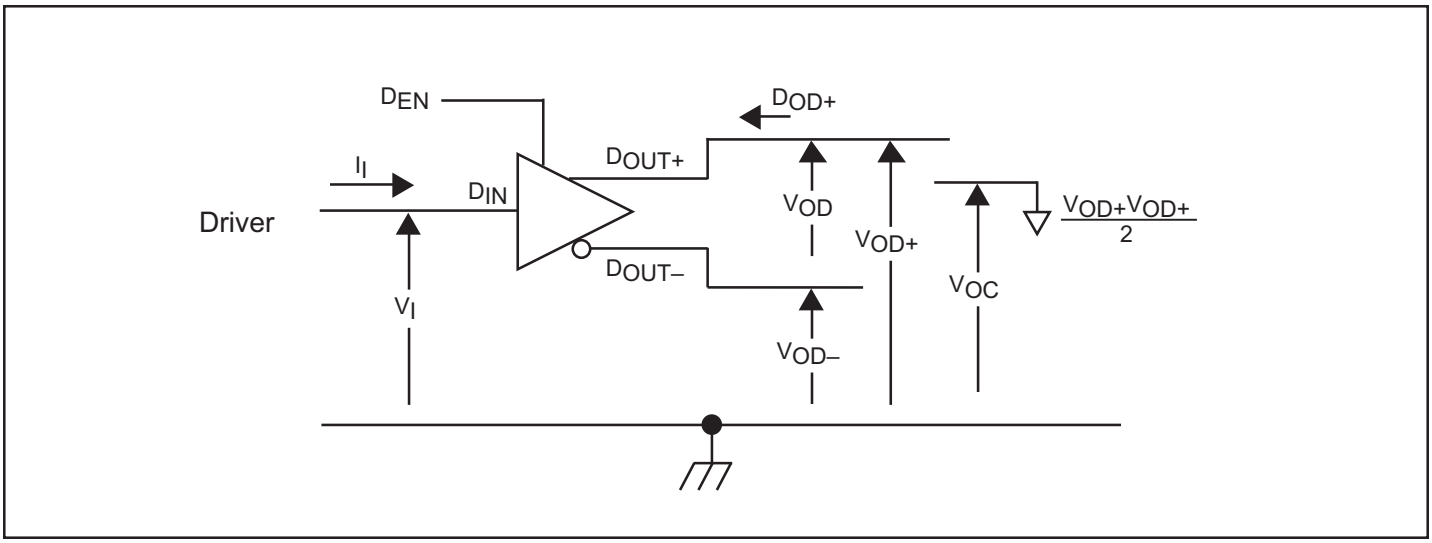
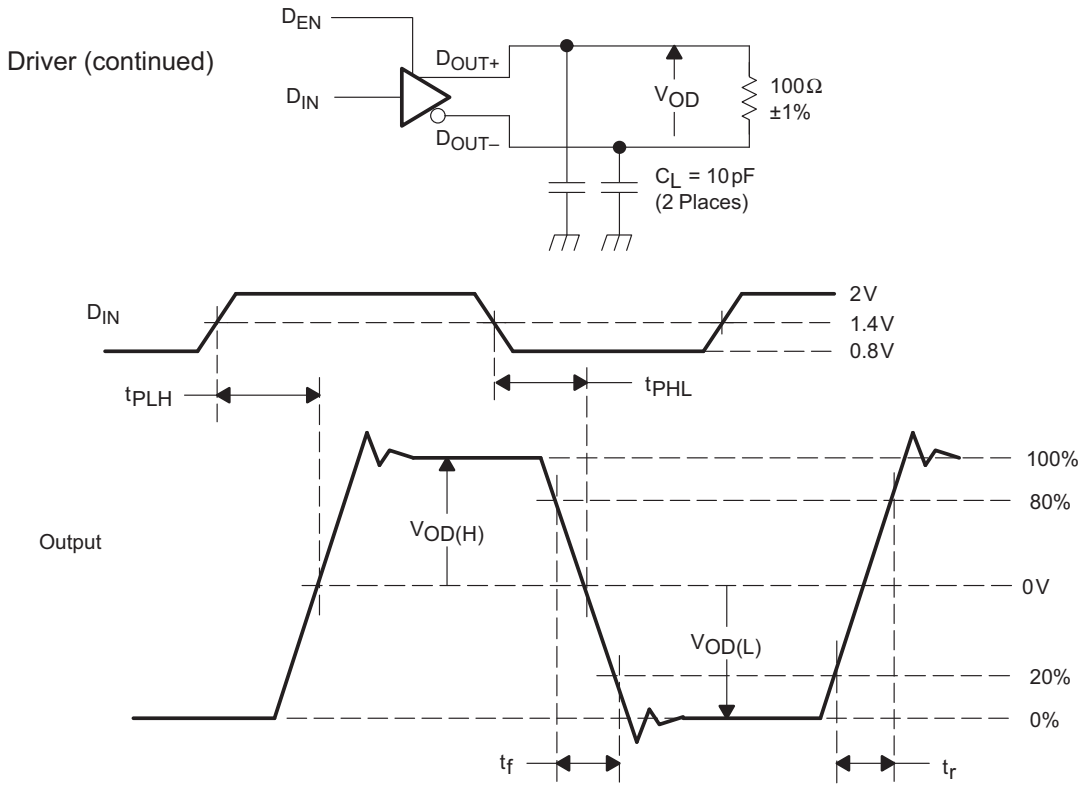


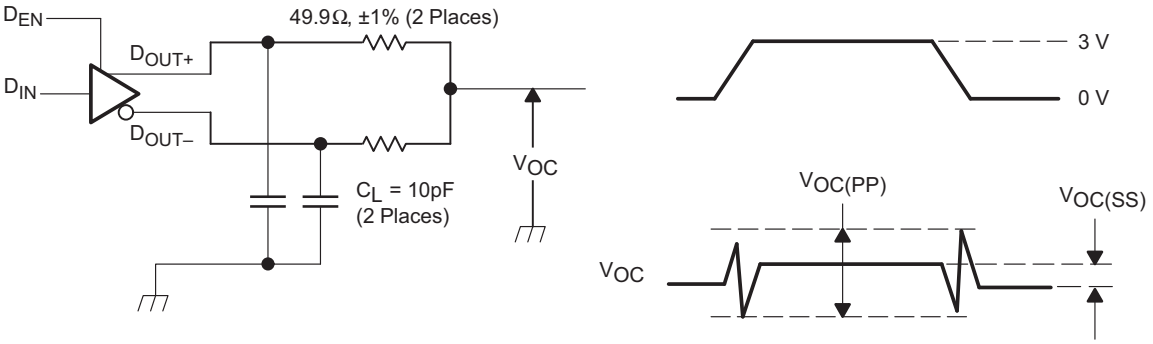
Figure 1. Driver Voltage and Current Definitions

Parameter Measurement Information



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or t_f £ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

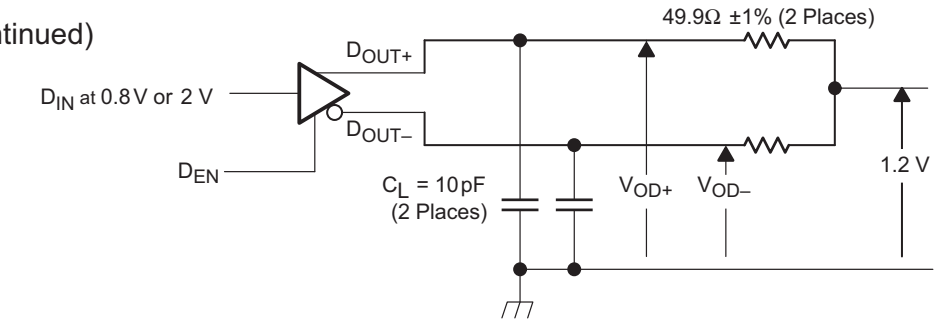


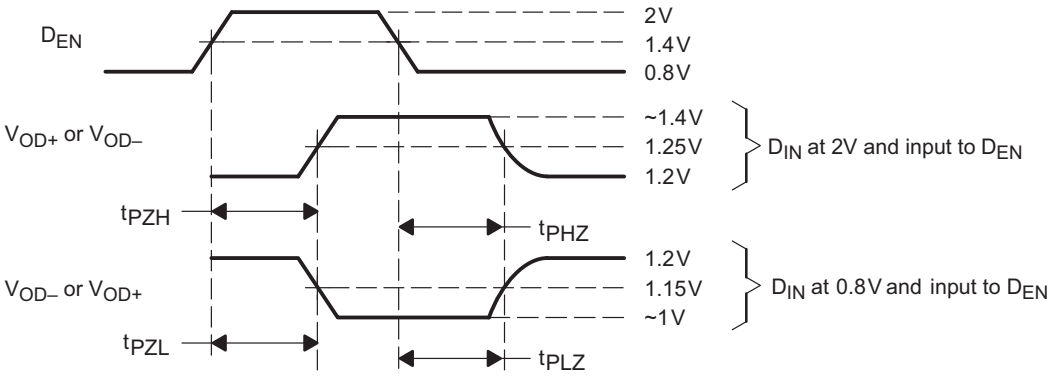
NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or t_f £ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

Parameter Measurement Information (continued)

Driver (continued)





NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or t_f £1ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06mm of the D.U.T.

Figure 4. Enable and Disable Timing Circuit and Definitions

Parameter Measurement Information (continued)

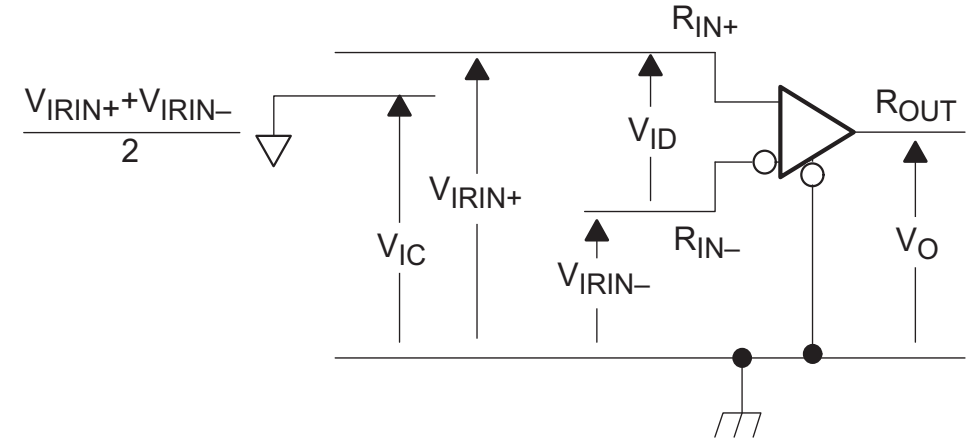


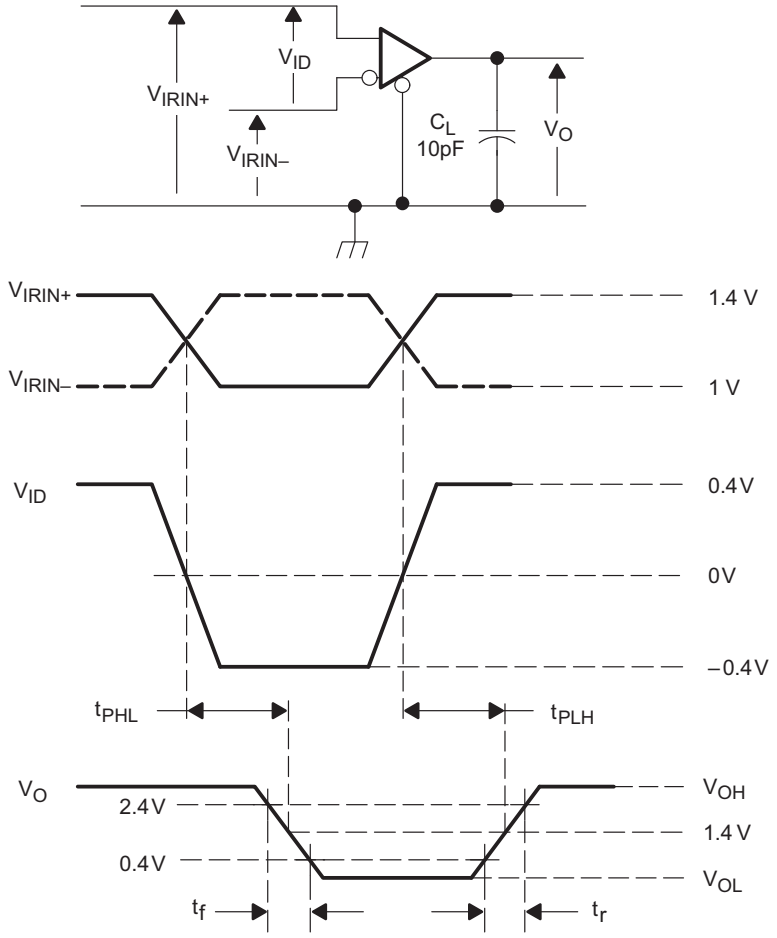
Figure 5. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IRIN+}	V_{IRIN+}	V_{ID}	V_{IC}
1.225	1.175	50	1.2
1.175	1.225	–50	1.2
2.375	2.325	50	2.35
2.325	2.375	–50	2.35
0.1	0	50	0.05
0	0.05	–50	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

Parameter Measurement Information (continued)

Receiver (continued)

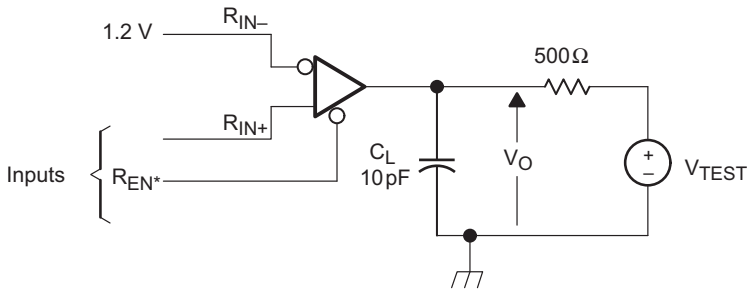


Note A: All input pulses are supplied by a genertor having the following characteristics: t_r or t_f 1ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms

Parameter Measurement Information

Receiver (continued)



NOTE A: All input pulses are supplied by a genertor having the following characteristics: t_r or t_f 1ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse wide = 500 ±10ns. CL includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

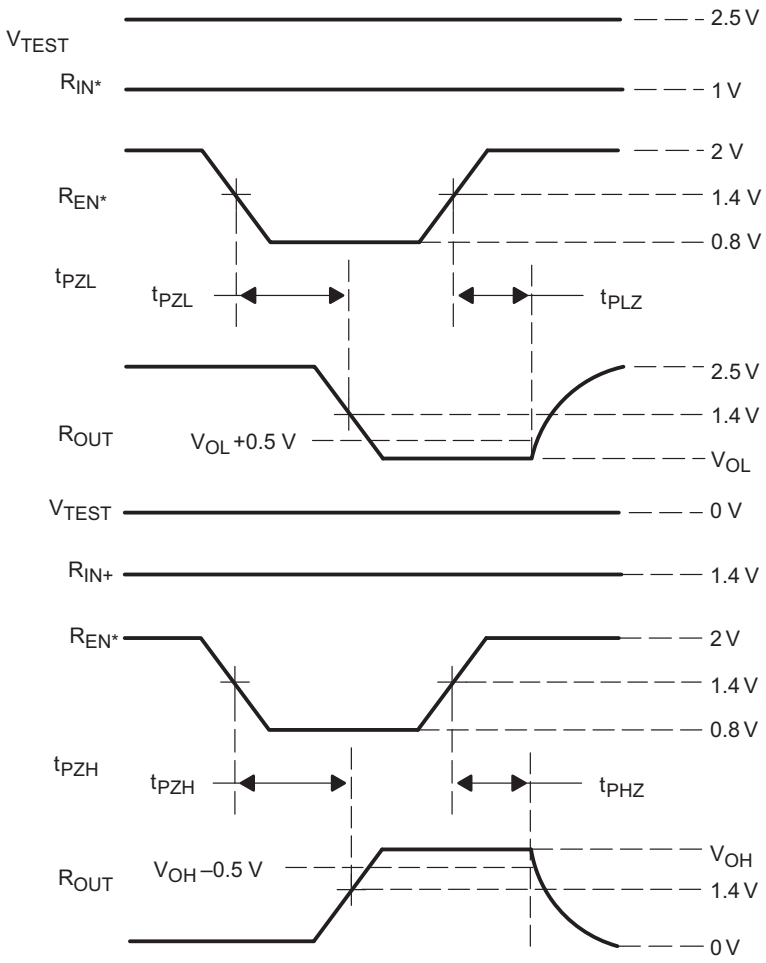
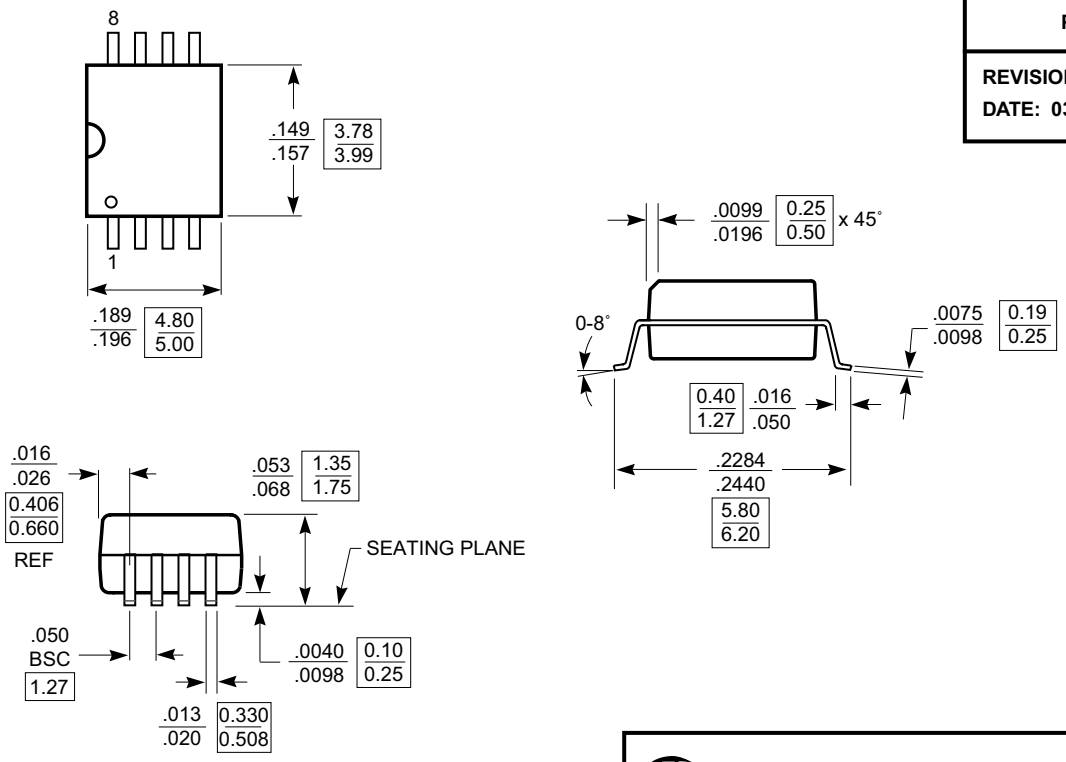


Figure 7. Enable/Disable Time Test Circuit and Waveforms

Packaging Mechanical: 8-Pin SOIC (W)

DOCUMENT CONTROL NO.
PD - 1001
REVISION: F
DATE: 03/09/05



X.XX / X.XX DENOTES DIMENSIONS IN MILLIMETERS

Notes:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012D/AA

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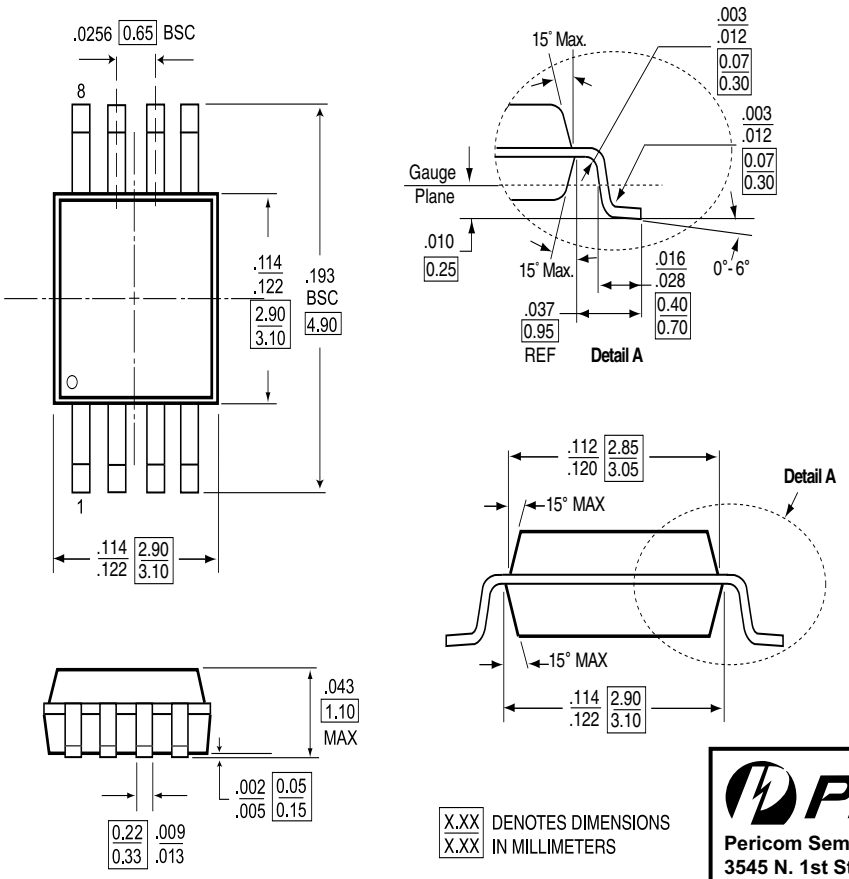
DESCRIPTION: 8-Pin, 150-Mil Wide, SOIC

PACKAGE CODE: W

Packaging Mechanical: 8-Pin MSOP (U)



Notes:
1) Controlling Dimensions inMillimeters
2) Ref. JEDEC MO-187E/AA

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DESCRIPTION: 8-Pin Mini Small Outline Package, MSOP

PACKAGE CODE: U

Ordering Information

Ordering Code	Package Code	Package Description
PI90LV179UE	U	Pb-free & Green, 8-pin MSOP
PI90LV179WE	W	Pb-free & Green, 8-pin SOIC

Note:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/