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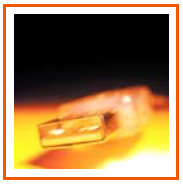
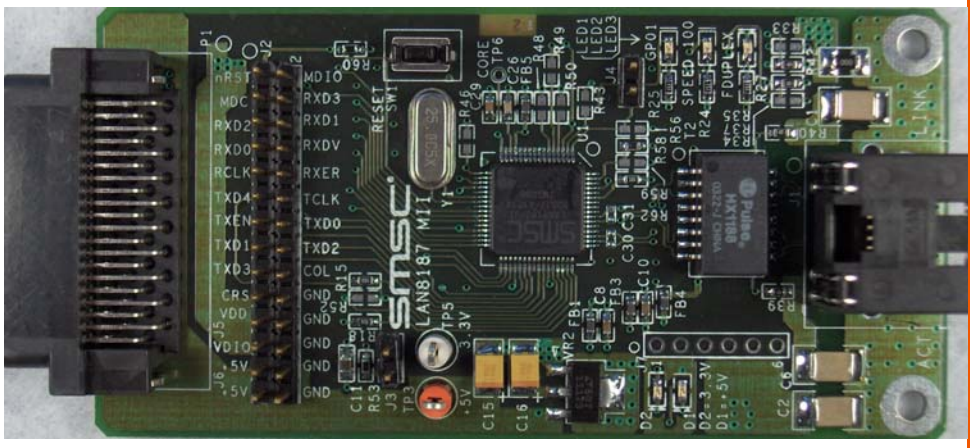


EVB8187 User Manual



1 Introduction

The LAN8187 is a low-power, small form factor, highly integrated analog interface IC for high-performance embedded Ethernet applications. The LAN8187 requires only a single +3.3v supply, and has an integrated +1.8v supply to run the core digital logic.

The EVB8187 is a customer evaluation board that interfaces a standard 40 pin MII connector from an existing MAC controller to the SMSC LAN8187 Ethernet PHY, and out to an RJ-45 Ethernet Jack for 10/100 connectivity.

1.1 References

Concepts and material available in the following documents may be helpful when reading this document.

Table 1 References

Document	Location
SMSC LAN8700 Datasheet *SMSC LAN8187 Datasheet*	http://www.smsc.com/main/datasheet.html
AN13-9 Migrating from the LAN83C183 10/100 PHY to the LAN83C185 10/100 PHY *AN13-2 Scalable Reference Design for Migrating from the SMSC LAN83C185 Non Auto MDIX to a Future SMSC LAN8187 HP Auto MDIX Configuration* *AN8-13 Suggested Magnetics*	http://www.smsc.com/main/appnotes.html

2 Details

The EVB8187 shown in Figure 1 is a Daughter Card designed to plug into a user's test system, using the 40 pin MII conector. The MII connector is an AMP 40 pin Right Angle through hole MII connector, PN AMP-174218-2, reference designator P1. The mating connector is PN AMP 174217-2. The pinout for the plug is shown in Table 4 .

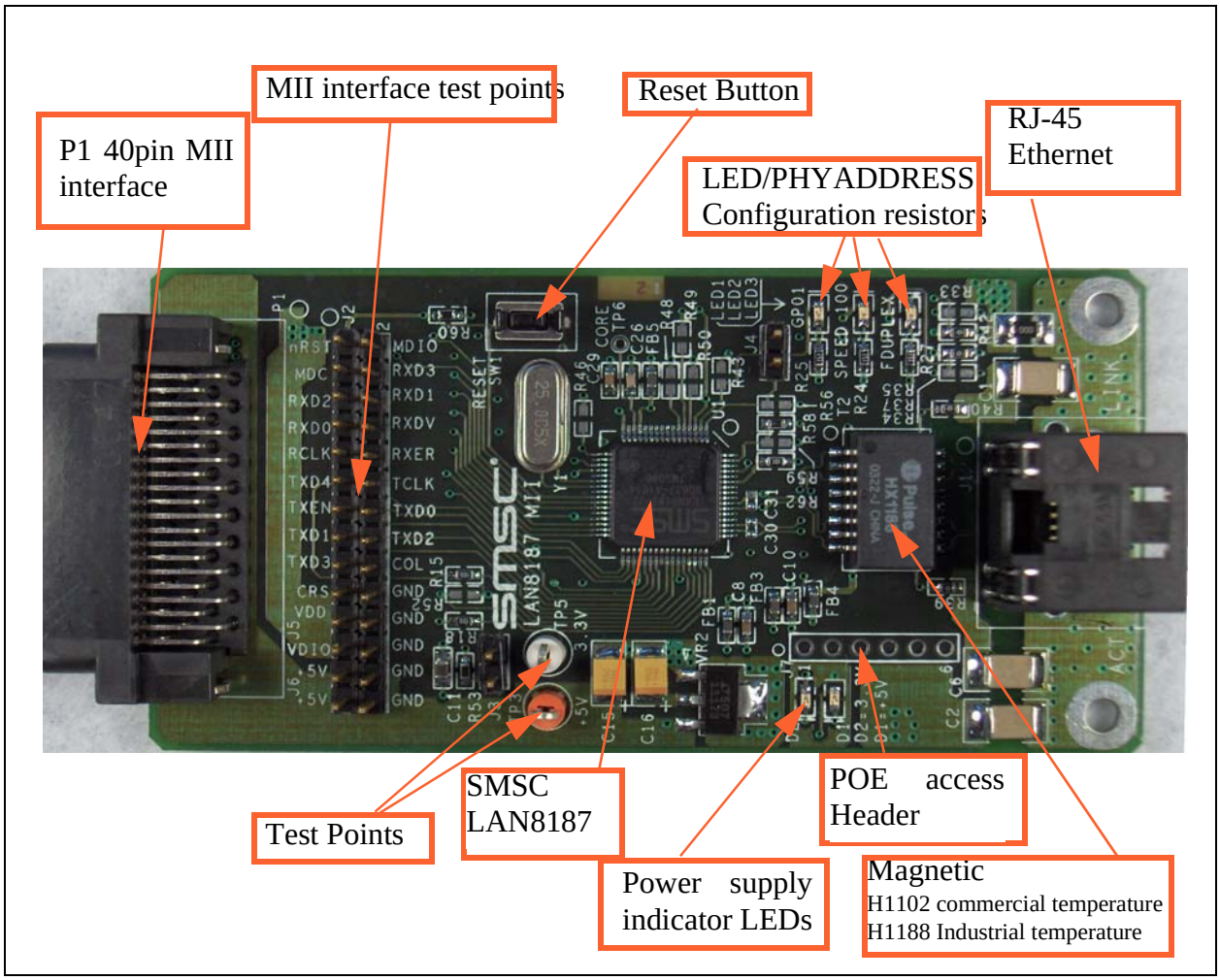


Figure 1 Top View of the EVB8187†

†.actual board may vary.

2.1 Power

Power is provided to the onboard +3.3v regulator by the +5v power coming from the MII connector P1.

Standby power of +5v can be supplied externally by the test point loop at TP3 with ground connected to pin 20 of header J2.

Note: Standby power can also be applied at +3.3v to TP5 if the regulator VR2 is removed.

2.1.1 3.3 Volt Power Supply

The EVB8187 has an on-board step down DC-DC +3.3v power supply regulator (VR2) and uses the +5v input from the MII.

2.2 Configuration

This section gives an explanation to the configuration options available on the SMSC EVB8187.

2.2.1 PHY Address and LEDs

Resistors R24, R31, R37, R29, R38, R34, R35, R32, R36, R33, R27, R28, R25, and R26 are used to set the PHY address according to the table below.

Table 2 PHY address and LED configuration

NAME	PHY ADDRESS		LED OUTPUT	DESCRIPTION
SPEED100PHYAD0	LSB PHYAD0 = 1 LSB PHYAD0 = 0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Populate R24 Depopulate R31 LED2 orient up Populate R31 Depopulate R24 LED2 orient down
LINKPHYAD1	PHYAD1=1 PHYAD1=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Populate R37 Populate R29 Depopulate R38 Depopulate R34 Populate R38 Populate R34 Depopulate R37 Depopulate R29
ACTPHYAD2	PHYAD2=1 PHYAD2=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Populate R35 Populate R32 Depopulate R36 Depopulate R33 Populate R36 Populate R33 Depopulate R35 Depopulate R32
FDUPLEXPHYAD3	PHYAD3=1 PHYAD3=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Populate R27 Depopulate R28 LED3 orient up Populate R28 Depopulate R27 LED3 orient down
GPO1PHYAD4	MSB PHYAD4=1 MSB PHYAD4=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Populate R25 Depopulate R26 LED1 orient up Populate R26 Depopulate R25 LED1 orient down

The address lines are strapped as defined in the diagram below. The LED outputs will automatically change polarity based on the presence of an external pull-down resistor.

- If the LED pin is pulled high, by the **internal** 100K pull-up resistor, then the LED output will be active low.
- If the LED pin is pulled low, by an **external** 10K pull-down resistor, then the LED output will be active high.

To set the PHY address on the LED pins without LEDs or on the CRS/PHYAD4 pin, float the pin to set the address high or pull-down the pin with an **external** 10K resistor to GND to set the address low. See the Figure 2 below:

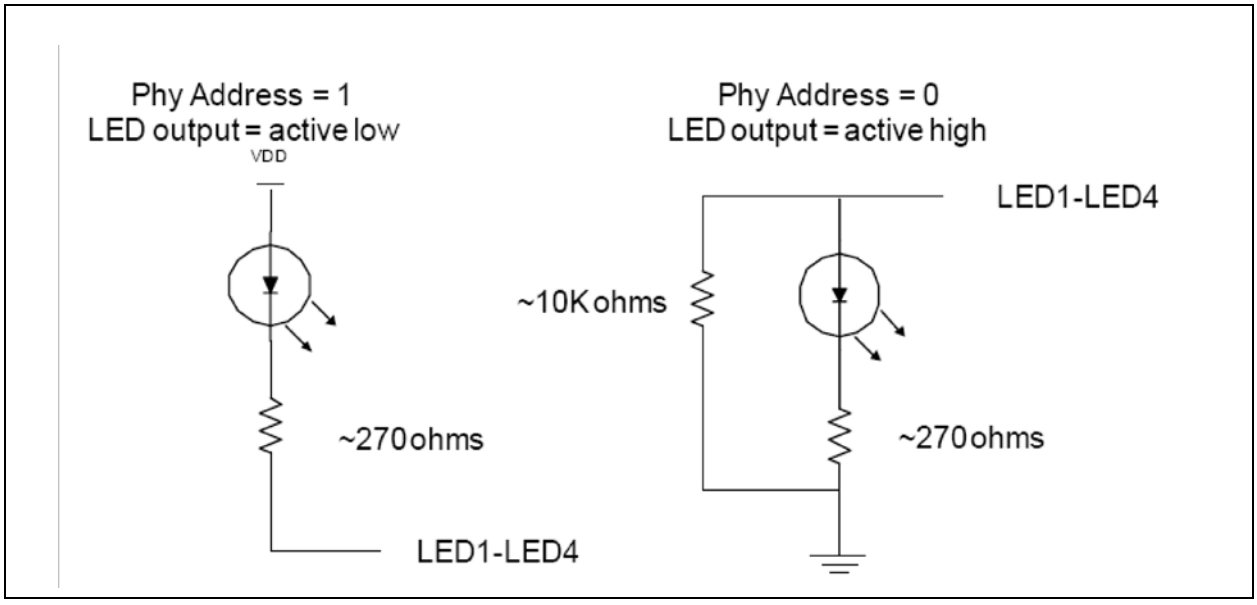


Figure 2 PHY Address Strapping with the LED pins.

2.2.2 Boot Mode Configuratino Options

There are Three resistors used to bootstrap the PHY into a specific mode. Table 3 below shows how to populate the resistor to configure the PHY into different modes upon bootup/after reset..

Table 3 PHY Address Configuration Resistors

MODE2 R48	MODE1 R49	MODE0 R50	BOOT MODE DESCRIPTION	MODE REGISTER BITS MODE [2:0]
Empty	Empty	Empty	All Capable AutoNegotiate Enable [Default]	111
Empty	Empty	**Populated**	Powerdown mode† startup..	110
Empty	**Populated**	Empty	Repeater Mode‡: 100Base-TX Half Duplex is advertised. Auto-negotiate enabled. CRS is active during Receive.	101
Empty	**Populated**	**Populated**	100Base-TX Half Duplex is Advertised. Auto-negotiation is enabled. CRS is active during Transmit and Receive.	100
Populated	Empty	Empty	100Base-TX Full Duplex. Auto-negotiate disabled. CRS is active during receive.	011
Populated	Empty	**Populated**	100Base-TX Half Duplex. Auto-negotiaion disabled. CRS is active during transmit and receive.	010
Populated	**Populated**	Empty	10Base-T Full Duplex. Auto-negotiation disabled.	001
Populated	**Populated**	**Populated**	10Base-T Half Duplex. Auto-negotiation disabled.	000

†.Please refer to the Datasheet Section 5.4 for more information on Powerdown mode.
‡.Please refer to the Datasheet Section 5.4 for more information on Repeater mode.

Note: An Empty resistor means an internal pull-up will bootstrap the Mode pin high to a logic 1. A Populated resistor will bootstrap the Mode pin low to a logic 0.

2.2.3 Pin 46 mode configuration

Pin 46 can either be configured to drive nINT (Active low output interrupt pin) or to drive TXER/TXD4 (Transmit Error pin or Transmit Data 4). This bootstrapping option is controlled by R51 on the board, which is a 10k pull-down to ground on RXD3/nINTSEL. Normally this resistor is empty and the pin is pulled high internally. This default is to configure pin 46 option as nINT. To change this to a TXER pin, the user needs to populate R51. Refer to the LAN8187 datasheet for instructions on changing the TXER pin to a TXD4 pin.

2.2.4 Digital Communications Mode

Resistor R56 will change the digital communications mode of the LAN8187 PHY. By default this resistor is empty. An empty resistor defaults the pin to low at bootup and configures the PHY for MII communication.

If R56 is populated with a 10k resistor, then the device will bootup in RMII mode. However, this EVB is not designed to handle RMII mode, the resistor is left as a reference for the end customer.

2.2.5 MDIO pullup

Resistor R61 is used to give a pullup to the MDIO pin. Normally the resistor is not needed because the MAC that the PHY is interfacing to has a pull-up built into its system.

2.2.6 AutoMDIX options

The LAN8187 supports AutoMDIX on the analog output pins.

The EVB8187 supports the option to disable AutoMDIX and to manually select the channel.

Jumper J3 is used to manually disable AutoMDIX funcion. Placing a jumper accross J3 will disable AutoMDIX functionality and prevent the automatic switching of the TX* with RX*. Please refer to the LAN8187 datasheet for more information on AutoMDIX function.

Resistor R57 is used to switch the channels. Normally R57 is empty and the chanels are normal (ie transmit is on TXP and TXN - receive on RXP and RXN). With R57 populated, the channels are switched (ie. transmit is on RXP and RXN - receive is on TXP and TXN).

The EVB-LAN8187 supports disabling the Automdix through the MDIO interface to the Internal registers. Setting bit 15 of register 27 to a 1 will disable AutoMDIX switching function. Please refer to the SMSC LAN8187 datasheet for more information.

2.3 LED indicators.

There are 7LEDs on the board, 5 placed on the board as discrete components, and 2 on the RJ-45 connector..

Table 2.1 LED indicators

Schem Reference	Silk screen Name	description
LED2	SPEED100	This LED indicates when the PHY is communicating in 100Base-TX mode. This LED will only come on when the PHY has a link established.
LED3	FDUPLEX	This LED indicates that the link is communicating in Full Duplex.
Green(link)	LINK	This LED indicates that a link to the other host has been made.
Yellow(Act)	ACT	This LED indicates that there is communication activity on the Ethernet Link.
led1	GPO1	This LED indicates that GPO1 output is low.
D1	+5V	This LED indicates that there is +5v power to the board
D2	+3.3V	This LED indicates that there is +3.3v power to the board.

2.4 Test Points

Table 2.2,Table 2.3 and Table 2.4 below identify the test points for debug purposes.

Table 2.2 Test Points

test points	description		test points	description
TP3	+5v power.		TP5	+3.3v power supply output.

Table 2.2 Test Points

test points	description		test points	description
TP6	VDDCORE†			

†.VDDCORE is the internal +1.8v regulated output, that needs a 4.7uF and a 0.1uF capacitor to decouple the voltage.

Table 2.3 Test points from header J2

Header Pin	description		Header Pin	description
1	nRST: active low reset signal from the MII plug or the on board reset button SW1		11	TX_ER: Transmit Error
2	MDIO: Management Data Input Ouput.		12	TX_CLK: Transmit clock
3	MDC: Management Clock		13	TX_EN: Transmit Enable
4	RXD3: Receive Data Bit 3		14	TXD0: Transmit Data Bit 0.
5	RXD2: Receive Data Bit 2		15	TXD1: Transmit Data Bit 1
6	RXD1: Receive Data Bit 1		16	TXD2: Transmit Data Bit 2
7	RXD0: Receive Data Bit 0		17	TXD3: Transmit Data Bit 3
8	RX_DV: Receive Data Valid		18	COL: Collision Detected.
9	RX_CLK: Receive Clock		19	CRS: Carrier Sense.
10	RX_ER: Receive Error		20	Digital Ground

Table 2.4 Test points from header J4.

Header Pin	Description		Header Pin	Description
1	GPO2: General Purpose Output pin 2.		2	GPO0: General purpose output pin 0.

2.5 Connector Pin-outs

2.5.1 MII Connector

The MII connector supplies +5v power to the board, as well as the digital control signals. The pinout for the connector is shown below in Table 4 .

Table 4 AMP MII connector pintou RA (P1)

1	+5V[3]	**11**	TX_ER†	**21**	+5V[2]	**31**	GND[9]

Table 4 AMP MII connector pintou RA (P1)

2	MDIO	**12**	TX_CLK	**22**	GND[18]	**32**	GND[8]
3	MDC	**13**	TX_EN	**23**	GND[17]	**33**	GND[7]
4	RXD3	**14**	TXD0	**24**	GND[16]	**34**	GND[6]
5	RXD2	**15**	TXD1	**25**	GND[15]	**35**	GND[5]
6	RXD1	**16**	TXD2	**26**	GND[14]	**36**	GND[4]
7	RXD0	**17**	TXD3	**27**	GND[13]	**37**	GND[3]
8	RX_DV	**18**	COL	**28**	GND[12]	**38**	GND[2]
9	RX_CLK	**19**	CRS	**29**	GND[11]	**39**	GND[1]
10	RX_ER	**20**	+5V[4]	**30**	GND[10]	**40**	+5V[1]

†.TX_ER from the MII is not used on the EVB-LAN8187, but can be monitored on the test header J2.

2.5.2 MII Pin Description

The signals are defined in Table 5 with a description relative to the EVB8187

Table 5 MII 40 PIN DESCRIPTION

NAME	DIRECTION RELATIVE TO EVB-LAN8187	ACTIVE LEVEL	DESCRIPTION
GND[18-1]	Power	n/a	**Ground Plane**.
+5V[4-1]]	Power	n/a	**+5v supply** from the MII connector. Converted to +3.3v on the EVB and used to power the LAN8187 PHY and +3.3v rail.
RXD[3-0]	Output	TBA	**Receive data bits 0 to 3** that are sent by the PHY to the receive path of the MII connector to the MAC controller.
TXD[3-0]	Input	TBA	**Transmit data bits 0 to 3** that are accepted by the PHY in the receive path from the MAC controller.
MDIO	Input/Ouptut	TBA	**Management Data Input Output:** serial managment data input/output.
MDC	Input	TBA	**Management Data Clock:** clock signal for the above MDIO signal.
RX_DV	Output	TBA	**Receive data valid:** this signal indicates that recovered and decoded data nibbles are being presented on RXD[3:0].
RX_CLK	Output	TBA	**Receive Clock**: 25Mhz in 100base-TX mode. 2.5Mhz in 10base-T mode.

Table 5 MII 40 PIN DESCRIPTION

NAME	DIRECTION RELATIVE TO EVB-LAN8187	ACTIVE LEVEL	DESCRIPTION
RX_ER	Output	TBA	**Receive Error:** Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY.
TX_ER	Input/Output	TBA	**Transmit Error or Transmit data 4:** This bit is set by the RXD3/nIntsel pin.
TX_CLK	Output	TBA	**Transmit Clock:** 25Mhz in 100base-TX mode. 2.5Mhz in 10base-T mode.
TX_EN	Input	TBA	**Transmit Enable:** Indicates that valid data is present on the TXD[3:0] signals, for transmission.
COL	Output	TBA	**MII Collision detection:** Assertion to indicate detection of collision.
CRS	Output	TBA	**Carrier Sense:** Assertion indicates detection of carrier.

2.5.3 RJ-45 Ethernet Jack

The pinout for the RJ-45 Jack is described in Table 6 below.

Table 6 RJ-45 Ethernet Jack Pin-out

PIN	DESCRIPTION
1	**TXP:** Transmit Positive
2	**TXN:** Transmit Negative
3	**RXP:** Receive Positive
4	Analog Reference to ground
5	Analog Reference to ground
6	**RXN:** Receive Negative
7	Analog Reference to ground
8	Analog Reference to ground

2.6 Clocking

2.6.1 Crystal Oscillator

The 25 MHz crystal Y1 is connected to the internal oscillator of the LAN8187. A PLL circuit in the LAN8187 generates all the timing needed by the PHY.

2.6.2 External Clock

The board can be configured to use an external clock if the crystal Y1 is removed and a 25Mhz +2.0v signal is injected onto pin Y1.1. Y1.2 is left floating.

2.6.3 TX_ER

R41 enables the user to tie the TXER from the MII connector to the nINT/TXER/TXD4 pin of the LAN8187. However, the user must also make sure to populate R51 to change the mode of Pin46 to TX_ER.

2.7 Schematics

Page 1 - Title page with block diagram.

Page 2 - Board Stackup.

Page 3 - LAN8187 and Magnetics.

Page 4 - Power and Miscellaneous.

EVB-LAN8187

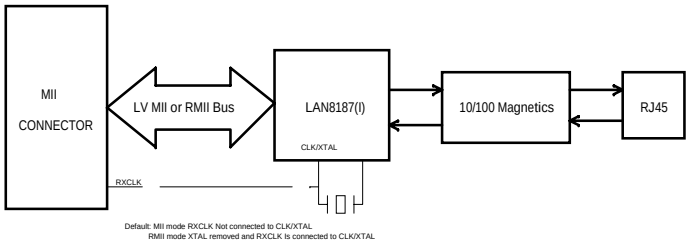
LAN8187(I) MII Customer Evaluation Board

Schematic Revision B

Design Details

Board: PCB-7058AZ-B
Chip: LAN8187I
Board Form Factor:
Assembly:

EVB BLOCK DIAGRAM



Revisions
Rev A001 added 15pF caps to outputs
Rev A002 swapped vddio and vdd33 power pins; corrected mdio pullup voltage; clarified mode table
Rev A003 corrected all other vddio pullups.
Rev A004 changed all (i) to (I)
Rev A005 deleted extra caps on 5V power supply; added FB6 to pin 1 of MII for VDDIO power; added note to move R54 close to R13; remove C6 and C21; add note to keep C15 and C16 close to reg; and added config option for MII pin 22 to be either gnd or nRST; added config option for MII pin 21 to be either gnd or gpo

Rev B added POE access header and changed power net name on pin 13 of PHY to VDD from VDD33

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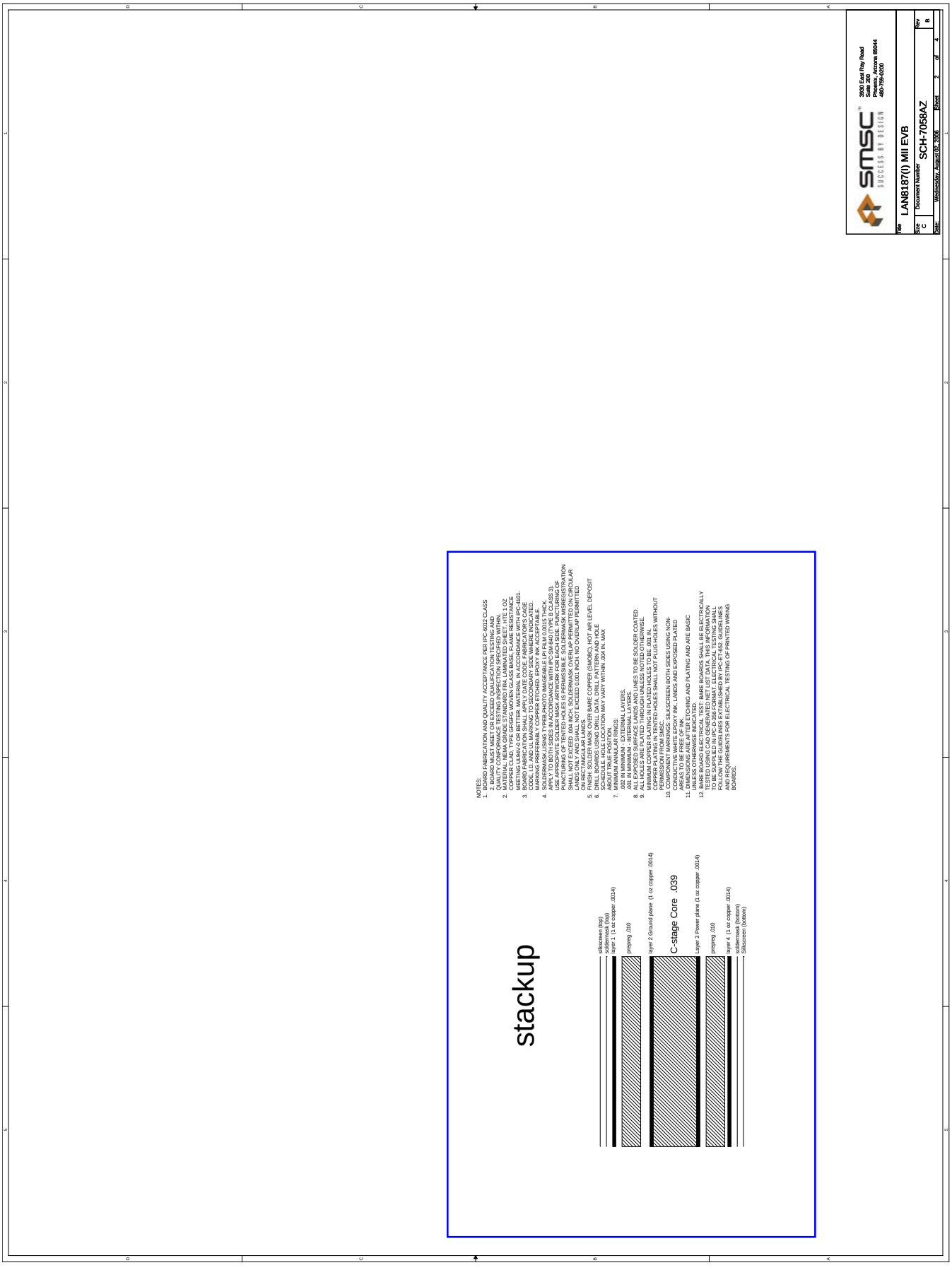

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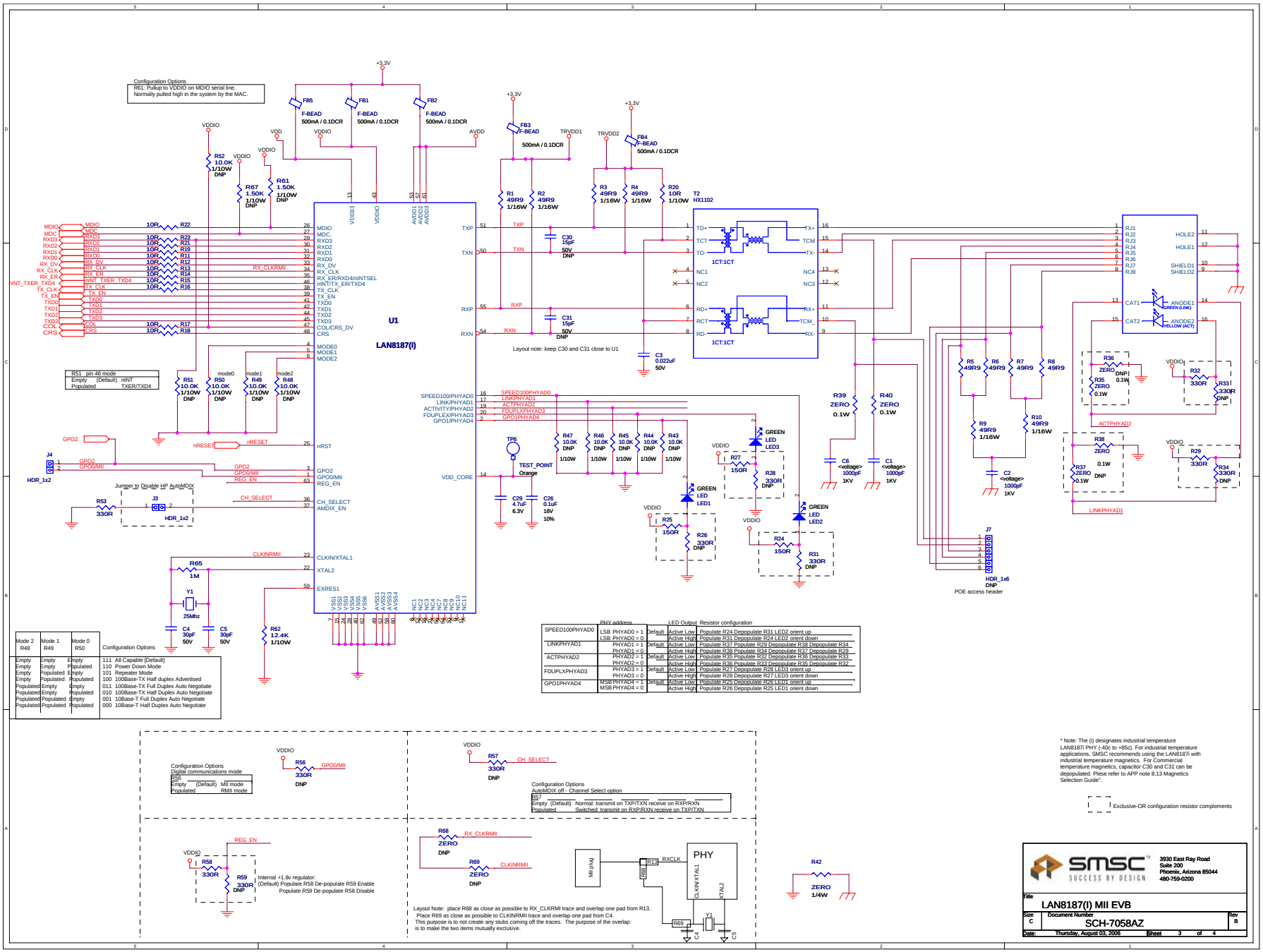
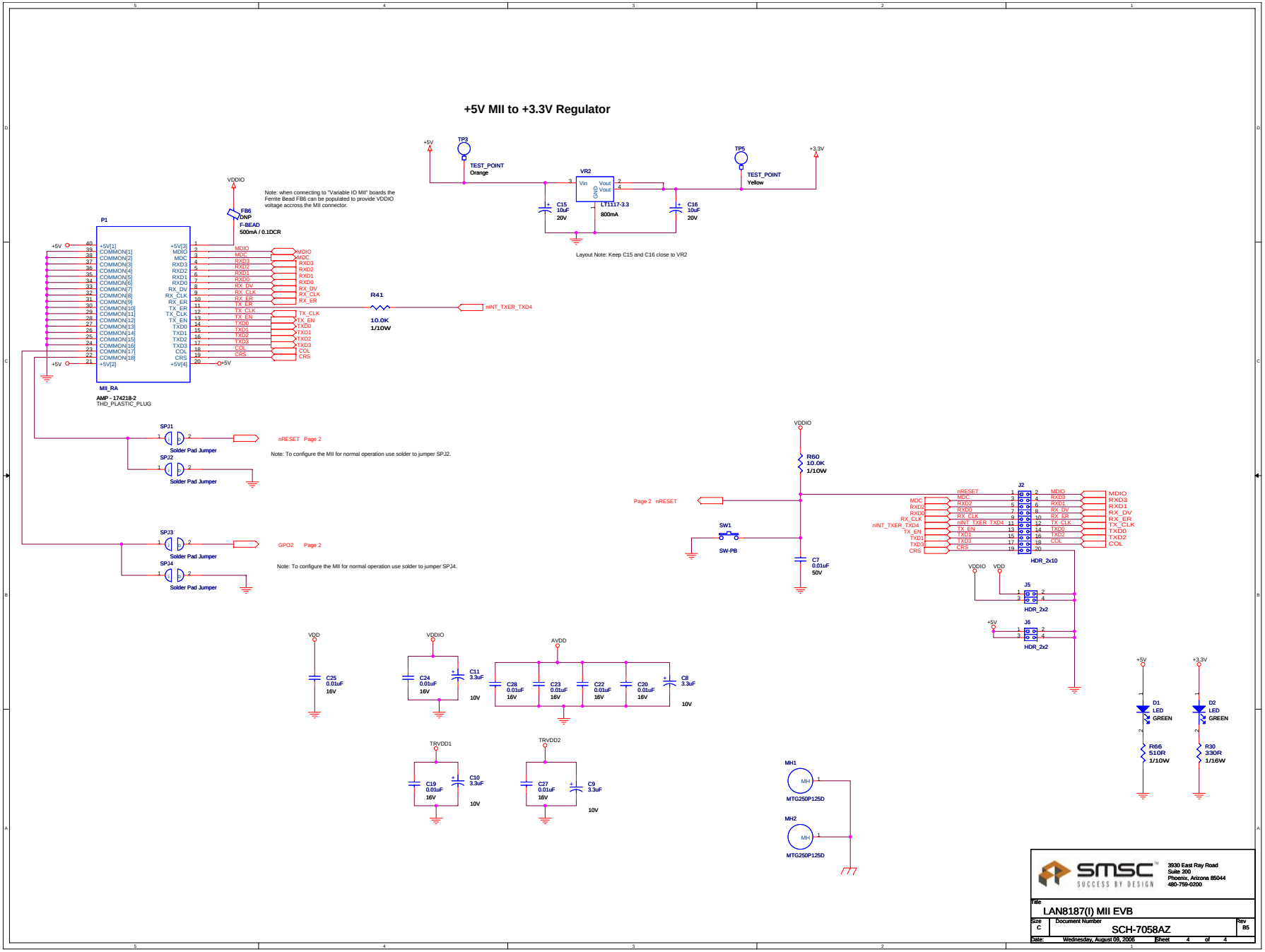


Mode 2 R48	Mode 1 R49	Mode 0 R50	Configuration Options
Empty	Empty	Empty	111 All Capable [Default]
Empty	Empty	Populated	110 Power Down Mode
Empty	Populated	Empty	101 Repeater Mode
Empty	Populated	Populated	100 100Base-TX Half duplex Advertised
Populated	Empty	Empty	011 100Base-TX Full Duplex Auto Negotiate
Populated	Empty	Populated	010 100Base-TX Half Duplex Auto Negotiate
Populated	Populated	Empty	001 10Base-T Full Duplex Auto Negotiate
Populated	Populated	Populated	000 10Base-T Half Duplex Auto Negotiate

	PHY address		LED Output	Resistor configuration
SPEED100PHYAD0	LSB PHYAD0 = 1	Default	Active Low	Populate R24 Depopulate R31 LED2 orient up
	LSB PHYAD0 = 0		Active High	Populate R31 Depopulate R24 LED2 orient down
LINKPHYAD1	PHYAD1 = 1	Default	Active Low	Populate R37 Depopulate R29 Depopulate R38 Depopulate R34
	PHYAD1 = 0		Active High	Populate R38 Depopulate R34 Depopulate R37 Depopulate R29
ACTPHYAD2	PHYAD2 = 1	Default	Active Low	Populate R35 Depopulate R32 Depopulate R36 Depopulate R33
	PHYAD2 = 0		Active High	Populate R36 Depopulate R33 Depopulate R35 Depopulate R32
FDUPLXPHYAD3	PHYAD3 = 1	Default	Active Low	Populate R27 Depopulate R28 LED3 orient up
	PHYAD3 = 0		Active High	Populate R28 Depopulate R27 LED3 orient down
GPO1PHYAD4	MSB PHYAD4 = 1	Default	Active Low	Populate R25 Depopulate R26 LED1 orient up
	MSB PHYAD4 = 0		Active High	Populate R26 Depopulate R25 LED1 orient down


+5V MII to +3.3V Regulator
TP3
TEST_POINT
Orange
TP5
TEST_POINT
Yellow
VR2
LT1117-3.3
800mA
C15
10uF
20V
C16
10uF
20V
Layout Note: Keep C15 and C16 close to VR2
VDDIO
FB6
DNP
F-BEAD
500mA / 0.1DCR
Note: when connecting to "Variable IO MII" boards the Ferrite Bead FB6 can be populated to provide VDDIO voltage across the MII connector.
P1
MII_RA
AMP - 174218-2
THD_PLASTIC_PLUG
R41
10.0K
1/10W
nINT_TXER_TXD4
SPJ1
SPJ2
SPJ3
SPJ4
Solder Pad Jumper
nRESET Page 2
GPO2 Page 2
Note: To configure the MII for normal operation use solder to jumper SPJ2.
Note: To configure the MII for normal operation use solder to jumper SPJ4.
R60
10.0K
1/10W
SW1
SW-PB
C7
0.01uF
50V
J2
HDR_2x10
J5
HDR_2x2
J6
HDR_2x2
C25
0.01uF
16V
C24
0.01uF
16V
C11
3.3uF
10V
C26
0.01uF
16V
C23
0.01uF
16V
C22
0.01uF
16V
C20
0.01uF
16V
C8
3.3uF
10V
C19
0.01uF
16V
C10
3.3uF
10V
C27
0.01uF
16V
C9
3.3uF
10V
TRVDD1
TRVDD2
MH1
MH2
MTG250P125D
D1
LED
GREEN
D2
LED
GREEN
R66
510R
1/10W
R30
330R
1/16W
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