

Monolithic N-Channel JFET Duals

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	$ V_{GS1} - V_{GS2} $ Max (mV)
SST421NL	-0.4 to -2	-40	0.3	10
SST423NL	-0.4 to -2	-40	0.3	25

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 0.6 pA
- Low Noise
- High CMRR: 102 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals

APPLICATIONS

- Ultralow Input Current Differential Amps
- High-Speed Comparators
- Impedance Converters

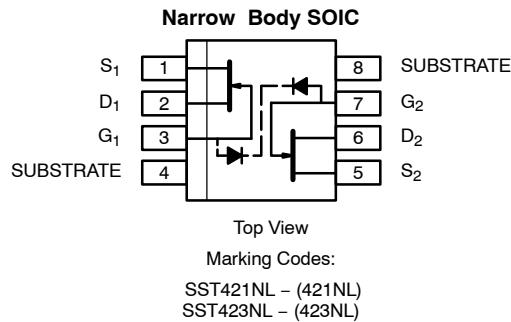
DESCRIPTION

The SST421NL/423NL are monolithic dual n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers low operating gate current.

The SO-8 package provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.

Pins 4 and 8 on SST421NL/423NL part numbers enable the substrate to be connected to a positive polarity, external bias (V_{DD}) to avoid latchup.

Similar versions of these part numbers are available in the hermetically sealed TO-78 package. Full military processing is available. See data sheets for part numbers U421/423.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-40 V
Gate-Gate Voltage	±40 V
Gate Current	10 mA
Lead Temperature ($1/16$ " from case for 10 sec.)	300 °C
Storage Temperature	-65 to 200 °C
Operating Junction Temperature	-55 to 150 °C

Power Dissipation :	Per Side ^a	300 mW
	Total ^b	500 mW

Notes

- Derate 2.4 mW/°C above 25 °C
- Derate 4 mW/°C above 25 °C

SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Specific Test Conditions	Typ ^a	Limits				Unit
				SST421NL		SST423NL		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-60	-40		-40		V
Gate-Gate Breakdown Voltage	V _{(BR)G1 - G2}	I _G = ± 1 μA, I _D = 0, I _S = 0	± 55	± 40		± 40		
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 nA	-1.2	-0.4	-2	-0.4	-2	
Saturation Drain Current	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V	400	60	1000	60	1000	μA
Gate Reverse Current	I _{GSS}	V _{GS} = -20 V, V _{DS} = 0 V T _A = 125 °C	-0.6		-50		-50	pA
			-0.3		-50		-50	nA
Gate Operating Current	I _G	V _{DG} = 10 V, I _D = 30 μA	-1.0					pA
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, I _D = 10 μA	2000					Ω
Gate-Source Voltage	V _{GS}	V _{DG} = 10 V, I _D = 30 μA	-0.8		-1.8		-1.8	V
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V	0.7					
Dynamic								
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 kHz	0.6	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g _{os}		4		10		10	μS
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 30 μA, f = 1 kHz	0.2	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g _{os}		0.4		3		3	μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	1.4		3		3	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		0.7		1.5		1.5	
Equivalent Input Noise Voltage	\bar{e}_n	V _{DS} = 10 V, I _D = 30 μA, f = 10 Hz	30					nV/ √Hz
Matching								
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 10 V, I _D = 30 μA			10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 10 V, I _D = 30 μA T _A = -55 to 125 °C			10		40	μV/°C
Common Mode Rejection Ratio	CMRR	V _{DG} = 10 to 20 V, I _D = 30 μA	102	90		80		dB

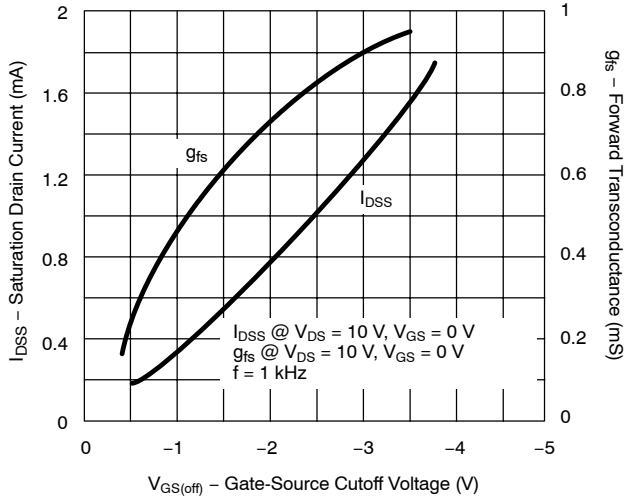
Notes

a. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.

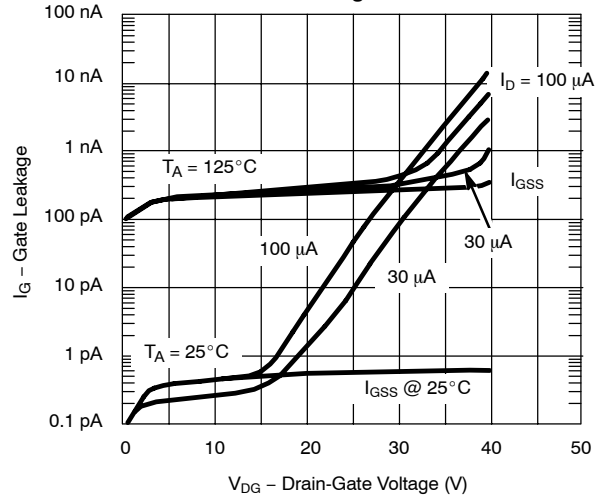
NNT

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

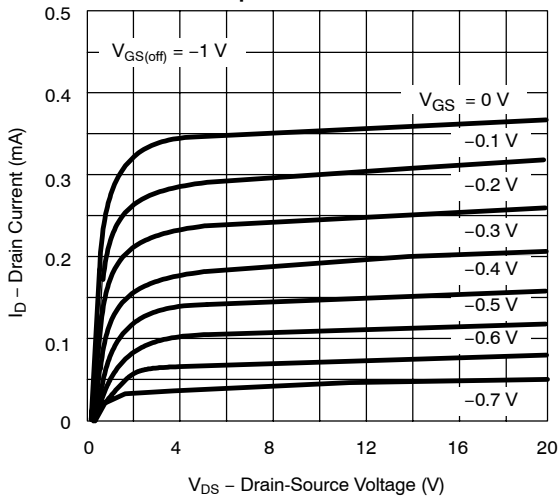
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



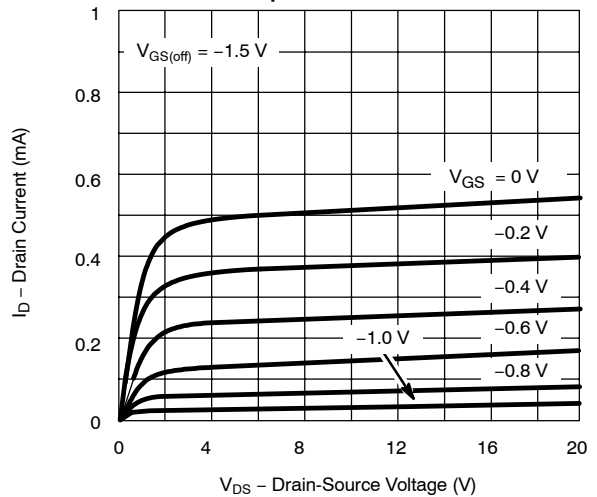
Gate Leakage Current



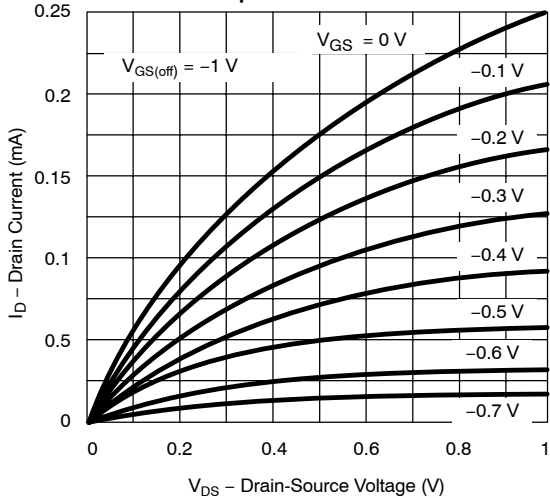
Output Characteristics



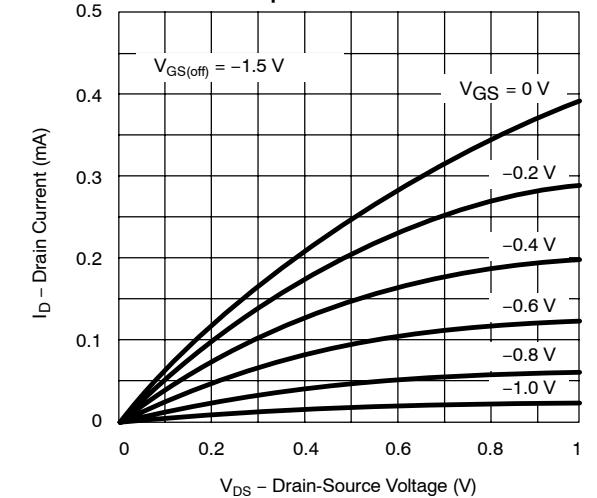
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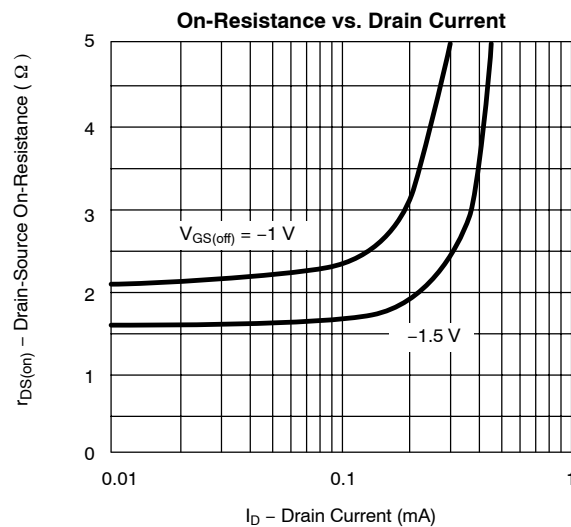
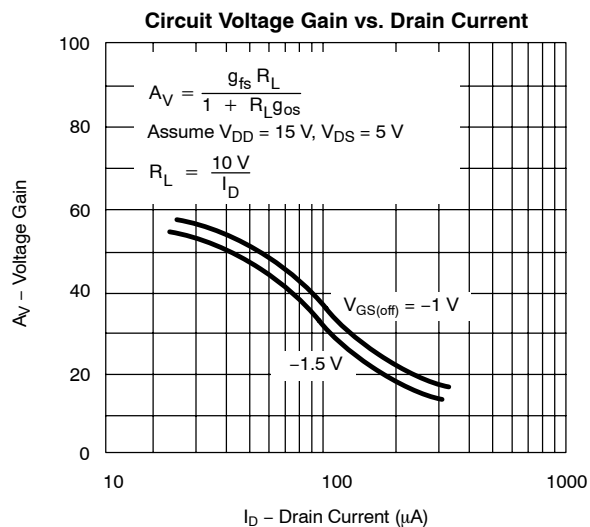
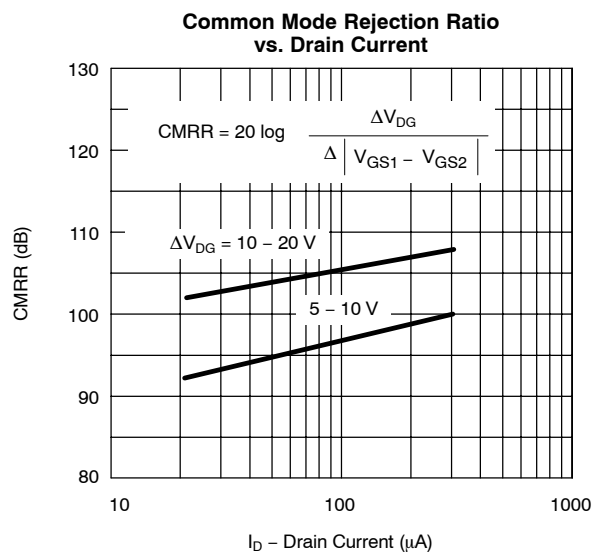
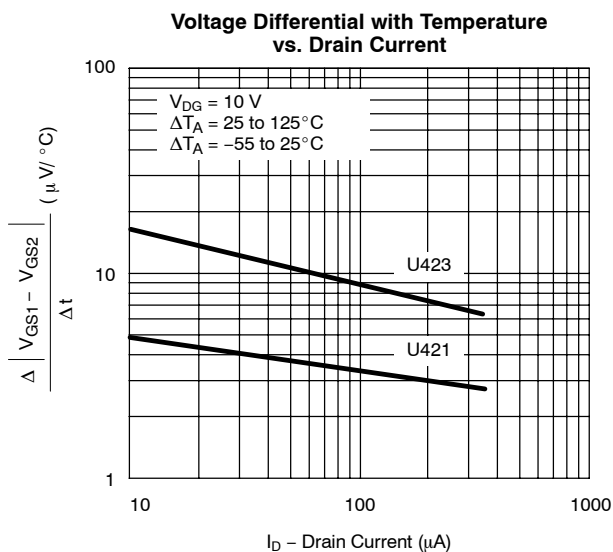
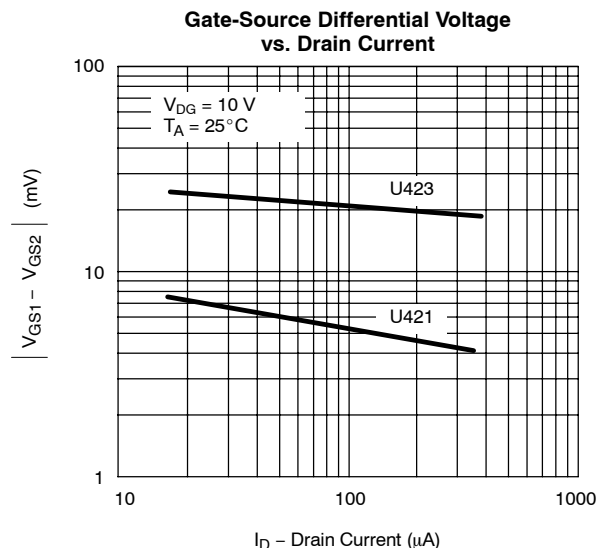
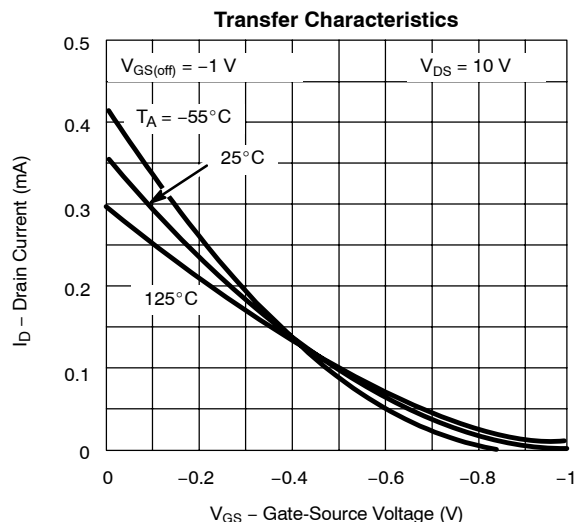
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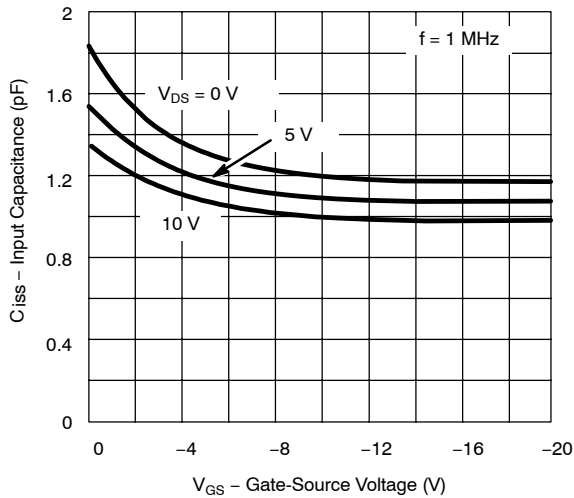


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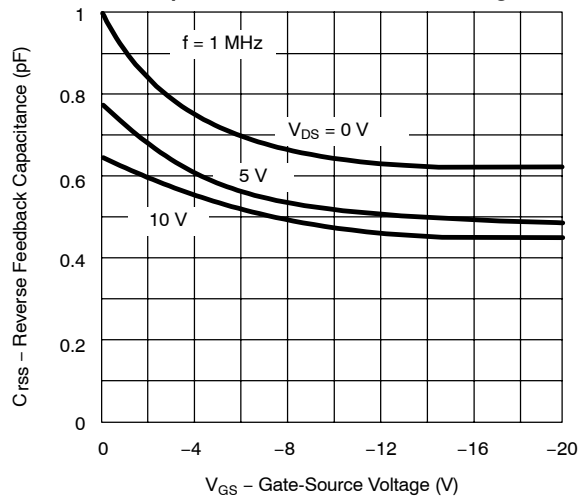


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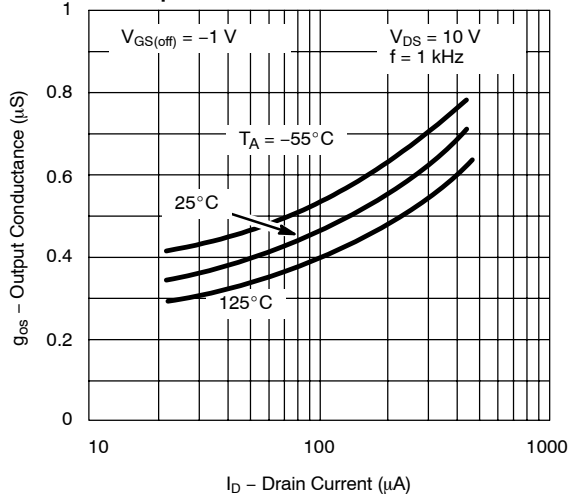
Common-Source Input Capacitance vs. Gate-Source Voltage



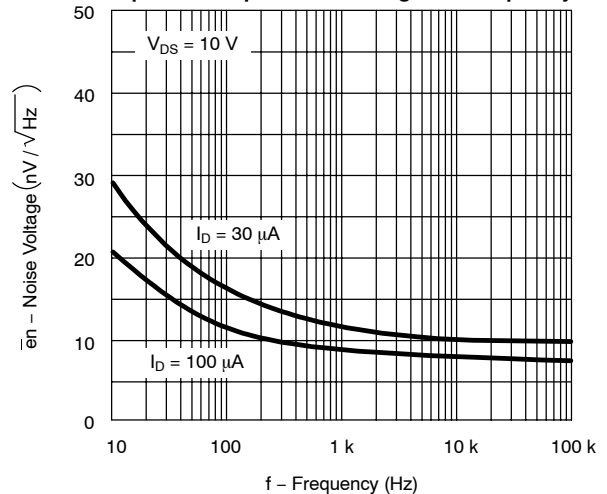
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



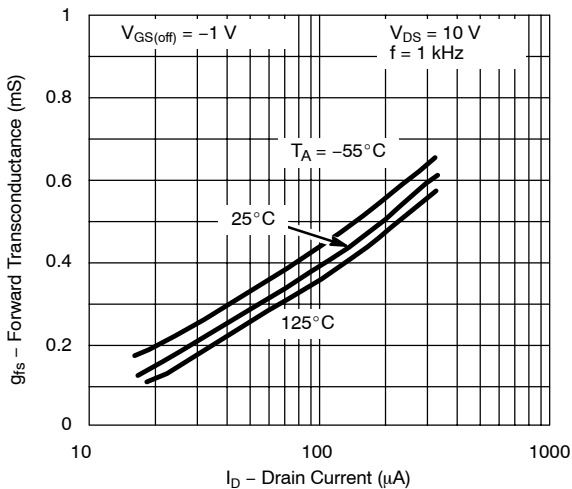
Output Conductance vs. Drain Current



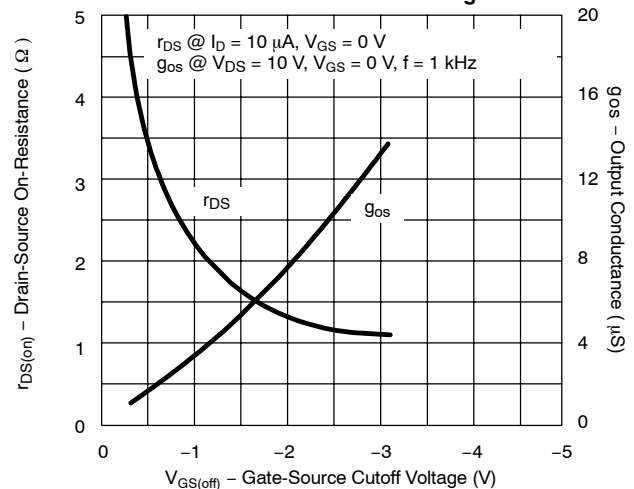
Equivalent Input Noise Voltage vs. Frequency



Common-Source Forward Transconductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage





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