P-Channel JFETs

J270 SST270
J271 SST271

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_{DSS} Min (mA)
J/SST270	0.5 to 2.0	30	6	–2
J/SST271	1.5 to 4.5	30	8	–6

FEATURES

- Low Cutoff Voltage: J270 <2 V
- High Input Impedance
- Very Low Noise
- High Gain

BENEFITS

- Full Performance from Low-Voltage Power Supply: Down to 2 V
- Low Signal Loss/System Error
- High System Sensitivity
- High-Quality, Low-Level Signal Amplification

APPLICATIONS

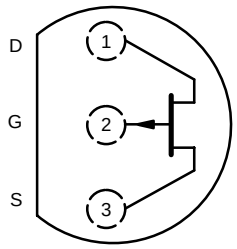
- High-Gain, Low-Noise Amplifiers
- Low-Current, Low-Voltage Battery Amplifiers
- Ultrahigh Input Impedance Pre-Amplifiers
- High-Side Switching

DESCRIPTION

The J/SST270 series consists of all-purpose amplifiers for designs requiring p-channel operation.

The TO-226AA (TO-92) plastic package provides a low-cost option, while the TO-236 (SOT-23) package provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information).

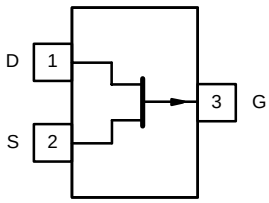
TO-226AA
(TO-92)



Top View

J270
J271

TO-236
(SOT-23)



Top View

SST270 (S0)*
SST271 (S1)*

*Marking Code for TO-236

ABSOLUTE MAXIMUM RATINGS

Gate-Drain Voltage . . . . . 30 V
Gate-Source Voltage . . . . . 30 V
Gate Current . . . . . –50 mA
Storage Temperature . . . . . –55 to 150°C
Operating Junction Temperature . . . . . –55 to 150°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Power Dissipation[a] . . . . . 350 mW

Notes
a. Derate 2.8 mW/°C above 25°C

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

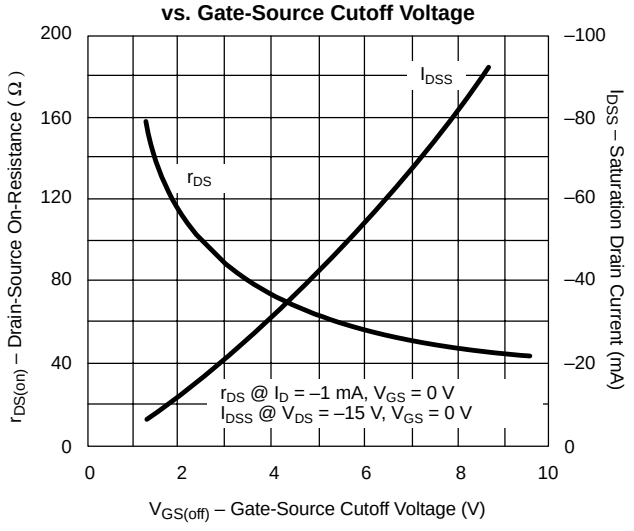
Parameter	Symbol	Test Conditions	Typ[a]	Limits J/SST270 Min	Limits J/SST270 Max	Limits J/SST271 Min	Limits J/SST271 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 μA , V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –15 V, I_D = –1 nA		0.5	2.0	1.5	4.5	
Saturation Drain Current[b]	I_{DSS}	V_{DS} = –15 V, V_{GS} = 0 V		–2	–15	–6	–50	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	10		200		200	pA
		T_A = 125°C	5					nA
Gate Operating Current	I_G	V_{DG} = –15 V, I_D = –1 mA	10					pA
Drain Cutoff Current	$I_{D(off)}$	V_{DS} = –15 V, V_{GS} = 10 V	–10					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = –1 mA , V_{DS} = 0 V	–0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = –15 V, V_{GS} = 0 V f = 1 kHz		6	15	8	18	mS
Common-Source Output Conductance	g_{os}				200		500	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = –15 V, V_{GS} = 0 V f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		4					
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = –10 V, V_{GS} = 0 V f = 1 kHz	20					nV/√Hz

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

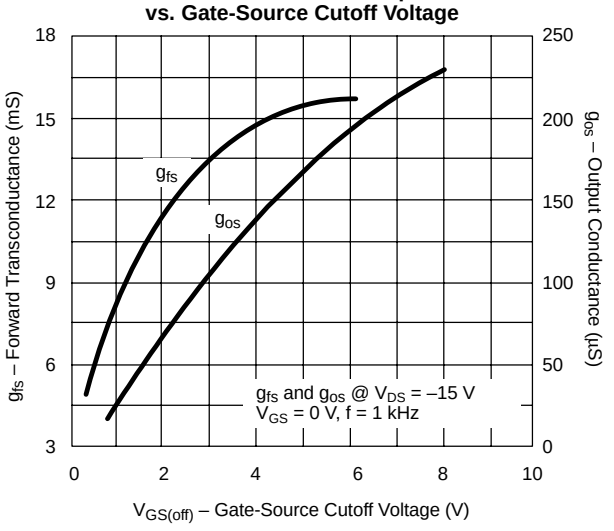
PSCIA

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

On-Resistance and Drain Current vs. Gate-Source Cutoff Voltage

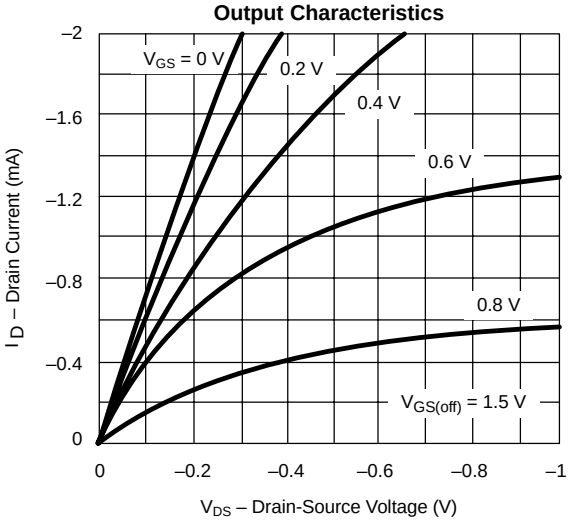


Forward Transconductance and Output Conductance vs. Gate-Source Cutoff Voltage

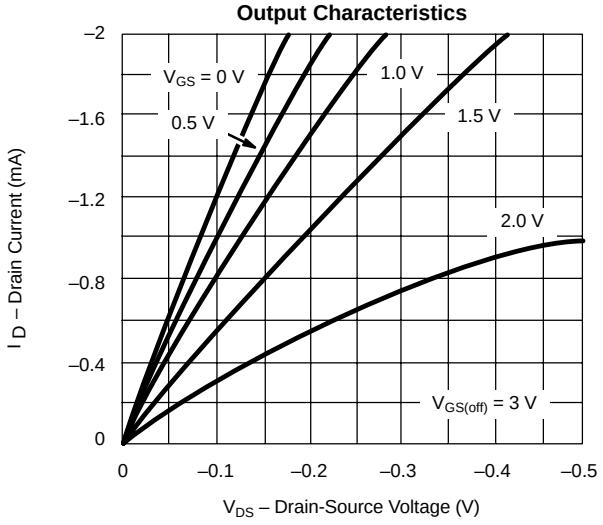


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

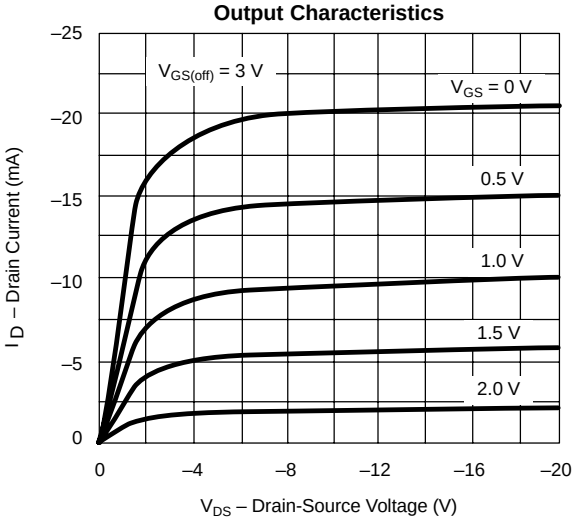
Output Characteristics



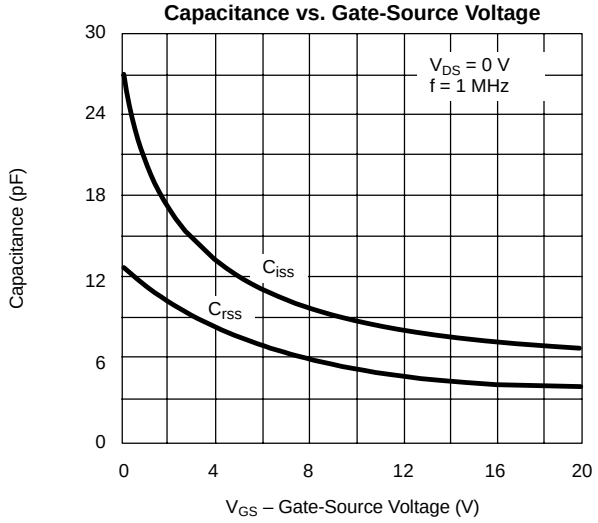
Output Characteristics



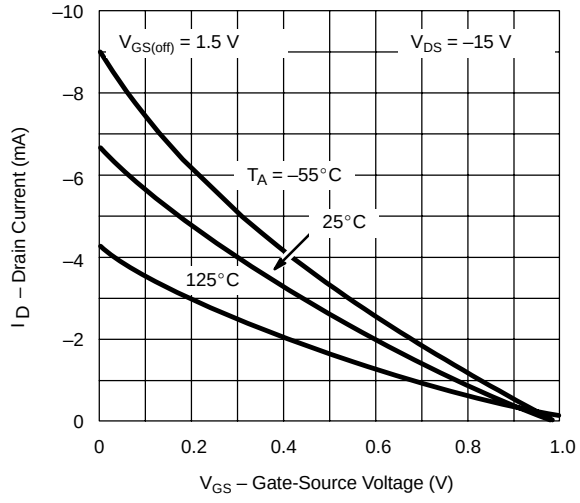
Output Characteristics



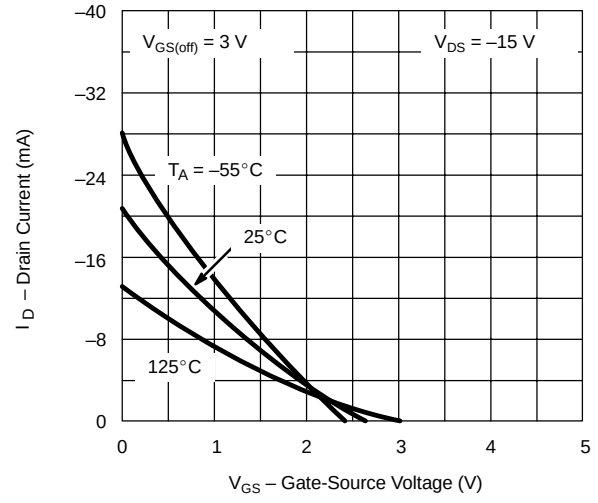
Capacitance vs. Gate-Source Voltage



Transfer Characteristics

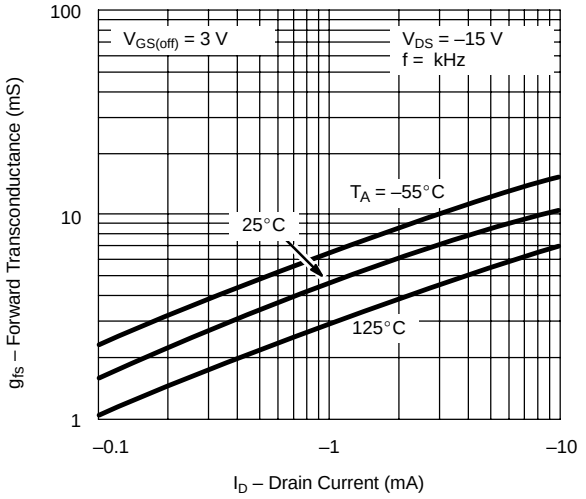


Transfer Characteristics

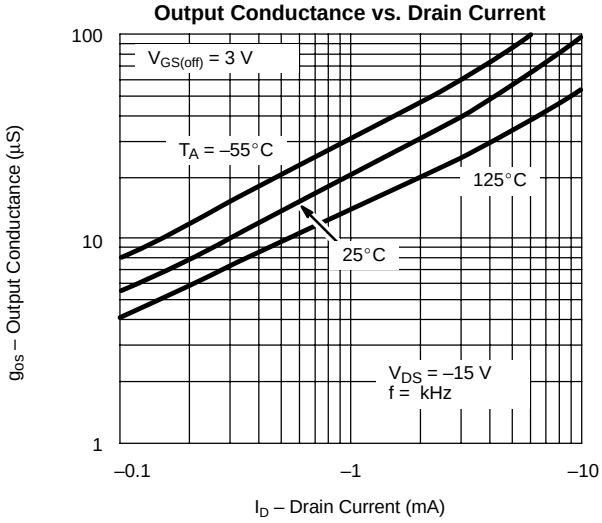


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

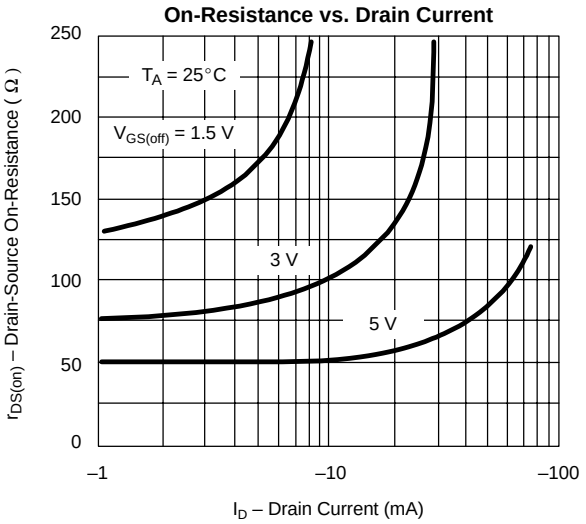
Transconductance vs. Drain Current



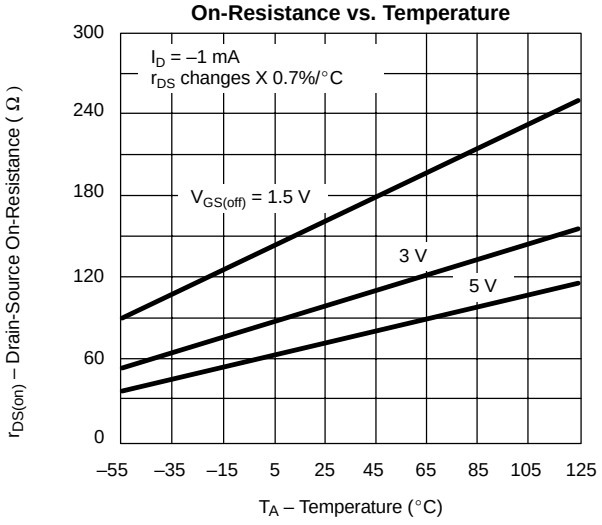
Output Conductance vs. Drain Current



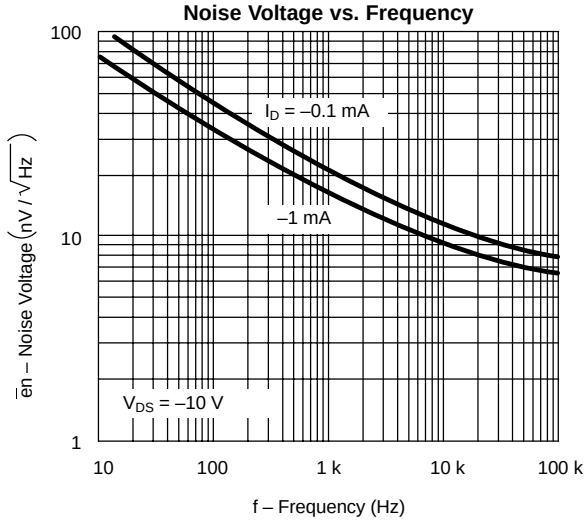
On-Resistance vs. Drain Current



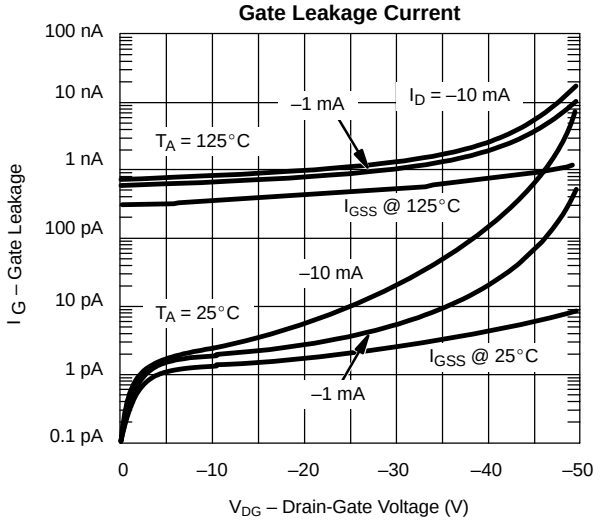
On-Resistance vs. Temperature



Noise Voltage vs. Frequency



Gate Leakage Current



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