

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Not recommended  
for new design

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Customer Support Dept.  
April 1, 2003

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# HD74CBT16212A

## 24-bit FET Bus-Exchange Switches



ADE-205-647A (Z)

Preliminary  
Rev. 1  
Feb. 2002

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### Description

The HD74CBT16212A devices provide 24-bits of high speed TTL-compatible bus switching or exchanging. The low on state resistance of the switch allows connections to be made with minimal propagation delay. Each device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

### Features

- Minimal propagation delay through the switch.
- 5  $\Omega$  switch connection between two ports.
- TTL-compatible input levels.
- Ultra low quiescent power.  
-Ideally suited for notebook applications.
- Package type  
Product code example: HD74CBT16212ATEL

Package type	Package code	Package suffix	Taping code
TSSOP-56pin	TTP-56DAV	T	EL(1,000pcs / Reel)

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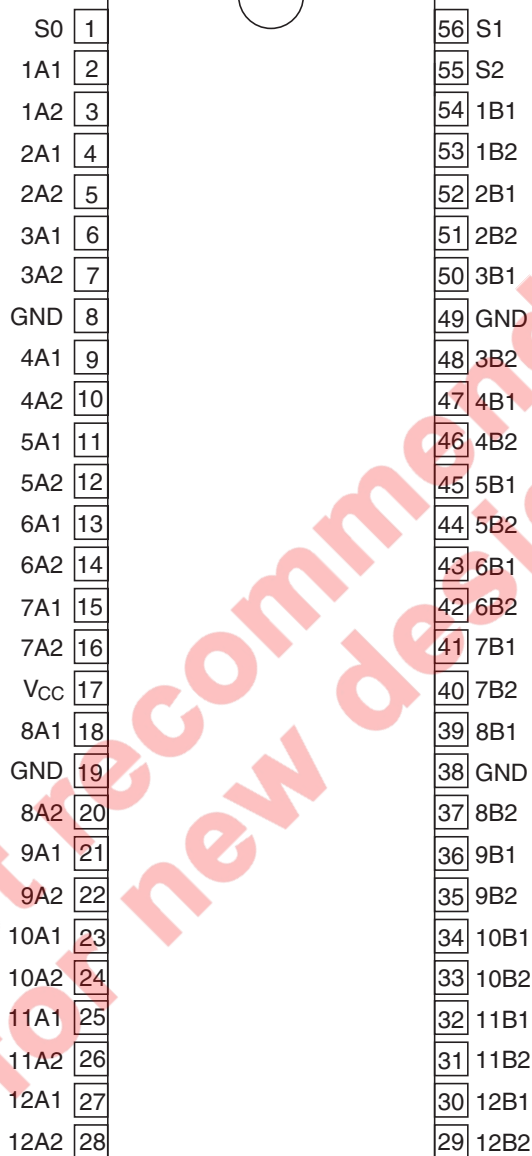
**Function Table**

Inputs			Inputs / Outputs		Function
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1 port	Z	A1 port = B1 port
L	H	L	B2 port	Z	A1 port = B2 port
L	H	H	Z	B1 port	A2 port = B1 port
H	L	L	Z	B2 port	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
H	H	H	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

H: High level  
L: Low level  
Z: High impedance

Not recommended  
for new design

Pin Arrangement



(Top view)

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Input clamp current	$I_{IK}$	-50	mA	$V_I < 0$
Continuous output current	$I_O$	128	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) <sup>2</sup>	$P_T$	1.32	W	
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

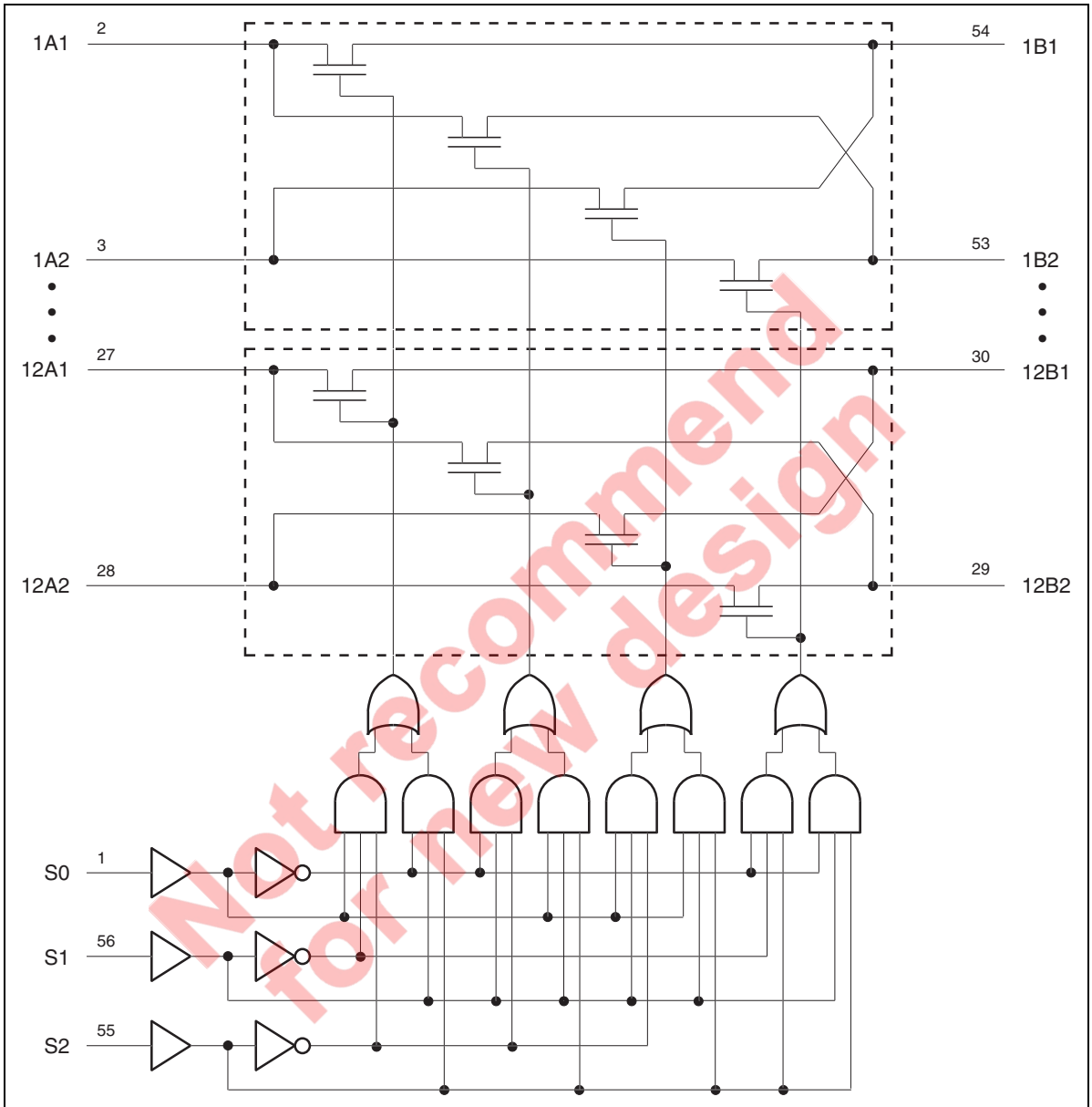
## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	4.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_{IO}$	0	5.5	V	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	5	ns / V	$V_{CC} = 4.5$ to $5.5$ V
Operating free-air temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.



Block Diagram



## DC Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ <sup>1</sup>	Max	Unit	Test conditions
Clamp diode voltage	V <sub>IK</sub>	4.5	—	—	-1.2	V	I <sub>IN</sub> = -18 mA
Input voltage	V <sub>IH</sub>	4.0 to 5.5	2.0	—	—	V	
	V <sub>IL</sub>	4.0 to 5.5	—	—	0.8		
On-state switch resistance <sup>2</sup>	R <sub>ON</sub>	4.0	—	14	20	Ω	V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA Typ at V <sub>CC</sub> = 4.0 V
		4.5	—	4	7		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA
		4.5	—	4	7		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA
		4.5	—	6	12		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±1.0	μA	V <sub>IN</sub> = 5.5 V or GND
Off-state leakage current	I <sub>OZ</sub>	5.5	—	—	±1.0	μA	0 ≤ A, B ≤ V <sub>CC</sub>
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	3	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 mA
Increase in I <sub>CC</sub> per input <sup>3</sup>	ΔI <sub>CC</sub>	5.5	—	—	2.5	mA	One input at 3.4 V, other inputs at V <sub>CC</sub> or GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), Ta = 25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## Capacitance

(Ta = 25°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	Test conditions
Control input capacitance	C <sub>IN</sub>	5.0	—	5	—	pF	V <sub>IN</sub> = 0 or 3 V
Input / output capacitance	C <sub>I/O(OFF)</sub>	5.0	—	9	—	pF	V <sub>O</sub> = 0 or 3 V S0, S1, or S2 = V <sub>CC</sub>

Note: This parameter is determined by device characterization is not production tested.

## Switching Characteristics

(Ta = -40 to 85°C)

- V<sub>CC</sub> = 4.0 V

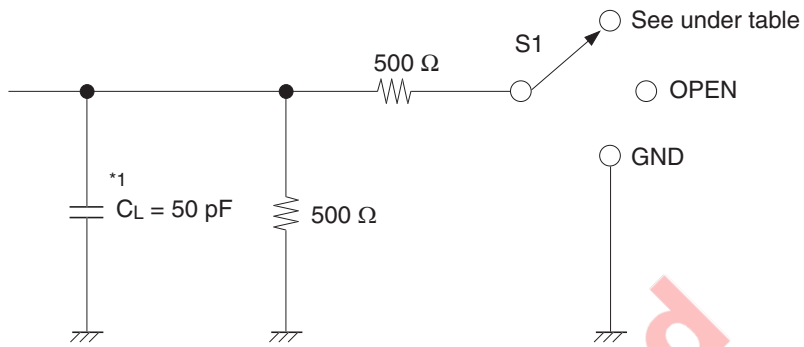
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time <sup>1)</sup>	t <sub>PLH</sub> t <sub>PHL</sub>	—	0.35	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	A or B	B or A
Propagation delay time	t <sub>PLH</sub> t <sub>PHL</sub>	—	10.0	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A or B
Enable time	t <sub>ZH</sub> t <sub>ZL</sub>	—	10.4	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A or B
Disable time	t <sub>HZ</sub> t <sub>LZ</sub>	—	9.2	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A or B

- V<sub>CC</sub> = 5.0±0.5 V

Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time <sup>1)</sup>	t <sub>PLH</sub> t <sub>PHL</sub>	—	0.25	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	A or B	B or A
Propagation delay time	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	9.1	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A or B
Enable time	t <sub>ZH</sub> t <sub>ZL</sub>	1.5	9.7	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A or B
Disable time	t <sub>HZ</sub> t <sub>LZ</sub>	1.5	8.8	ns	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω	S	A or B

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## Test Circuit

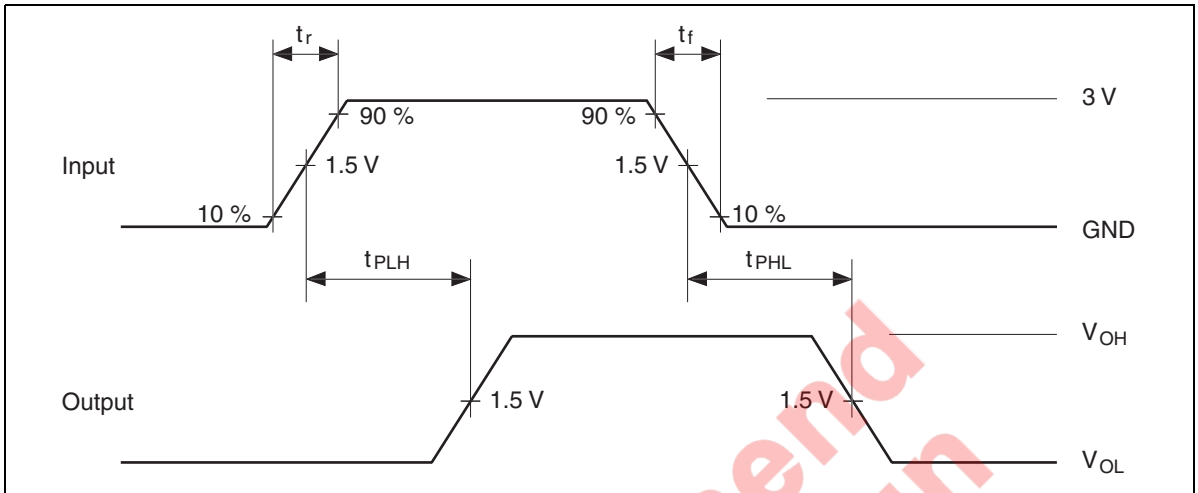


Load circuit for outputs

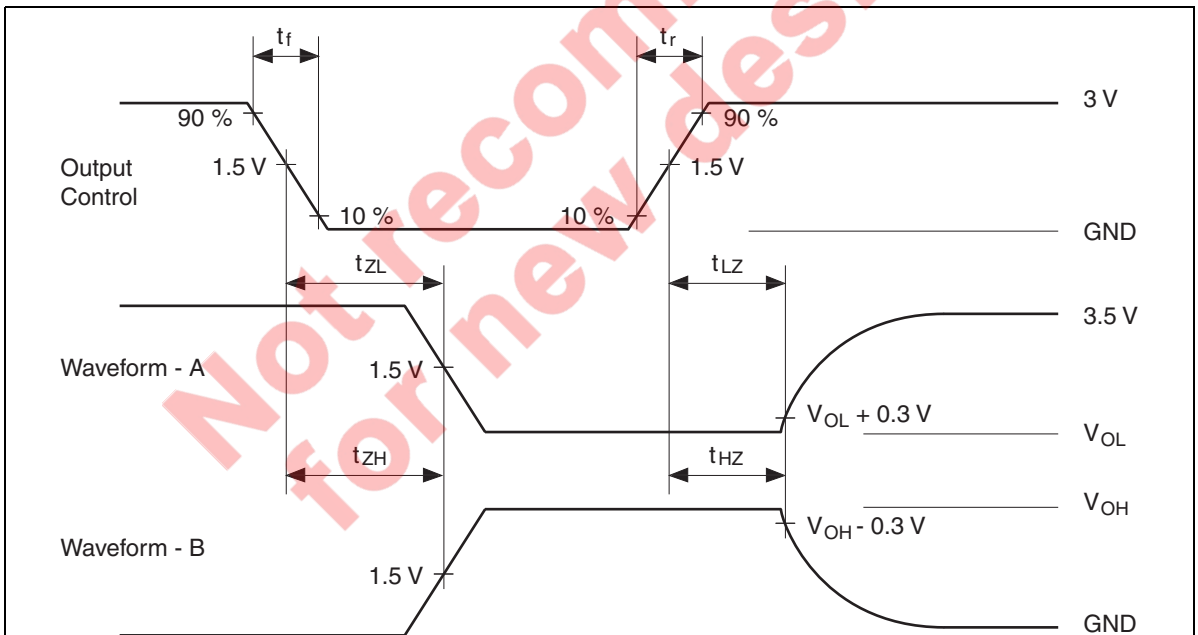
Symbol	S1
$t_{PLH} / t_{PHL}$	OPEN
$t_{ZH} / t_{HZ}$	OPEN
$t_{ZL} / t_{LZ}$	7 V

Note: 1.  $C_L$  includes probe and jig capacitance.

Waveforms – 1



Waveforms – 2

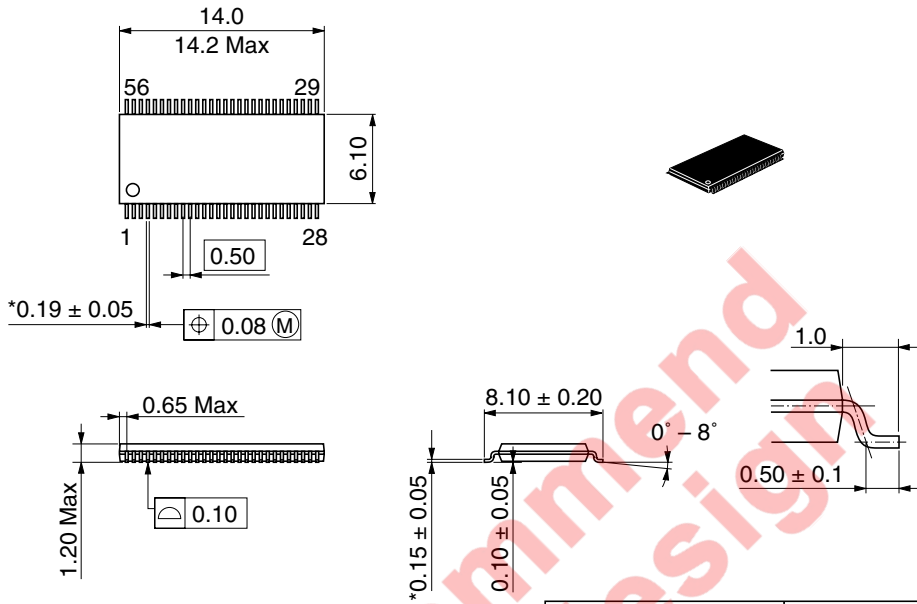


- Notes:
1. All input pulses are supplied by generators having the following characteristics :  
 $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

## Package Dimensions

As of July, 2001

Unit: mm



\*Pd plating

Hitachi Code	TTP-56DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.32 g

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