

Datasheet

Features

- CPU32+ Processor (4.5 MIPS at 25 MHz)
 - 32-bit Version of the CPU32 Core (Fully Compatible with the CPU32)
 - Background Debug Mode
 - Byte-misaligned Addressing
- Up to 32-bit Data Bus (Dynamic Bus Sizing for 8 and 16 Bits)
- Up to 32 Address Lines (At Least 28 Always Available)
- Complete Static Design (0 - 25 MHz Operation)
- Slave Mode to Disable CPU32+ (Allows Use with External Processors)
 - Multiple QUICCs Can Share One System Bus (One Master)
 - TS68040 Companion Mode Allows QUICC to be a TS68040 Companion Chip and Intelligent Peripheral (22 MIPS at 25 MHz)
 - Peripheral Device of TSPC603e (see DC415/D note)
- Four General-purpose Timers
 - Superset of MC68302 Timers
 - Four 16-bit Timers or Two 32-bit Timers
 - Gate Mode Can Enable/Disable Counting
- Two Independent DMAs (IDMAs)
- System Integration Module (SIM60)
- Communications Processor Module (CPM)
- Four Baud Rate Generators
- Four SCCs (Ethernet/IEEE 802.3 Optional on SCC1-Full 10 Mbps Support)
- Two SMC
- $V_{CC} = +5V \pm 5\%$
- $f_{max} = 25 \text{ MHz}$ and 33 MHz
- Military Temperature Range: $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$
- $P_D = 1.4\text{W}$ at 25 MHz; 5.25V
2W at 33 MHz; 5.25V



Description

The TS68EN360 QUad Integrated Communication Controller (QUICC™) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications activities. The QUICC (pronounced “quick”) can be described as a next-generation TS68302 with higher performance in all areas of device operation, increased flexibility, major extensions in capability, and higher integration.

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for the latest version of the datasheet

The term “quad” comes from the fact that there are four serial communications controllers (SCCs) on the device; however, there are actually seven serial channels: four SCCs, two serial management controllers (SMCs), and one serial peripheral interface (SPI).

Screening/Quality

This product is manufactured in full compliance with:

- QML (class Q)
- or according to e2v standards

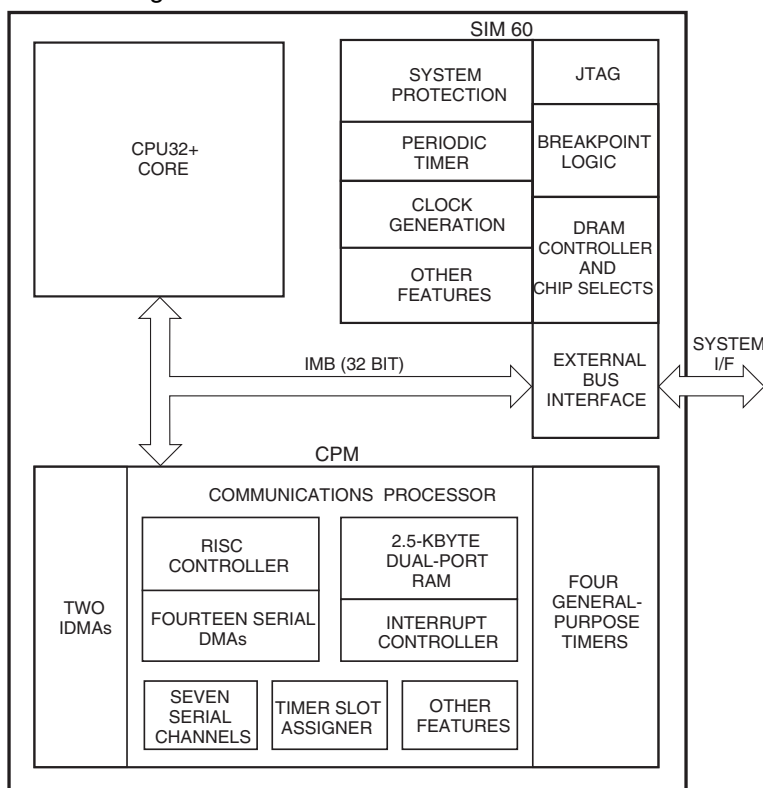
1. Introduction

1.1 QUICC Architecture Overview

The QUICC is 32-bit controller that is an extension of other members of the TS68300 family. Like other members of the TS68300 family, the QUICC incorporates the intermodule bus (IMB). The TS68302 is an exception, having an 68000 bus on chip. The IMB provides a common interface for all modules of the TS68300 family, which allows the development of new devices more quickly by using the library of existing modules. Although the IMB definition always included an option for an on-chip 32-bit bus, the QUICC is the first device to implement this option.

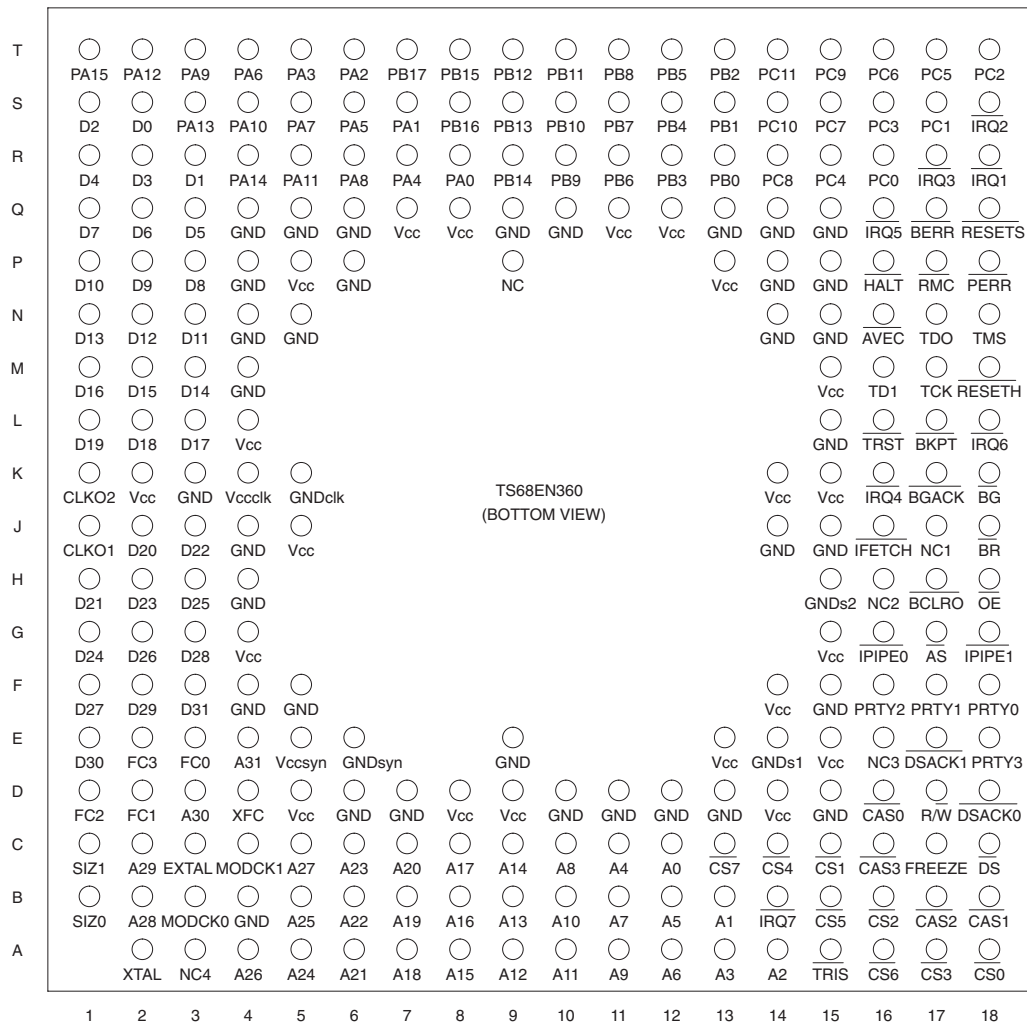
The QUICC is comprised of three modules: the CPU32+ core, the SIM60, and the CPM. Each module utilizes the 32-bit IMB. The TS68EN360 QUICC block diagram is shown in [Figure 1-1](#).

Figure 1-1. QUICC Block Diagram



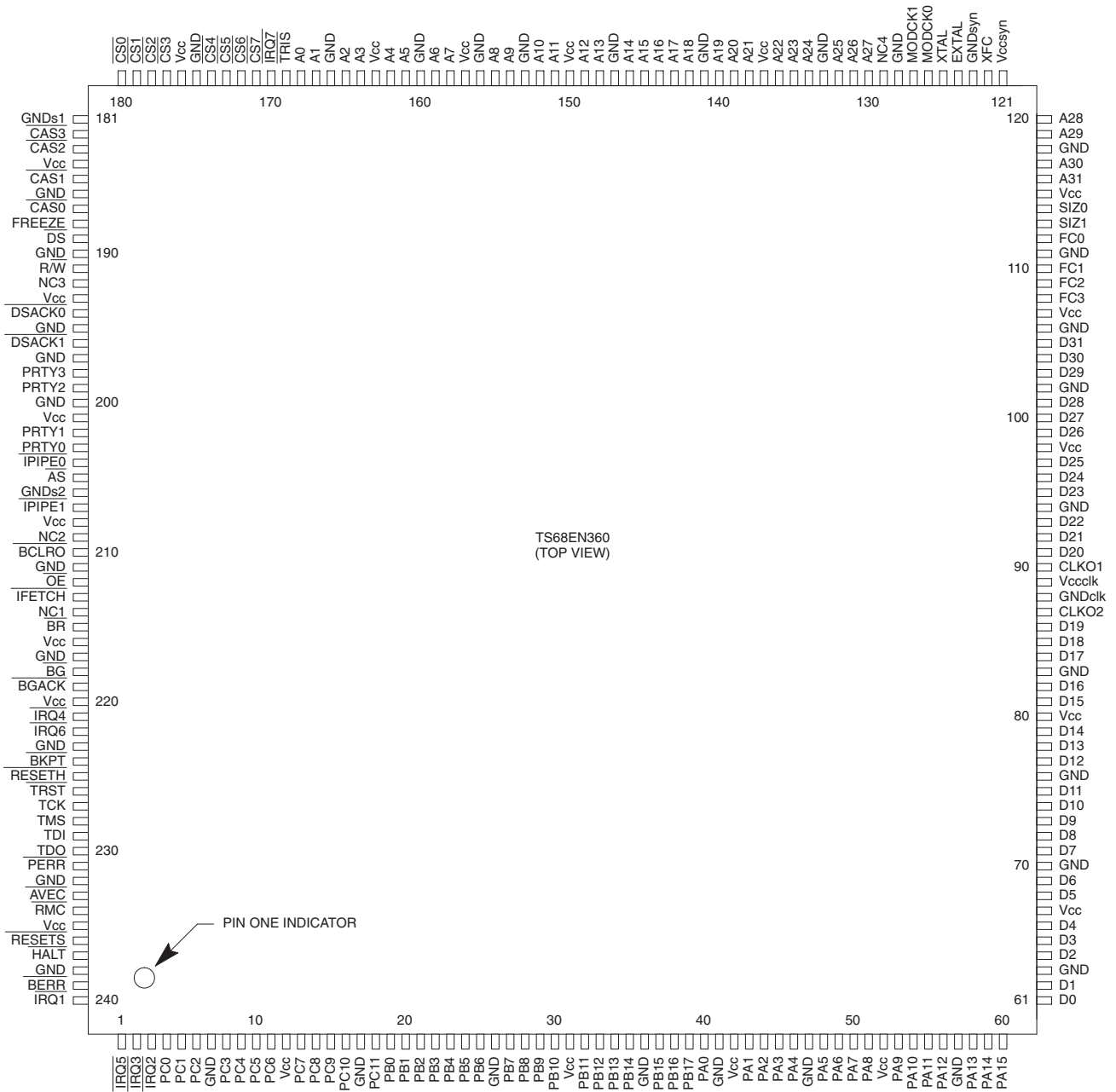
2. Pin Assignments

Figure 2-1. 241-lead Pin Grid Array (PGA)



Note: Pin P9 "NC" is for guide purposes only.

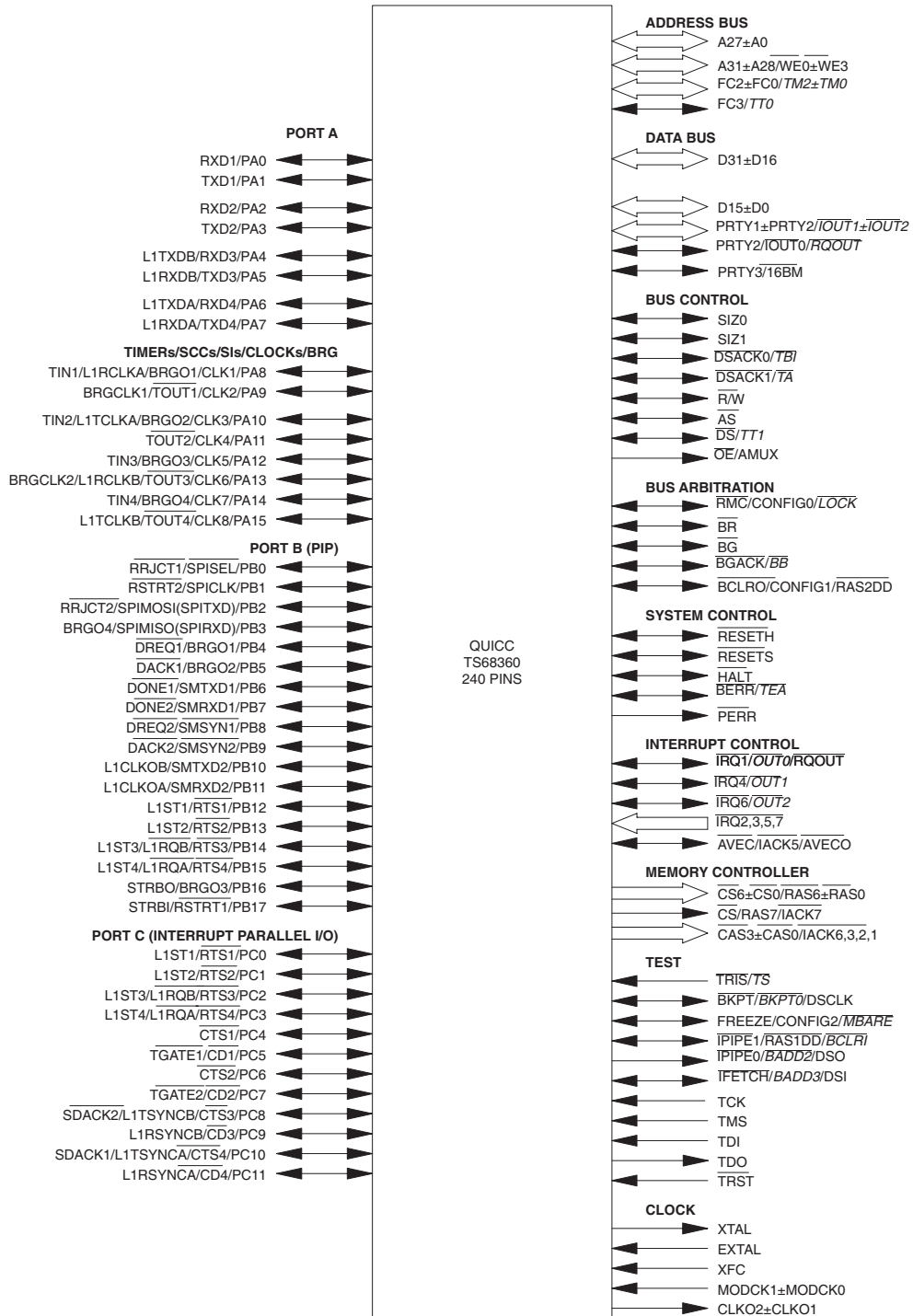
Figure 2-2. 240-lead Cerquad



3. Signal Description

3.1 Functional Signal Group

Figure 3-1. QUICC Functional Signal Groups



3.2 Signal Index

Table 1. System Bus Signal Index (Normal Operation)

| Group | Signal Name | Mnemonic | Function |
|-------------------|--|--|---|
| Address | Address Bus | A27-A0 | Lower 27 bits of address bus. (I/O) ⁽¹⁾ |
| | Address Bus/Byte Write Enables | A31-A28 $\overline{WE3-WE0}$ | Upper four bits of address bus (I/O), or byte write enable signals (O) ⁽¹⁾ for accesses to external memory or peripherals. |
| | Function Codes | FC3-FC0 | Identifies the processor state and the address space of the current bus cycle. (I/O) |
| Data | Data Bus 31 - 16 | D31-D16 | Upper 16-bit data bus used to transfer byte or word data. Used in 16-bit bus mode. (I/O) |
| | Data Bus 15 - 0 | D15-D0 | Lower 16-bit data bus used to transfer 3-byte or long-word data. (I/O) Not used in 16-bit bus mode. |
| Parity | Parity 2 - 0 | PRTY2-PRTY0 | Parity signals for byte writes/reads from/to external memory module. (I/O) |
| | Parity 3/ $\overline{16BM}$ | PRTY3/ $\overline{16BM}$ | Parity signals for byte writes/reads from/to external memory module or defines 16-bit bus mode. (I/O) |
| | Parity Error | \overline{PERR} | Indicates a parity error during a read cycle. (O) |
| Memory Controller | Chip Select Row Address Select 7 Interrupt Acknowledge 7 | \overline{CS} $\overline{RAS7}$ $\overline{IACK7}$ | Enables peripherals or DRAMs at programmed addresses (O) or interrupt level 7 acknowledge line. (O) |
| | Chip Select 6-0 Row Address Select 6-0 | $\overline{CS6-CS0}$ $\overline{RAS6-RAS0}$ | Enables peripherals or DRAMs at programmed addresses. (O) |
| | Column Address Select 3 - 0/Interrupt Acknowledge 1, 2, 3, 6 | $\overline{CAS3-CAS0}/$ $\overline{IACK6,3,2,1}$ | DRAM column address select or interrupt level acknowledge lines. (O) |
| Bus Arbitration | Bus Request | \overline{BR} | Indicates that an external device requires bus mastership. (I) ⁽¹⁾ |
| | Bus Grant | \overline{BG} | Indicates that the current bus cycle is complete and the QUICC has relinquished the bus. (O) |
| | Bus Grant Acknowledge | \overline{BGACK} | Indicates that an external device has assumed bus mastership. (I) |
| | Read-Modify-Write Cycle Initial Configuration 0 | \overline{RMC} CONFIG0 | Identifies the bus cycle as part of an indivisible read-modify-write operation (I/O) or initial QUICC configuration select. (I) |
| | Bus Clear Out/Initial Configuration 1/Row Address Select 2 Double-Drive | $\overline{BCLRO}/$ CONFIG1/ RAS2DD | Indicates that an internal device requires the external bus (Open-Drain O) or initial QUICC configuration select (I) or row address select 2 double-drive output. (O) |

Table 1. System Bus Signal Index (Normal Operation) (Continued)

| Group | Signal Name | Mnemonic | Function |
|-------------------|------------------------------------|---|--|
| Bus Control | Data and Size Acknowledge | $\overline{DSACK1} - \overline{DSACK0}$ | Provides asynchronous data transfer acknowledgement and dynamic bus sizing (open-drain I/O but driven high before three-stated) |
| | Address Strobe | \overline{AS} | Indicates that a valid address is on the address bus. (I/O) |
| | Data Strobe | \overline{DS} | During a read cycle, \overline{DS} indicates that an external device should place valid data on the data bus. During a write cycle, \overline{DS} indicates that valid data is on the data bus. (I/O) |
| | Size | SIZ1-SIZ0 | Indicates the number of bytes remaining to be transferred for this cycle. (I/O) |
| | Read/Write | R/\overline{W} | Indicates the direction of data transfer on the bus. (I/O) |
| | Output Enable Address Multiplex | $\overline{OE}/AMUX$ | Active during a read cycle indicates that an external device should place valid data on the data bus (O) or provides a strobe for external address multiplexing in DRAM accesses if internal multiplexing is not used. (O) |
| Interrupt Control | Interrupt Request Level 7-1 | $\overline{IRQ7}-\overline{IRQ1}$ | Provides external interrupt requests to the CPU32+ at priority levels 7-1. (I) |
| | Autovector/Interrupt Acknowledge 5 | $\overline{AVEC}/\overline{IACK5}$ | Autovector request during an interrupt acknowledge cycle (open-drain I/O) or interrupt level 5 acknowledge line. (O) |
| System Control | Soft Reset | \overline{RESETS} | Soft system reset. (open-drain I/O) |
| | Hard Reset | \overline{RESETH} | Hard system reset. (open-drain I/O) |
| | Halt | \overline{HALT} | Suspends external bus activity. (open-drain I/O) |
| | Bus Error | \overline{BERR} | Indicates an erroneous bus operation is being attempted. (open-drain I/O) |

Table 1. System Bus Signal Index (Normal Operation) (Continued)

| Group | Signal Name | Mnemonic | Function |
|----------------------------|--|--|--|
| Clock and Test | System Clock Out 1 | CLKO1 | Internal system clock output 1. (O) |
| | System Clock Out 2 | CLKO2 | Internal system clock output 2 - normally 2x CLKO1. (O) |
| | Crystal Oscillator | EXTAL, XTAL | Connections for an external crystal to the internal oscillator circuit. EXTAL (I), XTAL (O) |
| | External Filter Capacitor | XFC | Connection pin for an external capacitor to filter the circuit of the PLL. (I) |
| | Clock Mode Select 1-0 | MODCK1-MODCK0 | Selects the source of the internal system clock. (I) THESE PINS SHOULD NOT BE SET TO 00 |
| | Instruction Fetch/ Development Serial Input | $\overline{\text{IFETCH}}/\text{DSI}$ | Indicates when the CPU32+ is performing an instruction word prefetch (O) or input to the CPU32+ background debug mode. (I) |
| | Instruction Pipe 0/ Development Serial Output | $\overline{\text{IPIPE0}}/\text{DSO}$ | Used to track movement of words through the instruction pipeline (O) or output from the CPU32+ background debug mode. (O) |
| | Instruction Pipe 1/Row Address Select 1 Double-Drive | $\overline{\text{IPIPE1}}/\text{RAS1DD}$ | Used to track movement of words through the instruction pipeline (O), or a row address select 1 "double-drive" output (O) |
| | Breakpoint/Development Serial Clock | $\overline{\text{BKPT}}/\text{DSCLK}$ | Signals a hardware breakpoint to the QUICC (open-drain I/O), or clock signal for CPU32+ background debug mode (I) |
| | Freeze/Initial Configuration 2 | FREEZE/CONFIG2 | Indicates that the CPU32+ has acknowledged a breakpoint (O), or initial QUICC configuration select (I) |
| Clock and Test (Cont'd) | Three-State | $\overline{\text{TRIS}}$ | Used to three-state all pins if QUICC is configured as a master. Always Sampled except during system reset. (I) |
| | Test Clock | TCK | Provides a clock for Scan test logic. (I) |
| | Test Mode Select | TMS | Controls test mode operations. (I) |
| | Test Data In | TDI | Serial test instructions and test data signal. (I) |
| | Test Data Out | TDO | Serial test instructions and test data signal. (O) |
| | Test Reset | $\overline{\text{TRST}}$ | Provides an asynchronous reset to the test controller. (I) |
| Power | Clock Synthesizer Power | VCCSYN | Power supply to the PLL of the clock synthesizer |
| | Clock Synthesizer Ground | GNDSYN | Ground supply to the PLL of the clock synthesizer |
| | Clock Out Power | VCCCLK | Power supply to clock out pins |
| | Clock Out Ground | GNDCLK | Ground supply to clock out pins |
| | Special Ground 1 | GNDS1 | Special ground for fast AC timing on certain system bus signals |
| | Special Ground 2 | GNDS2 | Special ground for fast AC timing on certain system bus signals |
| | System Power Supply and Return | VCC, GND | Power supply and return to the QUICC |
| -- | No Connect | NC4-NC1 | Four no-connect pins |

Note: 1. I denotes input, O denotes output and I/O is input/output.

Table 3-1. Peripherals Signal Index

| Group | Signal Name | Mnemonic | Function |
|-------|-------------------------|--|--|
| SCC | Receive Data | RXD4-RXD1 | Serial receive data input to the SCCs. (I) |
| | Transmit Data | TXD4-TXD1 | Serial transmit data output from the SCCs. (O) |
| | Request to Send | $\overline{\text{RTS4}}\text{-}\overline{\text{RTS1}}$ | Request to send outputs indicate that the SCC is ready to transmit data. (O) |
| | Clear to Send | $\overline{\text{CTS4}}\text{-}\overline{\text{CTS1}}$ | Clear to send inputs indicate to the SCC that data transmission may begin. (I) |
| | Carrier Detect | $\overline{\text{CD4}}\text{-}\overline{\text{CD1}}$ | Carrier detect inputs indicate that the SCC should begin reception of data. (I) |
| | Receive Start | $\overline{\text{RSTR1}}$ | This output from SCC1 identifies the start of a receive frame. Can be used by an Ethernet CAM to perform address matching. (O) |
| | Receive Reject | RRJCT1 | This input to SCC1 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match. (I) |
| | Clocks | CLK8-CLK1 | Input clocks to the SCCs, SCMs, SI, and the baud rate generators. (I) |
| IDMA | DMA Request | $\overline{\text{DREQ2}}\text{-}\overline{\text{DREQ1}}$ | A request (input) to an IDMA channel to start an IDMA transfer. (I) |
| | DMA Acknowledge | $\overline{\text{DACK2}}\text{-}\overline{\text{DACK1}}$ | An acknowledgement (output) by the IDMA that an IDMA transfer is in progress. (O) |
| | DMA Done | $\overline{\text{DONE2}}\text{-}\overline{\text{DONE1}}$ | A bidirectional signal that indicates the last IDMA transfer in a block of data. (I/O) |
| TIMER | Timer Gate | $\overline{\text{TGATE2}}\text{-}\overline{\text{TGATE1}}$ | An input to a timer that enables/disables the counting function. (I) |
| | Timer Input | TIN4-TIN1 | Time reference input to the timer that allows it to function as a counter. (I) |
| | Timer Output | $\overline{\text{TOUT4}}\text{-}\overline{\text{TOUT1}}$ | Output waveform (pulse or toggle) from the timer as a result of a reference value being reached. (O) |
| SPI | SPI Master In Slave Out | SPIMISO | Serial data input to the SPI master (I); serial data output from an SPI slave. (O) |
| | SPI Master Out Slave In | SPIMOSI | Serial data output from the SPI master (O); serial data input to an SPI slave. (I) |
| | SPI Clock | SPICLK | Output clock from the SPI master (O); input clock to the SPI slave. (I) |
| | SPI Select | $\overline{\text{SPISEL}}$ | SPI slave select input. (I) |
| SMC | SMC Receive Data | SMRXD2-SMRXD1 | Serial data input to the SMCs. (I) |
| | SMC Transmit Data | SMTXD2-SMTXD1 | Serial data output from the SMCs. (O) |
| | SMC Sync | $\overline{\text{SMSYN2}}\text{-}\overline{\text{SMSYN1}}$ | SMC synchronization signal. (I) |

Table 3-1. Peripherals Signal Index (Continued)

| Group | Signal Name | Mnemonic | Function |
|-------|-----------------------------|-----------------------|--|
| SI | SI Receive Data | L1RXDA, L1RXDB | Serial input to the time division multiplexed (TDM) channel A or channel B |
| | SI Transmit Data | L1TXDA, L1TXDB | Serial output from the TDM channel A or channel B |
| | SI Receive Clock | L1RCLKA, L1RCLKB | Input receive clock to TDM channel A or channel B |
| | SI Transmit Clock | L1TCLKA, L1TCLKB | Input transmit clock to TDM channel A or channel B |
| | SI Transmit Sync Signals | L1TSYNCA, L1TSYNCB | Input transmit data sync signal to TDM channel A or channel B |
| | SI Receive Sync Signals | L1RSYNCA, L1RSYNCB | Input receive data sync signal to TDM channel A or channel B |
| | IDL Interface Request | L1RQA, L1RQB | IDL interface request to transmit on the D channel. Output from the SI |
| | SI Output Clock | L1CLKOA, L1CLKOB | Output serial data rate clock. Can output a data rate clock when the input clock is 2x the data rate |
| | SI Data Stobes | L1ST4-L1ST1 | Serial data strobe outputs can be used to gate clocks to external devices that do not have a built-in time slot assigner (TSA) |
| BRG | Baud Rate Generator Out 4-1 | BRGO4-BRGO1 | Baud rate generator output clock allows baud rate generator to be used externally |
| | BRG Input Clock | CLK2, CLK6 | Baud rate generator input clock from which BRG will derive the baud rates |
| PIP | Port B 15-0 | PB15-BP0 | PIP Data I/O Pins |
| | Strobe Out | STRBO | This input causes the PIP output data to be placed on the PIP data pins |
| | Strobe In | STRBI | This input causes data on the PIP data pins to be latched by the PIP as input data |
| SDMA | SDMA Acknowledge 2-1 | <u>SDACK2-SDACK1</u> | SDMA output signals used in RISC receiver to mark fields in the Ethernet receive frame |

4. Detailed Specification

This specification describes the specific requirements for the microcontroller TS68EN360 - 25 MHz and 33 MHz in compliance with MIL-STD-883 class B or e2v standard screening.

5. Applicable Documents

1. MIL-STD-883: test methods and procedures for electronics
2. MIL-PRF-38535: general specifications for microcircuits
3. DESC 5962-SMD-97607

The microcircuits are in accordance with the applicable document and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

Depending on the package, the terminal connections shall be as shown in [Figure 2-1](#) and [Figure 2-2](#).

5.1.2 Lead Material and Finish

Lead material and finish shall be as specified in MIL-STD-883 (see enclosed [“Ordering Information” on page 79](#))

5.1.3 Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 or as follow:

- PGA but see [“241-pin – PGA” on page 77](#)
- CERQUAD

The precise case outlines are described at the end of the specification ([“Package Mechanical Data” on page 77](#)) and into MIL-STD-1835.

5.2 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|----------------------------------|-----------|--------------|------|
| Supply Voltage ⁽¹⁾⁽²⁾ | V_{CC} | -0.3 to +6.5 | V |
| Input Voltage ⁽¹⁾⁽²⁾ | V_{IN} | -0.3 to +6.5 | V |
| Storage Temperature Range | T_{STG} | -55 to +150 | °C |

- Notes:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
 2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
 3. The supply voltage V_{CC} must start and restart from 0.0V; otherwise, the 360 will not come out of reset properly. Unless otherwise stated, all voltages are referenced to the reference terminal.

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD})

Table 5-2. Recommended Conditions of Use
Unless otherwise stated, all voltages are referenced to the reference terminal

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------|--------------------------------------|----------------------|-----|----------|------|
| V_{CC} | Supply Voltage Range | +4.75 | | +5.25 | V |
| V_{IL} | Logic Low Level Input Voltage Range | GND | | +0.8 | V |
| V_{IH} | Logic High Level Input Voltage Range | +2.0 | | V_{CC} | V |
| T_{case} | Operating Temperature | -55 | | +125 | °C |
| V_{OH} | High Level Output Voltage | +2.4 | | | V |
| f_{sys} | System Frequency | (For 25 MHz version) | | 25 | MHz |
| | | (For 33 MHz version) | | 33 | MHz |

Table 5-3. Thermal Characteristics

| Symbol | Parameter | | Value | Unit |
|---------------|--|-----------------|-------|------|
| θ_{JC} | Thermal Resistance - Junction to Case | 240-pin Cerquad | 2 | °C/W |
| | | 241-pin PGA | 7 | |
| θ_{JA} | Thermal Resistance - Junction to Ambient | 240-pin Cerquad | 27.4 | °C/W |
| | | 241-pin PGA | 22.8 | |

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

$$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$$

Where $P_{I/O}$ is the power dissipation on pins.

5.3 Power Considerations

The average chip-junction temperature, T_J , in °C can be obtained from:

$$T_J = T_A \div (P_D \cdot \theta_{JA}) \tag{1}$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance,
Junction-to-Ambient, C/W

$$P_D = P_{INT} + P_{I/O}$$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts-chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins-User Determined

For most applications, $P_{I/O} < 0.3 \cdot P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \Theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring P_D (at thermal equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A .

5.4 Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for e2v standard screening.

5.5 Marking

The documents where the markings are defined are identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as a minimum:

- e2v logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

6. Quality Conformance Inspection

6.1 DESC/MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspections are performed on a periodical basis.

7. Electrical Characteristics

7.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Static electrical characteristics for the electrical variants
- Dynamic electrical characteristics for TS68EN360 (25 MHz, 33 MHz)

For static characteristics, test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause [Table 7-1](#) of this specification.

7.2 Static Characteristics

The electrical specifications in this document are preliminary. (See numbered notes)

Table 7-1. Static Characteristics – GND = 0 V_{DC}, T_C = -55 to +125°C

| Characteristic | Symbol | Min | Max | Unit |
|--|------------------|------------------------|---------------------------------|------|
| Input High Voltage (except EXTAL) | V _{IH} | 2.0 | V _{CC} | V |
| Input Low Voltage (5V Part) | V _{IL} | GND | 0.8 | V |
| Input Low Voltage (Part Only; PA8-15, PB1, PC5, PC7, TCK) | V _{IL} | GND | 0.5 | V |
| Input Low Voltage (Part Only; All Other Pins) | V _{IL} | GND | 0.8 | V |
| EXTAL Input High Voltage | V _{IHC} | 0.8*(V _{CC}) | V _{CC} + 0.3 | V |
| Undershoot | – | – | -0.8 | V |
| Input Leakage Current (All Input Only Pins except for TMS, TDI and TRST) V _{in} = 0/5V | I _{in} | -2.5 | 2.5 | μA |
| Hi-Z (Off-State) Leakage Current (All Noncrystal Outputs and I/O Pins except TMS, TDI and TRST) V _{in} = 0/5V | I _{OZ} | -2.5 | -2.5 | μA |
| Signal Low Input Current V _{IL} = 0.8V (TMS, TDI and TRST Pins Only) | I _L | -0.5 | 0.5 | mA |
| Signal High Input Current V _{IH} = 2.0V (TMS, TDI and TRST Pins Only) | I _H | -0.5 | 0.5 | mA |
| Output High Voltage I _{OH} = -0.8 mA, V _{CC} = 4.75V All Noncrystal Outputs Except Open Drain Pins | V _{OH} | 2.4 | – | V |
| Output Low Voltage I _{OL} = 2.0 mA, CLK01-2, FREEZE, $\overline{\text{PIPE0-7}}$, $\overline{\text{FETCH}}$, $\overline{\text{BKPT0}}$ I _{OL} = 3.2 mA, A31-A0, D31-D0, FC3-0, SIZ0-1, PA0, 2, 4, 6, 8-15, PB0-5, PB8-17, PC0-11, TDO, $\overline{\text{PERR}}$, PRTY0-3, $\overline{\text{IOUT0-2}}$, $\overline{\text{AVECO}}$, $\overline{\text{AS}}$, $\overline{\text{CAS3-0}}$, $\overline{\text{BLCRO}}$, $\overline{\text{RAS0-7}}$ I _{OL} = 5.3 mA, $\overline{\text{DSACK0-7}}$, R/W, $\overline{\text{DS}}$, $\overline{\text{OE}}$, $\overline{\text{RMC}}$, $\overline{\text{BG}}$, $\overline{\text{BGACK}}$, $\overline{\text{BERR}}$ I _{OL} = 7 mA, TXD1-4 I _{OL} = 8.9 mA, PB6, PB7, $\overline{\text{HALT}}$, $\overline{\text{RESET}}$, $\overline{\text{BR}}$ (Output) | V _{OL} | – | 0.5 0.5 0.5 0.5 0.5 | V |
| Input Capacitance All I/O Pins | C _{in} | – | 20 | pF |
| Load Capacitance (except CLK01-2) | C _L | – | 100 | pF |
| Load Capacitance (CLK01-2) | C _{Lc} | – | 50 | pF |
| Power | V _{CC} | 4.75 | 5.25 | V |

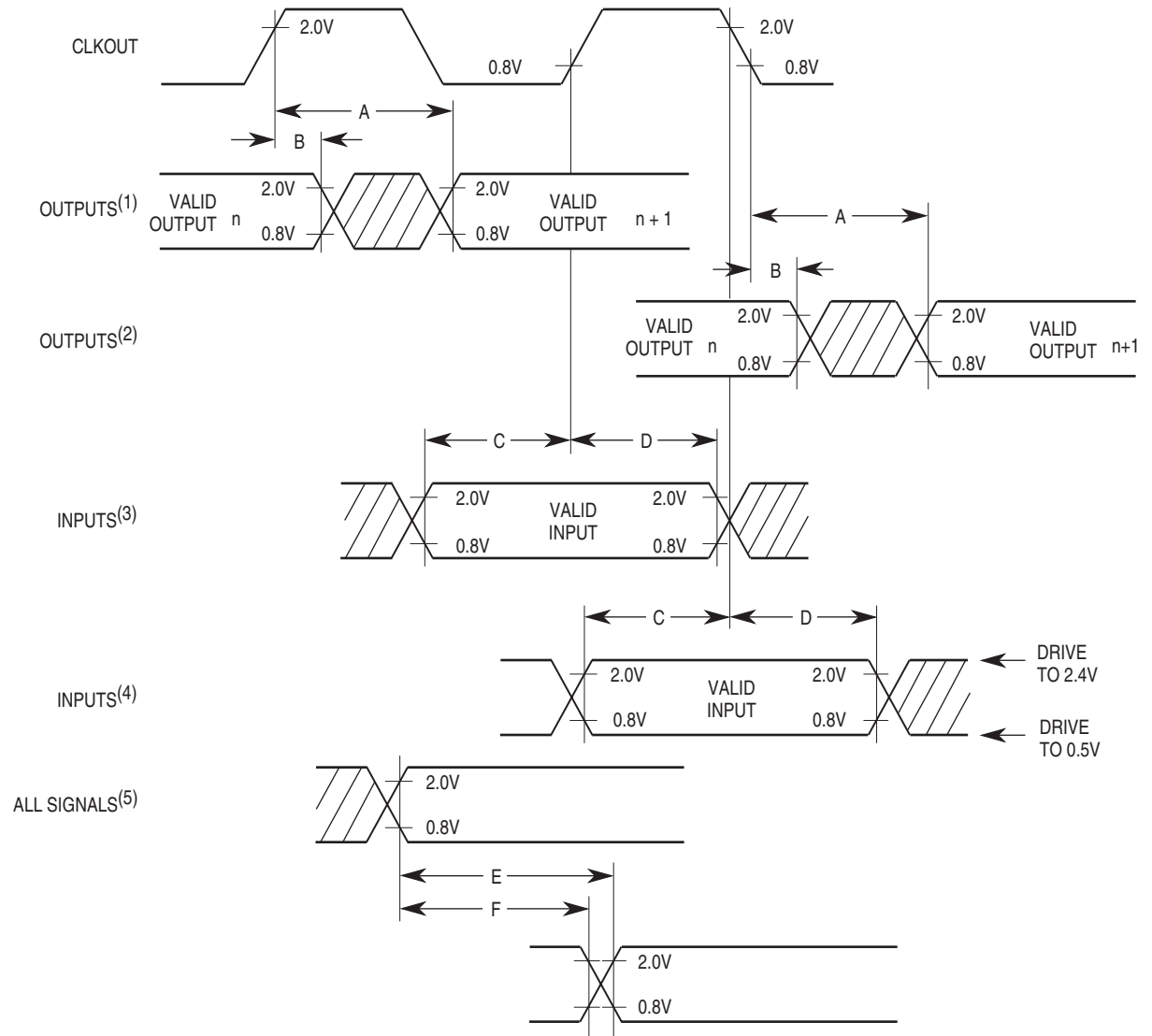
7.3 Dynamic Characteristics

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in [Figure 7-1](#). To test the parameters guaranteed by e2v inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times and are measured as shown. Finally, the measurement for signal-to-signal specifications are shown.

Note that the testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

Figure 7-1. Drive Levels and Test Points For AC Specifications



- Notes:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock
 2. This output timing is applicable to all parameters specified relative to the falling edge of the clock
 3. This input timing is applicable to all parameters specified relative to the rising edge of the clock
 4. This input timing is applicable to all parameters specified relative to the falling edge of the clock
 5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal

Legend:

- a) Maximum output delay specification
- b) Minimum output hold time
- c) Minimum input setup time specification
- d) Minimum input hold time specification
- e) Signal valid to signal valid specification (maximum or minimum)
- f) Signal valid to signal invalid specification (maximum or minimum)

7.4 AC Power Dissipation

Table 7-2. Typical Current Drain

| Mode of Operation | Symbol | System Clock Frequency | BRGCLK Clock Frequency | SyncCLK Clock Frequency | Typ | Unit |
|--|------------|---------------------------|--------------------------|-------------------------|-----|------|
| Normal mode (Rev A ⁽¹⁾ and Rev B ⁽²⁾) | I_{DD} | 25 MHz | 25 MHz | 25 MHz | 250 | mA |
| Normal Mode (Rev C ⁽³⁾ and Newer) | I_{DD} | 25 MHz | 25 MHz | 25 MHz | 237 | mA |
| Normal Mode | I_{DD} | 33 MHz | 33 MHz | 33 MHz | 327 | mA |
| Low Power Mode | I_{DDSB} | Divide by 2 12.5 MHz | Divide by 16 1.56 MHz | Divide by 2 12.5 MHz | 150 | mA |
| Low Power Mode | I_{DDSB} | Divide by 4 6.25 MHz | Divide by 16 1.56 MHz | Divide by 4 6.25 MHz | 85 | mA |
| Low Power Mode | I_{DDSB} | Divide by 16 1.56 MHz | Divide by 16 1.56 MHz | Divide by 4 6.25 MHz | 35 | mA |
| Low Power Mode | I_{DDSB} | Divide by 256 97.6 kHz | Divide by 16 1.56 MHz | Divide by 4 6.25 MHz | 20 | mA |
| Low Power Mode | I_{DDSB} | Divide by 256 97.6 kHz | Divide by 64 390 kHz | Divide by 64 390 kHz | 13 | mA |
| Low Power Stop VCO Off ⁽⁴⁾ | I_{DDSP} | | | | 0.5 | mA |
| PLL Supply Current | | | | | | |
| PLL Disabled | I_{DDPD} | | | | TBD | |
| PLL Enabled | I_{DDPE} | | | | TBD | |

- Notes: 1. Rev A mask is C63T
 2. Rev B masks are C69T and F35G
 3. Current Rev C masks are E63C, E68C and F15W
 4. EXTAL frequency is 32 kHz

All measurements were taken with only CLK01 enabled, $V_{CC} = 5.0V$, $V_{IL} = 0V$ and $V_{IH} = V_{CC}$

Table 7-3. Maximum Power Dissipation

| System Frequency | V_{CC} | Max P_D | Unit | Mask |
|------------------|----------|-----------|------|---|
| 25 MHz | 5.25V | 1.80 | W | REV A ⁽¹⁾ and REV B ⁽²⁾ |
| 25 MHz | 5.25V | 1.45 | W | REV C ⁽³⁾ and Newer |
| 25 MHz | 3.6V | 0.65 | W | REV C ⁽³⁾ and Newer |
| 33 MHz | 5.25V | 2.00 | W | REV C ⁽³⁾ and Newer |

- Notes: 1. Rev A mask is C63T
 2. Rev B masks are C69T and F35G
 3. Current Rev C masks are E63C, E68C and F15W

7.5 AC Electrical Specifications Control Timing

Table 7-4. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-2)

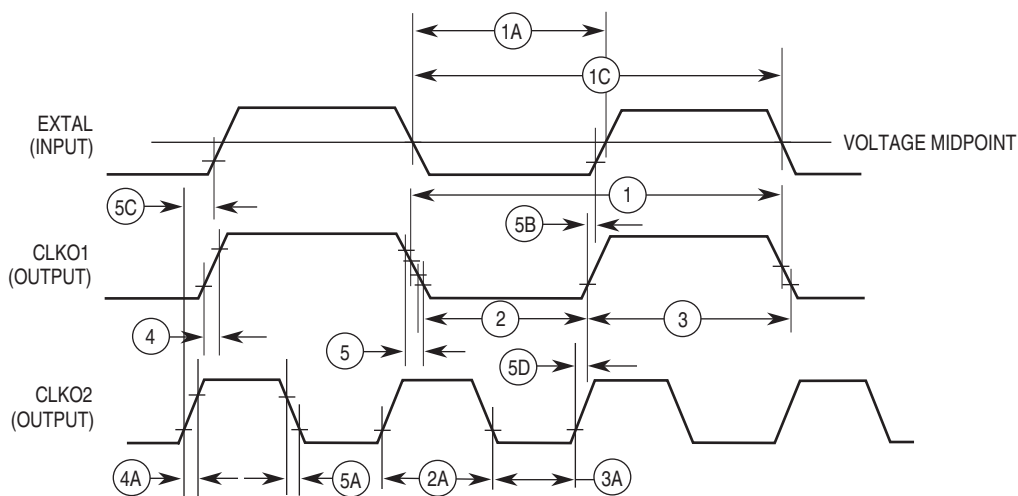
| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|--------|--|---------------------|-------------------|-------|-----------|-------|------|
| | | | Min | Max | Min | Max | |
| | System Frequency | f _{sys} | dc ⁽¹⁾ | 25.00 | | 33.34 | MHz |
| | Crystal Frequency | f _{XTAL} | 25 | 6000 | 25 | 6000 | kHz |
| | On-Chip VCO System Frequency | f _{sys} | 20 | 50 | 20 | 67 | MHz |
| | Start-up Time With external clock (oscillator disabled) or after changing the multiplication factor MF | t _{pll} | | 2500 | | | clks |
| | CLKO1-2 stability | Δ _{CLK} | TBD | TBD | | | % |
| 1 | CLKO1 Period | t _{cyc} | 40 | – | 30 | – | ns |
| 1A | EXTAL Duty Cycle, MF | t _{dcyc} | 40 | 60 | 40 | 60 | % |
| 1C | External Clock Input Period | t _{EXTcyc} | 40 | – | 30 | – | ns |
| 2, 3 | CLKO1 Pulse Width (Measured at 1.5V) | t _{CW1} | 19 | – | 14 | – | ns |
| 2A, 3A | CLKO2 Pulse Width (Measured at 1.5V) | t _{CW2} | 9.5 | – | 7 | – | ns |
| 4, 5 | CLKO1 Rise and Fall Times (Full drive) | t _{Crf1} | – | 2 | – | 2 | ns |
| 4A, 5A | CLKO2 Rise and Fall Times (Full drive) | t _{Crf2} | – | 2 | – | 1.6 | ns |
| 5B | EXTAL to CLKO1 Skew-PLL enabled (MF < 5) | t _{EXTP1} | | a | | a | ns |
| 5C | EXTAL to CLKO2 Skew-PLL enabled (MF < 5) | t _{EXTP2} | | a | | a | ns |
| 5D | CLKO1 to CLKO2 Skew | e2v _{KW} | | a | | a | ns |

Note: 1. Note that the minimum VCO frequency and the PLL default values put some restrictions on the minimum system frequency.

The following calculation should be used to determine the actual value for specifications 5B, 5C and 5D.

- 5B: 25 MHz ±(0.9 ns + 0.25 x (rise time)) (1.4 ns at rise = 2 ns; 1.9 ns at rise = 4 ns)
- 33 MHz ±(0.5 ns + 0.25 x (rise time)) (1 ns at rise = 2 ns; 1.5 ns at rise = 4 ns)
- 5C: 25/33 MHz ±(2 ns + 0.25 x (rise time)) (2.5 ns at rise = 2 ns; 3 ns at rise = 4 ns)
- 5D: 25 MHz ±(3 ns + 0.5 x (rise time)) (4 ns at rise = 2 ns; 5 ns at rise = 4 ns)
- 33 MHz ±(2.5 ns + 0.5 x (rise time)) (3.5 ns at rise = 2 ns; 4.5 ns at rise = 4 ns)

Figure 7-2. Clock Timing



7.6 External Capacitor For PLL

Table 7-5. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary.

| Characteristic | Symbol | Min | Max | Unit |
|---|------------------|----------|----------|------|
| PLL External Capacitor (XFC to VCCSYN) | C _{XFC} | | | |
| MF < 5 (Recommended value MF x 400 pF) ⁽¹⁾ | | MF x 340 | MF x 480 | pF |
| MF > 4 (Recommended value MF x 540 pF) ⁽¹⁾ | | MF x 380 | MF x 970 | pF |

Note: 1. MF – multiplication factor.

7.6.1 Examples:

- Notes:
- MODCK1 pin = 0, MF = 1 ⇒ C_{XFC} = 400 pF
 - MODCK1 pin = 1, crystal is 32.768 kHz (or 4.192 MHz), initial MF = 401, initial frequency = 13.14 MHz, later on MF is changed to 762 to support a frequency of 25 MHz. Minimum C_{XFC} is: 762 x 380 = 289 nF, Maximum C_{XFC} is: 401 x 970 = 390 nF. The recommended C_{XFC} for 25 MHz is: 762 x 540 = 414 nF. 289 nF < C_{XFC} < 390 nF and closer to 414 nF. The proper available value for C_{XFC} is 390 nF.
 - MODCK1 pin = 1, crystal is 32.768 kHz (or 4.192 MHz), initial MF = 401, initial frequency = 13.14 MHz, later on MF is changed to 1017 to support a frequency of 33.34 MHz. Minimum C_{XFC} is: 1017 x 380 = 386 nF, Maximum C_{XFC} is: 401 x 970 = 390 nF ⇒ 386 nF < C_{XFC} < 390 nF. The proper available value for C_{XFC} is 390 nF.
 - In order to get higher range, higher crystal frequency can be used (i.e. 50 kHz), in this case: Minimum C_{XFC} is: 667 x 380 = 253 nF, Maximum C_{XFC} is: 401 x 970 = 390 nF ⇒ 386 nF < C_{XFC} < 390 nF.

7.7 Bus Operation AC Timing Specifications

Table 7-6. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-3 to Figure 7-19)

| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|---------------------------|--|--------------------|--------|-----|-----------|-------|------|
| | | | Min | Max | Min | Max | |
| 6 | CLKO1 High to Address, FC, SIZ, \overline{RMC} Valid | t _{CHAV} | 0 | 15 | 0 | 12 | ns |
| 6A | CLKO1 High to Address Valid (GAMX = 1) | t _{CHAV} | 0 | 20 | 0 | 15 | ns |
| 7 | CLKO1 High to Address, Data, FC, SIZ, \overline{RMC} High Impedance | t _{CHAZx} | 0 | 40 | 0 | 30 | ns |
| 8 | CLKO1 High to Address, Data, FC, SIZ, \overline{RMC} Invalid | t _{CHAZn} | -2 | – | -2 | – | ns |
| 9 | CLKO1 Low to \overline{AS} , \overline{DS} , \overline{OE} , \overline{WE} , \overline{IFETCH} , \overline{IPIPE} , \overline{IACKx} Asserted | t _{CLSA} | 3 | 20 | 3 | 15 | ns |
| 9 ⁽¹⁰⁾ | CLKO1 Low to $\overline{CSx}/\overline{RASx}$ Asserted | t _{CLSA} | 4 | 16 | 4 | 12 | ns |
| 9B ⁽¹¹⁾ | CLKO1 High to $\overline{CSx}/\overline{RASx}$ Asserted | t _{CHCA} | 4 | 16 | 4 | 12 | ns |
| 9A ⁽²⁾⁽¹⁰⁾ | \overline{AS} to \overline{DS} or $\overline{CSx}/\overline{RASx}$ or \overline{OE} Asserted (Read) | t _{STSA} | -6 | 6 | -5.625 | 5.625 | ns |
| 9C ⁽²⁾⁽¹¹⁾ | \overline{AS} to $\overline{CSx}/\overline{RASx}$ Asserted | t _{STCA} | 14 | 26 | 9 | 21 | ns |
| 11 ⁽¹⁰⁾ | Address, FC, SIZ, \overline{RMC} , valid to \overline{AS} , $\overline{CSx}/\overline{RASx}$, \overline{OE} , \overline{WE} , (and \overline{DS} Read) Asserted | t _{AVSA} | 10 | – | 8 | – | ns |
| 11A ⁽¹¹⁾ | Address, FC, SIZ, \overline{RMC} , Valid to $\overline{CSx}/\overline{RASx}$ Asserted | t _{AVCA} | 30 | – | 22.5 | – | ns |
| 12 | CLKO1 Low to \overline{AS} , \overline{DS} , \overline{OE} , \overline{WE} , \overline{IFETCH} , \overline{IPIPE} , \overline{IACKx} Negated | t _{CLSN} | 3 | 20 | 3 | 15 | ns |
| 12 ⁽¹⁶⁾ | CLKO1 Low to $\overline{CSx}/\overline{RASx}$ Negated | t _{CLSN} | 4 | 16 | 4 | 12 | ns |
| 12A ⁽¹³⁾⁽¹⁶⁾ | CLKO1 High to $\overline{CSx}/\overline{RASx}$ Negated | t _{CHCN} | 4 | 16 | 4 | 12 | ns |
| 12B | CS negate to WE negate (CSNTQ = 1) | e2v _{TW} | 15 | – | 12 | – | ns |
| 13 ⁽¹²⁾ | \overline{AS} , \overline{DS} , \overline{CSx} , \overline{OE} , \overline{WE} , \overline{IACKx} Negated to Address, FC, SIZ Invalid (Address Hold) | t _{SNAI} | 10 | – | 7.5 | – | ns |
| 13A ⁽¹³⁾ | \overline{CSx} Negated to Address, FC, SIZ, Invalid (Address Hold) | t _{CNAI} | 30 | – | 22.5 | – | ns |
| 14 ⁽¹⁰⁾⁽¹²⁾ | \overline{AS} , \overline{CSx} , \overline{OE} , \overline{WE} (and \overline{DS} Read) Width Asserted | t _{SWA} | 75 | – | 56.25 | – | ns |
| 14C ⁽¹¹⁾⁽¹³⁾ | \overline{CSx} Width Asserted | t _{CWA} | 35 | – | 26.25 | – | ns |
| 14A | \overline{DS} Width Asserted (Write) | t _{SWAW} | 35 | – | 26.25 | – | ns |
| 14B | \overline{AS} , \overline{CSx} , \overline{OE} , \overline{WE} , \overline{IACKx} , (and \overline{DS} Read) Width Asserted (Fast Termination Cycle) | t _{SWDW} | 35 | – | 26.25 | – | ns |
| 14D ⁽¹³⁾ | \overline{CSx} Width Asserted (Fast Termination Cycle) | t _{CWDW} | 15 | – | 10 | – | ns |
| 15 ⁽³⁾⁽¹⁰⁾⁽¹²⁾ | \overline{AS} , \overline{DS} , \overline{CSx} , \overline{OE} , \overline{WE} Width Negated | t _{SN} | 35 | – | 26.25 | – | ns |
| 16 | CLKO1 High to \overline{AS} , \overline{DS} , R/W High Impedance | t _{CHSZ} | – | 40 | – | 30 | ns |
| 17 ⁽¹²⁾ | \overline{AS} , \overline{DS} , \overline{CSx} , \overline{WE} Negated to R/W High | t _{SNRN} | 10 | – | 7.5 | – | ns |
| 17A ⁽¹³⁾ | \overline{CSx} Negated to R/W High | t _{CNRN} | 30 | – | 22.5 | – | ns |

Table 7-6. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-3 to Figure 7-19) (Continued)

| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|------------------------|--|--------------------|--------|-----|-----------|------|-------|
| | | | Min | Max | Min | Max | |
| 18 | CLKO1 High to R/W High | t _{CHRH} | 0 | 20 | 0 | 15 | ns |
| 20 | CLKO1 High to R/W Low | t _{CHRL} | 3 | 20 | 3 | 15 | ns |
| 21 ⁽¹⁰⁾ | R/W High to \overline{AS} , \overline{CSx} , \overline{OE} Asserted | t _{RAAA} | 10 | – | 7.5 | – | ns |
| 21A ⁽¹¹⁾ | R/W High to \overline{CSx} Asserted | t _{RACA} | 30 | – | – | – | ns |
| 22 | R/W Low to \overline{DS} Asserted (Write) | t _{RASA} | 47 | – | 36 | – | ns |
| 23 | CLKO1 High to Data-Out | t _{CHDO} | – | 23 | – | 18 | ns |
| 23A | CLKO1 High to Parity Valid | t _{CHPV} | – | 25 | – | 20 | ns |
| 23B | Parity Valid to \overline{CAS} Low | t _{PVCL} | 3 | – | 3 | – | ns |
| 24 ⁽¹²⁾ | Data-Out, Parity-Out Valid to Negating Edge of \overline{AS} , \overline{CSx} , \overline{WE} , (Fast Termination Write) | t _{DVASN} | 10 | – | 7.5 | – | ns |
| 25 ⁽¹²⁾ | \overline{DS} , \overline{CSx} , \overline{WE} Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold) | t _{SNDOI} | 10 | – | 7.5 | – | ns |
| 25A ⁽¹³⁾ | \overline{CSx} Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold) | t _{CNDOI} | 35 | – | 25 | – | ns |
| 26 | Data-Out, Parity-Out Valid to \overline{DS} Asserted (Write) | t _{DVSA} | 10 | – | 7.5 | – | ns |
| 27 ⁽¹⁵⁾ | Data-In, Parity-In to CLKO1 Low (Data-Setup) | t _{DICL} | 1 | – | 1 | – | ns |
| 27B ⁽¹⁴⁾ | Data-In, Parity-In Valid to CLKO1 Low (Data-Setup) | t _{DICL} | 20 | – | 15 | – | ns |
| 27A | Late \overline{BERR} , \overline{HALT} , \overline{BKPT} Asserted to CLKO1 Low (Setup Time) | t _{BELCL} | 10 | – | 7.5 | – | ns |
| 28 ⁽¹⁸⁾ | \overline{AS} , \overline{DS} Negated to \overline{DSACKx} , \overline{BERR} , \overline{HALT} Negated | t _{SNDN} | 0 | 50 | 0 | 37.5 | ns |
| 29 ⁽⁴⁾ | \overline{DS} , \overline{CSx} , \overline{OE} , Negated to Data-In Parity-In Invalid (Data-In, Parity-In Hold) | t _{SNDI} | 0 | – | 0 | – | ns |
| 29A ⁽⁴⁾ | \overline{DS} , \overline{CSx} , \overline{OE} Negated to Data-In High Impedance | t _{SHDI} | – | 40 | – | 30 | ns |
| 30 ⁽⁴⁾ | CLKO1 Low to Data-In, Parity-In Invalid (Fast Termination Hold) | t _{CLDI} | 10 | – | 7.5 | – | ns |
| 30A ⁽⁴⁾ | CLKO1 Low to Data-In High Impedance | t _{CLDH} | – | 60 | – | 45 | ns |
| 31 ⁽⁵⁾⁽¹⁵⁾ | \overline{DSACKx} Asserted to Data-in, Parity-In Valid | t _{DADI} | – | 32 | – | 24 | ns |
| 31A | \overline{DSACKx} Asserted to \overline{DSACKx} Valid (Skew) | t _{DADV} | – | 10 | – | 7.5 | ns |
| 31B ⁽⁵⁾⁽¹⁴⁾ | \overline{DSACKx} Asserted to Data-in, Parity-In Valid | t _{DADI} | – | 35 | – | 26 | ns |
| 32 | \overline{HALT} an \overline{RESET} Input Transition Time | t _{HRrf} | – | 140 | – | – | ns |
| 33 | CLKO1 High to \overline{BG} Asserted | t _{CLBA} | – | 20 | – | 15 | ns |
| 34 | CLKO1 High to \overline{BG} Negated | t _{CLBN} | – | 20 | 22.5 | 15 | ns |
| 35 ⁽⁶⁾ | \overline{BR} Asserted to \overline{BG} Asserted (\overline{RMC} Not Asserted) | t _{BRAGA} | 1 | – | 1 | – | CLKO1 |
| 37 | \overline{BGACK} Asserted to \overline{BG} Negated | t _{GAGN} | 1 | 2.5 | 1 | 2.5 | CLKO1 |
| 39 | \overline{BG} Width Negated | t _{GH} | 2 | – | 2 | – | CLKO1 |

Table 7-6. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-3 to Figure 7-19) (Continued)

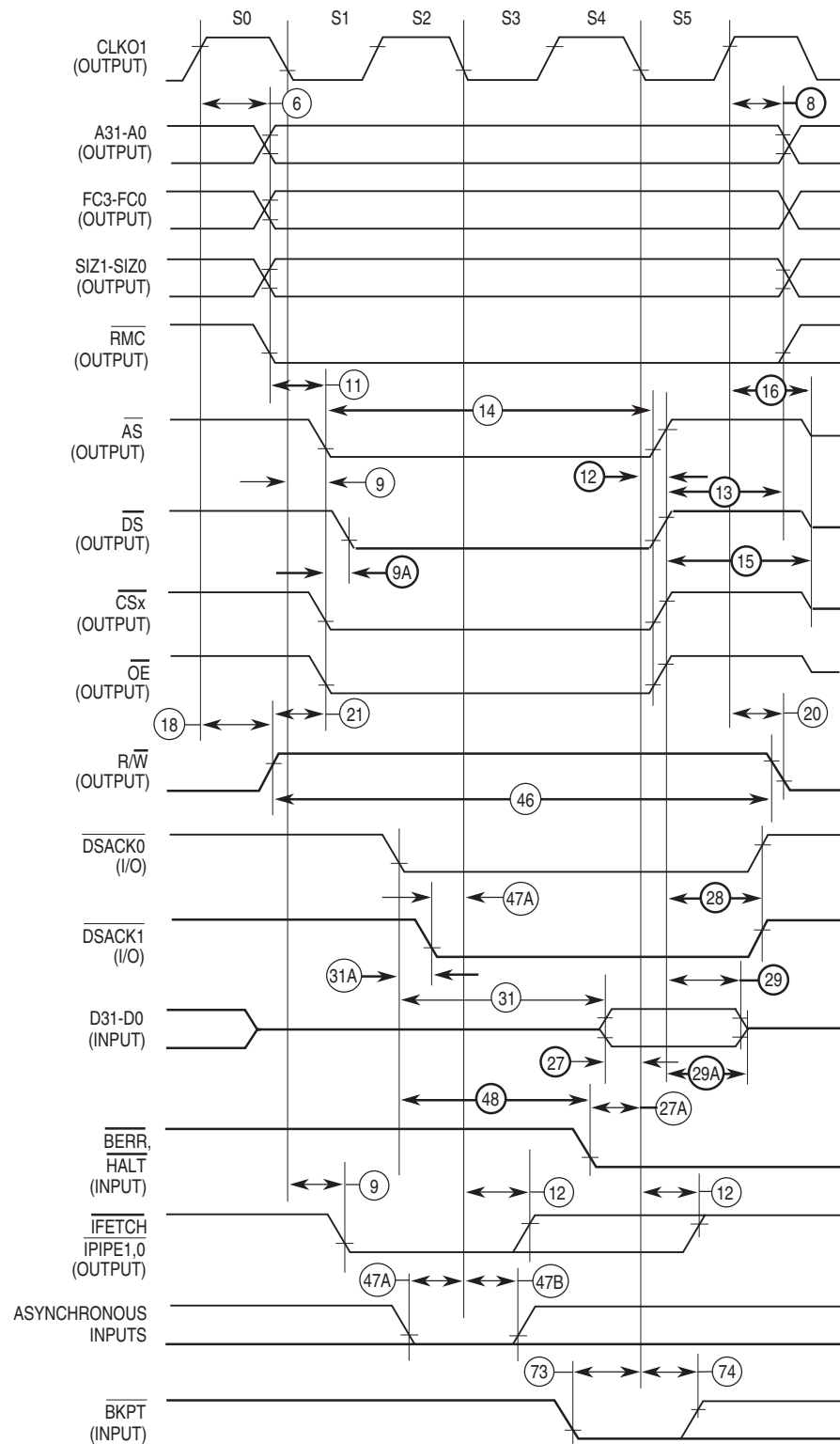
| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|----------------------|--|--------------------|--------|-----|-----------|------|-------|
| | | | Min | Max | Min | Max | |
| 39A | \overline{BG} Width Asserted | t _{GA} | 1 | – | 1 | – | CLKO1 |
| 46 | R \overline{W} Width Asserted (Write or Read) | t _{RWA} | 100 | – | 75 | – | ns |
| 46A | R \overline{W} Width Asserted (Fast Termination Write or Read) | t _{RWAS} | 75 | – | 56 | – | ns |
| 47A | Asynchronous Input Setup Time | t _{AIST} | 5 | – | 4 | – | ns |
| 47B | Asynchronous Input Hold Time | t _{AIHT} | 10 | – | 7.5 | – | ns |
| 48 ⁽⁵⁾⁽⁷⁾ | \overline{DSACKx} Asserted to \overline{BERR} , \overline{HALT} Asserted | t _{DABA} | – | 30 | – | 22.5 | ns |
| 53 | Data-Out, Parity-Out Hold from CLKO1 High | t _{DOCH} | 0 | – | 0 | – | ns |
| 54 | CLKO1 High to Dat-Out, Parity-Out High Impedance | t _{CHDH} | – | 20 | – | 15 | ns |
| 55 | R \overline{W} Asserted to Data Bus Impedance Change | t _{RADC} | 25 | – | 19 | – | ns |
| 56 | \overline{RESET} Pulse Width (Reset Instruction) | t _{HRPW} | 512 | – | 512 | – | CLKO1 |
| 56A | \overline{RESET} Pulse Width (Input from External Device) | t _{RPWI} | 20 | – | 20 | – | CLKO1 |
| 57 | \overline{BERR} Negated to \overline{HALT} Negated (Return) | t _{BNHN} | 0 | – | 0 | – | ns |
| 58 | CLKO1 High to \overline{BERR} , \overline{RESETS} , \overline{RESETH} Driven Low | t _{CHBRL} | – | 30 | – | 26 | ns |
| 58A | CLKO1 Low \overline{RESETH} Driven Low (upon Reset Instruction execution only) | t _{CLRL} | – | 30 | – | 26 | ns |
| 58B | CLKO1 High to \overline{BERR} , \overline{RESETS} , \overline{RESETH} tri-stated | t _{CLRL} | – | 20 | – | 15 | ns |
| 60 | CLKO1 High to \overline{BCLRO} Asserted | t _{CHBCA} | – | 20 | – | 15 | ns |
| 61 | CLKO1 High to \overline{BCLRO} Negated | t _{CHBCN} | – | 20 | – | 15 | ns |
| 62 ⁽⁹⁾ | \overline{BR} Synchronous Setup Time | t _{BRSU} | 5 | – | 3.75 | – | ns |
| 63 ⁽⁹⁾ | \overline{BR} Synchronous Hold Time | t _{BRH} | 10 | – | 7.5 | – | ns |
| 64 ⁽⁹⁾ | \overline{BGACK} Synchronous Setup Time | t _{BGSU} | 5 | – | 3.75 | – | ns |
| 65 ⁽⁹⁾ | \overline{BGACK} Synchronous Hold Time | t _{BGH} | 10 | – | 7.5 | – | ns |
| 66 | \overline{BR} Low to CLKO1 Rising Edge (040 comp. mode) | t _{BRCH} | 5 | – | 5 | – | ns |
| 70 | CLKO1 Low to Data Bus Driven (Show Cycle) | t _{SCLDD} | 0 | 30 | 0 | 22.5 | ns |
| 71 | Data Setup Time to CLKO1 Low (Show Cycle) | t _{SCLDS} | 10 | – | 7.5 | – | ns |
| 72 | Data Hold from CLKO1 Low (Show Cycle) | t _{SCLDH} | 6 | – | 3.75 | – | ns |
| 73 | \overline{BKPT} Input Setup Time | t _{BKST} | 10 | – | 7.5 | – | ns |
| 74 | \overline{BKPT} Input Hold Time | t _{BKHT} | 6 | – | 3.75 | – | ns |
| 75 | \overline{RESETH} Low to Config2-0, MOD1-0, B16M Valid | t _{MST} | – | 500 | – | 500 | CLKO1 |
| 76 | Config2-0 | t _{MSH} | 0 | – | 0 | – | ns |
| 77 | MOD1-0 Hold Time, B16M Hold Time | t _{MSH} | 10 | – | 10 | – | CLKO1 |

Table 7-6. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-3 to Figure 7-19) (Continued)

| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|--------|--|---------------------|--------|--------------------------|-----------|--------------------------|-------|
| | | | Min | Max | Min | Max | |
| 80 | DSI Input Setup Time | t _{DSISU} | 10 | – | 7.5 | – | ns |
| 81 | DSI Input Hold Time | t _{DSIH} | 6 | – | 3.75 | – | ns |
| 82 | DSCLC Setup Time | t _{DSCSU} | 10 | – | 7.5 | – | ns |
| 83 | DSCLC Hold Time | t _{DSCH} | 6 | – | 3.75 | – | ns |
| 84 | DSO Delay Time | t _{DSOD} | – | t _{cyc} +2 0 | – | t _{cyc} +2 0 | ns |
| 85 | DSCLK Cycle | t _{DSCCYC} | 2 | – | 2 | – | CLKO1 |
| 86 | CLKO1 High to Freeze Asserted | t _{FRZA} | 0 | 35 | 0 | 26.25 | ns |
| 87 | CLKO1 High to Freeze Negated | t _{FRZN} | 0 | 35 | 0 | 26.25 | ns |
| 88 | CLKO1 High to $\overline{\text{FETCH}}$ High Impedance | t _{IFZ} | 0 | 35 | 0 | 26.25 | ns |
| 89 | CLKO1 High to $\overline{\text{FETCH}}$ Valid | t _{IF} | 0 | 35 | 0 | 26.25 | ns |
| 90 | CLKO1 High to $\overline{\text{PERR}}$ Asserted | t _{CHPA} | 0 | 20 | 0 | 15 | ns |
| 91 | CLKO1 High to $\overline{\text{PERR}}$ Negated | t _{CHPN} | 0 | 20 | 0 | 15 | ns |
| 92 | V _{CC} Ramp-Up Time At Power-On Reset | t _{RMIN} | 5 | – | 5 | – | ns |

- Notes:
1. All AC timing is shown with respect to 0.8V and 2.0V levels unless otherwise noted.
 2. This number can be reduced to 5 ns if strobes have equal loads.
 3. If multiple chip selects are used, the $\overline{\text{CSx}}$ width negated (#15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select.
 4. Hold times are specified with respect to $\overline{\text{DS}}$ or $\overline{\text{CSx}}$ on asynchronous reads and with respect to CLKO1 on fast termination reads. The user is free to use either hold time for fast termination reads.
 5. If the asynchronous setup (#17) requirements are satisfied, the $\overline{\text{DSACKx}}$ low to data setup time (#31) and $\overline{\text{DSACKx}}$ low to $\overline{\text{BERR}}$ low setup time (#48) can be ignored. The data must only satisfy the data-in to CLKO1 low setup time (#27) for the following clock cycle: $\overline{\text{BERR}}$ must only satisfy the late $\overline{\text{BERR}}$ low to CLKO1 low setup time (#27A) for the following clock cycle.
 6. To ensure coherency during every operand transfer, $\overline{\text{BG}}$ will not be asserted in response to $\overline{\text{BR}}$ until after cycles of the current operand transfer are complete and $\overline{\text{RMC}}$ is negated.
 7. In the absence of $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$ is an asynchronous input using the asynchronous setup time (#47).
 8. During interrupt acknowledge cycles, the processor may insert up to two wait states between states S0 and S1.
 9. Specs are for Synchronous Arbitration only. ASTM = 1.
 10. $\overline{\text{CSx}}$ specs are for TRLX = 0.
 11. $\overline{\text{CSx}}$ specs are for TRLX = 1.
 12. $\overline{\text{CSx}}$ specs are for CSNTQ = 0.
 13. $\overline{\text{CSx}}$ specs are for CSNTQ = 1; or $\overline{\text{RASx}}$ specs for DRAM accesses.
 14. Specs are read cycles with parity check and PBEE = 1.
 15. Specs are read cycles with parity check and PBEE = 0, PAREN = 1.
 16. $\overline{\text{RASx}}$ specs are for page miss case.
 17. Specifications only apply to $\overline{\text{CSx}}/\overline{\text{RASx}}$ pins.
 18. Specification applies to non fast termination cycles. In fast termination cycles, the $\overline{\text{BERR}}$ signal must be negated by 20 ns after negation of $\overline{\text{AS}}$, $\overline{\text{DS}}$.

Figure 7-3. Read Cycle



Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-4. Fast Termination Read Cycle (Parity Check PAREN = 1, PBEE = 0)

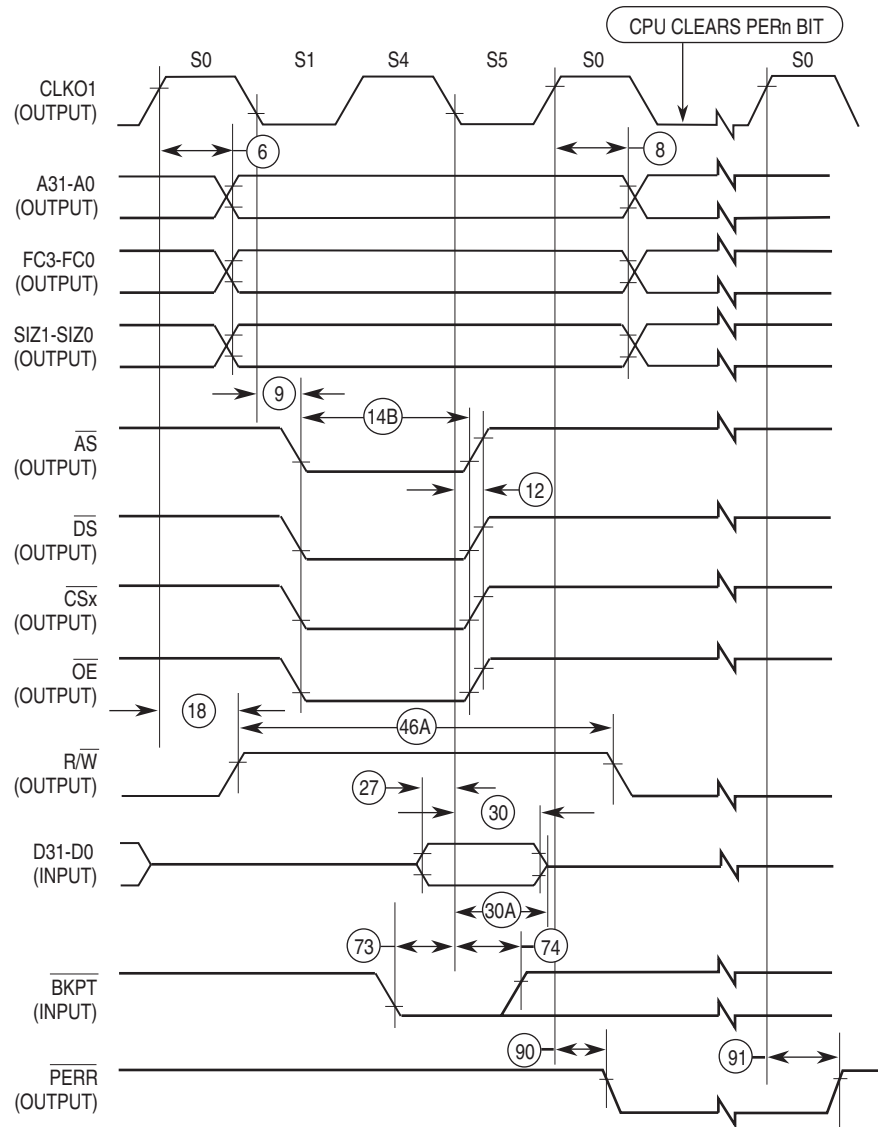
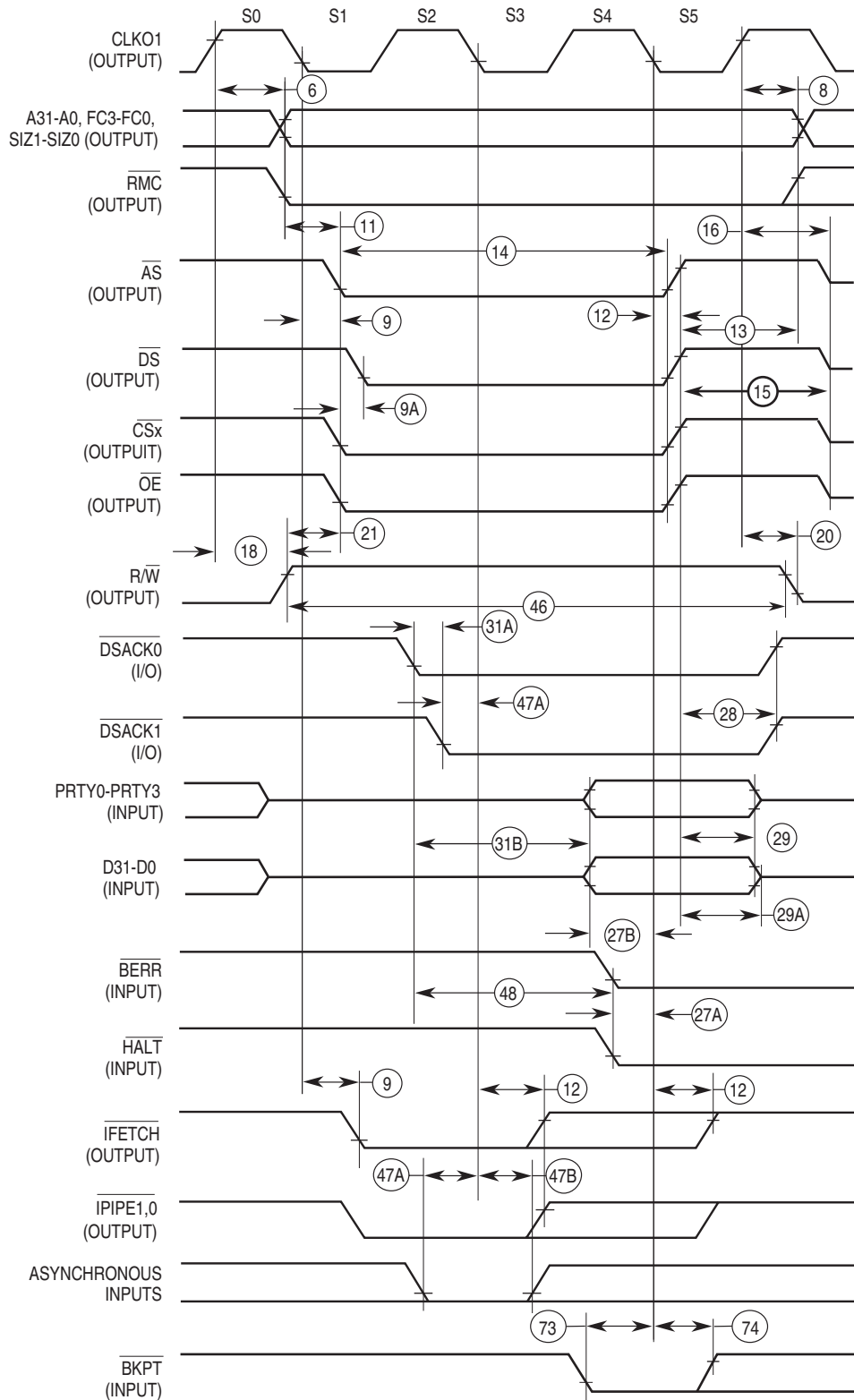


Figure 7-5. Read Cycle (With Parity Check, PBEE = 1)



Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-6. SRAM: Read Cycle (TRLX = 1)

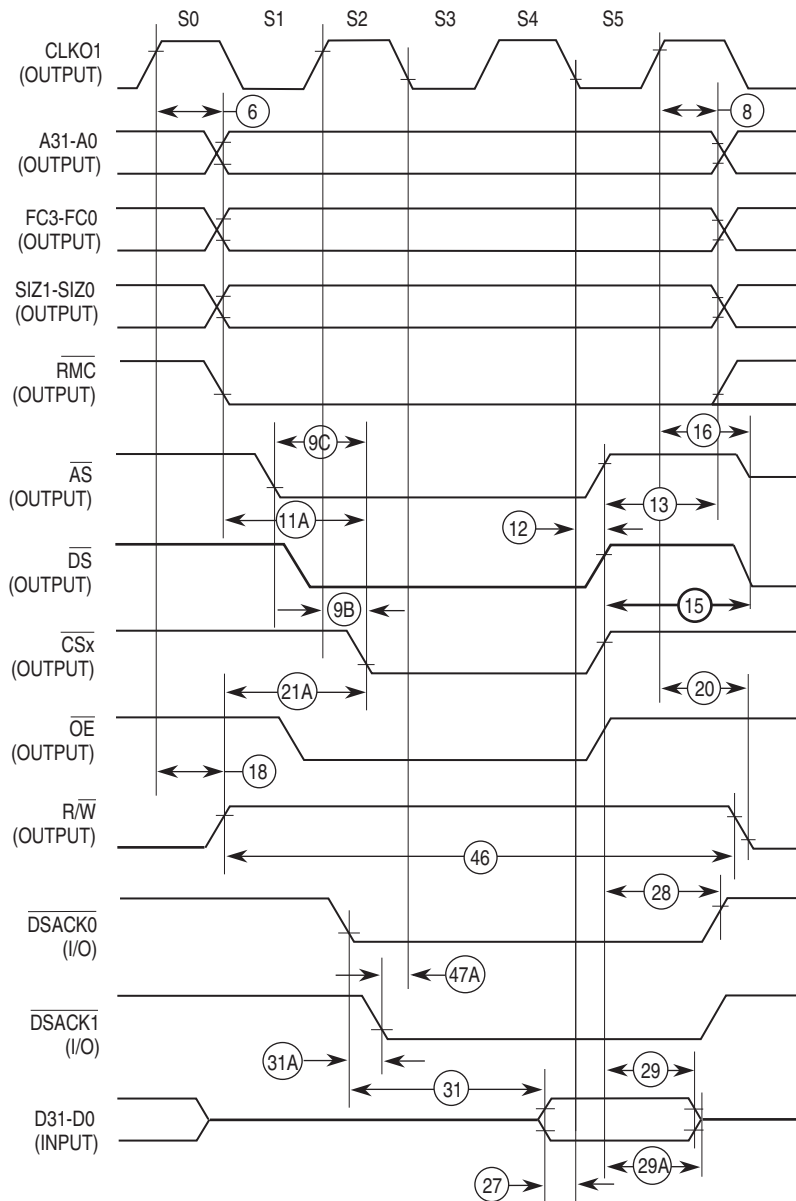
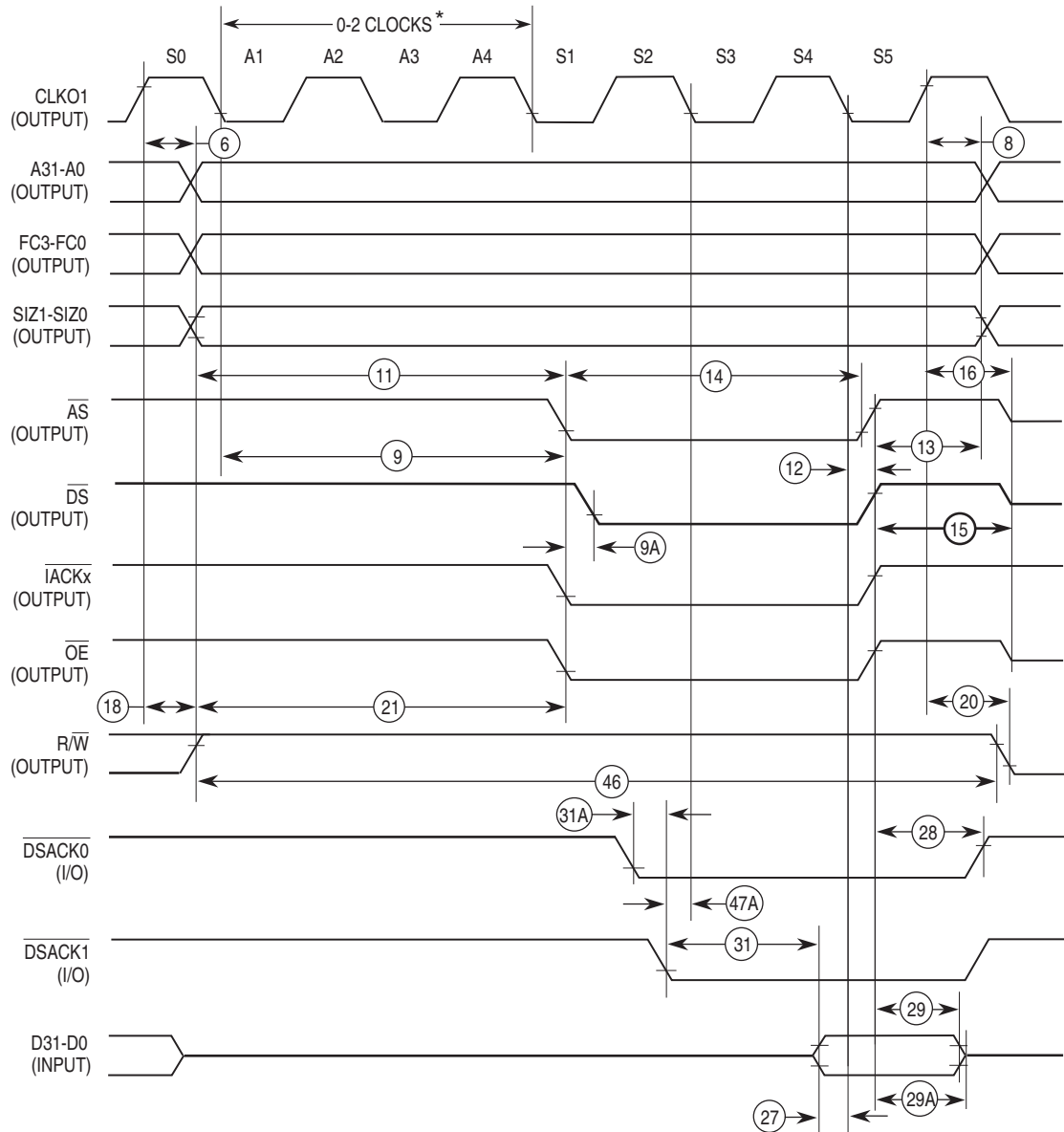
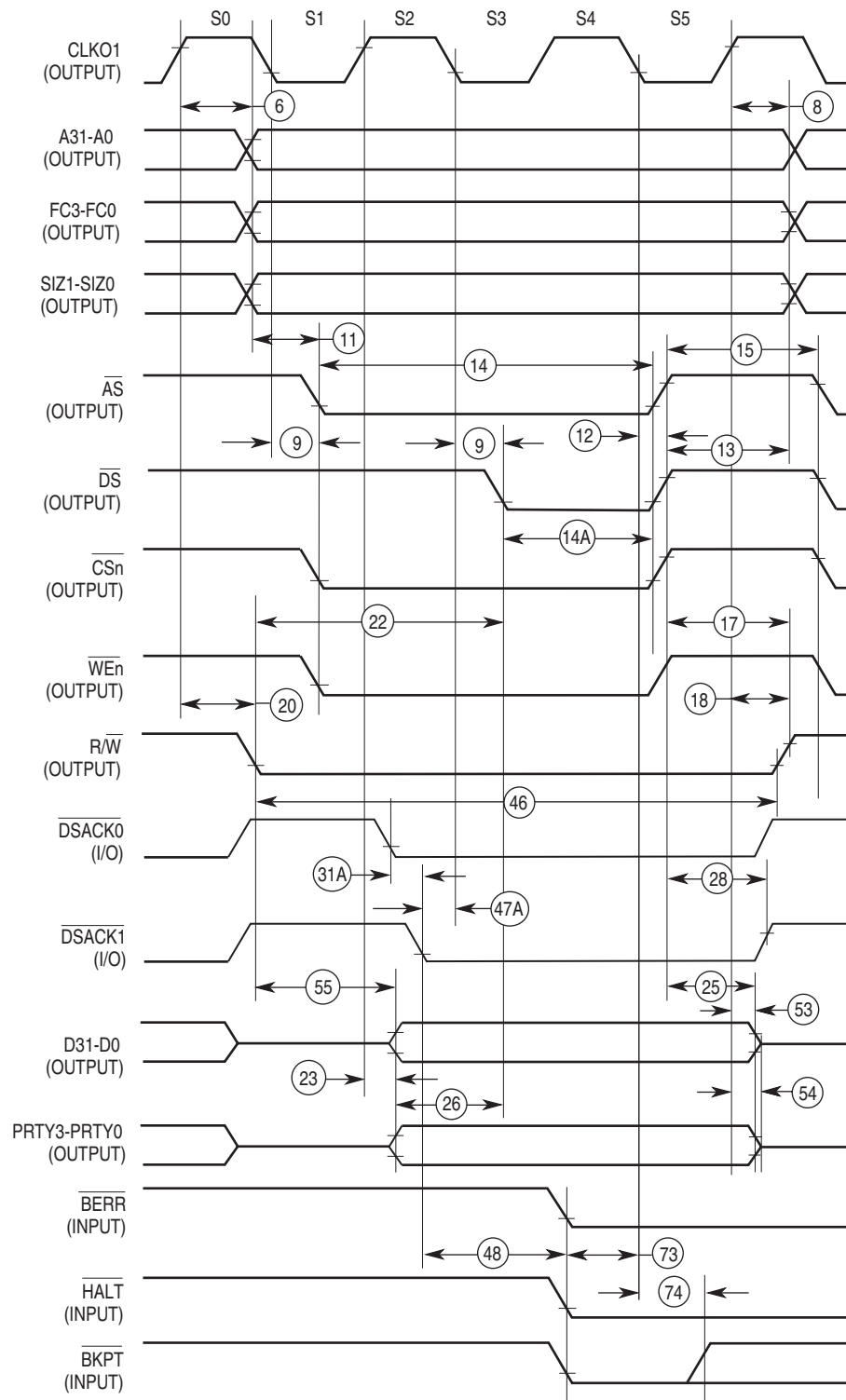


Figure 7-7. CPU32+ IACK Cycle



Note: Up to two wait states may be inserted by the processor between states S0 and S1.

Figure 7-8. Write Cycle



Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-9. Fast Termination Write Cycle

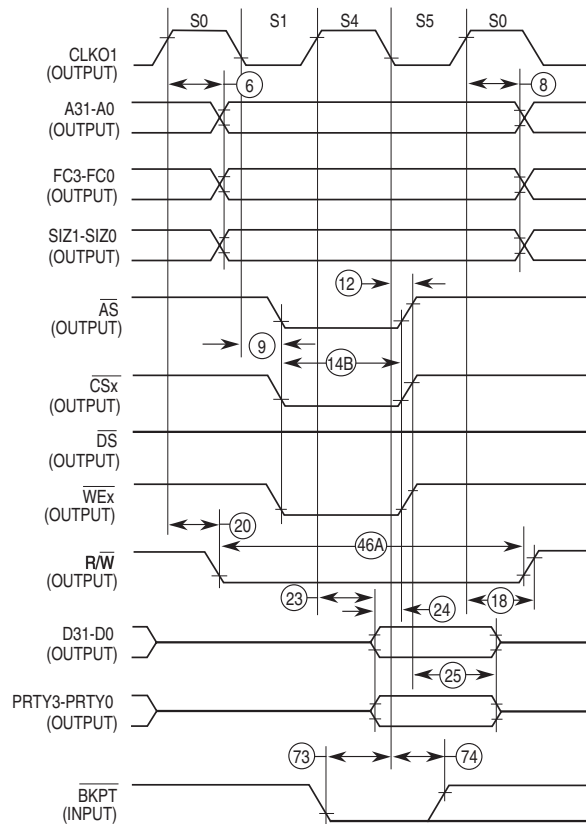


Figure 7-10. SRAM: Fast Termination Write Cycle (CSNTQ = 1)

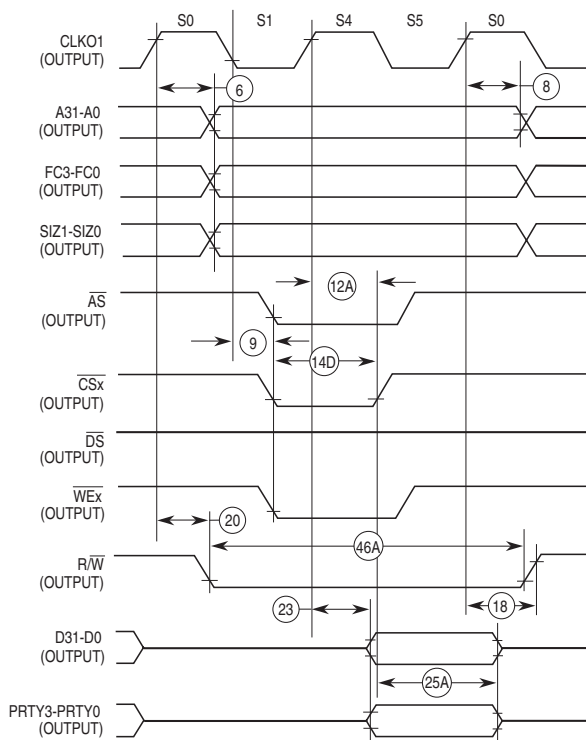
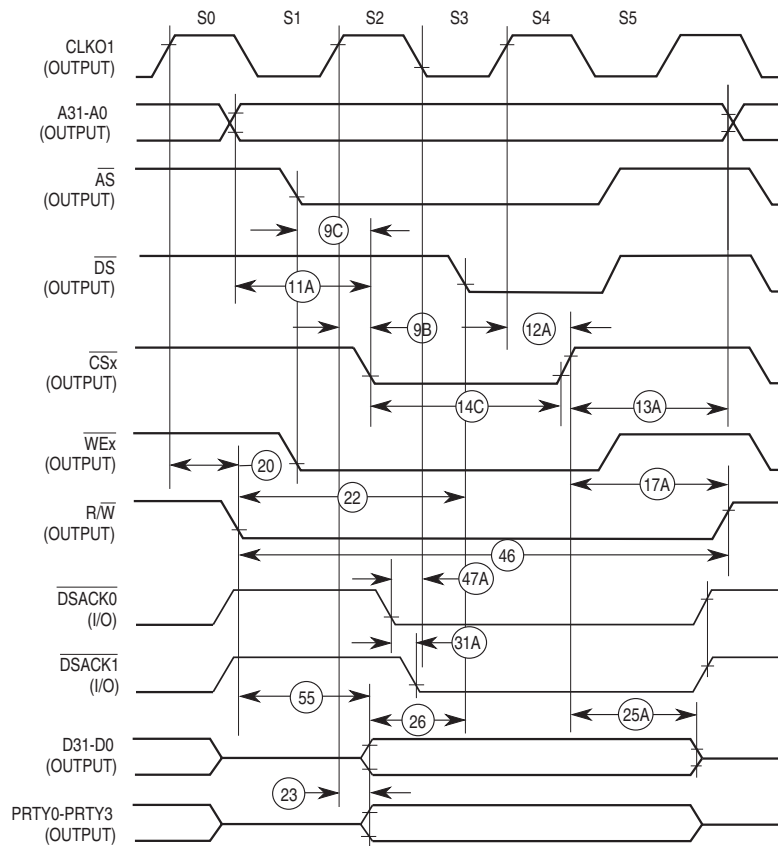


Figure 7-11. SRAM: Write Cycle (TRLX = 1, CSNTQ = 1, TCYC = 0)



Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-12. ASYNC Bus Arbitration – IDLE Bus Case

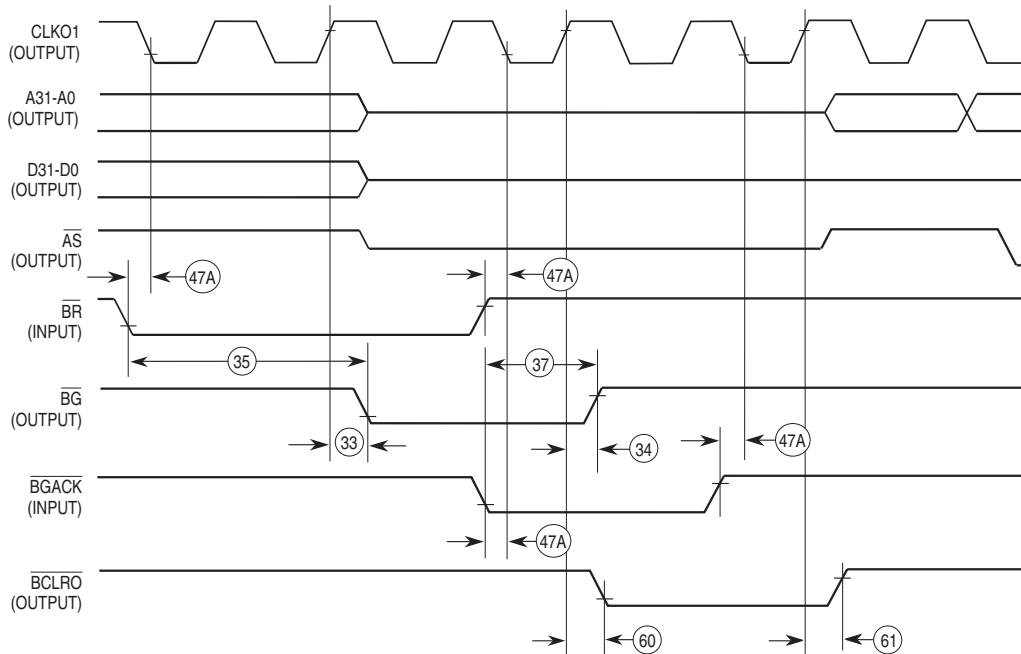


Figure 7-13. ASYNC Bus Arbitration – Active Bus Case

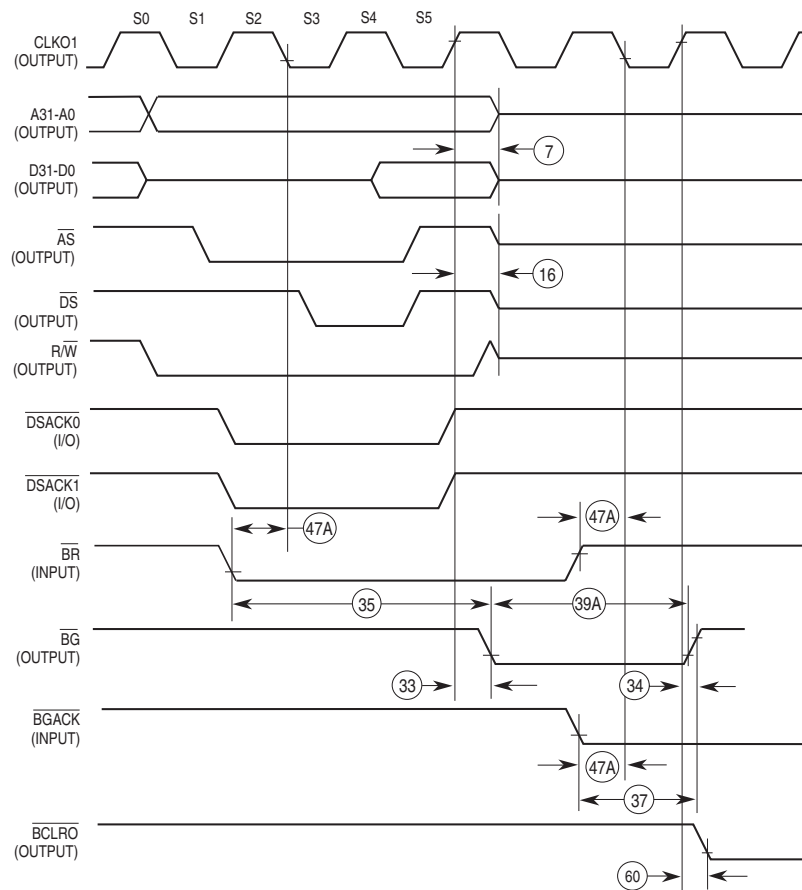


Figure 7-14. SYNC Bus Arbitration – IDLE Bus Case

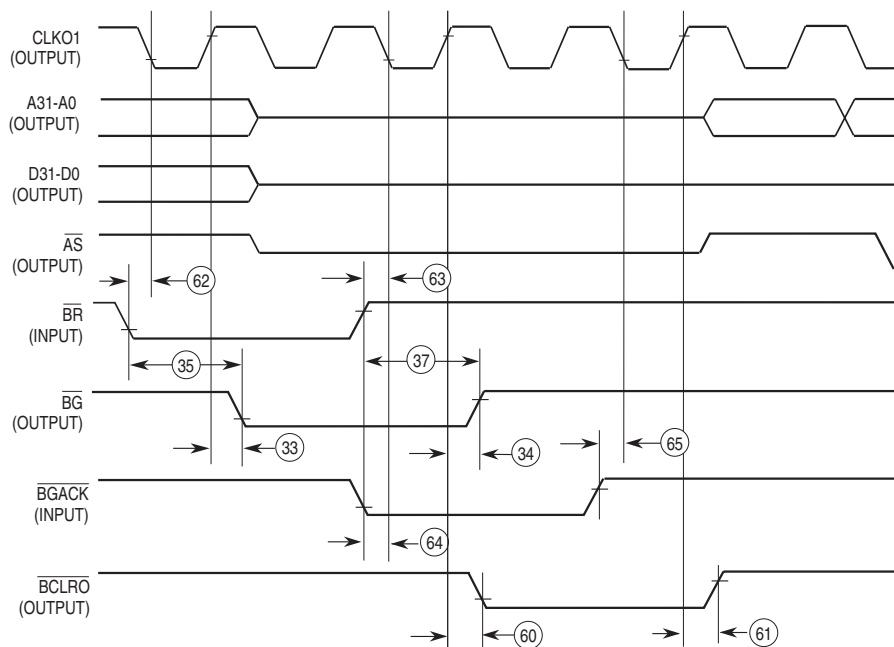


Figure 7-15. SYNC Bus Arbitration – Active Bus Case

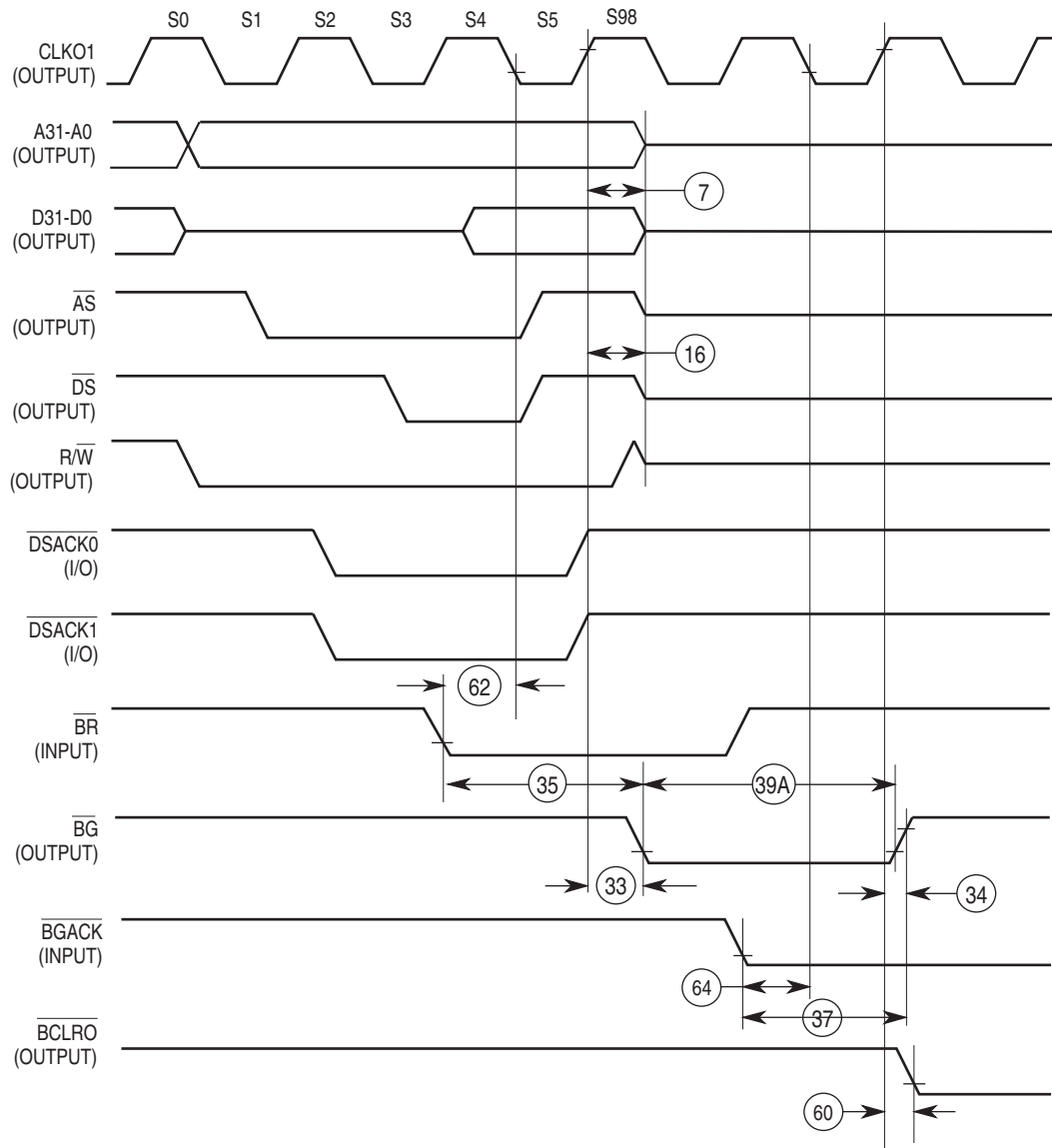


Figure 7-16. Configuration and Clock Mode Select Timing

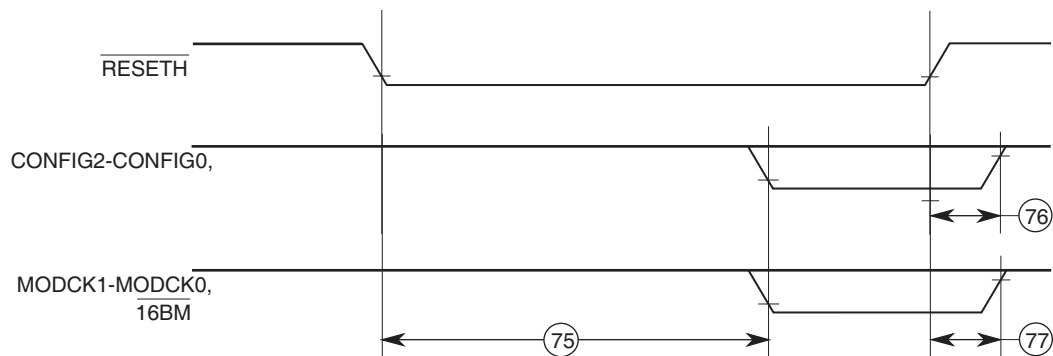


Figure 7-17. Show Cycle

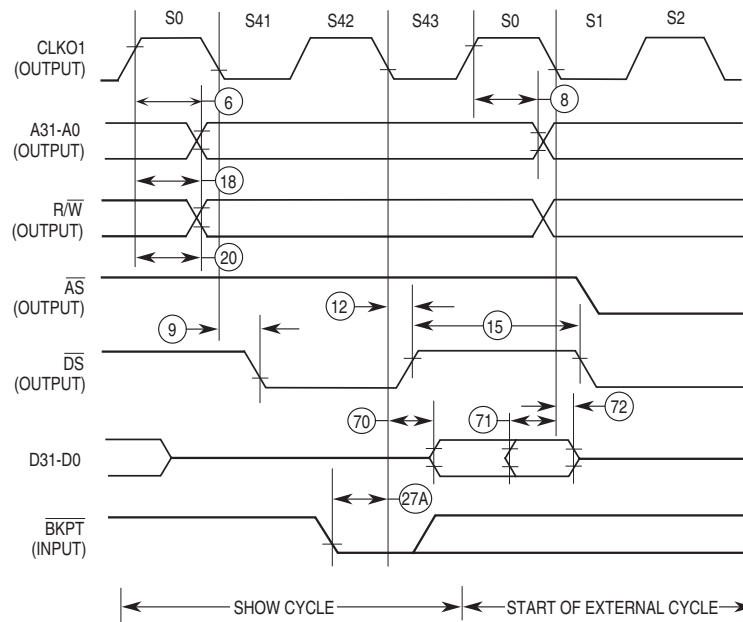


Figure 7-18. Background Debug Mode FREEZE Timing

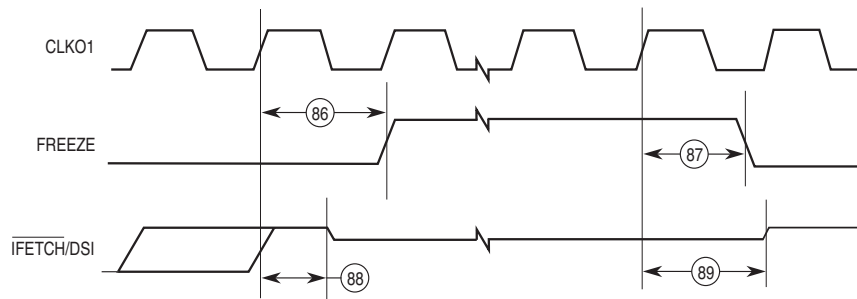


Figure 7-19. Background Debug Mode Serial Port Timing

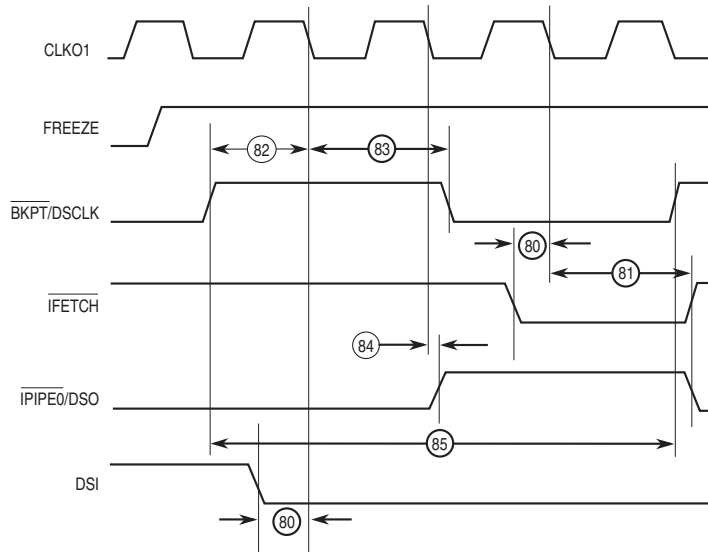
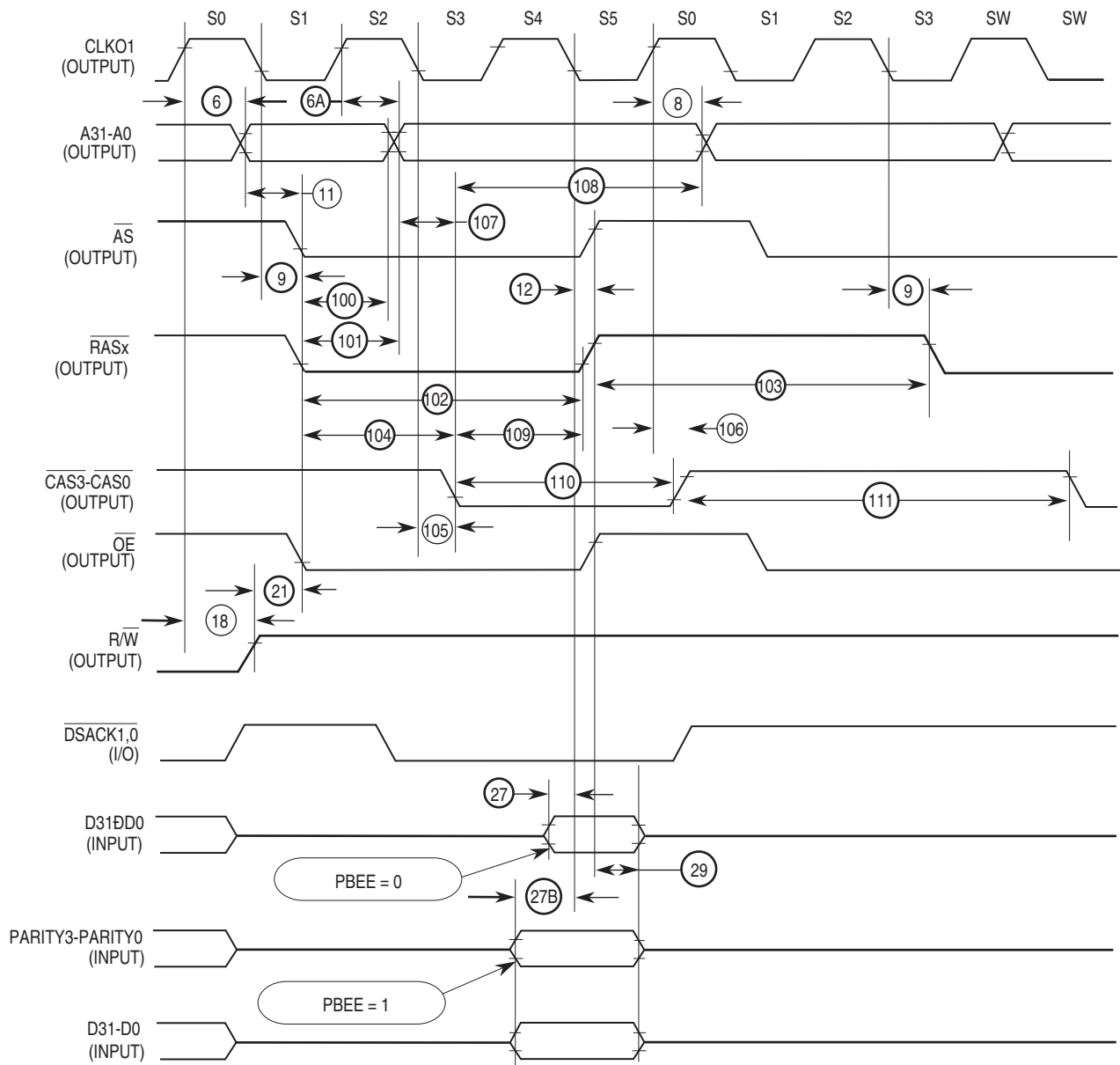


Figure 7-20. DRAM: Normal Read Cycle (Internal Mux, TRLX = 0)



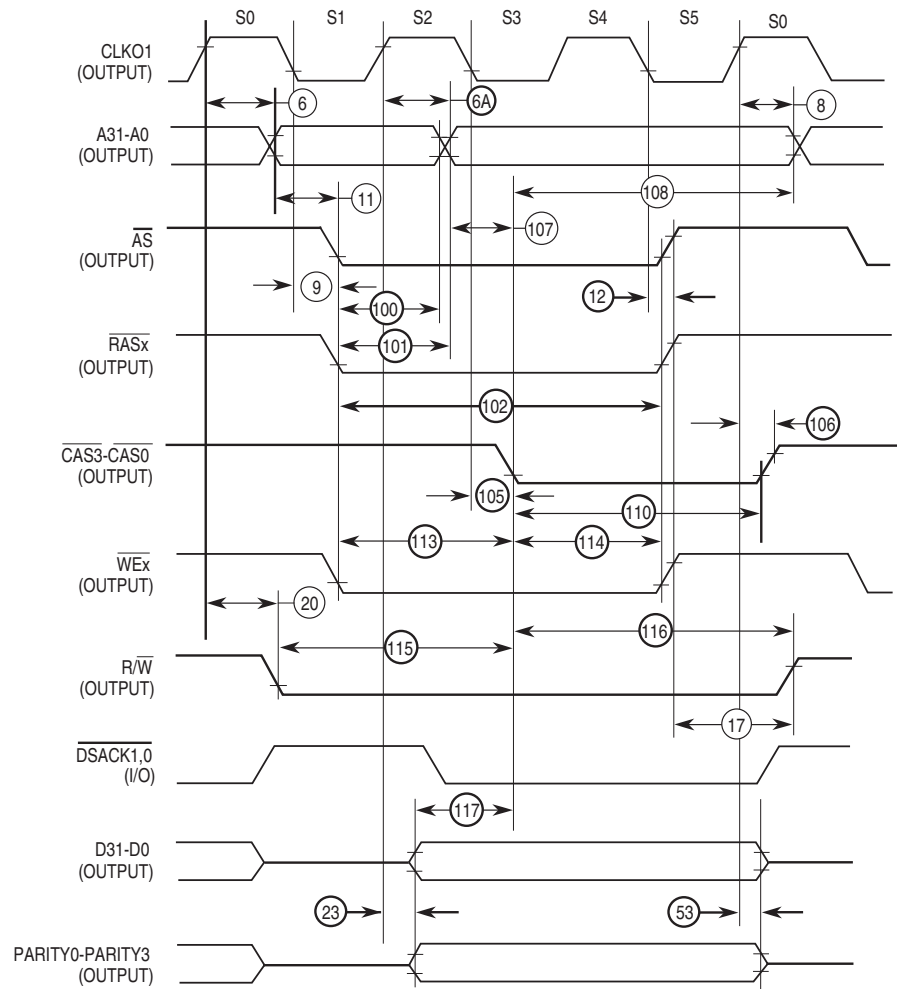
Note: All timing is shown with respect to 0.8V and 2.0V levels.

7.8 Bus Operation – DRAM Accesses AC Timing Specification

Table 7-7. GND = 0 V_{DC}, TC = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-20 to Figure 7-24)

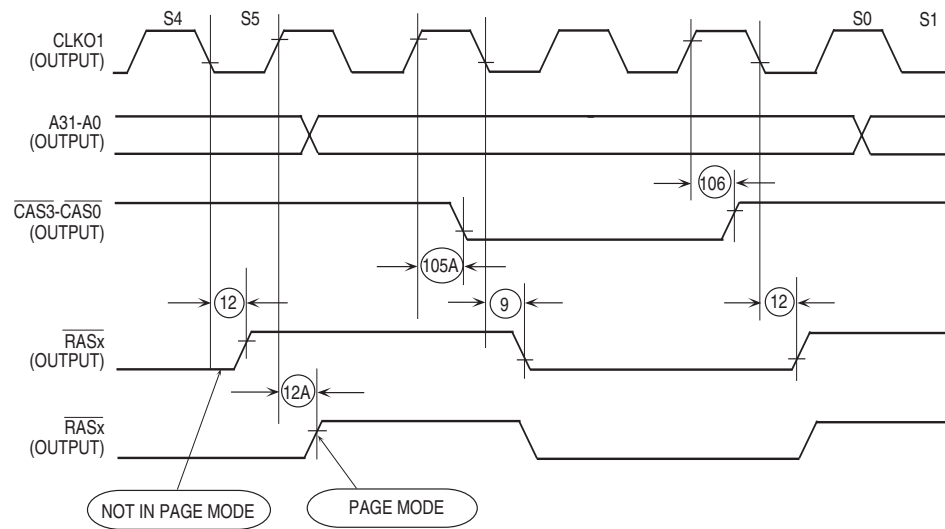
| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|------------------|--|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 100 | $\overline{\text{RASx}}$ Asserted to Row Address Invalid | 15 | | 11.25 | | ns |
| 101 | $\overline{\text{RASx}}$ Asserted to column Address Valid | 20 | | 15 | | ns |
| 102 | $\overline{\text{RASx}}$ Width Asserted | 75 | | 56.25 | | ns |
| 103A | $\overline{\text{RASx}}$ width Negated (Back to back Cycle) Non page mode at WBTQ = 0 | 75 | | 56.25 | | ns |
| 103B | $\overline{\text{RASx}}$ width Negated (Back to back Cycle) Page mode at WBTQ = 0 | 55 | | 41.25 | | ns |
| 103C | $\overline{\text{RASx}}$ width Negated (Back to back Cycle) Non page mode at WBTQ = 1 | 115 | | 86.25 | | ns |
| 103D | $\overline{\text{RASx}}$ width Negated (Back to back Cycle) Page mode at WBTQ = 1 | 95 | | 69.23 | | ns |
| 104 | $\overline{\text{RASx}}$ Asserted to $\overline{\text{CASx}}$ Asserted | 35 | | 26.25 | | ns |
| 105 | CLKO1 Low to $\overline{\text{CASx}}$ Asserted | 3 | 13 | 2 | 10 | ns |
| 105A | CLKO1 High to $\overline{\text{CASx}}$ Asserted (Refresh Cycle) | 3 | 13 | 2 | 10 | ns |
| 106 | CLKO1 High to $\overline{\text{CASx}}$ Negated | 3 | 13 | 2 | 10 | ns |
| 107 | Column Address Valid to $\overline{\text{CASx}}$ Asserted | 15 | | 11.25 | | ns |
| 108 | $\overline{\text{CASx}}$ Asserted to Column Address Negated | 40 | | 30 | | ns |
| 109 | $\overline{\text{CASx}}$ Asserted to $\overline{\text{RASx}}$ Negated | 35 | | 27 | | ns |
| 110 | $\overline{\text{CASx}}$ Width Asserted | 50 | | 37.5 | | ns |
| 111 ¹ | $\overline{\text{CASx}}$ Width Negated (Back to Back Cycles) | 95 | | 71.25 | | ns |
| 111A | $\overline{\text{CASx}}$ Width Negated (Page Mode) | 20 | | 15 | | ns |
| 113 | $\overline{\text{WE}}$ Low to $\overline{\text{CASx}}$ Asserted | 35 | | 27 | | ns |
| 114 | $\overline{\text{CASx}}$ Asserted to $\overline{\text{WE}}$ Negated | 35 | | 27 | | ns |
| 115 | R $\overline{\text{W}}$ Low to $\overline{\text{CASx}}$ Asserted (Write) | 52.5 | | 40 | | ns |
| 116 | $\overline{\text{CASx}}$ Asserted to R $\overline{\text{W}}$ High (Write) | 55 | | 41.25 | | ns |
| 117 | Data-Out, Parity-Out Valid to $\overline{\text{CASx}}$ Asserted | 10 | | 7.5 | | ns |
| 119 | CLKO1 High to AMUX Negated | 3 | 16 | 2 | 12 | ns |
| 120 | CLKO1 High to AMUX Asserted | 3 | 16 | 2 | 12 | ns |
| 121 | AMUX High to $\overline{\text{RASx}}$ Asserted | 15 | | 11.25 | | ns |
| 122 | $\overline{\text{RASx}}$ Asserted to AMUX Low | 15 | | 11.25 | | ns |
| 123 | AMUX Low to $\overline{\text{CASx}}$ Asserted | 15 | | 11.25 | | ns |
| 124 | $\overline{\text{CASx}}$ Asserted to AMUX High | 55 | | 41.25 | | ns |
| 125 | $\overline{\text{RAS}}/\overline{\text{CASx}}$ Negated to R $\overline{\text{W}}$ change | 0 | | 0 | | ns |

Figure 7-21. DRAM: Normal Write Cycle



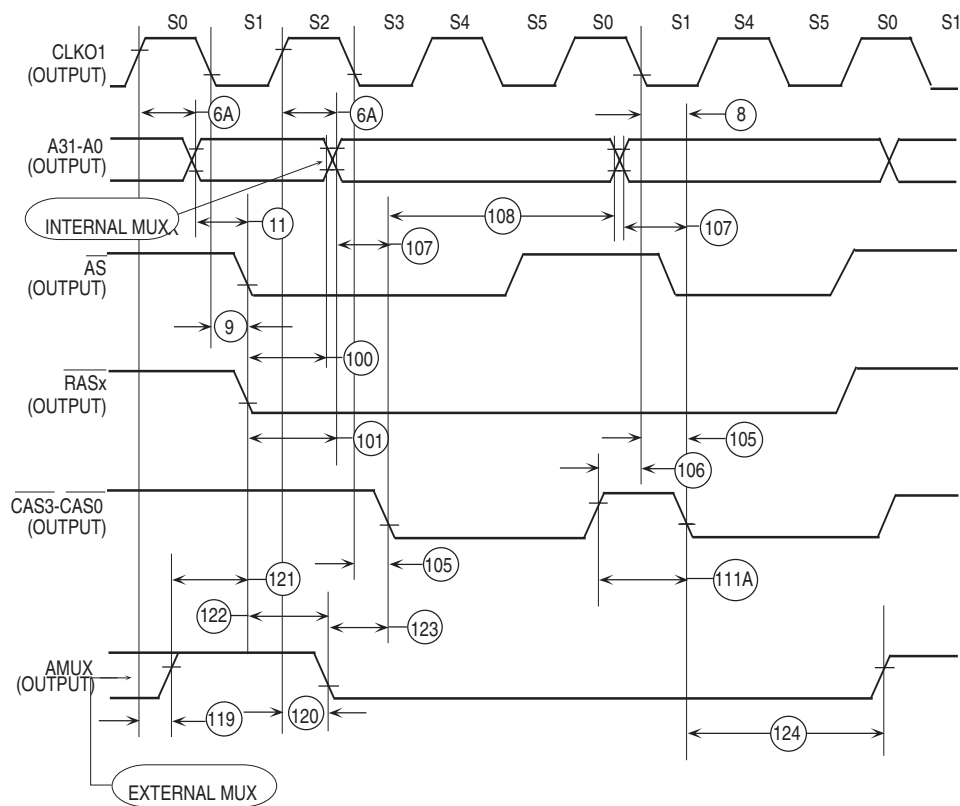
Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-22. DRAM: Refresh Cycle



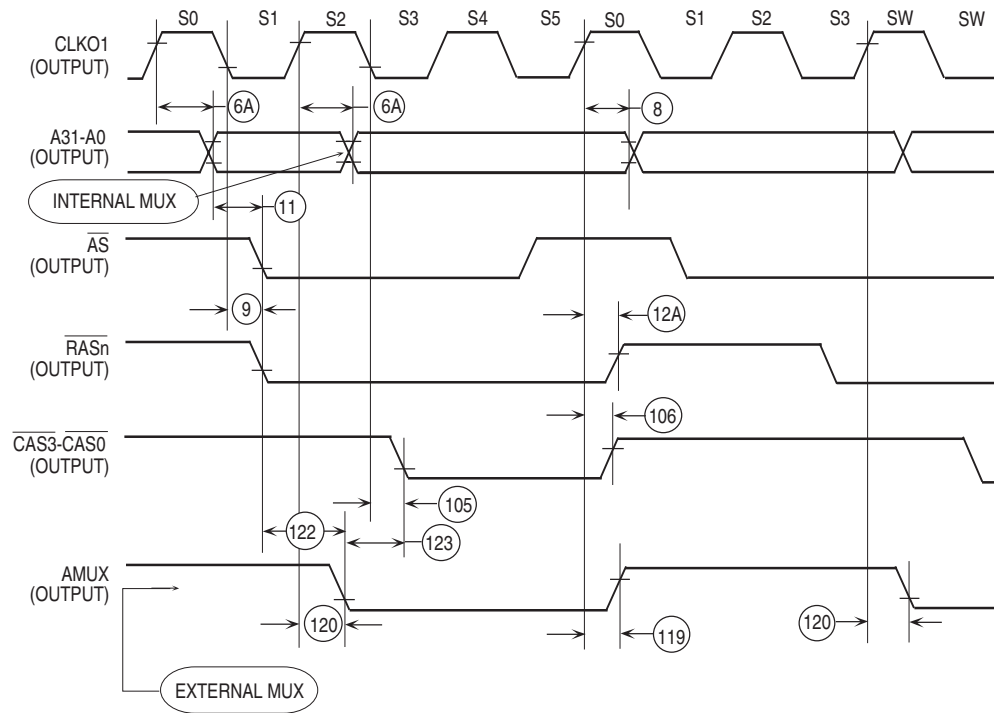
Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-23. DRAM: Page Mode – Page-Hit



Note: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 7-24. DRAM: Page Mode – Page-Miss



Note: All timing is shown with respect to 0.8V and 2.0V levels.

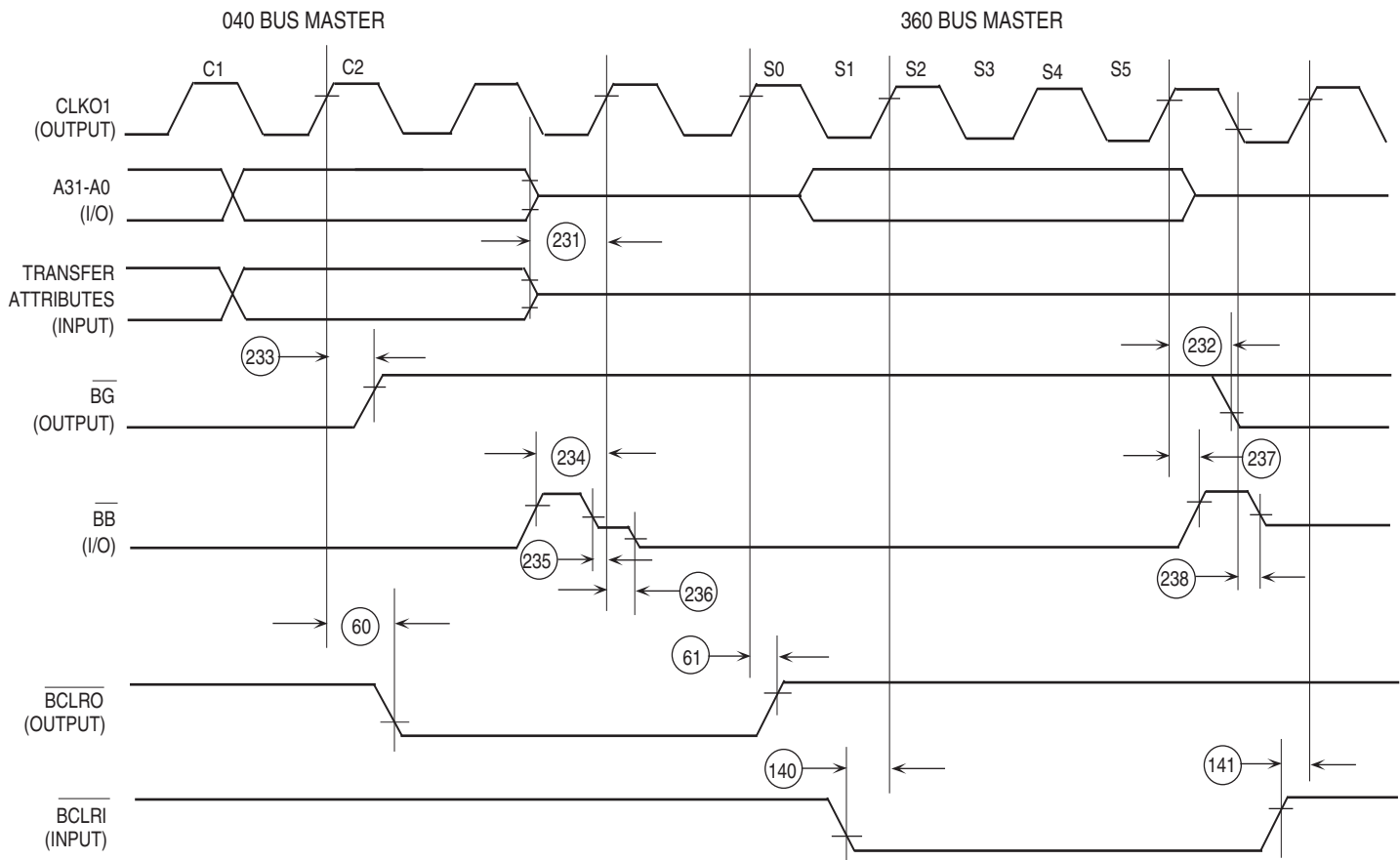
7.9 040 Bus Type Slave Mode Bus Arbitration AC Electrical Specifications

Table 7-8. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-25)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------------------|---|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 231 | Address, Transfer Attributes High Impedance to Clock High | 7 | – | 6 | – | ns |
| 232 ⁽¹⁾ | Clock High to \overline{BG} Low | – | 20 | – | 15 | ns |
| 233 | Clock High to \overline{BG} High | 4 | 20 | 4 | 15 | ns |
| 234 | \overline{BB} High to Clock High (040 output) | 7 | – | 6 | – | ns |
| 235 | \overline{BB} High Impedance to Clock High (040 output) | 0 | – | 0 | – | ns |
| 236 | Clock High to \overline{BB} Low (360 Output) | – | 20 | – | 15 | ns |
| 237 | Clock High to \overline{BB} High (360 Output) | – | 20 | – | 15 | ns |
| 238 | Clock Low to \overline{BB} High Impedance (360 output) | – | 20 | – | 15 | ns |

Note: 1. \overline{BG} remains low until either the SDMA or the IDMA requests the external bus.

Figure 7-25. TS68040 Companion Mode Arbitration



Notes: 1. TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R \overline{W} , \overline{LOCK} .
 2. \overline{BG} always remains asserted until either the SDMA or the IDMA requests the external bus

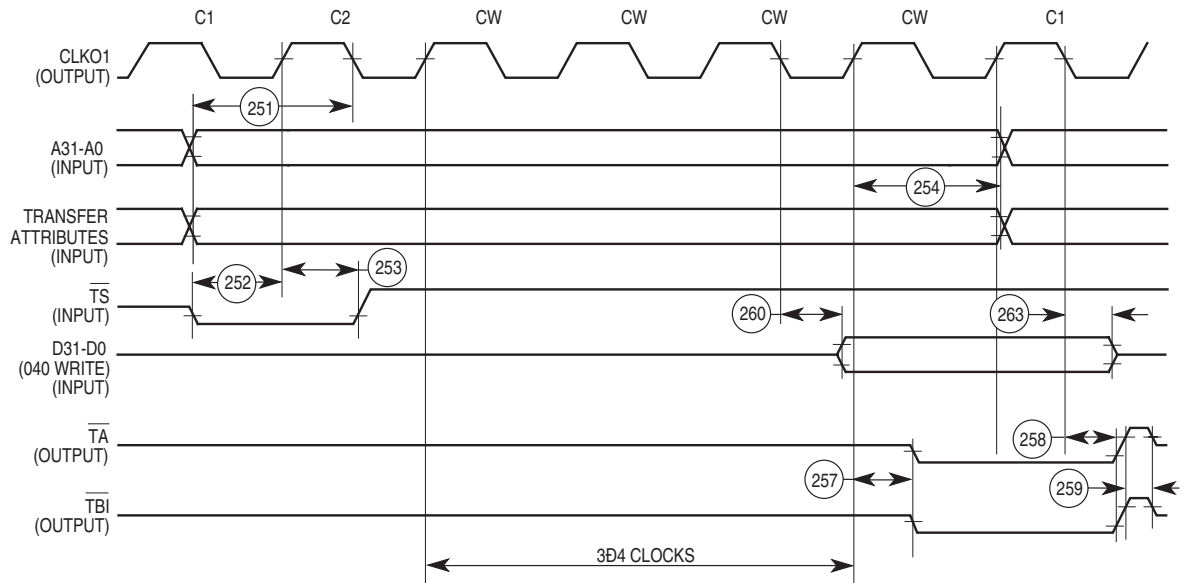
7.10 040 Bus Type Slave Mode Internal Read/Write/Lack Cycles AC Electrical Specifications

Table 7-9. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary
(See Figure 7-26 to Figure 7-29)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|-----------------------|--|----------|-----|-----------|-------|------|
| | | Min | Max | Min | Max | |
| 251 ⁽¹⁾ | Address, Transfer Attributes Valid to Clock Low | 15 | – | 11.25 | – | ns |
| 252 | \overline{TS} Low to Clock High | 7 | – | 6 | – | ns |
| 253 | Clock High to \overline{TS} High | 5 | – | 3 | – | ns |
| 254 | Clock high to Address, Transfer Attributes Invalid | 0 | – | 0 | – | ns |
| 255 | Data-In, \overline{MBARE} Valid to Clock High (040 Write) | 0 | – | 0 | – | ns |
| 256 | Clock High to Data-In, \overline{MBARE} Hold Time | 0 | – | 0 | – | ns |
| 257 | Clock High to \overline{TA} , \overline{TBI} Low (External to External) | 4 | 20 | 4 | 15 | ns |
| 257 | Clock High to \overline{TA} , \overline{TBI} Low (External to Internal) | 4 | 23 | 4 | 18 | ns |
| 258 ⁽²⁾⁽³⁾ | Clock High to \overline{TA} , \overline{TBI} High | 4 | 20 | 4 | 15 | ns |
| 259 | \overline{TA} , \overline{TBI} High to \overline{TA} , \overline{TBI} High Impedance | – | 15 | – | 11.25 | ns |
| 260 | Clock Low to Data-Out Valid (040 Read) | – | 20 | – | 15 | ns |
| 262 | Clock Low to Data-Out Invalid | – | 20 | – | 15 | ns |
| 263 | Clock Low to Data-Out High Impedance | – | 15 | – | | ns |
| 264 | Clock High to \overline{AVECO} Low | – | 20 | – | 15 | ns |
| 265 | Clock Low to \overline{AVECO} High Impedance | – | 30 | – | 23 | ns |
| 266 | Clock Low to \overline{IACK} Low | – | 30 | – | 23 | ns |
| 267 | Clock High to \overline{IACK} High | – | 30 | – | 23 | ns |
| 268 | Clock Low to \overline{AVEC} Low | – | 30 | – | 23 | ns |

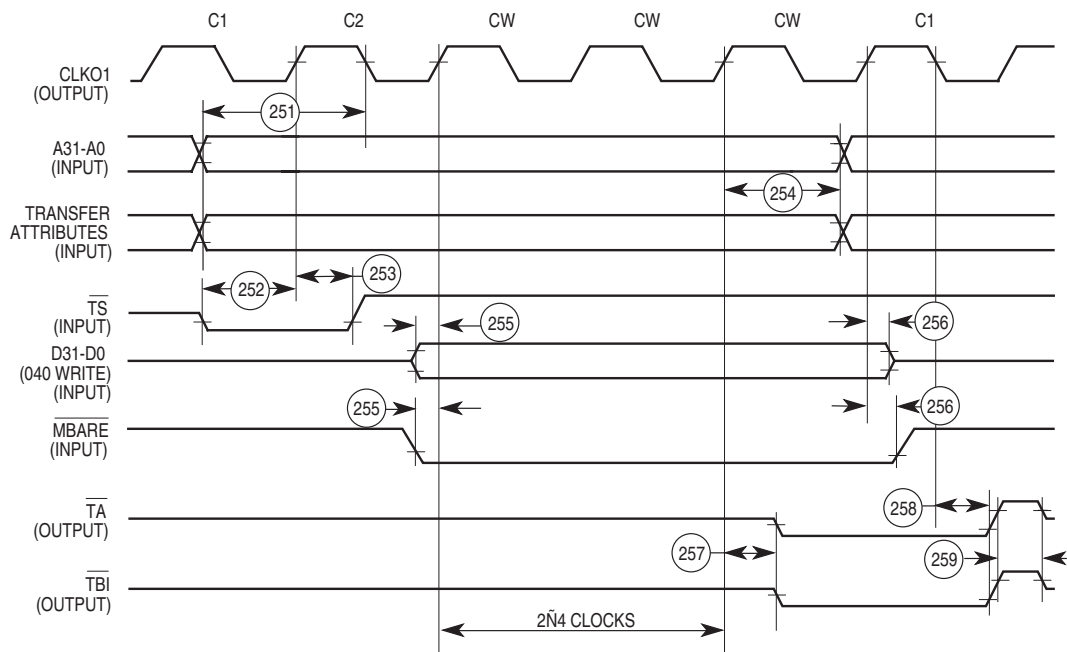
- Notes:
1. Transfer attributes signals = SIZx, TTx, TMx, R \overline{W} and LOCK.
 2. When TS68040 is accessing the internal registers, specification 258 is from clock low not clock high.
 3. The clock reference is EXTAL, not CLK01.TS68040 Internal Registers Read Cycles

Figure 7-26. TS68040 Internal Registers Read Cycles



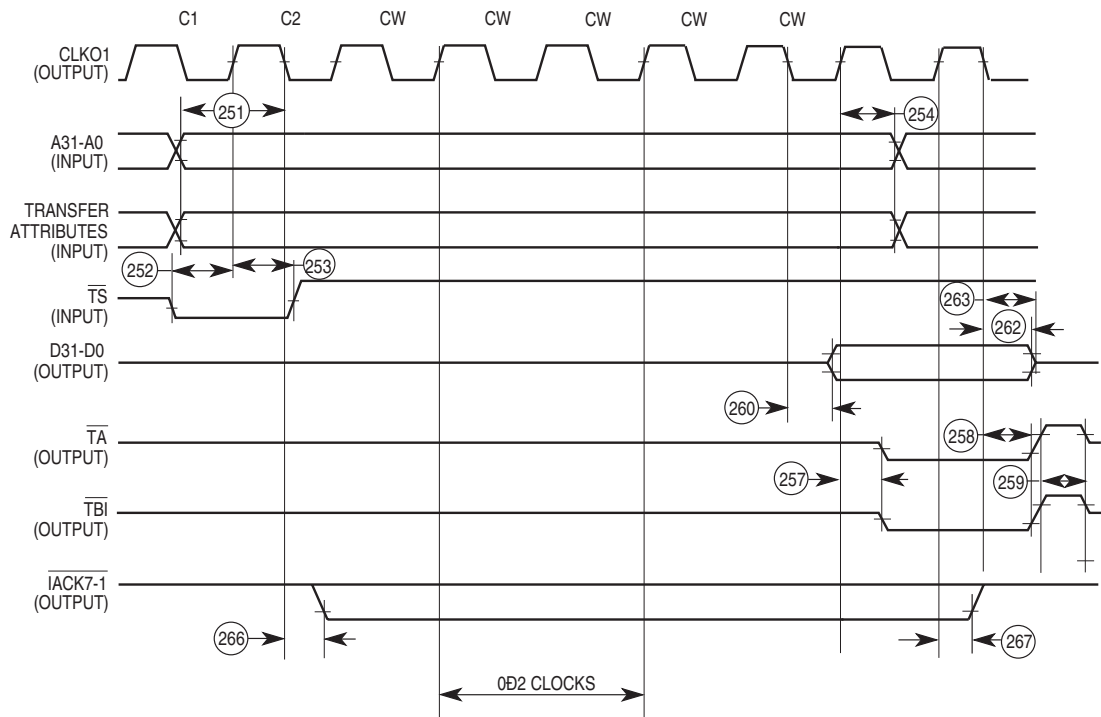
- Notes:
1. Three wait states are inserted when reading the SIM, dual-port RAM, and CPM. Four wait states are inserted when reading the SI RAM. Additional wait states may be inserted when the SHEN1-SHEN0 = 10 and one of the internal masters is accessing an internal peripheral.
 2. TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.

Figure 7-27. TS68040 Internal Registers Write Cycles



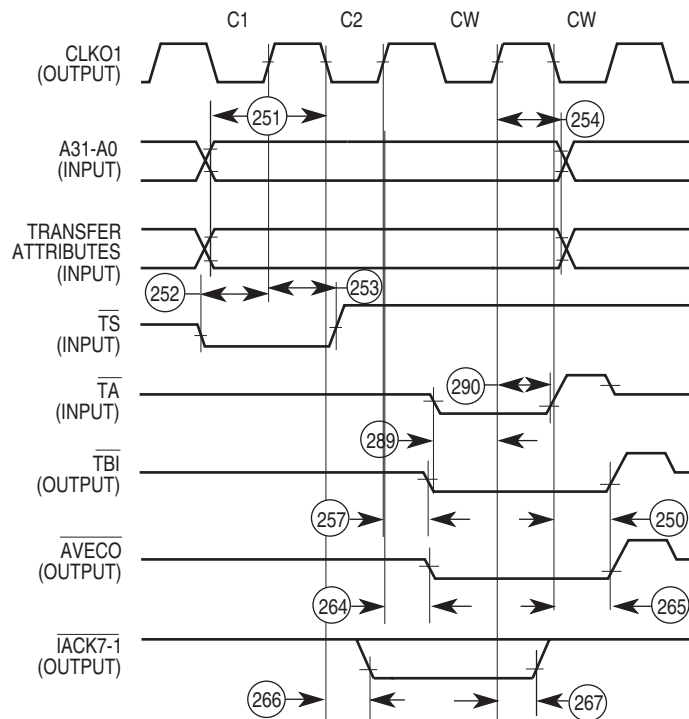
- Notes:
1. Two wait states are inserted when writing. Three wait states are inserted when writing to the dual-port RAM and CPM. Four wait states are inserted when writing to the SI RAM. Additional wait states may be inserted when the SHEN1-SHEN0 = 10 and one of the internal masters is accessing an internal peripheral.
 2. TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.

Figure 7-28. TS68040 IACK Cycles (Vector Driven)



- Notes: 1. TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.
 2. Up to two wait states may be inserted for internal peripheral.

Figure 7-29. TS68040 IACK Cycles (No Vector Driven)



Note: TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.

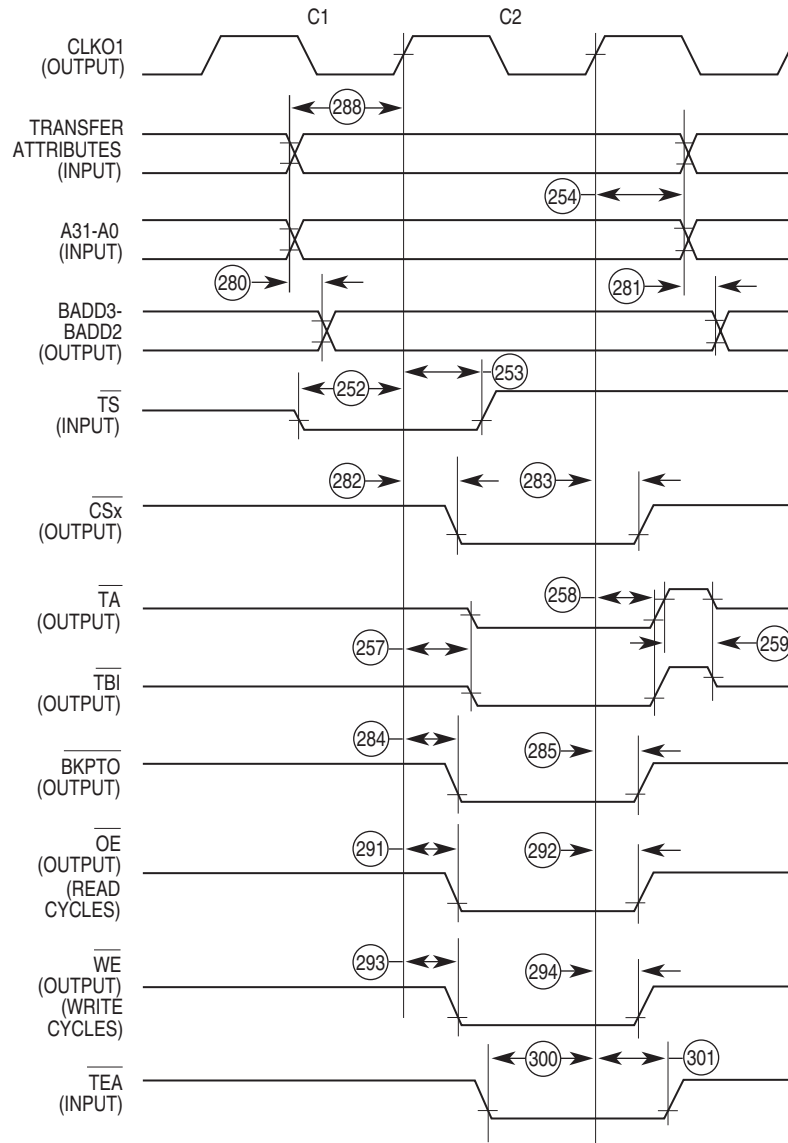
7.11 040 Bus Type SRAM/DRAM Cycles AC Electrical Specifications

Table 7-10. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-30 to Figure 7-34)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------------------|--|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 280 | Address Valid to BADD2-3 Valid | – | 20 | – | 15 | ns |
| 280A | BADD2-3 Valid to CAS Assertion | 15 | – | 10 | – | ns |
| 281 | Address Invalid to BADD2-3 Invalid | 0 | – | 0 | – | ns |
| 282 | Clock High to $\overline{\text{CSx/RASx}}$ Low (TSS40 = 0) | 4 | 16 | 4 | 12 | ns |
| 283 | Clock High to $\overline{\text{CSx/RASx}}$ High (CSNT40 = 0) | 4 | 16 | 4 | 12 | ns |
| 284 | Clock High to BRK Low | – | 20 | – | 15 | ns |
| 284A | Clock Low to BRK Low | – | 20 | – | 15 | ns |
| 285 | Clock high to BRK High | – | 20 | – | 15 | ns |
| 286 | Clock Low to $\overline{\text{CSx/RASx}}$ Low (TSS40 = 1) | 4 | 16 | 4 | 12 | ns |
| 287 | Clock Low to $\overline{\text{CSx/RASx}}$ High (CSNT40 = 1) | 4 | 16 | 4 | 12 | ns |
| 288 ⁽¹⁾ | Address Transfer Attributes Valid to Clock High (TSS40 = 0) | 10 | – | 10 | – | ns |
| 289 ⁽²⁾ | $\overline{\text{TA}}$ Low to Clock High (External Termination) | 11 | – | 9 | – | ns |
| 290 ⁽²⁾ | Clock High to $\overline{\text{TA}}$ High (External Termination) | – | 20 | – | 15 | ns |
| 291 | Clock High to $\overline{\text{OE}}$ Low (Read Cycles) | – | 20 | – | 15 | ns |
| 292 | Clock High to $\overline{\text{OE}}$ High (Read Cycles) | – | 20 | – | 15 | ns |
| 293 | Clock High to $\overline{\text{WE}}$ Low (Write Cycles) | – | 20 | – | 15 | ns |
| 294 | Clock High to $\overline{\text{WE}}$ High (Write Cycles) | – | 20 | – | 15 | ns |
| 295 | Clock High to $\overline{\text{CASx}}$ Low | 4 | 13 | 4 | 10 | ns |
| 295A | Clock Low to $\overline{\text{CASx}}$ Low (040 Burst Read only) | 4 | 13 | 4 | 10 | ns |
| 296 ⁽³⁾ | Clock High to $\overline{\text{CASx}}$ High | 4 | 13 | 4 | 10 | ns |
| 297 | Clock Low to AMUX Low | 3 | 16 | 3 | 12 | ns |
| 298 | Clock High to AMUX High | 3 | 16 | 3 | 12 | ns |
| 299 | Clock High to BADD2-3 Valid (040 Burst Cycles) | 4 | 20 | 4 | 15 | ns |
| 300 ⁽²⁾ | $\overline{\text{TEA}}$ Low to Clock High | 11 | – | – | – | ns |
| 301 ⁽²⁾ | Clock High to $\overline{\text{TEA}}$ High | 2 | 20 | 2 | 15 | ns |
| 302 | Data, Parity Valid to Clock High (Data, Parity Setup) | 7 | – | 6 | – | ns |
| 303 | Clock High to Data, Parity Invalid (Data, Parity Hold) | 7 | – | 5 | – | ns |
| 305 | CLKO1 High (After $\overline{\text{TS}}$ Low) to Parity Valid | – | 20 | – | 15 | ns |
| 306 | CLKO1 High (After $\overline{\text{TA}}$ Low) to Parity Hi-Z | 4 | 20 | – | 15 | ns |

- Notes: 1. Transfer attributes signals = SIZx, TTx, TMx, R/W and LOCK.
 2. $\overline{\text{TEA}}/\overline{\text{TA}}$ should not be asserted on a DRAM burst access, or on the same clock or before $\overline{\text{RASx}}/\overline{\text{CSx}}$ is asserted.
 3. The clock reference is EXTAL, not CLK01.

Figure 7-30. TS68040 SRAM Read/Write Cycles (TSS40 = 0, CSNT40 = 0)



Note: TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.

Figure 7-31. TS68040 SRAM Read/Write Cycles (TSS40 = 1, CSNT40 = 1)

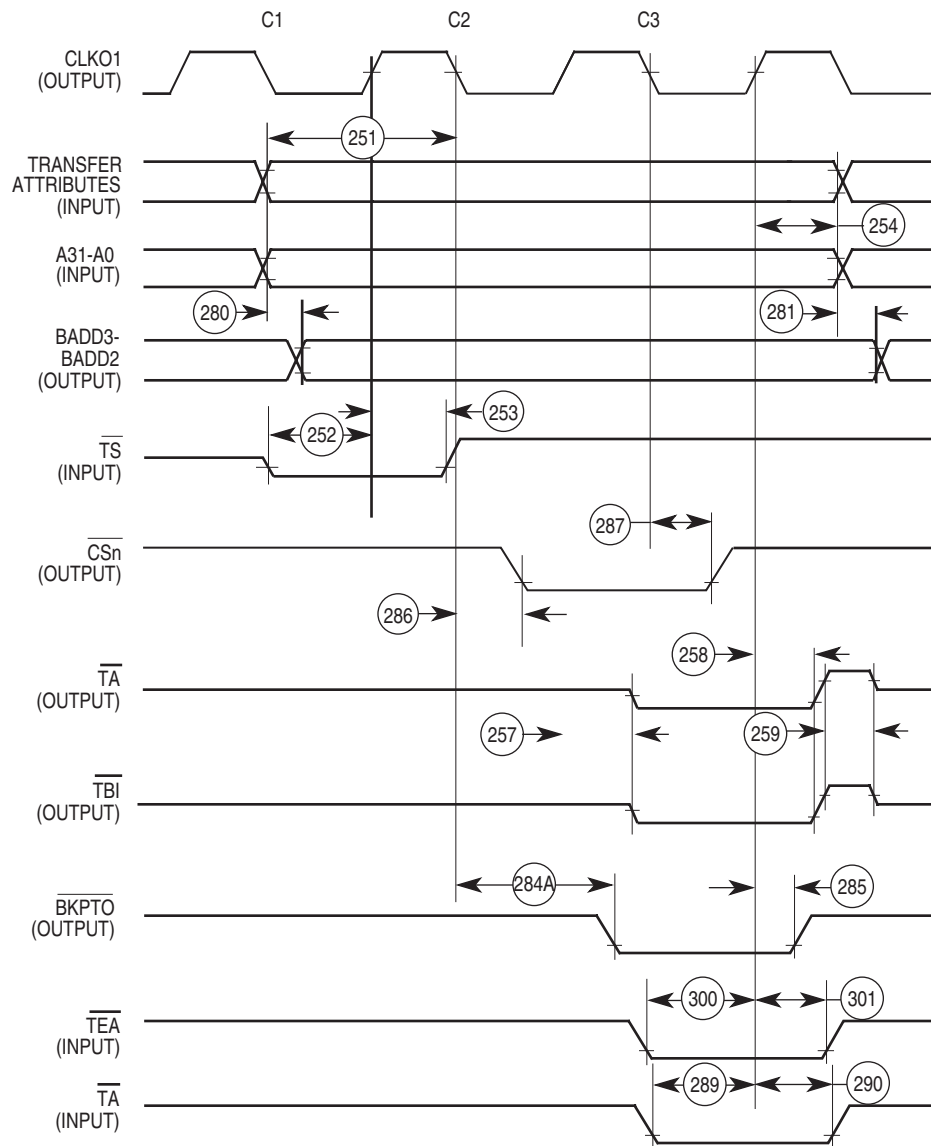


Figure 7-32. External TS68040 DRAM Cycles Timing Diagram

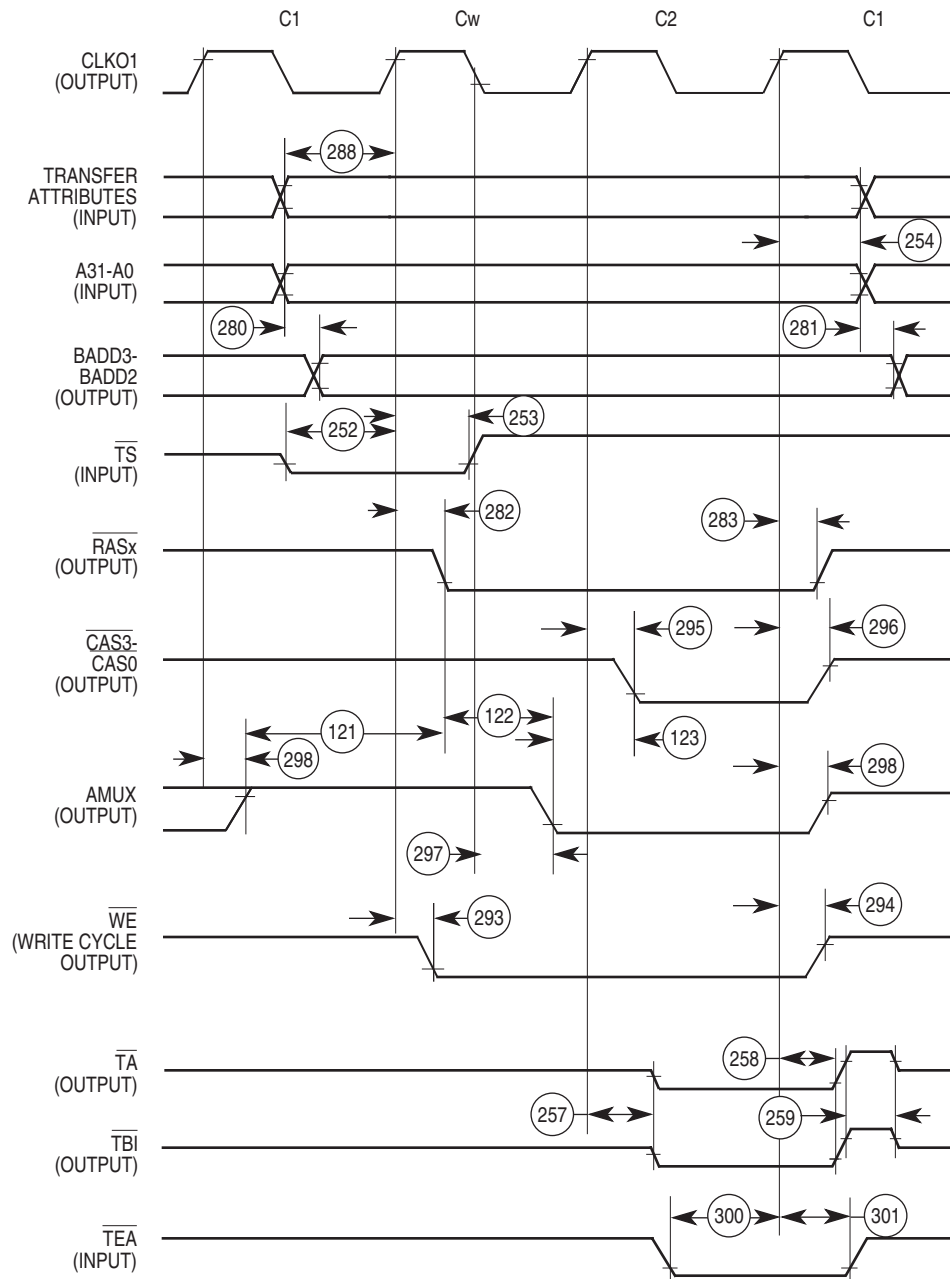


Figure 7-33. External TS68040 DRAM Burst Cycles Timing Diagram

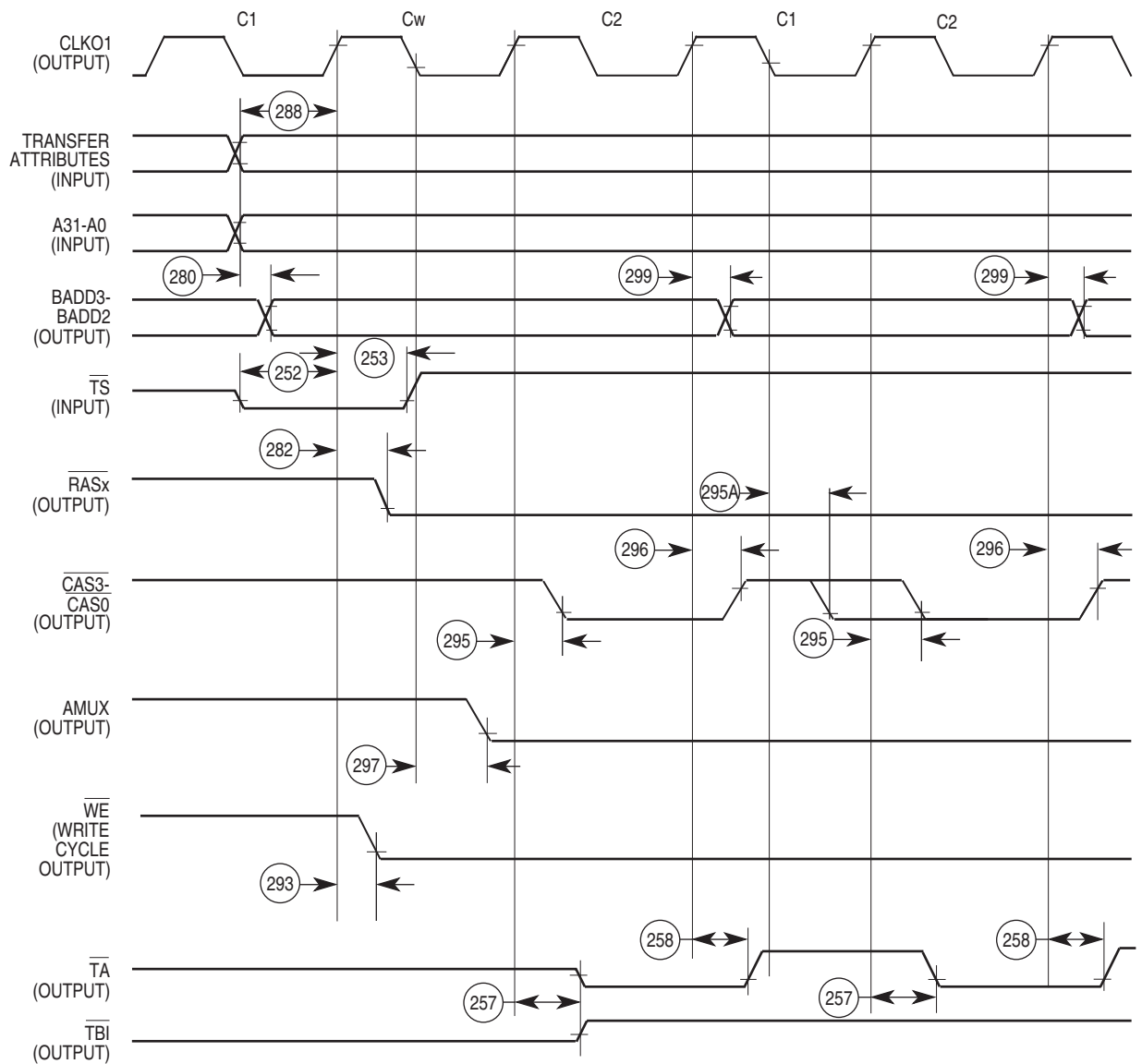
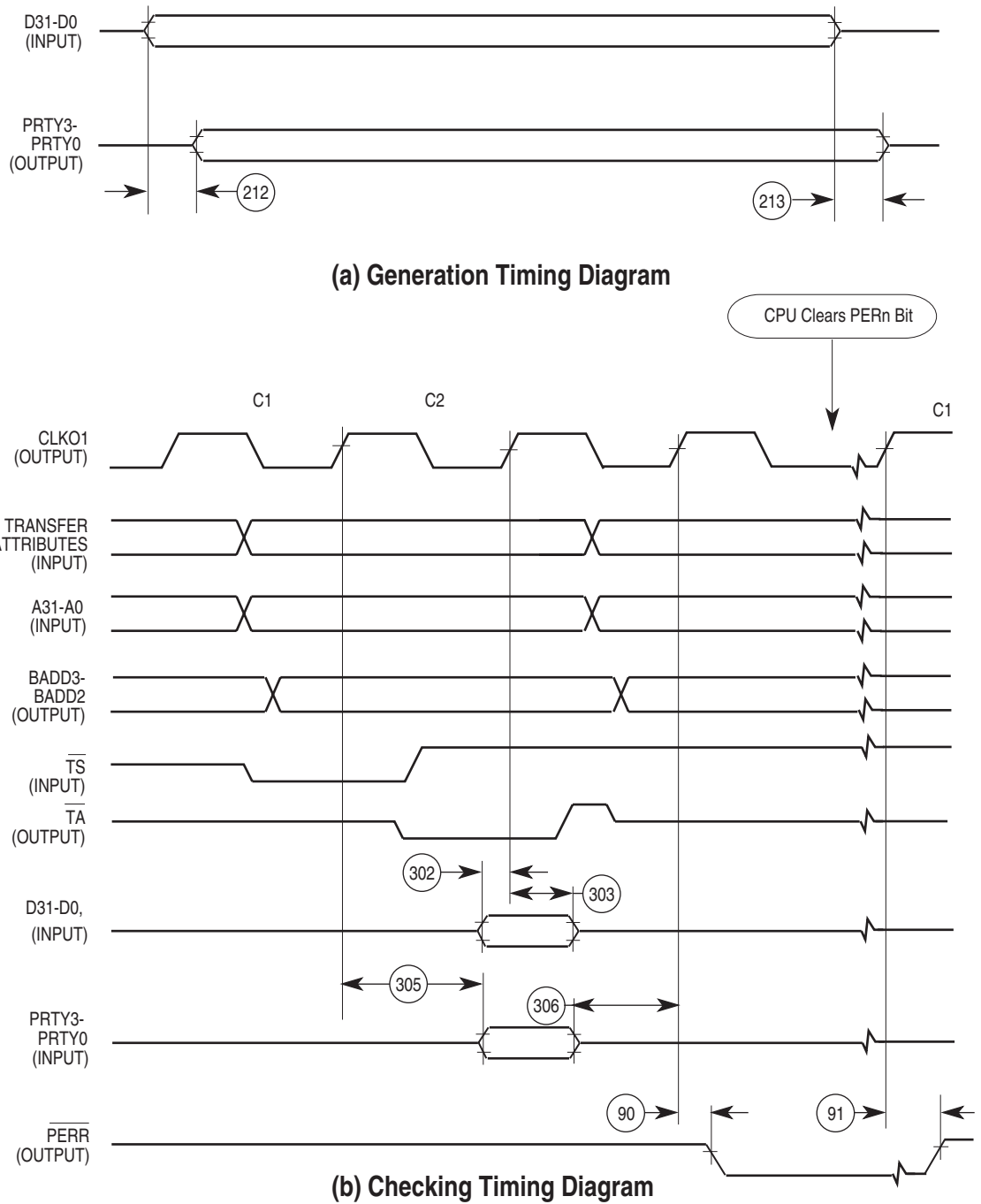


Figure 7-34. External TS68040 Parity Bit Checking Timing Diagram



7.12 IDMA AC Electrical Specifications

Table 7-11. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-35 and Figure 7-36)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|-------------------|---|----------------------------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 1 | CLKO1 Low to \overline{DACK} , \overline{DONE} Asserted | 3 | 24 | 3 | 18 | ns |
| 2 | CLKO1 Low to \overline{DACK} , \overline{DONE} Negated | 3 | 24 | 3 | 18 | ns |
| 3 ⁽¹⁾ | \overline{DREQx} Asserted to \overline{AS} Asserted (for DMA Bus Cycle) | $3t_{cyc} + t_{AIST} + t_{CLSA}$ | | | | |
| 4 ⁽¹⁾ | Asynchronous Input Setup Time to CLKO1 Low | 12 | – | 9 | – | ns |
| 5 ⁽¹⁾ | Asynchronous Input Hold Time from CLKO1 Low | 0 | – | 0 | – | ns |
| 6 | \overline{AS} to \overline{DACK} Assertion Skew | 0 | 20 | 0 | 15 | ns |
| 7 | \overline{DACK} to \overline{DONE} Assertion Skew | -8 | 8 | -6 | 6 | ns |
| 8 | \overline{AS} , \overline{DACK} , \overline{DONE} Width Asserted | 70 | – | 52.5 | – | ns |
| 8A | \overline{AS} , \overline{DACK} , \overline{DONE} Width Asserted (Fast Termination Cycle) | 28 | – | 20.5 | – | ns |
| 10 ⁽¹⁾ | Asynchronous Input Setup Time to CLKO1 Low | 5 | – | 4 | – | ns |
| 11 ⁽¹⁾ | Asynchronous Input Hold Time from CLKO1 Low | 10 | – | 7.5 | – | ns |
| 12 ⁽²⁾ | DREQ Input Setup Time to CLKO1 Low | 20 | – | 15 | – | ns |
| 13 ⁽²⁾ | DREQ Input Hold Time from CLKO1 Low | 5 | – | 3.75 | – | ns |
| 14 ⁽²⁾ | DONE Input Setup Time to CLKO1 Low | 20 | – | 15 | – | ns |
| 15 ⁽²⁾ | DONE Input Hold Time From CLKO1 Low | 5 | – | 3.75 | – | ns |
| 16 ⁽²⁾ | DREQ Asserted to \overline{AS} Asserted | 2 | – | 2 | – | clk |

- Notes: 1. These specifications are for asynchronous mode.
 2. These specifications are for synchronous mode.

Figure 7-35. IDMA Signal Asynchronous Timing Diagram

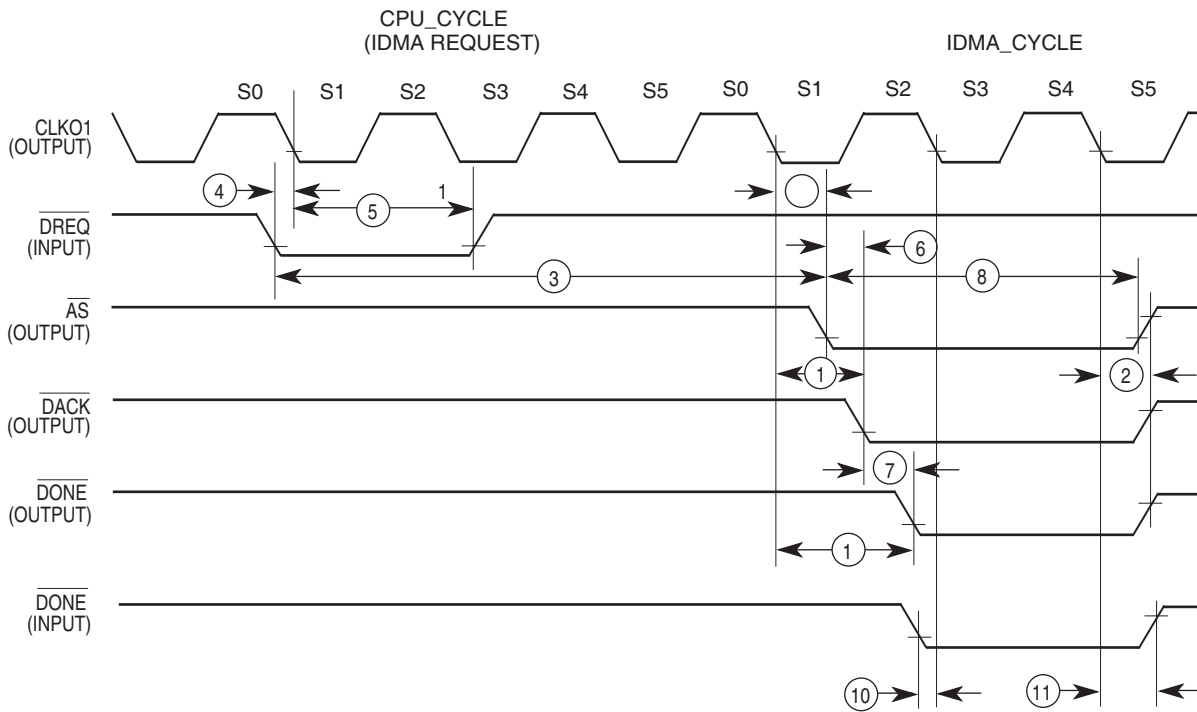
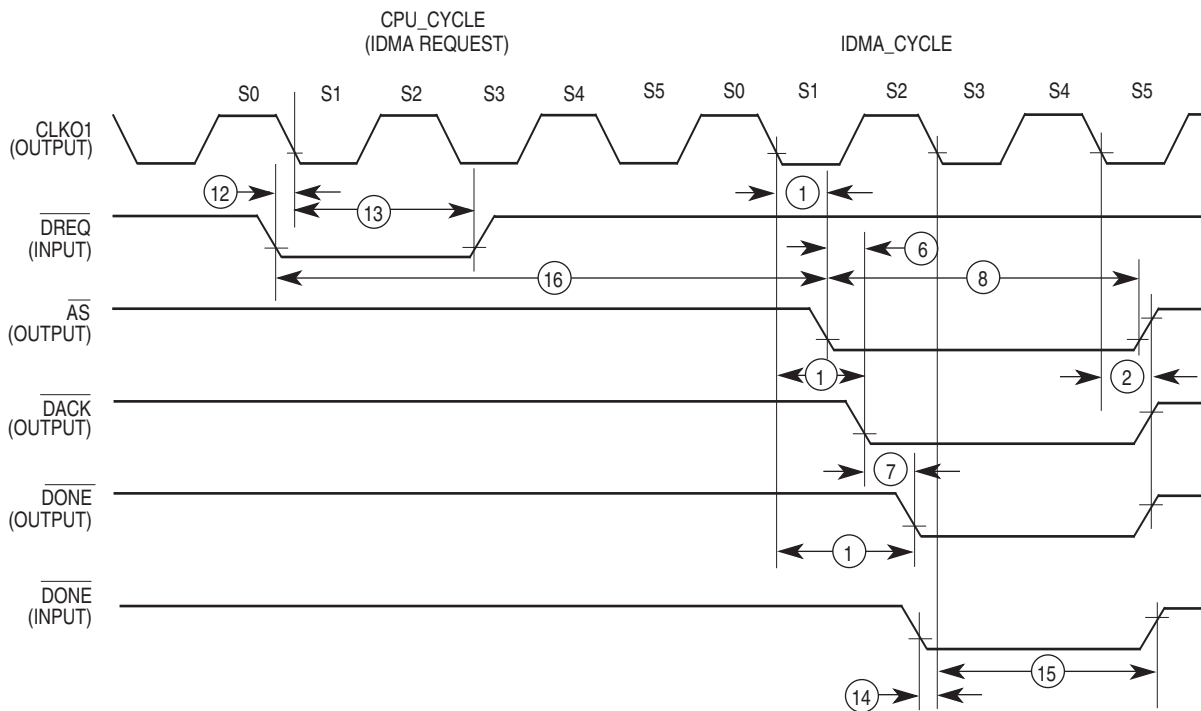


Figure 7-36. IDMA Signal Synchronous Timing Diagram



7.13 PIP/PIO Electrical Specifications

Table 7-12. GND = 0 V_{DC}; T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-37 to Figure 7-41)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|---|----------------|-----|----------------|-----|------|
| | | Min | Max | Min | Max | |
| 21 | Data-In Setup Time to STBI Low | 0 | – | 0 | – | ns |
| 22 | Data-In Hold Time to STBI High | 2.5 – t3 | – | 2.5 – t3 | – | clk |
| 23 | STBI Pulse Width | 1.5 | – | 1.5 | – | clk |
| 24 | STBO Pulse Width | 1 CLK01 – 5 ns | – | 1 CLK01 – 5 ns | – | –v |
| 25 | Data-Out Setup Time to STBO Low | 2 | – | 2 | – | clk |
| 26 | Data-Out Hold Time from STBO High | 5 | – | 5 | – | clk |
| 27 | STBI Low to STBO Low (Rx Interlock) | – | 2 | – | 2 | clk |
| 28 | STBI Low to STBO High (Tx Interlock) | 2 | – | 2 | – | clk |
| 29 | Data-In Setup Time to Clock Low | 20 | – | 15 | – | ns |
| 30 | Data-In Hold Time from Clock Low | 10 | – | 7.5 | – | ns |
| | Clock High to Data-Out Valid (CPU Writes Data, Control, or Direction) | – | 25 | – | 25 | ns |

Note: 1. t3 = spec. 3 on Table 7-4.

Figure 7-37. PIP Rx (Interlock Mode)

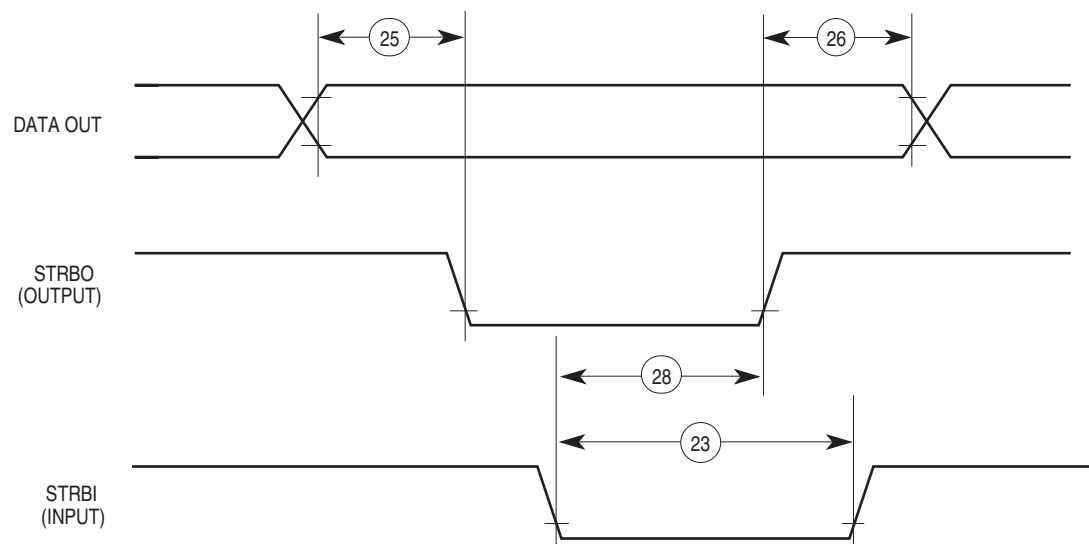


Figure 7-38. PIP Tx (Interlock Mode)

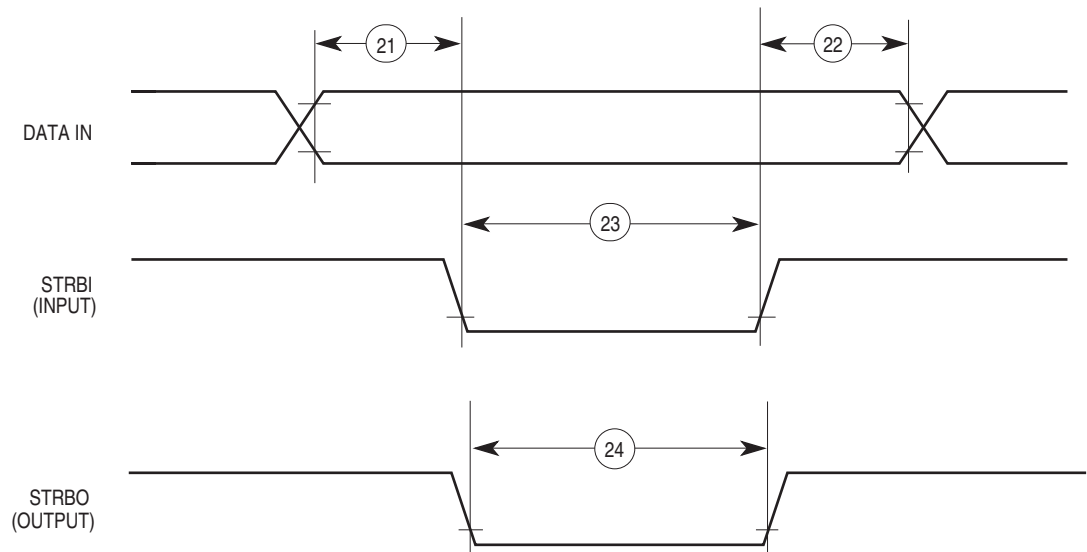


Figure 7-39. PIP Tx (Pulse Mode)

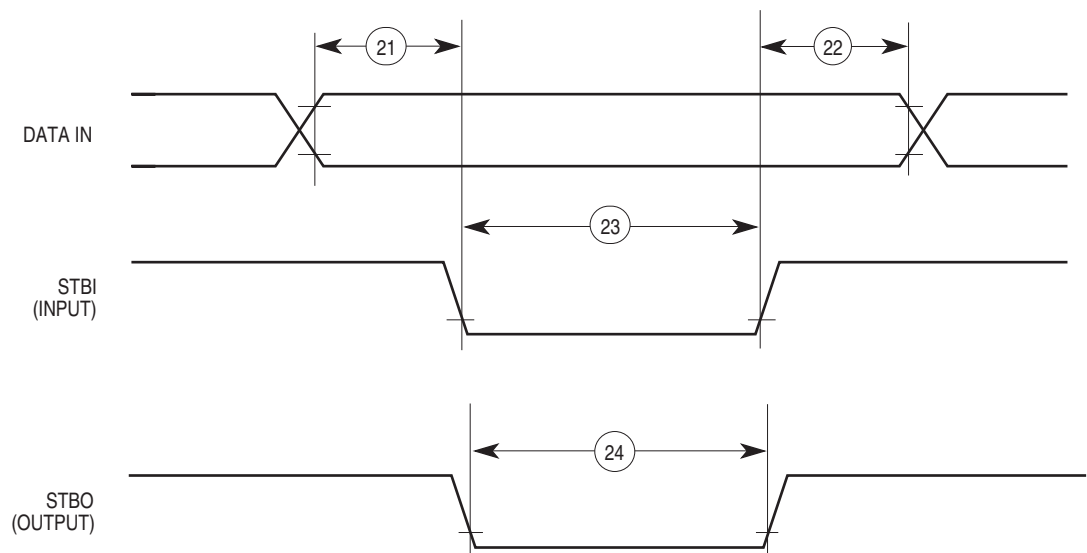


Figure 7-40. PIP Tx (Pulse Mode)

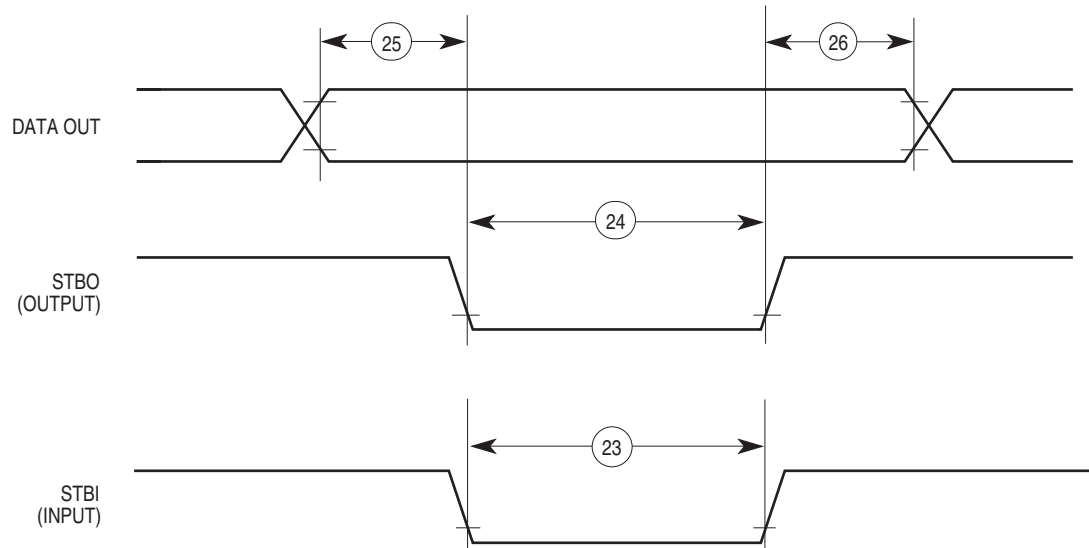
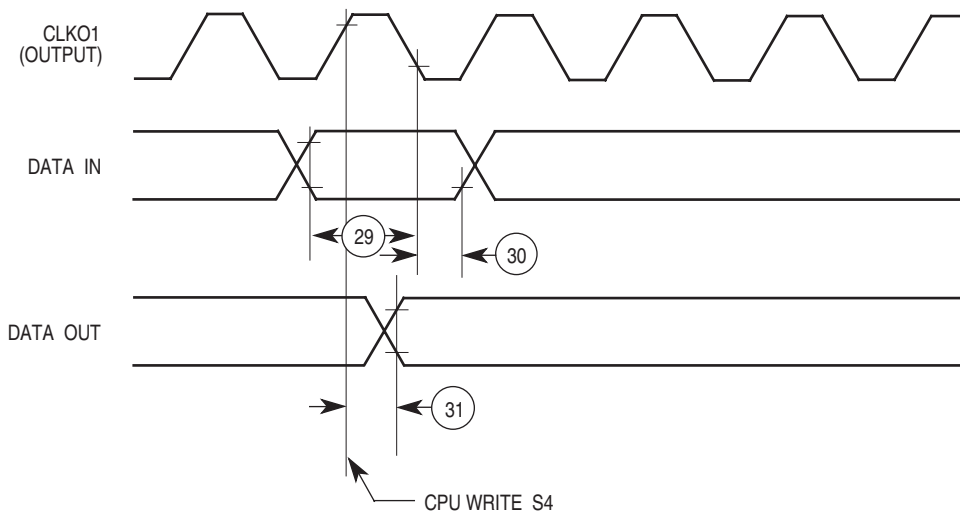


Figure 7-41. Parallel I/O Data-in/Data-out Timing Diagram



7.14 Interrupt Controller AC Electrical Specifications

Table 7-13. GND = 0 V_{DC}; T_C = -55 to +125°C. The electrical specifications in this document are preliminary. (See Figure 7-42 and Figure 7-43)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|--|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 35 | Port C Interrupt Pulse Width Low (Edge Triggered Mode) | 70 | – | 55 | – | ns |
| 36 | Minimum Time Between Active Edges Port C | 70 | – | 55 | – | clk |
| 37 | Clock High to $\overline{\text{IOUT}}$ Valid (Slave Mode) | – | 20 | – | 17 | ns |
| 38 | Clock High to $\overline{\text{RQOUT}}$ Valid (Slave Mode) | – | 20 | – | 17 | ns |

Figure 7-42. Interrupts Timing Diagram

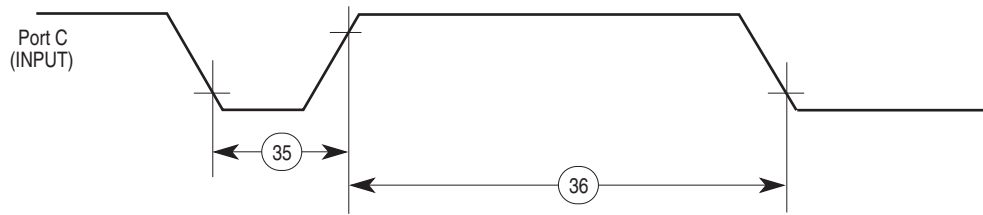
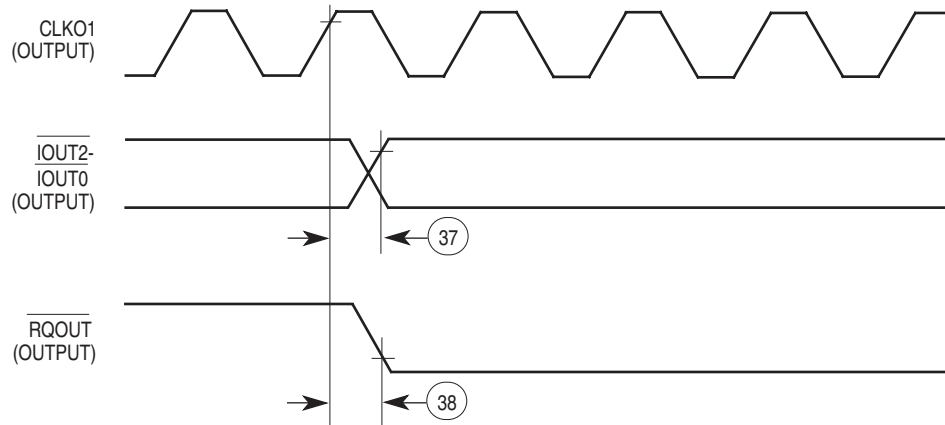


Figure 7-43. Slave Mode: Interrupts Timing Diagram

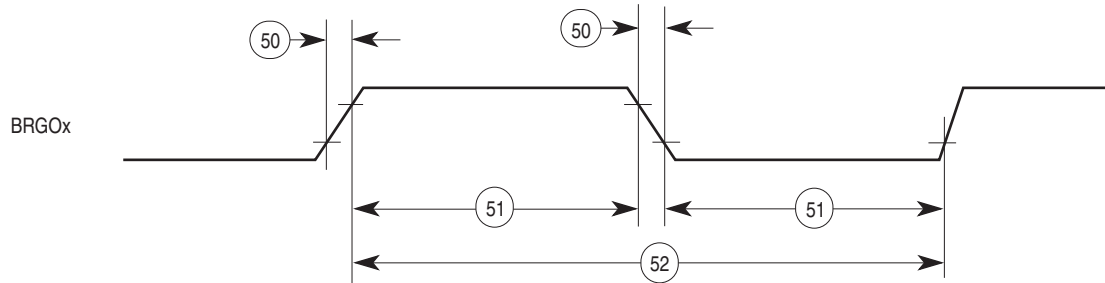


7.15 BAUD RATE GENERATOR AC Electrical Specifications

Table 7-14. GND = 0 V_{DC}, T_C = -55 to +125 °C. The electrical specifications in this document are preliminary (See [Figure 7-44](#))

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|-------------------------|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 50 | BRGO Rise and Fall Time | – | 10 | – | 7.5 | ns |
| 51 | BRGO Duty Cycle | 40 | 60 | 40 | 60 | % |
| 52 | BRGO Cycle | 40 | | 30 | | ns |

Figure 7-44. Baud Rate Generator Output Signals

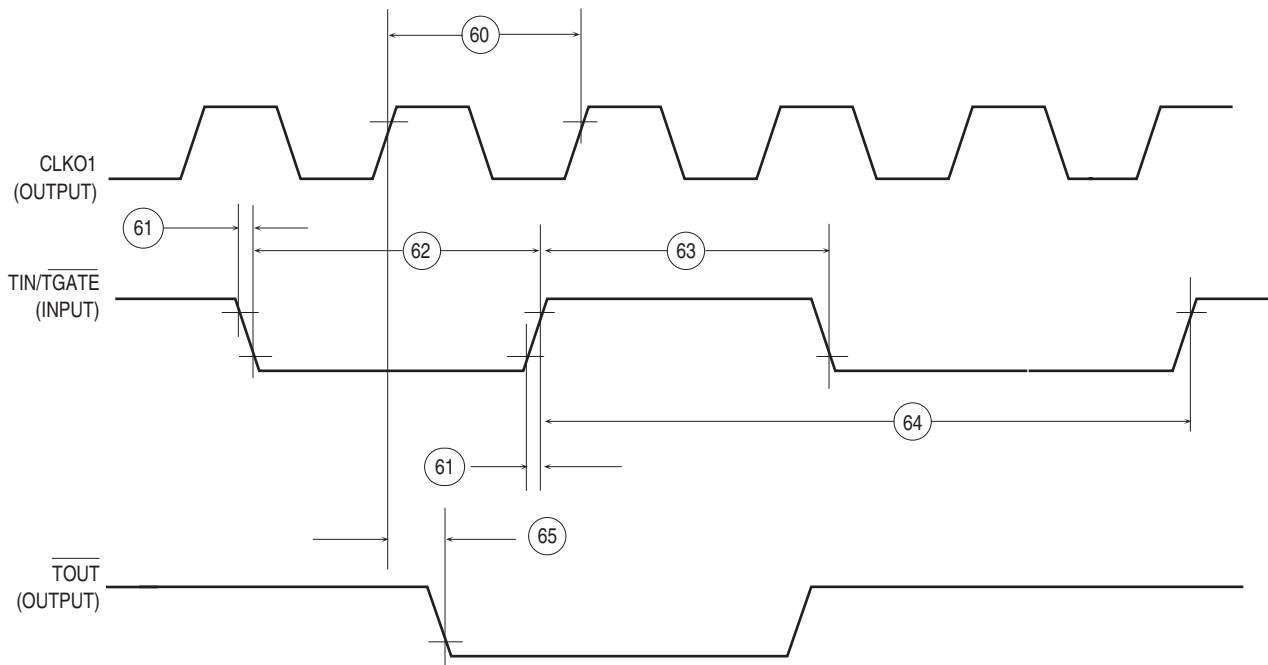


7.16 Timer Electrical Specifications

Table 7-15. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-45)

| Number | Characteristic | Symbol | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|--|-----------------|----------|-----|-----------|-----|------|
| | | | Min | Max | Min | Max | |
| 61 | TIN/TGATE Rise and Fall Time | t _{rf} | 10 | – | 10 | – | ns |
| 62 | TIN/TGATE Low Time | – | 1 | – | 1 | – | clk |
| 63 | TIN/TGATE High Time | – | 2 | – | 2 | – | clk |
| 64 | TIN/TGATE Cycle Time | – | 3 | – | 3 | – | clk |
| 65 | CLKO1 High to $\overline{\text{TOUT}}$ Valid | t _{TO} | 3 | 25 | 3 | 22 | ns |

Figure 7-45. CPM General-purpose Timers



7.17 SI Electrical Specifications

Table 7-16. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See [Figure 7-46](#) to [Figure 7-50](#))

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|----------------------|---|----------|------|-----------|-----|--------|
| | | Min | Max | Min | Max | |
| 70 ⁽¹⁾⁽³⁾ | L1RCLK, L1TCLK Frequency (DCS = 0) | – | 10 | – | 10 | MHz |
| 71 ⁽¹⁾ | L1RCLK, L1TCLK Width Low (DCS = 0) | P+10 | – | P+10 | – | ns |
| 71A ⁽²⁾ | L1RCLK, L1TCLK Width High (DCS = 0) | P+10 | – | P+10 | – | ns |
| 72 | L1TXD, L1ST(1-4), L1RQ, L1CLKO Rise/Fall Time | – | 15 | – | 15 | ns |
| 73 | L1RSYNC, L1TSYNC Valid to L1CLK Edge (SYNC Setup Time) | 20 | – | 20 | – | ns |
| 74 | L1CLK Edge to L1RSYNC, L1TSYNC Invalid (SYNC Hold Time) | 35 | – | 35 | – | ns |
| 75 | L1RSYNC, L1TSYNC Rise/Fall Time | – | 15 | – | 15 | ns |
| 76 | L1RXD Valid to L1CLK Edge (L1RXD Setup Time) | 42 | – | 42 | – | ns |
| 77 | L1CLK Edge to L1RXD Invalid (L1RXD Hold Time) | 35 | – | 35 | – | ns |
| 78 | L1CLK Edge to L1ST(1-4) Valid | 10 | 45 | 10 | 45 | ns |
| 78A ⁽⁴⁾ | L1SYNC Valid to L1ST(1-4) Valid | 10 | 45 | 10 | 45 | ns |
| 79 | L1CLK Edge to L1ST(1-4) Invalid | 10 | 45 | 10 | 45 | ns |
| 80 | L1CLK Edge to L1TXD Valid | 10 | 65 | 10 | 65 | ns |
| 80A ⁽⁴⁾ | L1TSYNC Valid to L1TXD Valid | 10 | 65 | 10 | 65 | ns |
| 81 | L1CLK Edge to L1TXD High Impedance | 0 | 42 | 0 | 42 | ns |
| 82 | L1RCLK, L1TCLK Frequency (DSC = 1) | – | 12.5 | – | 16 | MHz |
| 83 | L1RCLK, L1TCLK Width Low (DSC = 1) | P+10 | – | P+10 | – | ns |
| 83A ⁽²⁾ | L1RCLK, L1TCLK Width High (DSC = 1) | P+10 | – | P+10 | – | ns |
| 84 | L1CLK Edge to L1CLKO Valid (DSC = 1) | – | 30 | – | 30 | ns |
| 85 ⁽³⁾ | L1RQ Valid Before Falling Edge of L1TSYNC | 1 | – | 1 | – | L1TCLK |
| 86 ⁽³⁾ | L1GR Setup Time | 42 | – | 42 | – | ns |
| 87 ⁽³⁾ | L1RG Hold Time | 42 | – | 42 | – | ns |
| 88 | L1CLK Edge to L1SYNC Valid (FSD = 00, CNT = 0000, BYT = 0, DSC = 0) | – | 0 | – | 0 | ns |

- Notes:
1. The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
 2. Where P = 1/CLKO1. Thus for a 25 MHz CLKO1 rate, P = 40 ns.
 3. These specs are valid for IDL mode only.
 4. The strobes and Txd on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

Figure 7-46. SI Receive Timing with Normal Clocking (DSC = 0)

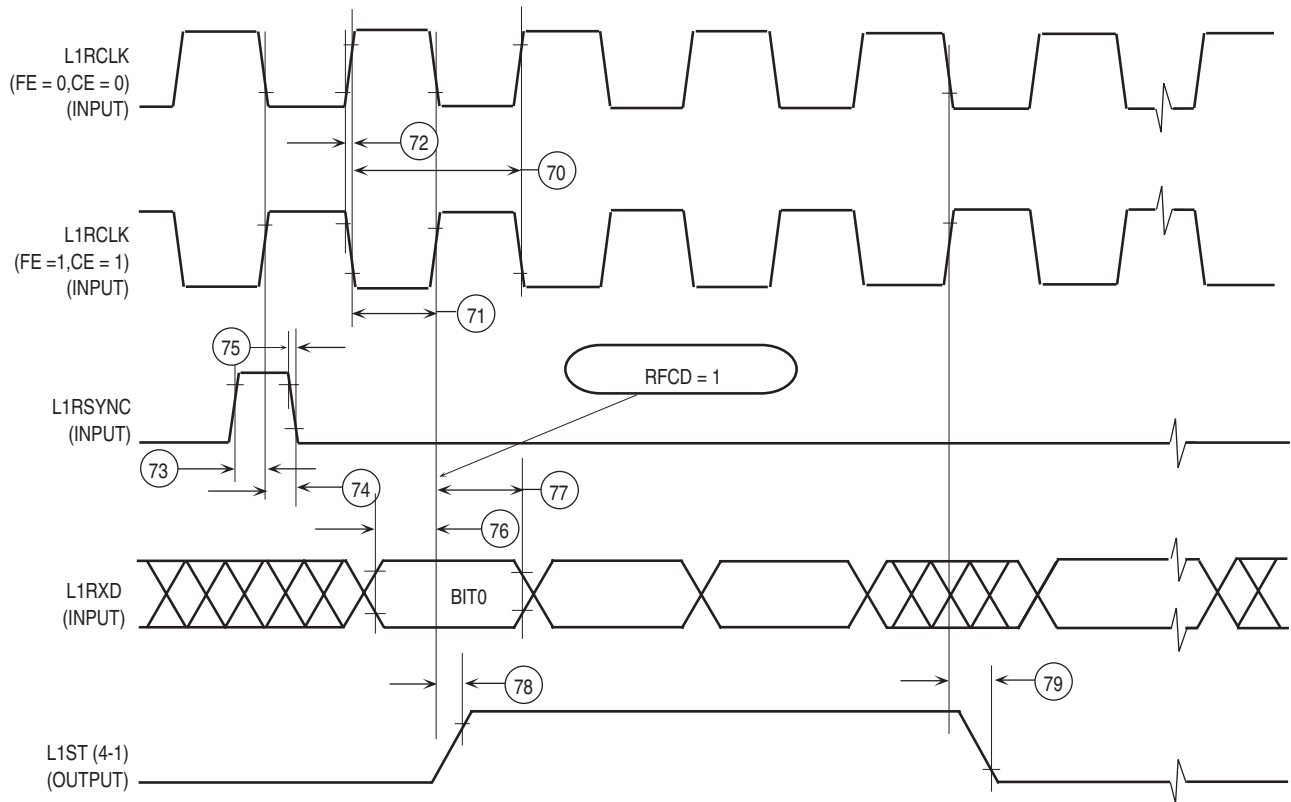


Figure 7-47. SI Receive Timing with Double Speed Clocking (DSC = 1)

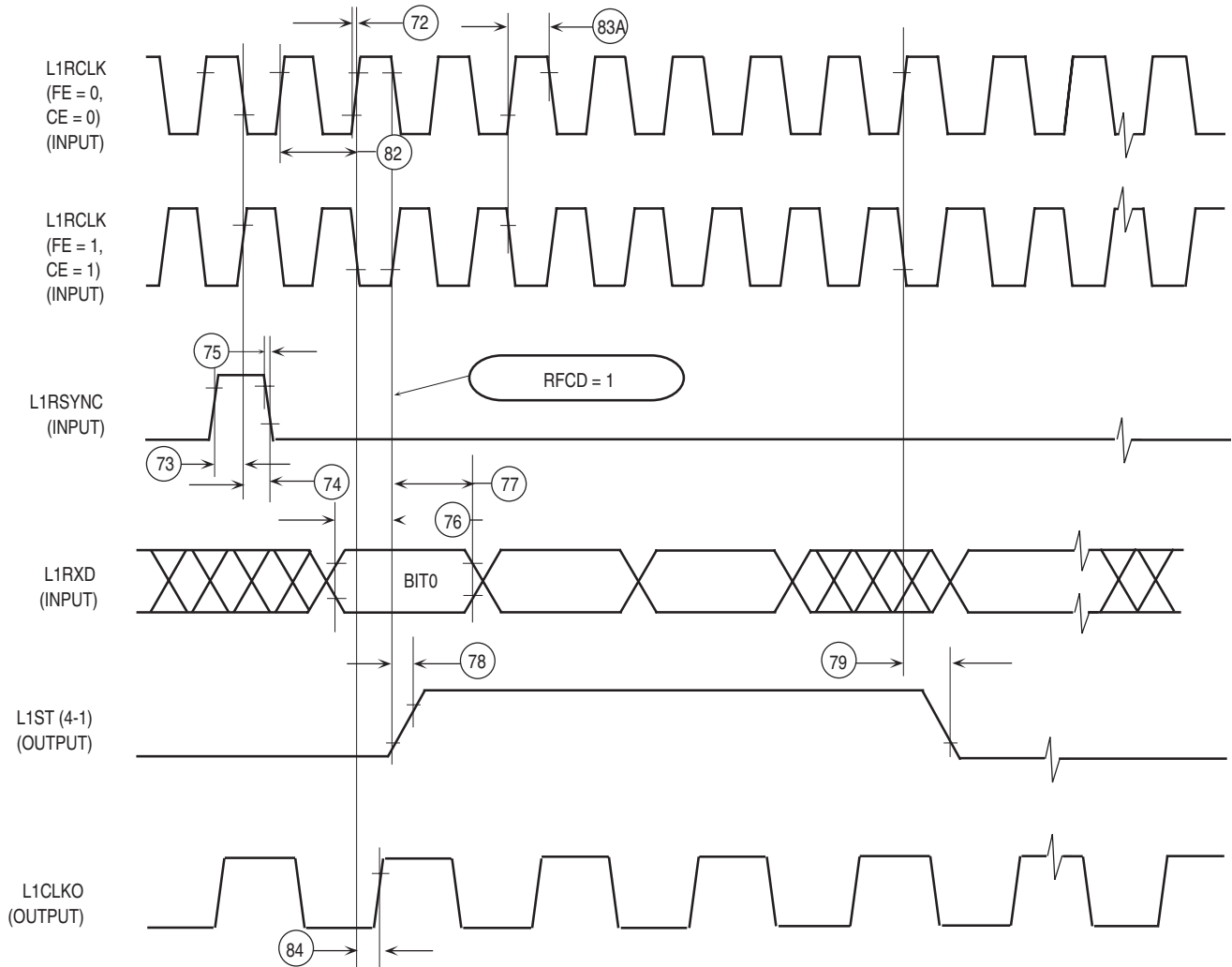


Figure 7-48. SI Transmit Timing with Normal Clocking (DSC = 0)

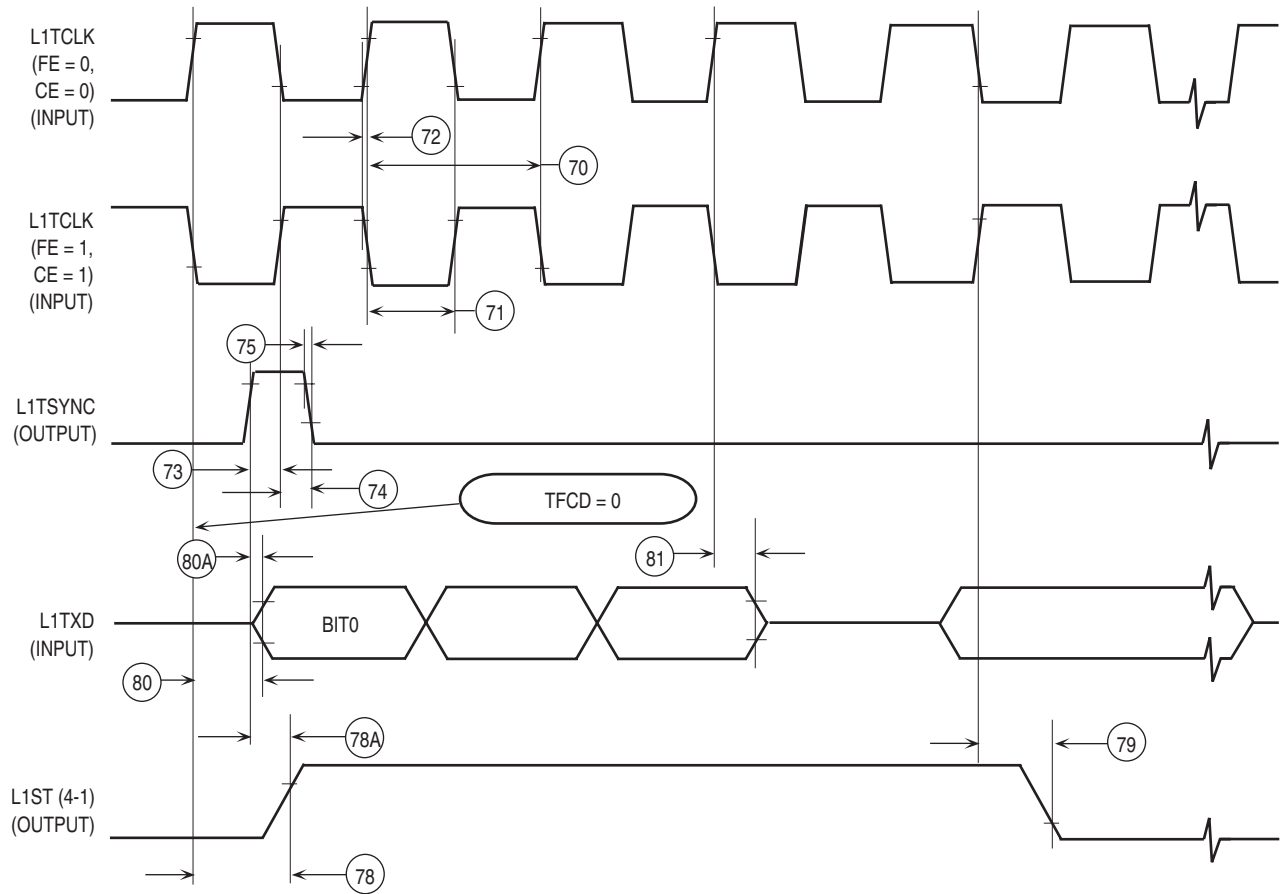


Figure 7-49. SI Transmit Timing with Double Speed Clocking (DSC = 1)

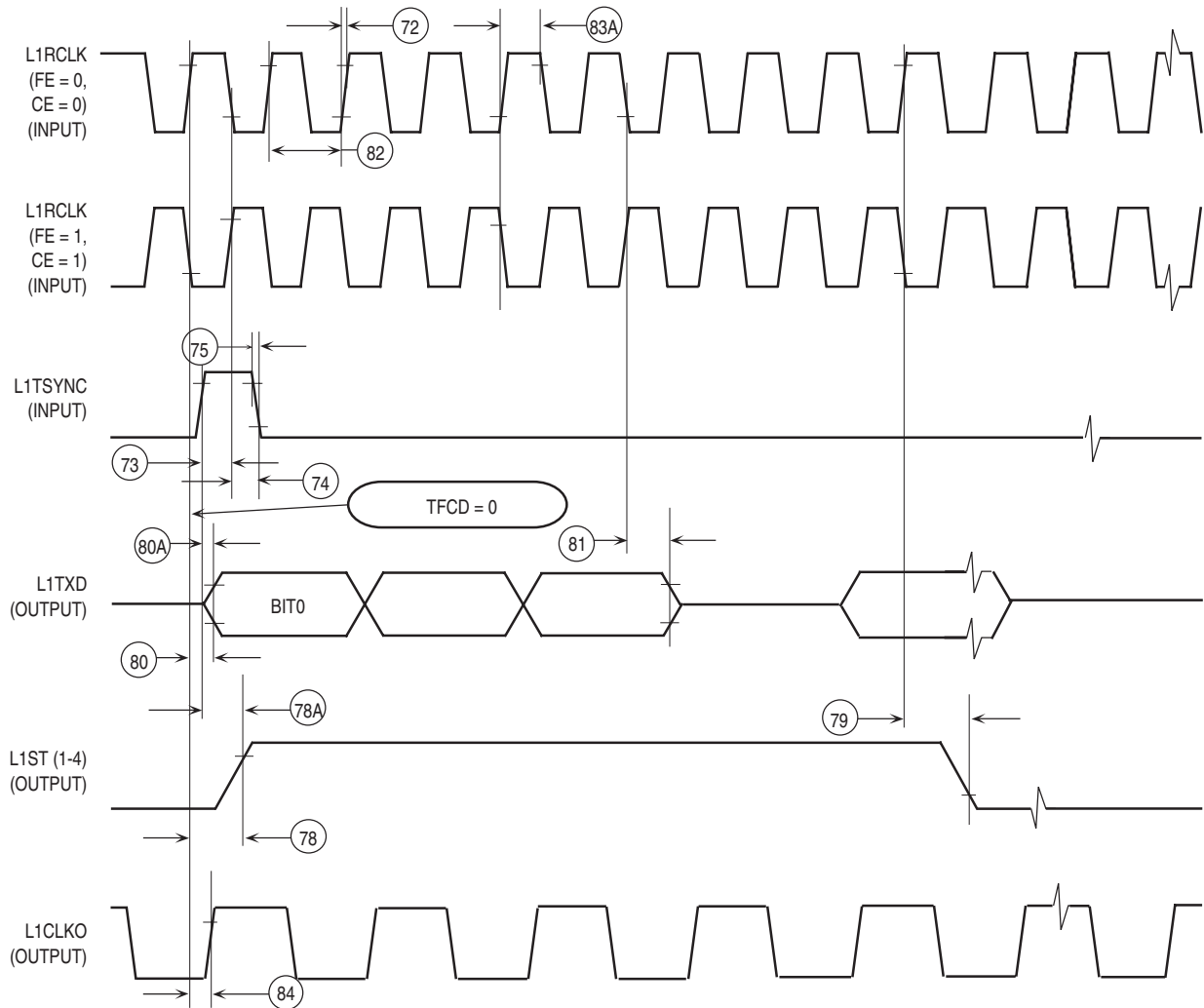
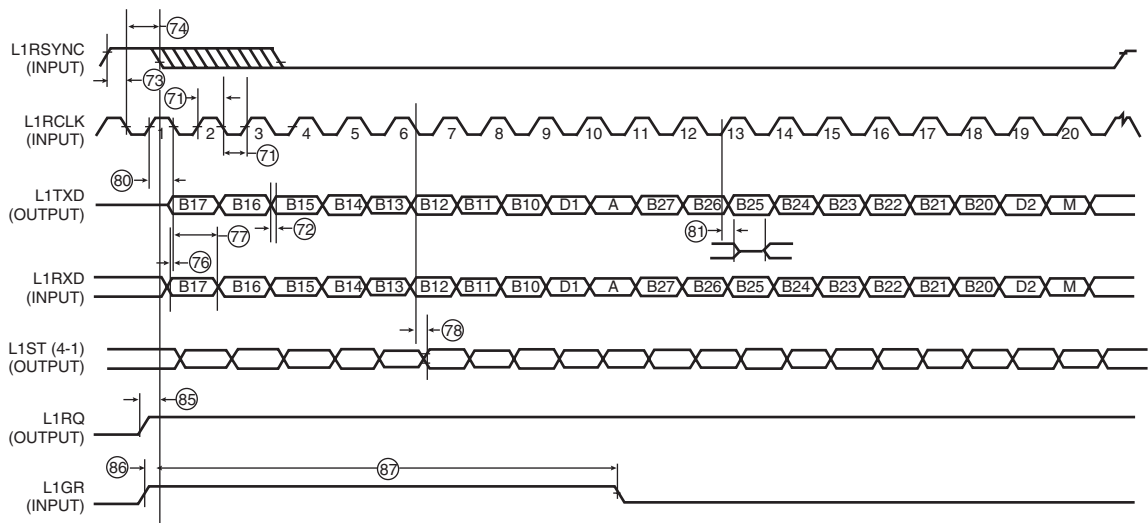


Figure 7-50. IDL Timing SI Transmit Timing with Double Speed Clocking (DSC = 1)



7.18 SCC in NMSI Mode-external Clock Electrical Specifications

Table 7-17. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-51 to Figure 7-53)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------------------|--|--------------|-----|--------------|-----|------|
| | | Min | Max | Min | Max | |
| 100 ⁽¹⁾ | RCLK1 and TCLK1 Width High | CLKO1 | – | CLKO1 | – | |
| 101 | RCLK1 and TCLK1 Width Low | CLKO1 + 5 ns | – | CLKO1 + 5 ns | – | |
| 102 | RCLK1 and TCLK1 Rise/Fall Time | – | 15 | – | 15 | ns |
| 103 | TXD1 Active Delay (From TCLK1 Falling Edge) | 0 | 50 | 0 | 50 | ns |
| 104 | $\overline{\text{RTS1}}$ Active/Inactive Delay (From TCLK1 Falling Edge) | 0 | 50 | 0 | 50 | ns |
| 105 | $\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge | 40 | – | 40 | – | ns |
| 106 | RXD1 Setup Time to RCLK1 Rising Edge | 40 | – | 40 | – | ns |
| 107 ⁽²⁾ | RXD1 Hold Time from RCLK1 Rising Edge | 0 | – | 0 | – | ns |
| 108 | $\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge | 40 | – | 40 | – | ns |

Notes: 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1.
 2. Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

7.19 SCC in NMSI Mode-internal Clock Electrical Specifications

Table 7-18. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-51 to Figure 7-53)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------------------|--|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 100 ⁽¹⁾ | RCLK1 and TCLK1 Frequency | 0 | 8.3 | 0 | 11 | MHz |
| 102 | RCLK1 and TCLK1 Rise/Fall Time | – | – | – | – | ns |
| 103 | TXD1 Active Delay (From TCLK1 Falling Edge) | 0 | 30 | 0 | 30 | ns |
| 104 | $\overline{\text{RTS1}}$ Active/Inactive Delay (From TCLK1 Falling Edge) | 0 | 30 | 40 | – | ns |
| 105 | $\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge | 40 | – | 40 | – | ns |
| 106 | RXD1 Setup Time to RCLK1 Rising Edge | 40 | – | 0 | – | ns |
| 107 ⁽²⁾ | RXD1 Hold Time from RCLK1 Rising Edge | 0 | – | 40 | – | ns |
| 108 | $\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge | 40 | – | 0 | 30 | ns |

Notes: 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.
 2. Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Figure 7-51. SCC NMSI Receive

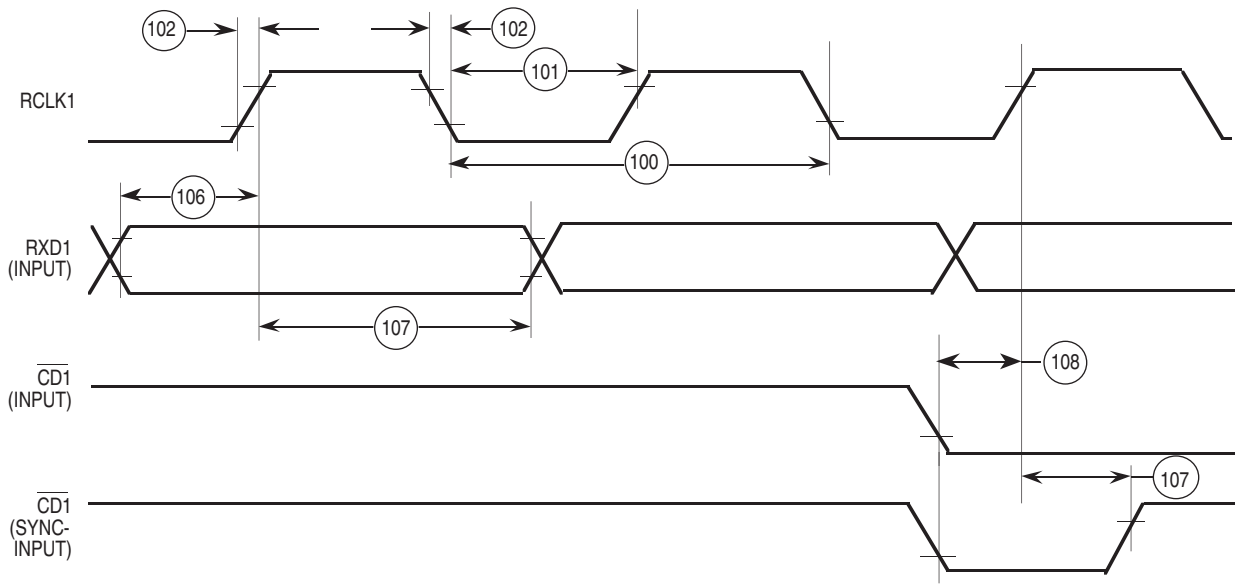


Figure 7-52. SCC NMSI Transmit

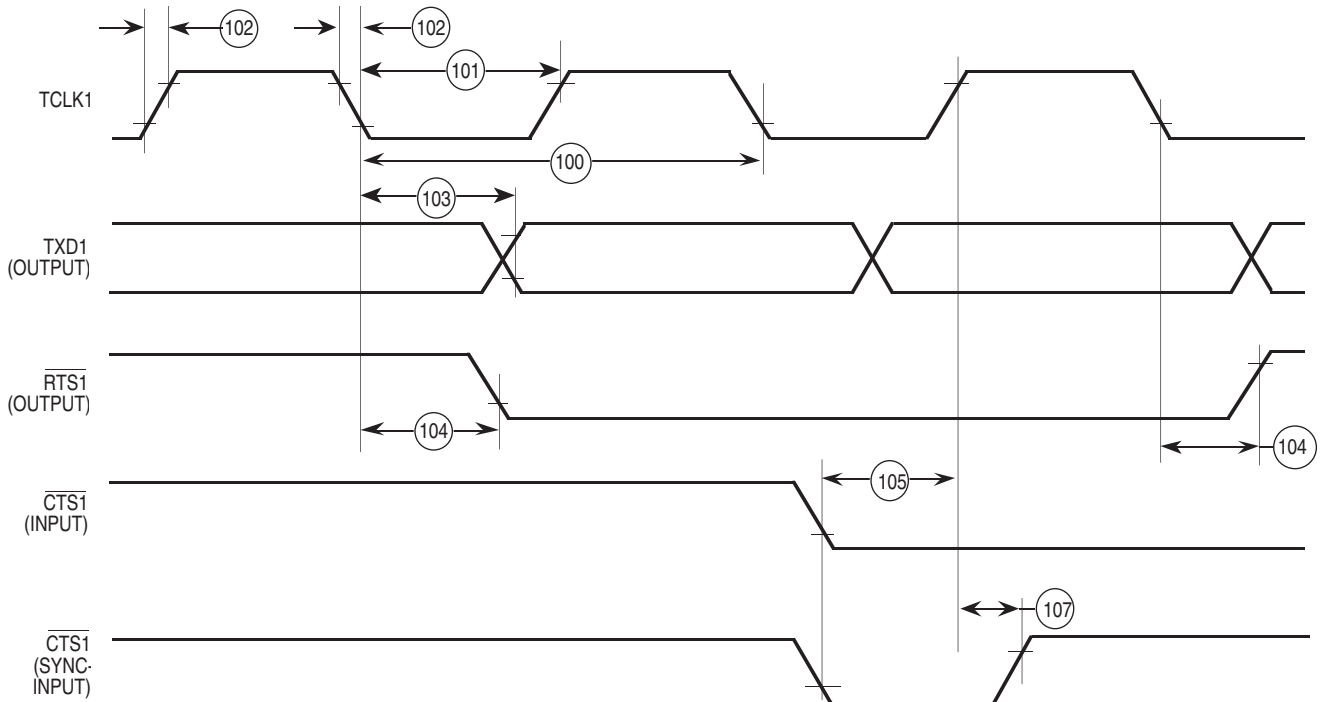
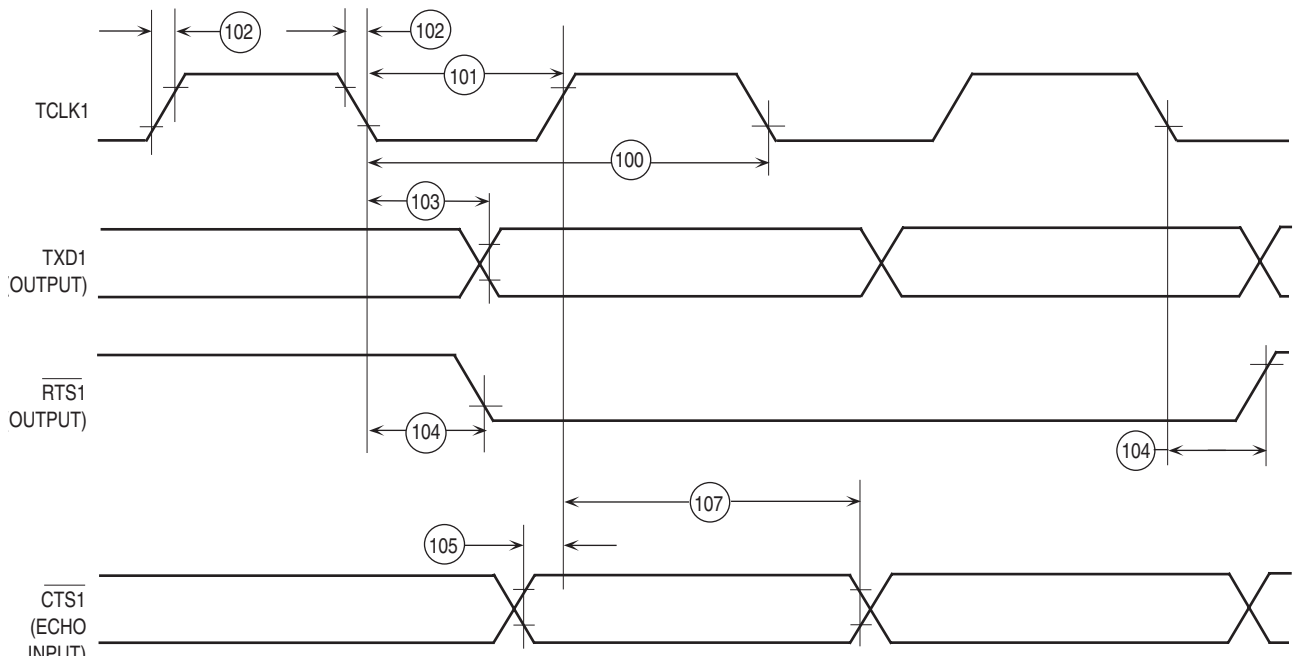


Figure 7-53. HDLC BUS Timing



7.20 Ethernet Electrical Specifications

Table 7-19. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See [Figure 7-54](#) to [Figure 7-59](#))

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------------------|---|--------------|-----|--------------|-----|-------|
| | | Min | Max | Min | Max | |
| 120 | CLSN Width High | 40 | – | 40 | – | ns |
| 121 | RCLK1 Rise/Fall Time | – | 15 | – | 15 | ns |
| 122 | RCLK1 Width Low | CLKO1 + 5 ns | – | CLKO1 + 5 ns | – | |
| 123 ⁽¹⁾ | RCLK1 Width High | CLKO1 | – | CLKO1 | – | |
| 124 | RXD1 Setup Time | 20 | – | 20 | – | ns |
| 125 | RXD1 Hold Time | 5 | – | 5 | – | ns |
| 126 | RENA Active Delay (from RCLK1 rising edge of the last data bit) | 10 | – | 10 | – | ns |
| 127 | RENA Width Low | 100 | – | 100 | – | ns |
| 128 | TCLK1 Rise/Fall Time | – | 15 | – | 15 | ns |
| 129 | TCLK1 Width Low | CLKO1 + 5 ns | – | CLKO1 + 5 ns | – | |
| 130 ⁽¹⁾ | TCLK1 Width High | CLKO1 | – | CLKO1 | – | |
| 131 | TXD1 Active Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 132 | TXD1 Inactive Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 133 | TENA Active Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 134 | TENA Inactive Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 135 | RSTRT Active Delay (from TCLK1 falling edge) | 10 | 50 | 10 | 50 | ns |
| 136 | RSTRT Inactive Delay (from TCLK1 falling edge) | 10 | 50 | 10 | 50 | ns |
| 137 | RRJCT Width Low | 1 | – | 1 | – | CLKO1 |
| 138 ⁽²⁾ | CLKO1 Low to $\overline{\text{SDACK}}$ Asserted | – | 20 | – | 20 | ns |
| 139 ⁽²⁾ | CLKO1 Low to $\overline{\text{SDACK}}$ Negated | – | 20 | – | 20 | ns |

- Notes: 1. SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1
2. $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

Figure 7-54. Ethernet Collision Timing

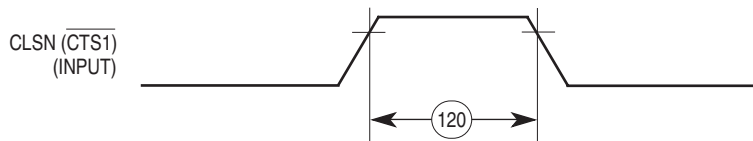


Figure 7-55. Ethernet Receive Timing

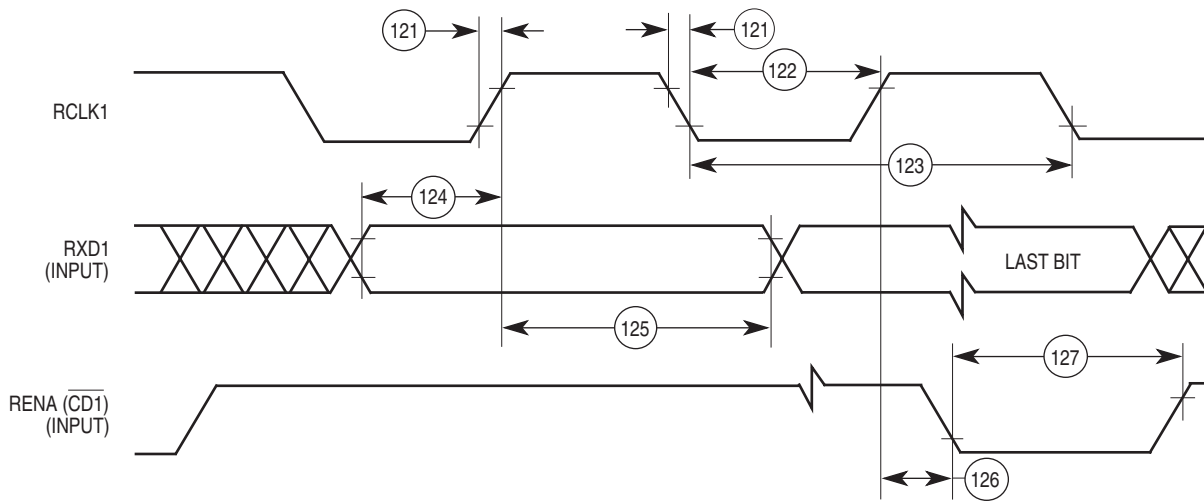
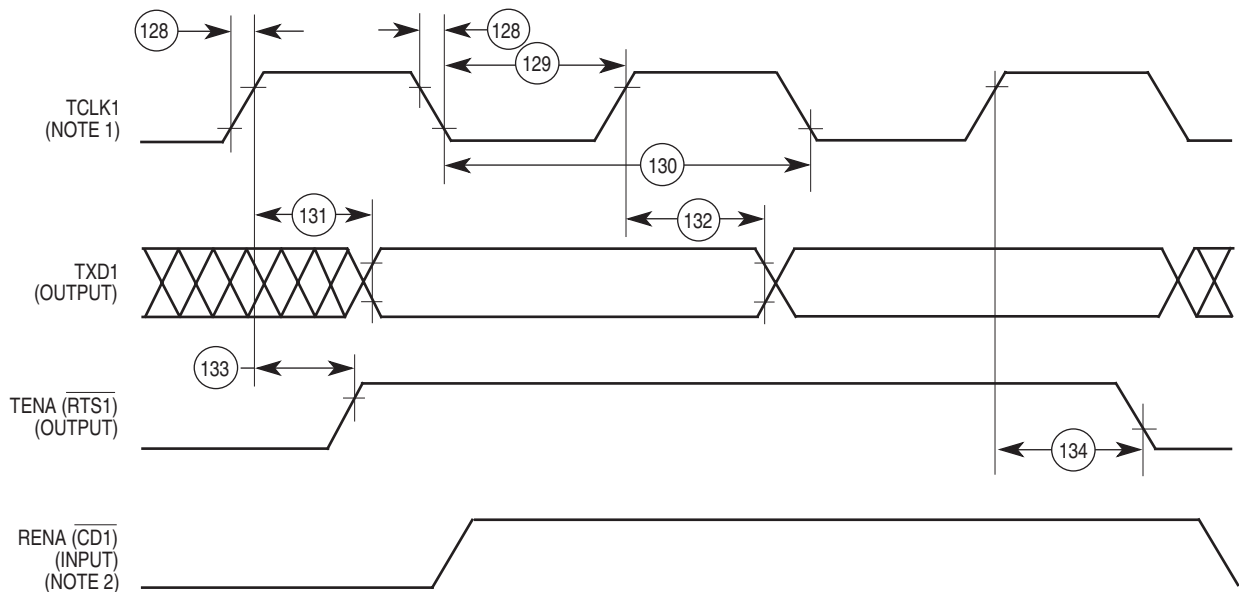
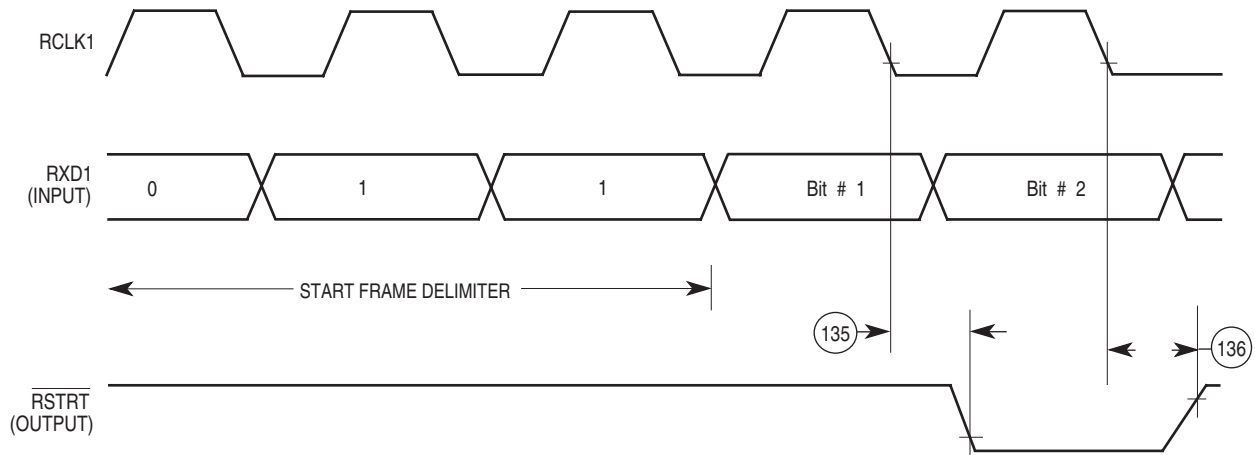


Figure 7-56. Ethernet Transmit Timing



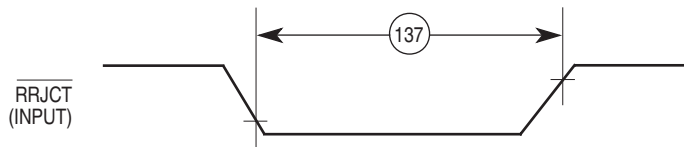
- Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
 2. If RENA is deasserted before TENA, or RENA is not asserted at all during transit, then CSL bit is set in the buffer descriptor at the end of frame transmission.

Figure 7-57. CAM Interface Receive Start Timing



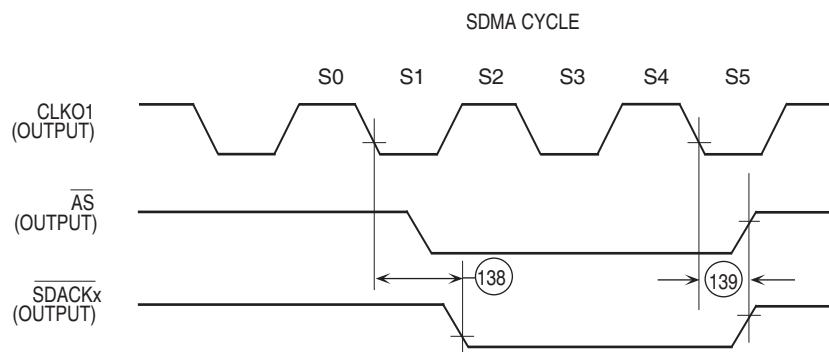
Note: Valid for the ethernet protocol only.

Figure 7-58. CAM Interface Reject Timing



Note: Valid for the ethernet protocol only.

Figure 7-59. SDACK Timing Diagram



Note: \overline{SDACKx} is asserted when the SDMA writes the received Ethernet frame into memory.

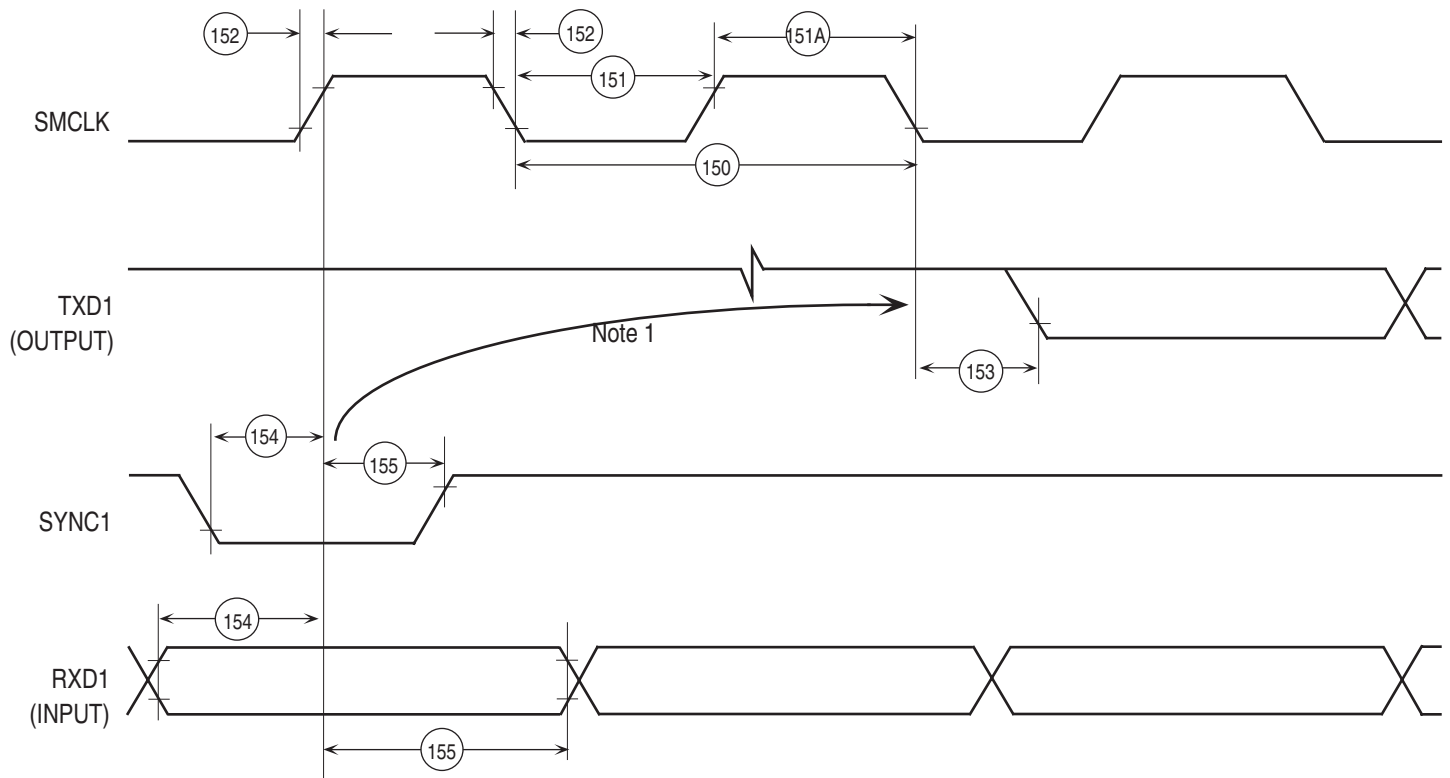
7.21 SMC Transparent Mode Electrical Specifications

Table 7-20. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-60)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------------------|--|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 150 ⁽¹⁾ | SMCLK Clock Period | 100 | – | 100 | – | ns |
| 151 | SMCLK Width Low | 50 | – | 50 | – | ns |
| 151A | SMCLK Width High | 50 | – | 50 | – | ns |
| 152 | SMCLK Rise/Fall Time | – | 15 | – | 15 | ns |
| 153 | SMTXD Active Delay (from SMCLK falling edge) | 10 | 50 | 10 | 50 | ns |
| 154 | SMRXD/SYNC1 Setup Time | 20 | – | 20 | – | ns |
| 155 | SMRXD/SYNC1 Hold Time | 5 | – | 5 | – | ns |

Note: 1. The ratio SyncCLK/SMCLK must be greater or equal to 2/1. SMC Transparent.

Figure 7-60. SMC Transparent



Note: This delay is equal to an integer number of "Character length" clocks

7.22 SPI Master Electrical Specifications

Table 7-21. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See [Figure 7-61](#) and [Figure 7-62](#))

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|--|----------|------|-----------|------|------|
| | | Min | Max | Min | Max | |
| 160 | Master Cycle Time | 4 | 1024 | 4 | 1024 | tcyc |
| 161 | Master Clock (SPICLK) High or Low Time | 2 | 512 | 2 | 512 | tcyc |
| 162 | Master Data Setup Time (Inputs) | 50 | – | 50 | – | ns |
| 163 | Master Data Hold Time (Inputs) | 0 | – | 0 | – | ns |
| 164 | Master Data Valid (after SPICLK Edge) | – | 20 | – | 20 | ns |
| 165 | Master Data Hold Time (Outputs) | 0 | – | 0 | – | ns |
| 166 | Rise Time: Output | | 15 | | 15 | ns |
| 167 | Fall Time: Output | | 15 | | 15 | ns |

Figure 7-61. SPI Master (CP = 0)

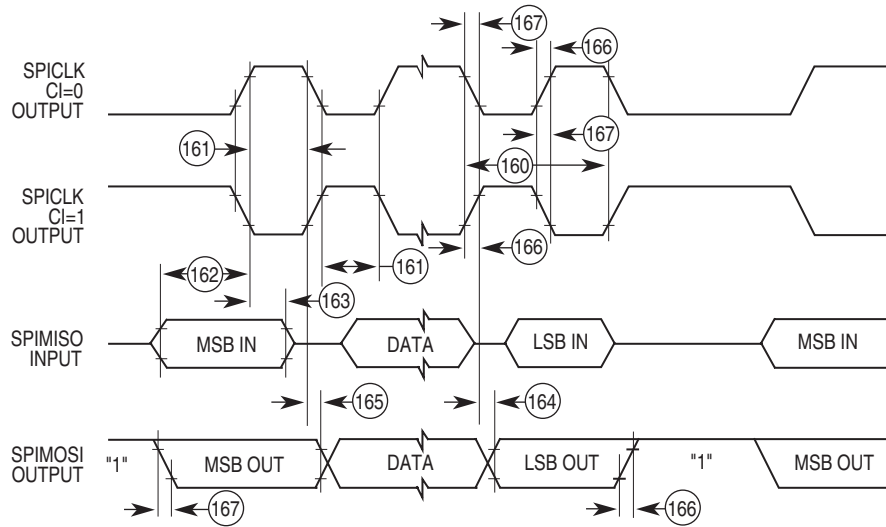
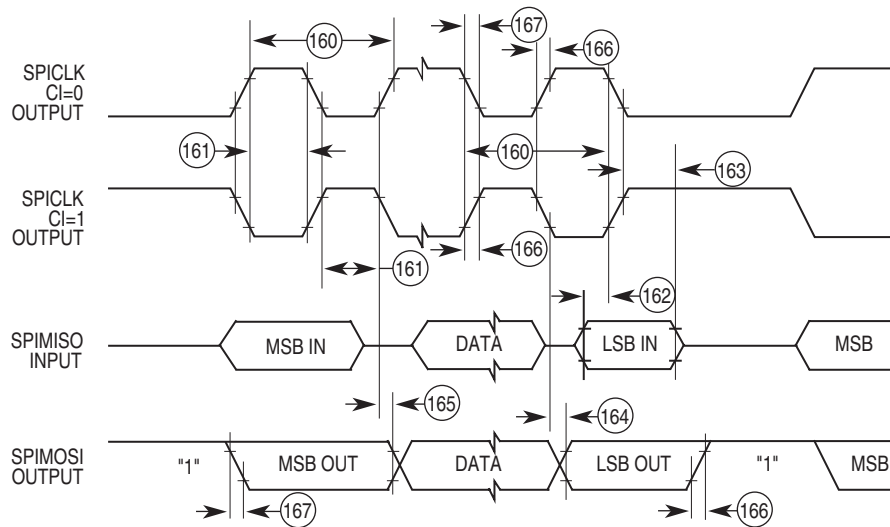


Figure 7-62. SPI Master (CP = 1)



7.23 SPI Slave Electrical Specifications

Table 7-22. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-63 and Figure 7-64)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|---|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| 170 | Slave Cycle Time | 2 | – | 2 | – | tcyc |
| 171 | Slave Enable Lead Time | 15 | | 15 | | ns |
| 172 | Slave Enable Lag Time | 15 | | 15 | | ns |
| 173 | Slave Clock (SPICLK) High or Low Time | 1 | – | 1 | – | tcyc |
| 174 | Slave Sequential Transfer Delay (Does Not Require Deselect) | 1 | | 1 | | tcyc |
| 175 | Slave Data Setup Time (Inputs) | 20 | – | 20 | – | ns |
| 176 | Slave Data Hold Time (Inputs) | 20 | – | 20 | – | ns |
| 177 | Slave Access Time | | 50 | | 50 | ns |
| 178 | Slave SPIMISO Disable Time | | 50 | | 50 | ns |
| 179 | Slave Data Valid (after SPICLK Edge) | – | 50 | – | 50 | ns |
| 180 | Slave Data Hold Time (Outputs) | 0 | – | 0 | – | ns |
| 181 | Rise Time: Input | | 15 | | 15 | ns |
| 182 | Fall Time: Input | | 15 | | 15 | ns |

Figure 7-63. SPI Slave (CP = 0)

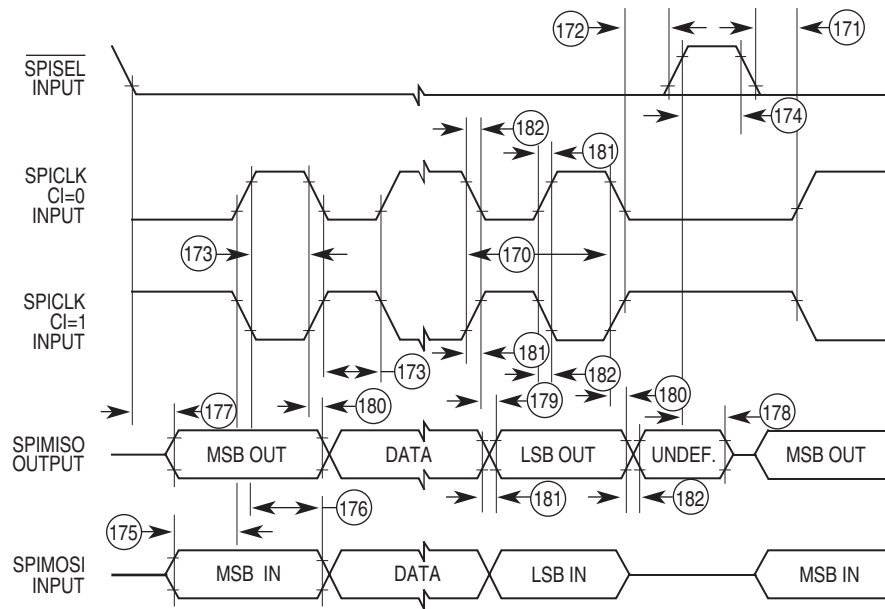
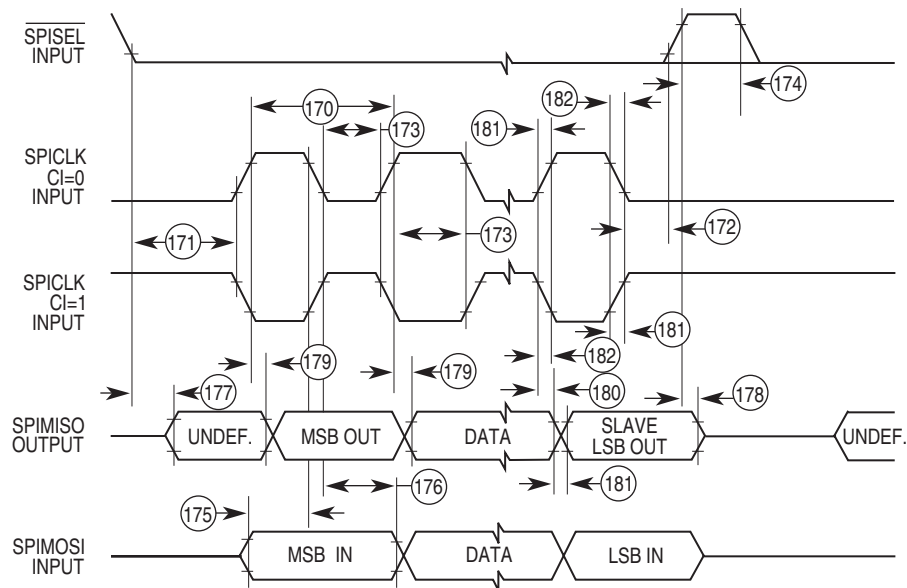


Figure 7-64. SPI Slave (CP = 1)



7.24 JTAG Electrical Specifications

Table 7-23. GND = 0 V_{DC}, T_C = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7-65 and Figure 7-68)

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|--------|--|----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| | TCK Frequency of Operation | 0 | 25 | 0 | 25 | MHz |
| 1 | TCK Cycle Time in Crystal Mode | 40 | – | 40 | – | ns |
| 2 | TCK Clock Pulse Width Measured at 1.5V | 18 | – | 18 | – | ns |
| 3 | TCK rise and Fall Times | 0 | 3 | 0 | 3 | ns |
| 6 | Boundary Scan Input Data Setup Time | 10 | – | 10 | – | ns |
| 7 | Boundary Scan Input Data Hold Time | 18 | – | 18 | – | ns |
| 8 | TCK Low to Output Data Valid | 0 | 30 | 0 | 30 | ns |
| 9 | TCK Low to Output High Impedance | 0 | 40 | 0 | 40 | ns |
| 10 | TMS, TDI Data Setup Time | 10 | – | 10 | – | ns |
| 11 | TMS, TDI Data Hold Time | 10 | – | 10 | – | ns |
| 12 | TCK Low to TDO Data Valid | 0 | 20 | 0 | 20 | ns |
| 13 | TCK Low to TDO High Impedance | 0 | 20 | 0 | 20 | ns |
| 14 | $\overline{\text{TRST}}$ Assert Time | 100 | – | 100 | – | ns |
| 15 | $\overline{\text{TRST}}$ Setup Time to TCK Low | 40 | – | 40 | – | ns |

Figure 7-65. Test Clock Input Timing Diagram

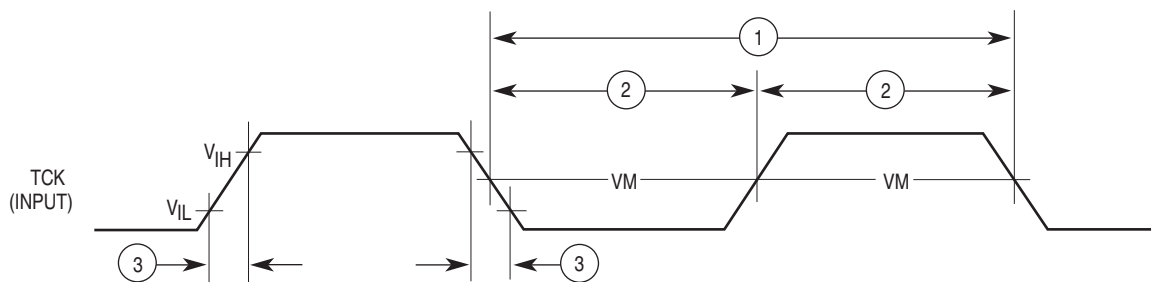


Figure 7-66. $\overline{\text{TRST}}$ Timing Diagram

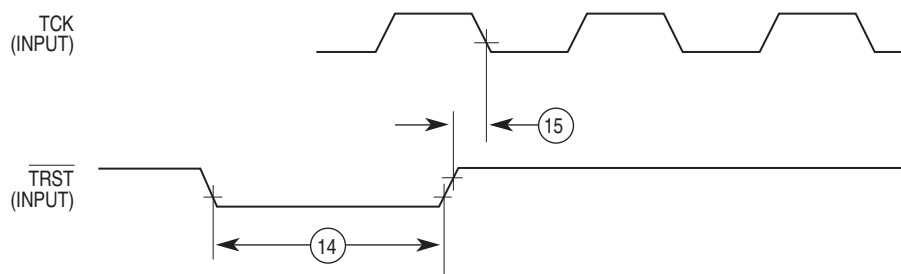


Figure 7-67. Boundary Scan (JTAG) Timing Diagram

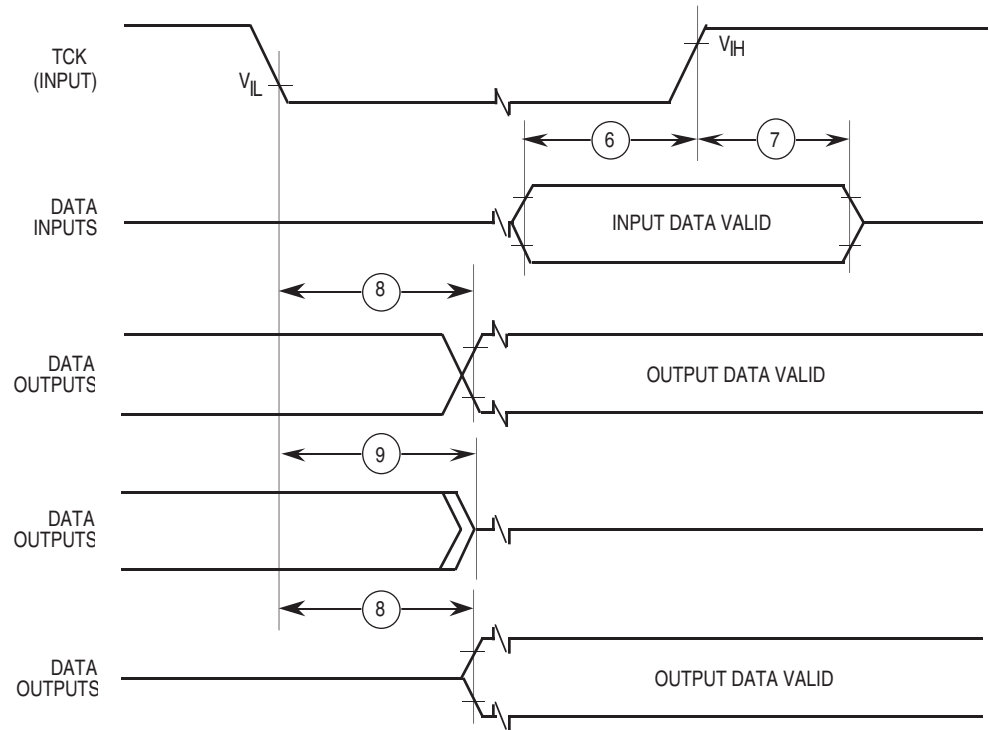
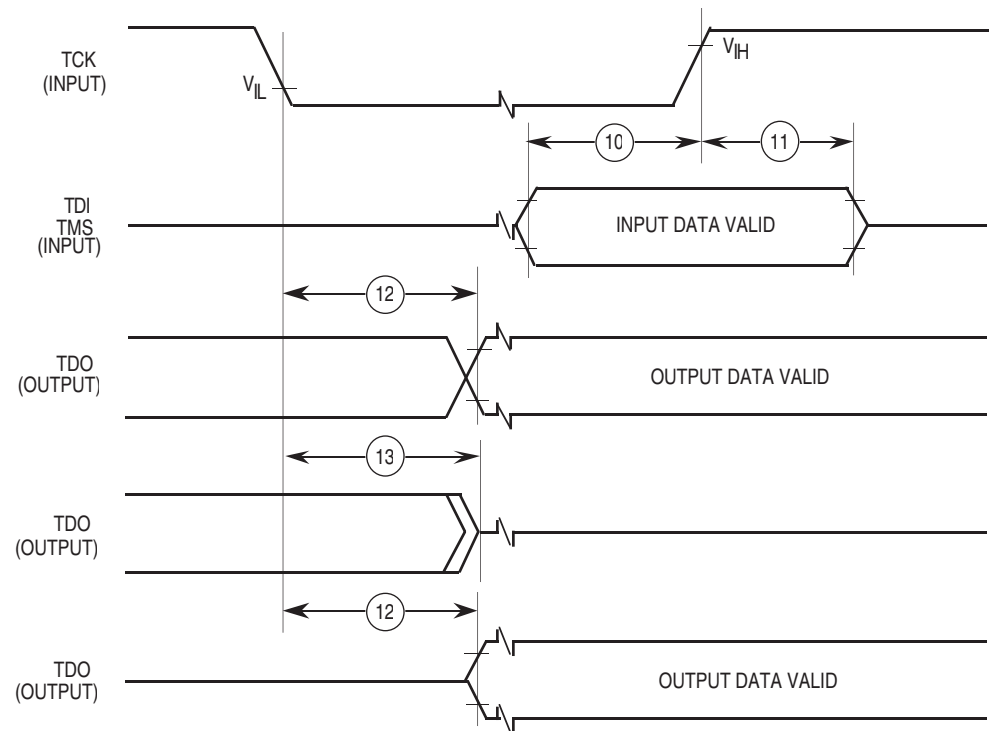


Figure 7-68. Test Access Port Timing Diagram



8. Functional Description

8.1 CPU32+ Core

The CPU32+ core is a CPU32 that has been modified to connect directly to the 32-bit IMB and apply the larger bus width. Although the original CPU32 core had a 32-bit internal data path and 32-bit arithmetic hardware, its interface to the IMB was 16 bits. The CPU32+ core can operate on 32-bit external operands with one bus cycle. This allows the CPU32+ core to fetch a long-word instruction in one bus cycle and to fetch two word-length instructions in one bus cycle, filling the internal instruction queue more quickly. The CPU32+ core can also read and write 32-bit of data in one bus cycle.

Although the CPU32+ instruction timings are improved, its instruction set is identical to that of the CPU32. It will also execute the entire 68000 instruction set. It contains the same background debug mode (BDM) features as the CPU32. No new compilers, assemblers or other software support tools need be implemented for the CPU32+; standard CPU32 tools can be used.

The CPU32+ delivers approximately 4.5 MIPS at 25 MHz, based on the standard (accepted) assumption that a 10-MHz 68000 delivers 1 VAX MIPS. If an application requires more performance, the CPU32+ can be disabled, allowing the rest of the QUICC to operate as an intelligent peripheral to a faster processor. The QUICC provides a special mode called TS68040 companion mode to allow it to conveniently interface to members of the TS68040 family. This two-chip solution provides a 22-MIPS performance at 25 MHz.

The CPU32+ also offers automatic byte alignment features that are not offered on the CPU32. These features allow 16- or 32-bit data to be read or written at an odd address. The CPU32+ automatically performs the number of bus cycles required.

8.2 System Integration Module (SIM60)

The SIM60 integrates general-purpose features that would be useful in almost any 32-bit processor system. The term "SIM60" is derived from the QUICC part number, TS68EN360. The SIM60 is an enhanced version of the SIM40 that exists on the TS68332 device.

First, new features, such as a DRAM controller and breakpoint logic, have been added. Second, the SIM40 was modified to support a 32-bit IMB as well as a 32-bit external system bus. Third, new configurations, such as slave mode and internal accesses by an external master, are supported.

Although the QUICC is always a 32-bit device internally, it may be configured to operate with a 16-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported. Bus sizing allows 8-16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode and 8- and 16-bit peripherals and memory to exist in the 16-bit system bus mode.

8.3 Communications Processor Module (CPM)

The CPM contains features that allow the QUICC to excel in communications and control applications. These features may be divided into three sub-groups:

- Communications Processor (CP)
- Two IDMA Controllers
- Four General-purpose Timers

The CP provides the communication features of the QUICC. Included are a RISC processor, four SCCs, two SMCs, one SPI, 2.5K bytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and fourteen serial DMA channels to support the SCCs, SMCs, and SPI.

The IDMA provides two channels of general-purpose DMA capability. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC controller may access the IDMA registers directly in the buffer chaining modes. The QUICC IDMA is similar to, yet an enhancement of, the one IDMA channel found on the TS68302.

The four general-purpose timers on the QUICC are functionally similar to the two general-purpose timers found on the TS68302. However, they offer some minor enhancements, such as the internal cascading of two timers to form a 32-bit timer. The QUICC also contains a periodic interval timer in the SIM60, bringing the total to five on-chip timers.

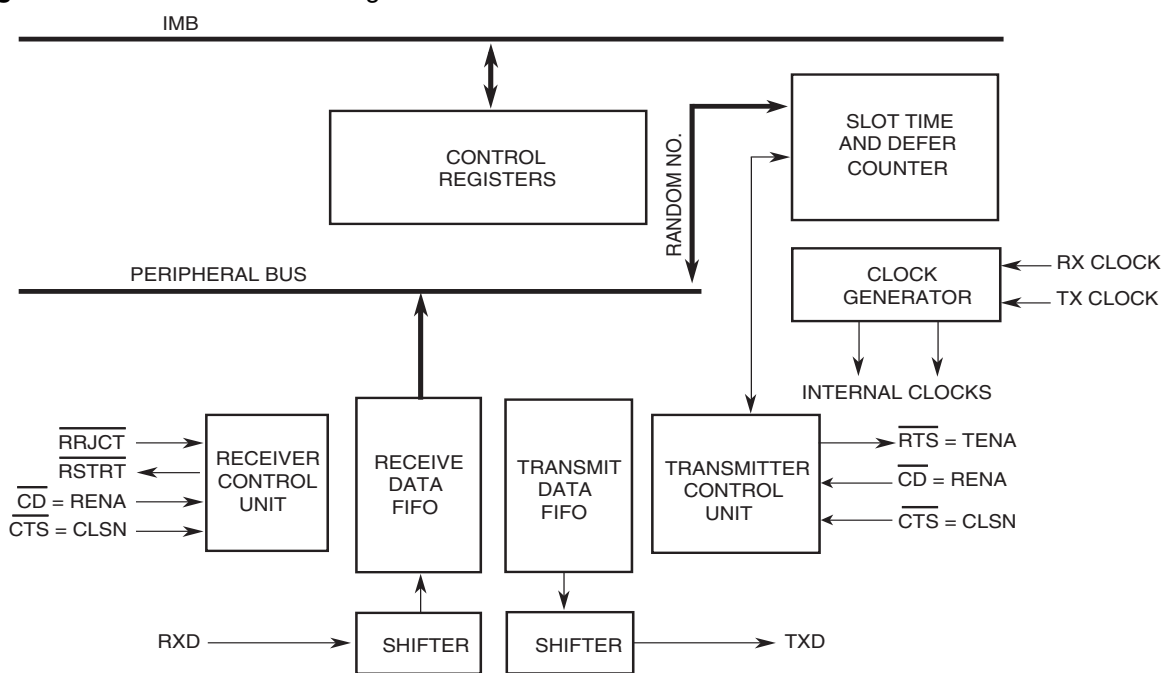
8.4 Ethernet on QUICC

The Ethernet protocol is available only on the Ethernet version of the QUICC called the TS68EN360. The non-Ethernet version of the QUICC is the MC68360. The term "QUICC" is the overall device name that denotes all versions of the device.

The TS68EN360 is a superset of the MC68360, having the additional option allowing Ethernet operation on any of the four SCCs. Due to performance reasons not all SCCs can be configured as Ethernet controllers at the same time. The TS68EN360 is not restricted only to Ethernet operation. HDLC, UART, and other protocols may be used to allow dynamic switching between protocols. See Appendix A Serial Performance for available SCC performance.

When the MODE bits of the SCC GSMR select the Ethernet protocol, then that SCC performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions (see Figure 8-1)

Figure 8-1. Ethernet Block Diagram



8.5 Upgrading Designs from the TS68302

Since the QUICC is a next-generation TS68302, many designers currently using the TS68302 may wish to use the QUICC in a follow-on design. The following paragraphs briefly discuss this endeavor in terms of architectural approach, hardware issues, and software issues.

8.5.1 Architectural Approach

The QUICC is the logical extension of the TS68302, but the overall architecture and philosophy of the TS68302 design remains intact in the QUICC. The QUICC keeps the best features of the TS68302, while making the changes required to provide for the increased flexibility, integration, and performance requested by customers. Because the CPM is probably the most difficult module to learn, anyone who has used the TS68302 can easily become familiar with the QUICC since the CPM architectural approach remains intact.

The most significant architectural change made on the QUICC was the translation of the design into the standard 68300 family IMB architecture, resulting in a faster CPU and different system integration features.

Although the features of the SIM60 do not exactly correspond to those of the TS68302 SIM, they are very similar.

Because of the similarity of the QUICC SIM60 and CPU to other members of the 68300 family, such as the TS68332, previous users of these devices will be comfortable with these same features on the QUICC.

8.5.2 Hardware Compatibility Issues

The following list summarizes the hardware differences between the TS68302 and the QUICC:

- Pinout – The pinout is not the same. The QUICC has 240 pins; the TS68302 has 132 pins
- Package – Both devices offer PGA and PQFP packages. However, the QUICC QFP package has a 20-mil pitch; whereas, the TS68302 QFP package has a 25-mil pitch
- System Bus – The system bus signals now look like those of the TS68020 as opposed to those of the 68000. It is still possible to interface 68000 peripherals to the QUICC, utilizing the same techniques used to interface them to a TS68020
- System Bus in Slave Mode – A number of QUICC pins take on new functionality in slave mode to support an external TS68EC040. On the TS68302, the pin names generally remained the same in slave mode
- Peripheral Timing – The external timings of the peripherals (SCCs, timers, etc.) are very similar (if not identical) to corresponding peripherals on the TS68302
- Pin Assignments – The assignment of peripheral functions to I/O pins is different in several ways. First, the QUICC contains more general-purpose parallel I/O pins than the TS68302. However, the QUICC offers many more functions than even a 240-pin package would normally allow, resulting in more multifunctional pins than the TS68302

8.5.3 Software Compatibility Issues

The following list summarizes the major software differences between the TS68302 and the QUICC:

- Since the CPU32+ is a superset of the 68000 instruction set, all previously written code will run. However, if such code is accessing the TS68302 peripherals, it will require some modification
- The QUICC contains an 8-Kbyte block of memory as opposed to a 4-Kbyte block on the TS68302. The register addresses within that memory map are different
- The code used to initialize the system integration features of the TS68302 has to be modified to write the corresponding features on the QUICC SIM60
- As much as possible, QUICC CPM features were made identical to those of the TS68302 CP. The most important benefit is that the code flow (if not the code itself) will port easily from the TS68302 to the QUICC. The nuances learned from the TS68302 will still be useful in the QUICC
- Although the registers used to initialize the QUICC CPM are new (for example, the SCM on the TS68302 is replaced with the GSMR and PSMR on the QUICC), most registers retain their original purpose such as the SCC event, SCC mask, SCC status, and command registers. The parameter RAM of the SCCs is very similar, and most parameter RAM register names and usage are retained. More importantly, the basic structure of a buffer descriptor (BD) on the QUICC is identical to that of the TS68302, except for a few new bit functions that were added. (In a few cases, a bit in a BD status word had to be shifted)
- When porting code from the TS68302 CP to the QUICC CPM, the software writer may find that the QUICC has new options to simplify what used to be a more code-intensive process. For specific examples, see the INIT TX AND RX PARAMETERS, GRACEFUL STOP TRANSMIT, and CLOSE BD commands

9. Preparation for Delivery

9.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535 or e2v standards.

9.2 Certificate of Compliance

e2v offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or e2v standard and guarantying the parameters not tested at temperature extremes for the entire temperature range.

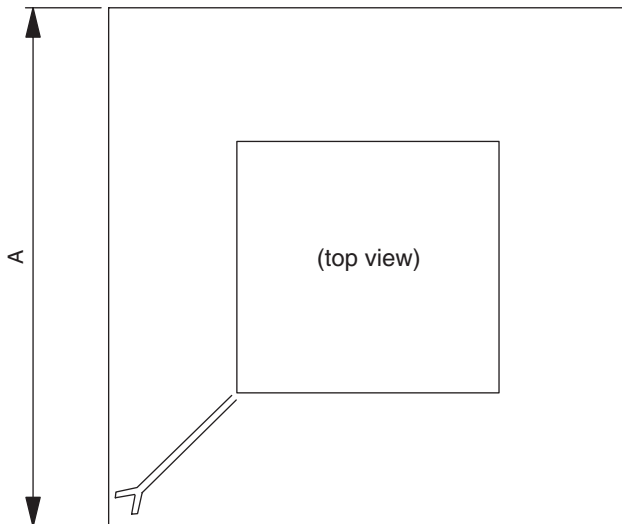
10. Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

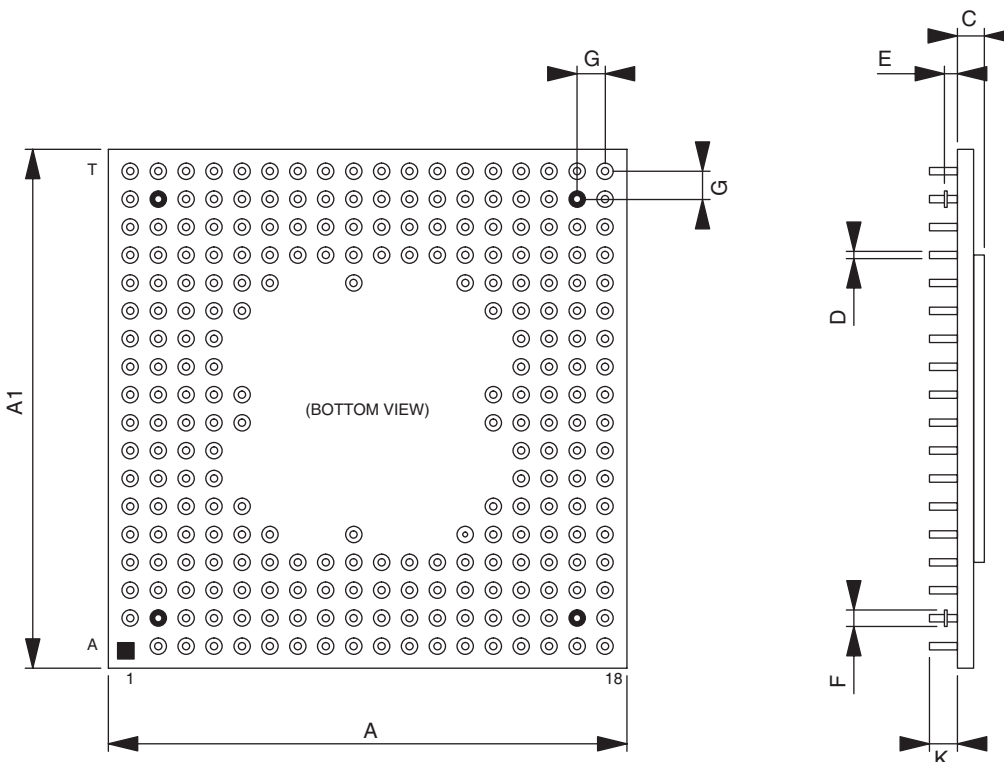
- a) Devices should be handled on benches with conductive and grounded surfaces
- b) Ground test equipment, tools and operator
- c) Do not handle devices by the leads
- d) Store devices in conductive foam or carriers
- e) Avoid use of plastic, rubber, or silk in MOS areas
- f) Maintain relative humidity above 50% if practical

11. Package Mechanical Data

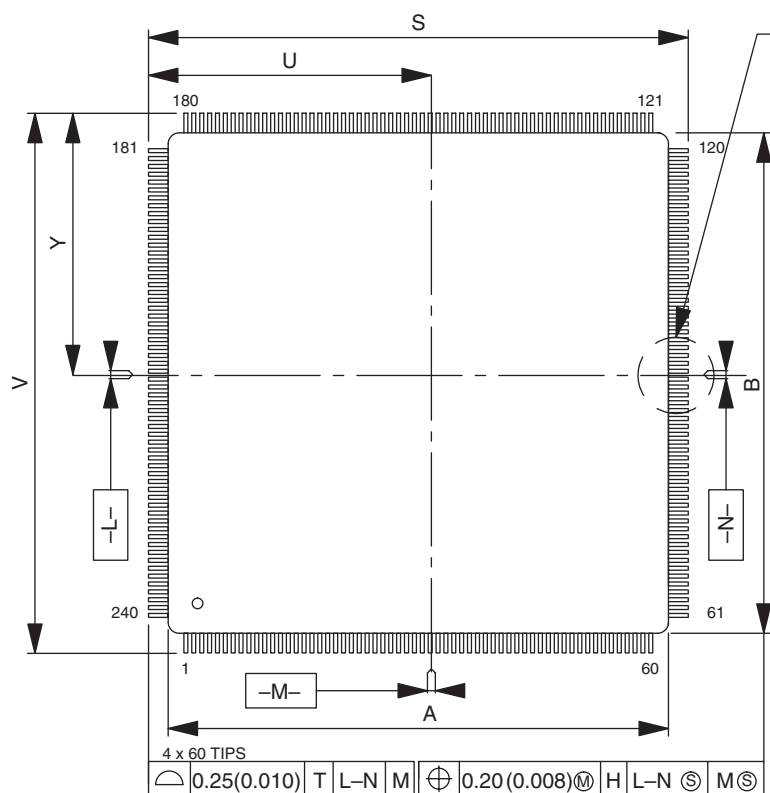
11.1 241-pin – PGA



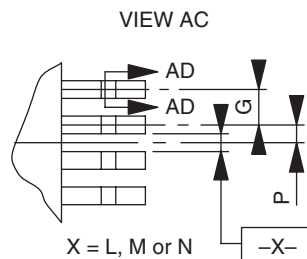
| Dim | Inches | | Millimeters | |
|-----|-------------|-------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.840 | 1.880 | 46.74 | 47.75 |
| C | 0.110 | 0.140 | 2.79 | 3.56 |
| D | 0.016 | 0.020 | 0.41 | 0.51 |
| E | 0.045 | 0.055 | 1.143 | 1.4 |
| F | 0.045 | 0.055 | 1.143 | 1.4 |
| G | 0.100 BASIC | | 2.54 BASIC | |
| K | 0.150 | 0.170 | 3.81 | 4.32 |



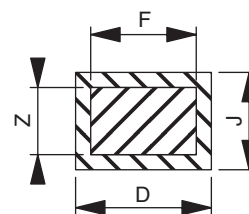
11.2 240-pin – CERQUAD



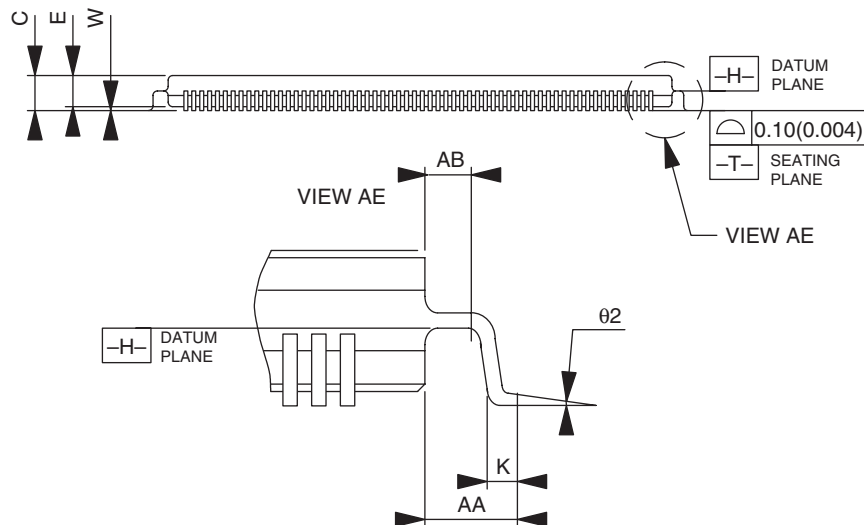
VIEW AC
4 PLACES



SECTION AD
240 PLACES



| | | | | | | | |
|---|-------------|---|---|-----|---|---|---|
| ⊕ | 0.08(0.003) | Ⓜ | T | L-N | ⊗ | M | ⊗ |
|---|-------------|---|---|-----|---|---|---|



- Notes:
1. Dimensioning and tolerancing per ASME Y 14.5, 1994.
 2. Controlling dimension: millimeter.
 3. Datum plane -H- is located at bottom of lead and is coincident with the lead where the lead exits the ceramic body at the bottom of the parting line.
 4. Datums -L-, -M- and -N- to be determined at datum plane -H-.
 5. Dimensions S and V to be determined at seating plane -T-.
 6. Dimensions A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|--------|
| | MIN | MAX | MIN | MAX |
| A | 30.86 | 31.75 | 1.215 | 1.250 |
| B | 30.86 | 31.75 | 1.215 | 1.250 |
| C | 3.67 | 4.15 | 0.144 | 0.163 |
| D | 0.20 | 0.30 | 0.0079 | 0.012 |
| E | 3.10 | 3.90 | 0.122 | 0.154 |
| F | 0.19 | 0.25 | 0.0075 | 0.010 |
| G | 0.50 BSC | | 0.019 BSC | |
| J | 0.13 | 0.175 | 0.005 | 0.007 |
| K | 0.45 | 0.55 | 0.018 | 0.021 |
| P | 0.25 BSC | | 0.010 BSC | |
| R | 0.15 BSC | | 0.006 BSC | |
| S | 34.41 | 34.75 | 1.355 | 1.37 |
| U | 17.30 BSC | | 0.681 BSC | |
| V | 34.41 | 34.75 | 1.355 | 1.37 |
| W | 0.25 | 0.75 | 0.0035 | 0.0232 |
| Y | 17.30 BSC | | 0.681 BSC | |
| Z | 0.12 | 0.13 | 0.005 | 0.005 |
| AA | 1.80 REF | | 0.071 REF | |
| AB | 0.95 REF | | 0.037 REF | |
| θ2 | 1° | 7° | 1° | 7° |

12. Ordering Information

| Product Code ⁽¹⁾ | Part Identifier | Temperature Range ⁽¹⁾ | Package ⁽¹⁾ | Hirel lead finish | Screening ⁽¹⁾ | Operating Frequency | Revision Level ⁽¹⁾ |
|-----------------------------|-----------------|--|--|---|---------------------------------------|--------------------------|-------------------------------|
| TS(X) ⁽²⁾ | 68EN360 | M : -55°C, +125°C V : -40°C, +110°C | R = Pin grid array 241 (gold) A = CERQUAD 240 (tin) | _ = Gold (for PGA) _ = Hot solder dip (for CERQUAD) 1 = Hot solder dip (for PGA - On request) | Blank: Standard B/Q: MIL-PRF-38535 | 25: 25 MHz 33: 33 MHz | L |

- Notes:
1. For availability of the different versions, contact your local e2v sales office.
 2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a TSX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

Table 12-1. Standard Microcircuit Drawing (SMD) Cross-Reference

| e2v Orderable Part-Number | Standard Microcircuit Drawing (SMD) Number | Standard | Package | Lead-Finish | Temperature | Frequency (MHz) |
|---------------------------|--|---------------|-------------|-------------|-------------|-----------------|
| TS68EN360MRB/Q25L | 5962-9760701MXC | MIL-PRF-38535 | PGA 241 | Gold | -55/+125 | 25 |
| TS68EN360MRB/Q33L | 5962-9760702MXC | MIL-PRF-38535 | PGA 241 | Gold | -55/+125 | 33 |
| TS68EN360MR1B/Q25L | 5962-9760701MXA | MIL-PRF-38535 | PGA 241 | Tinned | -55/+125 | 25 |
| TS68EN360MR1B/Q33L | 5962-9760702MXA | MIL-PRF-38535 | PGA 241 | Tinned | -55/+125 | 33 |
| TS68EN360MAB/Q25L | 5962-9760701MYA | MIL-PRF-38535 | CERQUAD 240 | Tinned | -55/+125 | 25 |
| TS68EN360MAB/Q33L | 5962-9760702MYA | MIL-PRF-38535 | CERQUAD 240 | Tinned | -55/+125 | 33 |

13. Document Revision History

Table 13-1 provides a revision history for this hardware specification.

Table 13-1. Revision History

| Revision Number | Date | Substantive Change(s) |
|-----------------|---------|--|
| 0886C | 04/2008 | Name change from Atmel to e2v Ordering information update |
| 2113B | 04/2005 | Cerquad Package Change. See page 77 |
| 2113A | 03/2002 | Initial Revision |

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