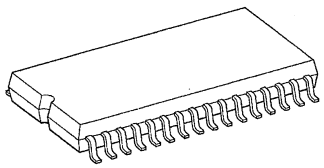
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TMPN3120FE5M

Neuron ® Chip
For Distributed Intelligent Control Networks (LONWORKS®)

The Neuron Chip TMPN3120FE5M provides double the performance of previous Neuron Chips. It supports a response time of 3 to 4 ms across a LONWORKS Network and has double the input / output (I / O) performance of the previous Neuron Chip in terms of both response time and data transmission speed.
The TMPN3120FE5M features an extra single-chip memory in the form of 3 Kbytes EEPROM, 4 Kbytes SRAM and 16 Kbytes ROM. It is therefore suitable for applications which require more complex operations and high speed communication control.
Neuron Chips have all the built-in communications and control functions required to implement LONWORKS nodes.
These nodes may then be easily integrated into highly-reliable distributed intelligent control networks.
The typical functions for this chip are explained below.



SOP32-P-525-1.27

Weight: 1.1g (Typ.)

FEATURES

- New features
  (In comparison with TMPN3120E1M and TMPN3120FE5M)
  - High-impedance communication port
  - 3 Kbytes EEPROM
  - 4 Kbytes static RAM

- Main features of the 20 MHz Neuron Chip
  (In comparison with the TMPN3120E1M and TMPN3120FE5M)
  - Increased communication speed
    The maximum transmission speed has been increased two-fold.
    1.25 Mbps → 2.5 Mbps (*1)
    *1: This value applies to Single-Ended Mode only.
  - Shortened response time
    The amount of time required from I / O input to I / O output has been greatly reduced.
    Maximum speed 7 ms → 3 ~ 4 ms
  - Increased IO object speed
    The execution time for all objects has been halved.
    Example) Serial I / O 9600 bps
    Parallel I / O 1.2 μs / byte
  - Development tool support
    The current LonBuilder® and NodeBuilder® development tools can be used to develop applications for the TMPN3120FE5M (L.B ver 3.01 is needed.). Updated symbol table files for the Neuron Chip firmware are available from Echelon. If your application requires a 20 MHz input clock, a utility program available from Echelon may be used to convert the programmer files
  - *** The conversion utilities can be obtained from the Echelon Web Site at http://www.echelon.com.**
- I / O Functions
  - Eleven programmable I / O pins.
  - Two programmable 16-bit timers and counters built in.
  - 34 different types of I / O functions to handle a wide range of input and output.
  - ROM firmware image containing pre-programmed I / O drivers, greatly simplifying application programs.
- Network functions
  - Two CPUs for communication protocol processing built in.
    The communications and application CPUs execute in parallel.
  - Equipped with a built-in LonTalk protocol which supports all seven levels of the OSI reference model with ISO.
  - The ROM firmware image contains a complete network operating system, greatly simplifying application programs.
  - Built-in twisted-pair wire transceiver with improved common mode and drive current capabilities.
  - Equipped with communications modes and communication speeds which support various types of external transceivers.
    Supports twisted-pair wire, power line, radio (RF), infrared, coaxial cables, and fiber optics.
  - Communication port transceiver modes and logical addresses stored within the EEPROM.
    Can be amended via the network.

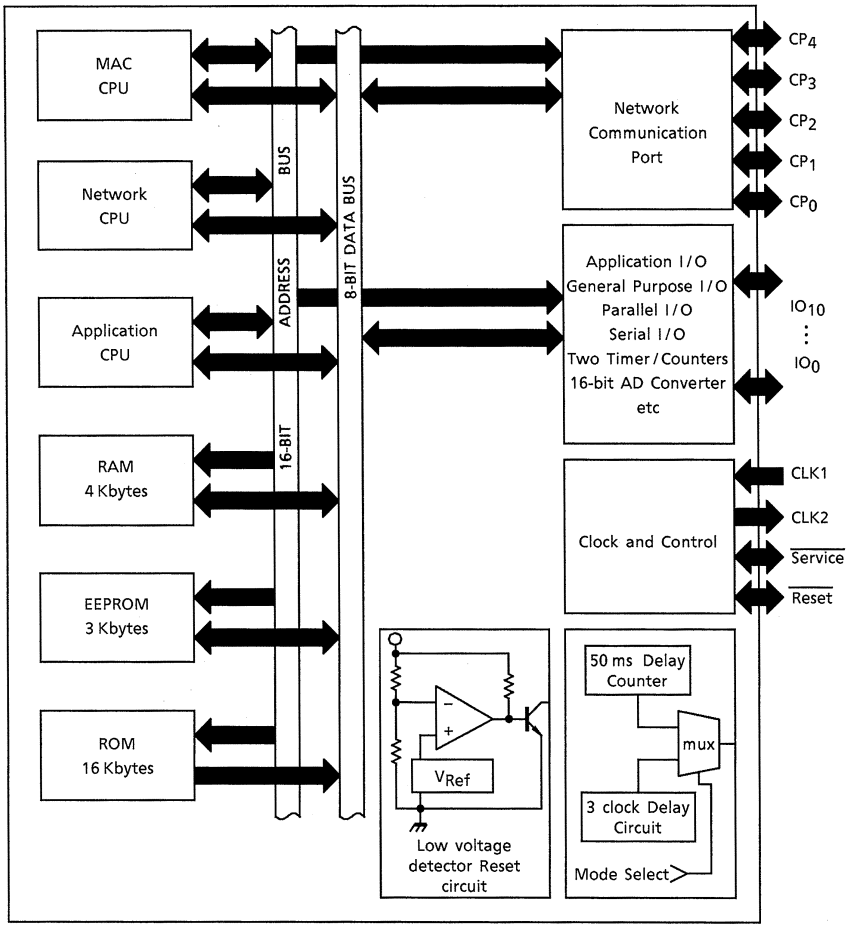
- Other functions
  - Application programs are also stored within the EEPROM.
    Can be updated by downloading over the network.
  - Built-in watch-dog timer.
  - Each chip has a unique ID number.
    Effective during the logical installation of networks.
  - Low electrical consumption mode supported with a sleep mode.
  - Built in Selectable Reset time
    Prolongs the power-ON reset time for at least 50 ms and keeps the operation stable during that time. The reset time can be selected 50ms delay mode or 3 clock delay mode by program after the device is in power-ON.
  - High-impedance communication port (CP0 to CP3)
    The Communication port pins (CP0 to CP3) attain high impedance. This eliminates the need for an external relay.
  - Built-in low-voltage detection circuit.
    Prevents incorrect operations and writing errors in the EEPROM during drops in power voltage.
    An external LVD must be used to assert reset at power supply voltage below 4.5 V if Neuron Chip is operated at 20 MHz.
  - Programmable LVD (Low Voltage Detection) circuit.
    LVDin pin is prepared in order to make it reset on arbitrary voltage.
  - Firmware version 10.
- Timing for the main I / O objects during 20 MHz Neuron Chip operations

I / O MODEL	10 MHz TIMING	20 MHz TIMING
Parallel	2.4μs / byte	1.2μs / byte
Bitshift	1, 10 or 15 kbps	2, 20 or 30 kbps
Magcard	Up to 8334 bps	Up to 16668 bps
Magtrack1	Up to 7246 bps	Up to 14492 bps
Neurowire Master	1, 10 or 20 kbps	2, 20 or 40 kbps
Neurowire Slave	Up to 18 kbps	Up to 36 kbps
Serial	600, 1200, 2400 or 4800 bps	1200, 2400, 4800 or 9600 bps
Touch	Supported	Not supported
Frequency Output	Resolution0.4 to 51.2μs Max Range 26.21 to 3355 ms	Resolution0.2 to 25.6μs Max Range 13.1 to 1678 ms
Other Timer / Counter	Resolution0.2 to 25.6μs Max Range 13.1 to 1678 ms	Resolution0.1 to 12.8μs Max Range 6.55 to 839 ms

The specifications for the main timers during 20 MHz operations are as follows :

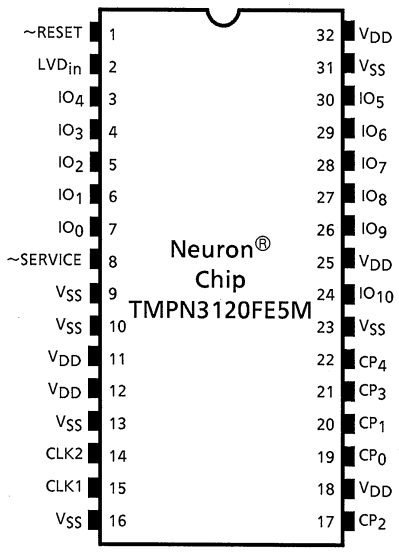
Watchdog Timer	420 ms
Millisecond Timers	1 to 32000 ms
Second Timers	1 to 65000 s
Delay ( ) Function	1 to 32767 counts
Get_Tick_Count ( ) Function	409.6μs per count

BLOCK DIAGRAM



ITEM	TMPN3120FE5M
CPU	8-bit CPU × 3
RAM	4,096 bytes
ROM	16,384 bytes
EEPROM	3,072 bytes
16-bit Timer / Counter	2 channels
External Memory Interface	Not available
Package	32-pin SOP

PIN CONNECTION



PIN FUNCTION

PIN No.	PIN NAME	I / O	PIN FUNCTION
15	CLK1	Input	Oscillator connection, or external clock input.
14	CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1.
1	~RESET	I / O (built-in pull-up)	Reset pin. (Active low)
8	~SERVICE	I / O (built-in configurable pull-up)	Service pin. Indicator output during operation.
7~4	IO_0~IO_3	I / O	Large current sink capacity (20 mA). General I / O port.
3, 30~28	IO_4~IO_7	I / O (built-in configurable pull-up)	General I / O port. One of IO_4 to IO_7 can be specified as No.1 timer / counter input. Output signal can be output to IO_0. IO_4 can be used as the No.2 timer / counter input with IO_1 as output.
27, 26, 24	IO_8~IO_{10}	I / O	General I / O port. Can be used for serial communication with other device.
11, 12, 18, 25, 32	V_{DD}	Input	Power input (5.0 V Typ.)
9, 10, 13, 16, 23, 31	V_{SS}	Input	Power input (0 V GND)
2	LVD_{in}	Input	Input pin for programmable LVD (Normally connect to V_{DD})
19, 20, 17, 21, 22	CP_0~CP_4	I / O	Bidirectional port for communications. Supports several communications protocols by specifying mode.

* : ● The ~SERVICE and IO_4 to IO_7 terminals are programmable pull-ups.
● All V_{DD} terminals must be externally connected.
● All V_{SS} terminals must be externally connected.

MAXIMUM RATINGS (V_{SS} = 0V, V_{SS} typ.)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	$V_{IN\ (1)}$	−0.3 to V_{DD} + 0.3 V	V
Input Voltage CP_0-CP_3	$V_{IN\ (2)}$	−0.5 to V_{DD} + 1.3 V $V_{IN\ (2)} \leq$ 7.3 (Note 1)	V
Drain Current	I_{DD}	200	mA
Source Current	I_{SS}	300	mA
Power Dissipation	P_D	800	mW
Storage Temperature	T_{stg}	−65~150	°C

Note1 : V_{IN}(2) don't exceed the 7.3v.

OPERATING CONDITIONS

ITEM	SYMBOL	MIN	TYP.	MAX	UNIT
Operating Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage (TTL)	V_{IH}	2.0	—	V_{DD}	V
	V_{IL}	V_{SS}	—	0.8	V
Input Voltage (CMOS)	V_{IH}	V_{DD} − 0.8 V	—	V_{DD}	V
	V_{IL}	V_{SS}	—	0.8	V
Input Voltage CP_0-CP_3 (differential mode)	V_{IH}	—	—	V_{DD} + 1.0 V	V
	V_{IL}	−0.1	—	—	
Operating Frequency	f_{osc}	0.625	—	20	MHz
Operating Temperature	T_{opr}	−40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC characteristic (V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = −40~85°C)
(Above operating conditions apply unless otherwise states.)

ITEM	SYMBOL	PINS	TEST CONDITION	MIN	MAX	UNIT
LOW Level Input Voltage (1)	V_{IL} (1)	IO_0~IO_{10} CP_0, CP_3, CP_4, ~SERVICE	—	0	0.8	V
LOW Level Input Voltage (2)	V_{IL} (2)	~RESET	—	0	V_{DD} × 0.3	V
HIGH Level Input Voltage (1)	V_{IH} (1)	IO_0~IO_{10} CP_0, CP_3, CP_4, ~SERVICE	—	2.0	V_{DD}	V
HIGH Level Input Voltage (2)	V_{IH} (2)	~RESET	—	V_{DD} − 0.7 V	V_{DD}	V
LOW Output Voltage (1)	V_{OL} (1)	IO_0~IO_3 ~SERVICE, ~RESET	I_{OL} = 20mA	0	0.8	V
			I_{OL} = 10mA	0	0.4	
LOW Output Voltage (2)	V_{OL} (2)	CP_2, CP_3	I_{OL} = 40mA	0	1.0	V
LOW Output Voltage (3)	V_{OL} (3)	Others (Note 1)	I_{OL} = 1.4mA	0	0.4	V
HIGH Output Voltage (1)	V_{OH} (1)	IO_0~IO_3	I_{OH} = −1.4mA	V_{DD} − 0.4 V	V_{DD}	V
HIGH Output Voltage (2)	V_{OH} (2)	~SERVICE	I_{OH} = −1.4mA	V_{DD} − 0.4 V	V_{DD}	V
HIGH Output Voltage (3)	V_{OH} (3)	CP_2, CP_3	I_{OH} = −40mA	V_{DD} − 1.0 V	V_{DD}	V
HIGH Output Voltage (4)	V_{OH} (4)	Others (Note 1)	I_{OH} = −1.4mA	V_{DD} − 0.4 V	V_{DD}	V
Input Current	I_{IN}	(Note 2)	V_{IN} = V_{SS}~V_{DD}	−10	10	μA
Pull-up Current	I_{PU} (Note 3)	IO_4~IO_7 ~SERVICE, ~RESET	V_{IN} = 0V	−30	−300	μA
Low-voltage Detection Level	V_{LVD}	V_{DD}	—	3.8	4.5	V

Note1 : Output voltage characteristics exclude the CLK2 pin.
Note2 : Excludes pull-up input pins.
Note3 : The IO_4 to IO_7 and ~SERVICE pins have programmable pull-ups. ~RESET has a fixed pull-up.

ITEM		SYMBOL	TYP.	MAX	UNIT
Operating Mode Current Consumption	20 MHz Clock	$I_{DD\ (OP)}$	34	55	mA
	10 MHz Clock		16	30	
	5 MHz Clock		8.5	15	
	2.5 MHz Clock		4.5	8	
	1.25 MHz Clock		2.3	5	
	0.625 MHz Clock		1.3	3	
Sleep Mode Current Consumption		$I_{DD\ (SLP)}$	16	100	μA

Note : Test conditions for current dissipation

V_{DD} = 5V, all output = with no load, all input = 0.2 V or below or V_{DD} − 0.2 V, programmable pull-up = off, crystal oscillator clock input, differential receiver disabled.

The current value (typ.) is a typical value when Ta = 25°C.

The current value (max) applies to the rated temperature range at V_{DD} = 5.5 V.

200μA (typ.) to 600μA (max) is added to the current of the differential receiver when the receiver is enabled.

The differential receiver is enabled by either of the following conditions :

- When the Neuron Chip is in Run mode and the communication ports are in Differential mode.
- When the Neuron Chip is in Sleep mode, the communication ports are in Differential mode, and the Comm Port Wakeup is not masked.

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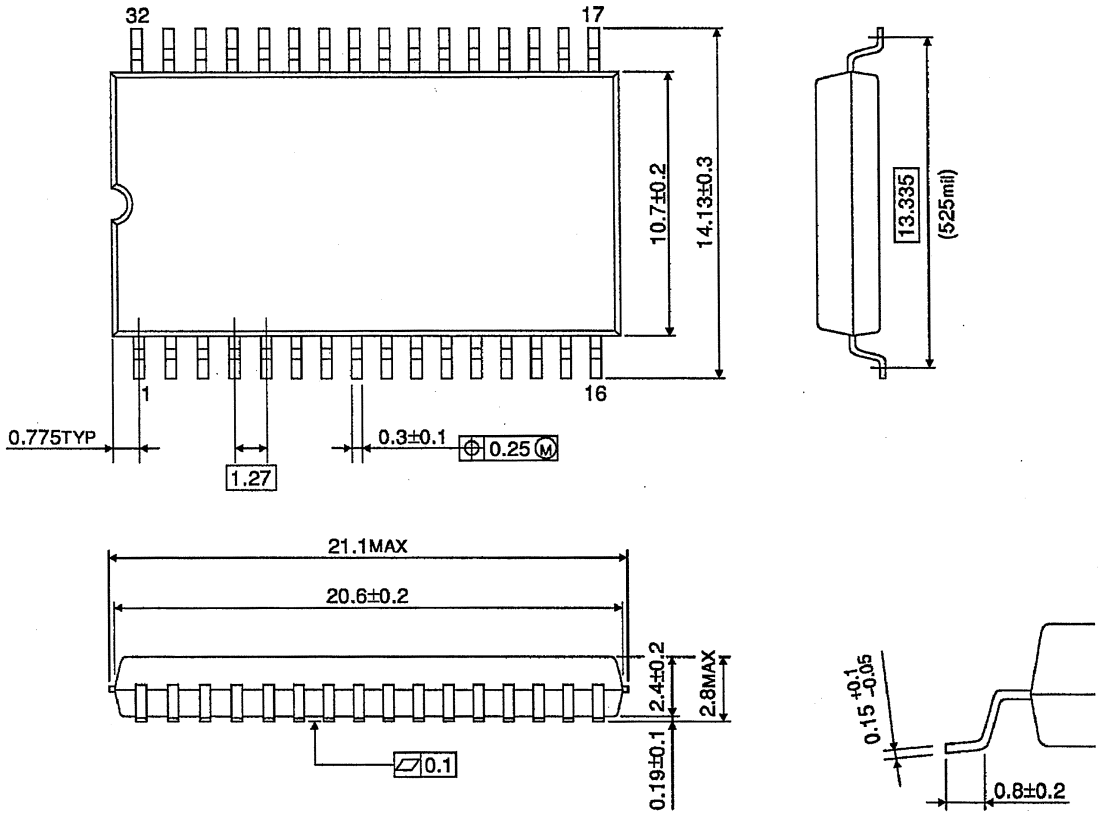
PACKAGE DIMENSIONS

SOP32-P-525-1.27 Unit : mm



Weight : 1.1 g (Typ.)