PHAST®-12N Device

STM-4/OC-12 SDH/SONET Overhead Terminator with Telecom Bus Interface

TXC-06312B

PRELIMINARY **DATA SHEET**

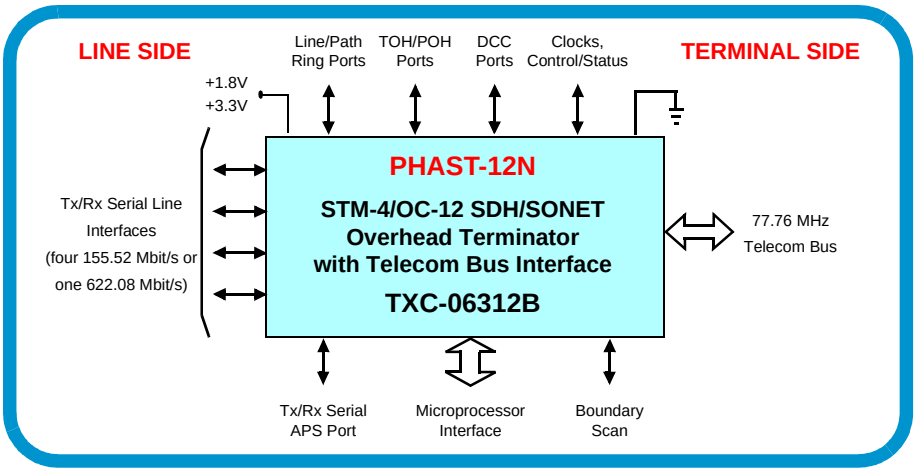
TXC-06312B-MB, Ed. 2
June 2005

FEATURES

- Bit-serial LVPECL SDH/SONET line interface with integrated clock recovery and clock synthesis
  - single 622.08 Mbit/s STM-4/OC-12 signal or
  - four 155.52 Mbit/s STM-1/OC-3 signals
- Bit-serial LVDS 622.08 Mbit/s APS port
- Supports 1+1, 1:1 and 1:n APS for STM-1/OC-3 and STM-4/OC-12 signals using a serial port interface
- Complete RS/section and MS/line overhead processing
- Complete high order path overhead processing at VC-3/VC-4/VC-4-Xc/ STS-1/STS-3c/STC-6c/STS-9c/STS-12c SPE level
- High order path cross connect with VC-3/STS-1 SPE granularity
- Byte-wide 77.76 MHz Telecom Bus terminal interface
- MS/Line or RS/Section DCC access port per line
- Ring Ports for line/path ring applications
- TOH and POH access port
- 16-bit wide microprocessor interface, selectable between Motorola or Intel
- Software device driver is provided
- Boundary scan and line loopback
- +3.3V and +1.8V power supplies, 3.3V digital I/O leads
- 376-lead plastic ball grid array (PBGA) package (23 mm x 23 mm)

APPLICATIONS

- SDH/SONET add/drop and terminal multiplexers
- Linear MS/Line protection
- Multiservice applications



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Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, must register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They must also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

LIST OF TABLES

Table **Page**

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated PHAST-12N device Data Sheet that have significant differences relative to the previous and now superseded PHAST-12N Data Sheet:

Updated PHAST-12N device Data Sheet: *PRELIMINARY* Edition 2, June 2005

Previous PHAST-12N device Data Sheet: *PRODUCT PREVIEW* Edition 1, December 2004

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date. Changed document status from *PRODUCT PREVIEW* to *PRELIMINARY*.
3-7	Updated "Table of Contents", "List of Figures" and "List of Tables".
9	Added "List of Data Sheet Changes".
23	Modified Name/Function column for Symbol Reserved.
25	Modified Name/Function column for Symbol LINETXCAP.
26	Modified Name/Function column for table Clock/Timing Interface.
45	Modified Conditions for Moisture Exposure Level and Note 3 for table Absolute Maximum Ratings and Environmental Limitations.
47	Added last sentence in Power Supply Sharing, Filtering and Other Requirements.
48	Added new sentence begin with "The placement of these resistors .....".
50	Changed Min and Max values for Parameter V_{DD}-V_{oH}, V_{DD}-V_{oL}, V_{DD}-V_{oS}, and Notes below the table.
56, 58, 60, 64	Modified Min value for Symbol T_S of Figure 7, Figure 9, Figure 11, and Figure 15.
65, 67	Added new Figure 16 and Figure 17.
68-82	Changed Min values for Symbol T_{D4} of Figure 18 through Figure 25.
87	Modified section Clock Architecture.

Page Number of Updated Data Sheet	Summary of the Change
91	Modified section Microprocessor Controlled Reset Per Clock Domain.
97	Modified diagram in section APS Interface.
97	Modified sections APS Interface Generator and APS Interface Monitor.
105	Added last paragraph in section APS Port Architecture.
113	Modified Figure 39 and added Figure title. Modified sections Generation of Frame Reference Pulse and Locking on External Frame Reference Pulse.
132	Added new section Drop Bus High Impedance.
134	Modified section Bursty Distribution of Errors.
135	Added last paragraph in section Poisson Distribution of Errors.
153	Modified Table 6, Name and Description columns for Offset 0x0006, Bits 7-0.
180	Modified Table 56, Description column for Offset 0x0000, Bits 12-0 and Table 57, Description column for Offset 0x0000, Bits 13-0.

APPLICABLE STANDARDS DOCUMENTATION

Standards documents applicable to the functions of the PHAST®-12N device are listed below.

Short Name	Description
ANSI T1.105	SONET - Basic description including Multiplex structure, rates and formats, 2001
ANSI T1.105.02	Synchronous Optical Networks (SONET), Payload Mappings, 2001
ANSI T1.107	Digital Hierarchy - Formats Specifications, 1995
ETSI EN 300-417 1-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - Generic processes and performance
ETSI EN 300-417 2-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - SDH and PDH physical section layer functions
ETSI EN 300-417 3-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - STM-N regenerator and multiplex section layer functions
ETSI EN 300-417 4-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - SDH path layer functions
ETSI EN 300-417 9-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - SDH concatenated path layer functions; Sub-part 1: Requirements
IEEE 1149.1	Standard Test Access Port and Boundary Scan Architecture (May 21, 1990)
IEEE 1596.3	Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) (March 21, 1996)
ITU-T G.707/Y.1322	Network Node interface for the Synchronous Digital Hierarchy (SDH) (10/2000)
ITU-T G.783	Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks (10/2001)
ITU-T G.803	Architecture of transport networks based on the SDH (03/2000).
ITU-T G.805	Generic functional architecture of transport networks (03/2000)
ITU-T G.806	Characteristics of transport equipment - Description methodology and generic functionality (10/2000)
Telcordia GR-253-CORE	SONET Common Generic Criteria, Rev 3, September 2000
Telcordia GR-499-CORE	Transport Systems Generic Requirements: Common Requirements, Issue 2, December 1998

OVERVIEW

The TranSwitch PHAST-12N is a highly integrated STM-4/OC-12 rate SDH/SONET overhead termination device designed for TDM payload mappings. A single PHAST-12N can terminate four individual STM-1/OC-3 lines or a single STM-4/ OC-12 line. It can perform clock synthesis and clock recovery for four 155.52 Mbit/s signals or a single 622.08 Mbit/s serial signal.

The PHAST-12N device provides RS/section and MS/line overhead processing, high order AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STC-6c/STS-9c/STS-12c pointer tracking and retiming, and high order VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE path overhead processing and performance monitoring. It provides full non-blocking cross connecting at the high order path level allowing path loopbacks, line/MSP protection and UPSR and SNC/P path protection.

The PHAST-12N device supports the following APS architectures:

1. STM-4/OC-12 mode: 1+1 or 1:1 APS using two devices connected via the APS port
2. STM-1/OC-3 mode: 1+1, 1:1 or 1:n (n<=3) APS using a single device without APS port
3. STM-1/OC-3 mode: 1+1, 1:1 or 1:n (n<=7) APS using two devices connected via the APS port

The device operates from 1.8V and 3.3V power supplies.

Major interfaces include:

1. Serial LVPECL line interfaces: single STM-4/OC-12 or four STM-1/OC-3
2. 77.76 MHz telecom bus interface
3. 622.08 Mbit/s serial LVDS APS port interface
4. Line/MS Alarm/Ring port selectable per line interface
5. SOH/TOH byte interface
6. DCC interface
7. High Order Path Alarm/Ring port selectable per SDH/SONET path
8. High Order POH byte interface
9. Motorola/Intel style microprocessor interface for configuration, alarms and performance monitoring
10. JTAG interface to IEEE 1149.1
11. Various reference clocks, and lead programmed HW configuration controls

The PHAST-12N software driver, API's and sample applications have the same architecture as other TranSwitch device software deliverables and is meant to be easily integrated with them. The application software calls the driver functions to configure, control and manage the PHAST-12N device. The device driver insulates the application from the internal details of the device register usage and provides a higher level of abstraction.

1.0 FEATURES

The following is a list of features supported by the PHAST-12N:

1.1 MODES OF OPERATION

- Line interfaces:
  - Four STM-1/OC-3 line interfaces, or
  - One STM-4/OC-12 line interface[1]
- SDH/SONET mapping:

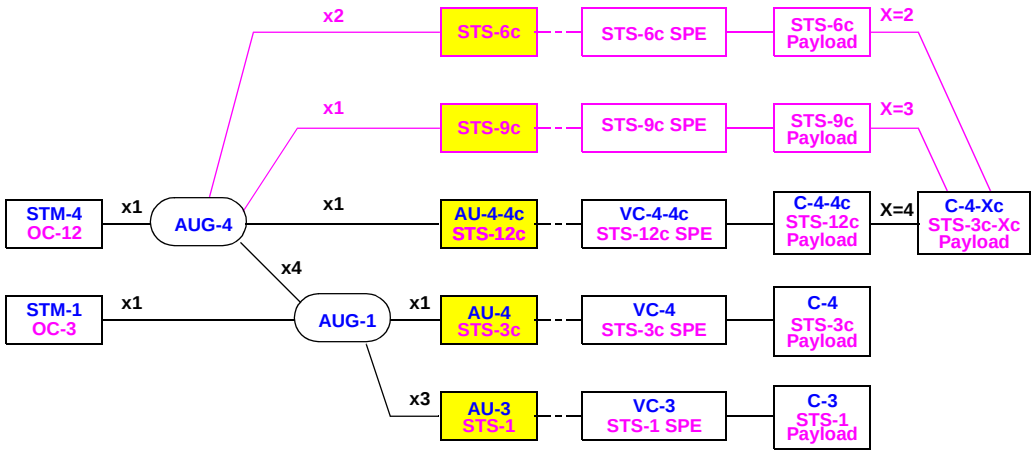


Figure 1. Supported SDH/SONET Mapping

1.2 LINE INTERFACE

- LVPECL serial line interfaces:
  - Line Interface #1 can handle 155.52 Mbit/s (STM-1/OC-3 mode) or 622.08 Mbit/s (STM-4/OC-12 mode) signals
  - Line Interfaces #2 to #4 handle 155.52 Mbit/s signals and are only used in STM-1/OC-3 mode

1. The term STM-4c/OC-12c is sometimes used to denote a STM-4/OC-12 interface transporting a contiguous concatenated VC-4-4c/STS-12c SPE high order path. The STM-4/OC-12 mode of operation allows transport of any type of high order path container. ITU-T/ANSI compliant terminology will be used throughout this document.

- Transmit clock synthesis
- Per line interface:
  - Receive clock recovery
  - Loss of Signal detection
  - Receive 19.44 MHz (STM-1/OC-3 mode) or 77.76 MHz (STM-4/OC-12 mode) clock output reference
  - General purpose input/output pins

1.3 APS PORT INTERFACE

- Single 622.08 Mbit/s LVDS serial interface:
  - Receive clock recovery
  - Transmit clock synthesis
  - Receive 77.76 MHz clock output reference
  - Transport of high order path data for four STM-1/OC-3 signals or one STM-4/OC-12 signal between two PHAST-12N devices
  - Transport of K1/K2 APS signal, signal fail and signal degrade indications for up to four lines between two PHAST-12N devices
- The APS port transports the payload and APS signaling between two mate devices. The APS finite state machine itself needs to be implemented by the external host software. The resulting bridge and switch requests are performed by configuring the cross connect.

1.4 RS/SECTION LAYER PROCESSING

- A1/A2 frame alignment
  - Out of frame and loss of frame detection
- J0 Trail Trace Identifier:
  - Insertion and monitoring of single repeating byte and 16-byte trace messages
  - Trace identifier mismatch detection
- Scrambling and descrambling
- B1 BIP-8 insertion and monitoring
- D1-D3 DCC accessible via the DCC port
- All received RSOH bytes are stored in on-chip memory and transmitted on the TOH port
- All RSOH bytes can be inserted from on-chip memory or from the TOH port

1.5 MS/LINE LAYER PROCESSING

- B2 BIP-24/96 insertion and monitoring
  - Degraded signal and excessive bit error detection
  - Block and bit error performance monitoring counters
- D4-D12 DCC can be accessible via the DCC port
- Insertion and monitoring of remote information (RDI, REI)
- Insertion and monitoring of MS/line AIS
- Insertion and monitoring of the K1/K2 APS signal

- Insertion and monitoring of the S1 synchronization status message (SSM)
- All received MSOH bytes are stored in on-chip memory and transmitted on the TOH port
- All MSOH bytes can be inserted from on-chip memory or from the TOH port

1.6 HIGH ORDER PATH LAYER PROCESSING

- J1 Trail Trace Identifier:
  - Insertion and monitoring of single repeating byte, 16-byte and 64-byte trace messages
  - Trace identifier mismatch detection
- B3 BIP-8 insertion and monitoring
  - Degraded signal and excessive bit error detection
  - Block and bit error performance monitoring counters
- C2 Trail Signal Label insertion and monitoring
  - Unequipped, VC-AIS, payload mismatch detection
- G1 insertion and monitoring
  - Single bit RDI and three bit E-RDI
  - REI insertion and block/bit performance monitoring counter
- H4 insertion and monitoring
  - Optionally insertion and monitoring of low order multiframe sequence
  - Bypass mode
- K3 insertion and monitoring
  - Automatic Protection Switching detection
- Unequipped and Supervisory Unequipped generation and detection
- Unidirectional mode
- Bypass mode
- All received POH bytes are stored in on-chip memory and transmitted on the POH port
- All POH bytes can be inserted from on-chip memory except for B3, which is used as an errormask

1.7 HIGH ORDER PATH CROSS CONNECT

- Non-blocking 36x36 cross connect:
  - 3 input and 3 output ports: line side, APS port and terminal side
  - 12 time slot channels per port
- VC-3/STS-1 SPE granularity allowing cross connecting at VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE level
- Path loopbacks and multi-casts are supported
- Each individual output channel can be forced to source an AIS or unequipped maintenance signal

1.8 TELECOM BUS INTERFACE

- Independent ADD and DROP bus
- 8-bit wide data bus
- 77.76 MHz clock
- SPE indication
- J0/C1 and J1 indication
- Optional V1 indication
- ADD bus timing modes:
  - ADD Slave mode: timing signals are inputs
  - ADD Master mode: timing signals are outputs

1.9 MICROPROCESSOR INTERFACE

- Bidirectional 16-bit wide Data bus (allowing 16-bit word accesses only)
- 14-bit wide Address bus
- The following microprocessor interface modes are supported:
  - Generic Motorola mode
  - Generic Intel mode (with separate address/data bus)
  - MPC860 mode,
  - MPC8260 Local Bus mode
- Interrupt request lead
- Interrupt mask bits for controlling generation of hardware interrupt requests

1.10 TESTING

- Line loopbacks
- High order path loopbacks via the cross connect
- Boundary scan

1.11 DEVICE DRIVER

- Device configuration
- Fault monitoring
- Performance monitoring

2.0 BLOCK DIAGRAM

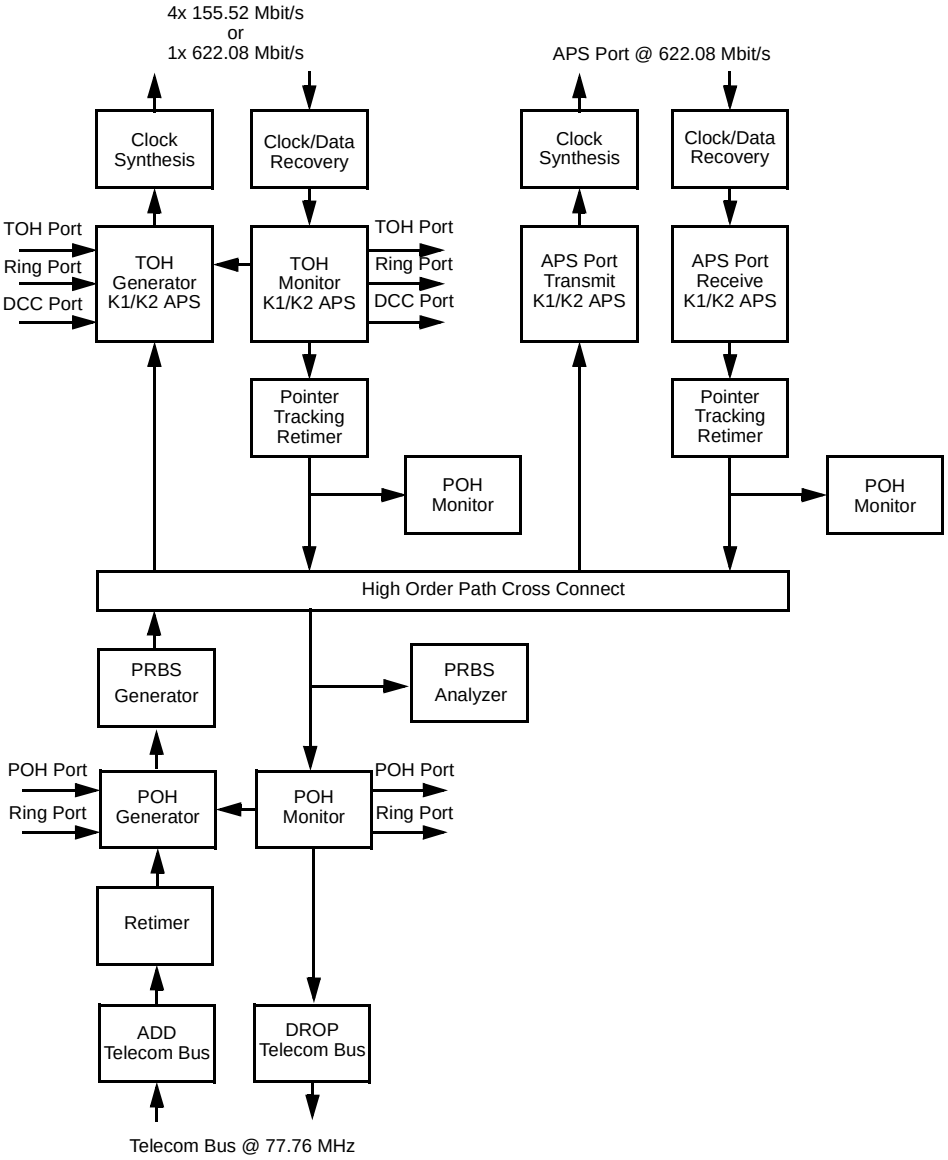
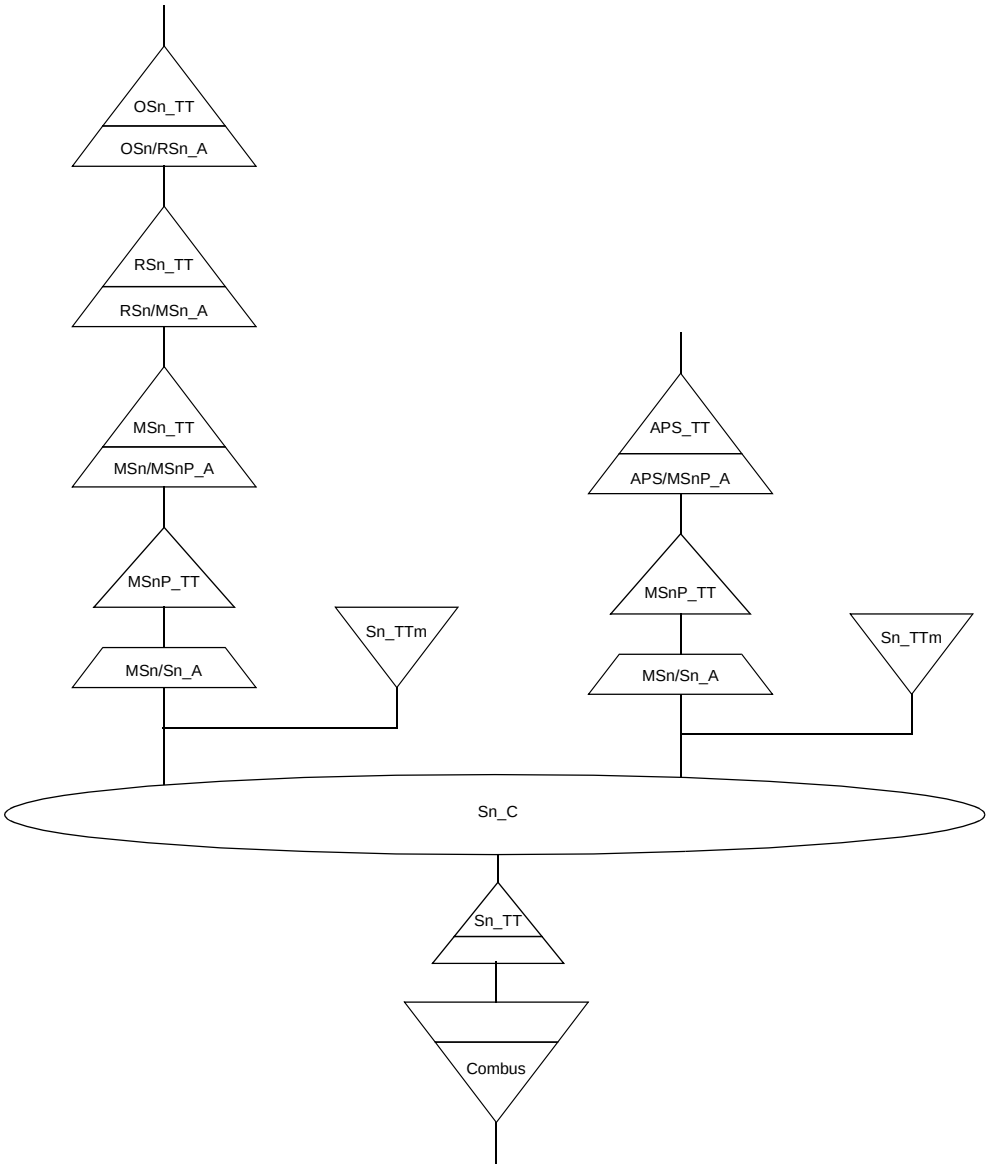


Figure 2. PHAST-12N TXC-06312B Block Diagram

3.0 FUNCTIONAL MODEL



Note: Additional information regarding the Functional Model of the PHAST-12N can be found in ITU-T G.783 Standards Documentation.

Figure 3. PHAST-12N Functional Model

4.0 BLOCK DIAGRAM DESCRIPTION

4.1 LINE SIDE

The PHAST-12N can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line. Each incoming line signal is monitored for loss of signal and clock and data recovery is performed. Reference clocks derived from each recovered clock are available.

The subsequent TOH Monitor will terminate all RS/section and MS/line overhead bytes compliant to the latest ITU/ETSI/ANSI standards. Additionally, the received raw TOH overhead bytes are stored in on-chip memory and output on the TOH port interface for external processing (except for BIP where the error mask is calculated). The received data communication channel bytes, selectable RS/section or MS/line, are output on a DCC port interface per line interface. The K1/K2 APS signal bytes are debounced and forwarded to the APS interface. RDI and REI are output on the external and internal line ring port interfaces for ring applications.

The PHAST-12N performs high order pointer processing on the H1/H2 bytes from the receive line interfaces. The high order path containers are retimed to the local System Clock.

High order POH monitoring is performed on all received high order path containers for SNC/P and UPSR applications.

In the transmit direction, the TOH Generator will insert all RS/section and MS/line overhead bytes. The TOH overhead bytes can be inserted from on-chip memory or the TOH port interface. Additionally the data communication channel bytes, selectable RS/section or MS/line, can be inserted from a DCC port interface. Remote information, RDI and REI can be inserted from the internal or external ring port interface. This selection can be made on a per line basis. The K1/K2 APS can be inserted from the APS port interface.

Finally four individual STM-1/OC-3 lines or a single STM-4/OC-12 line are transmitted using the device's System Clock.

4.2 APS PORT SIDE

The serial 622.08 Mbit/s APS port interface is monitored for loss of clock and data recovery is performed. A reference clock derived from the recovered clock is available.

The received APS port signal is monitored for signal quality and the APS information exchanged between two mate PHAST-12N devices, including K1/K2 APS signal, signal fail and signal degrade status, is stored for software access.

The PHAST-12N performs high order pointer processing on the H1/H2 bytes from the receive APS port. The high order path containers are retimed to the local System Clock.

High order POH monitoring is performed on all received high order path containers for SNC/P and UPSR applications.

In the transmit direction, the APS information exchanged between two mate PHAST-12N devices, including K1/K2 APS signal, signal fail and signal degrade status, is inserted either from on-chip memory or directly from the TOH monitor.

Finally, the serial 622.08 Mbit/s APS port signal is transmitted using the device's System Clock.

4.3 HIGH ORDER PATH CROSS CONNECT

The non-blocking high order path cross connect block can connect each output high order path time slot to each input high order path time slot. The presence of an active cross connect does not 'block' a cross connect to another output. AIS or unequipped maintenance signals can be inserted into each output time slot.

The cross connect has three input buses and three output buses: line side, APS port side and terminal side. Each bus contains the high order path containers equivalent to an STM-4/ STS-12.

4.4 TERMINAL SIDE

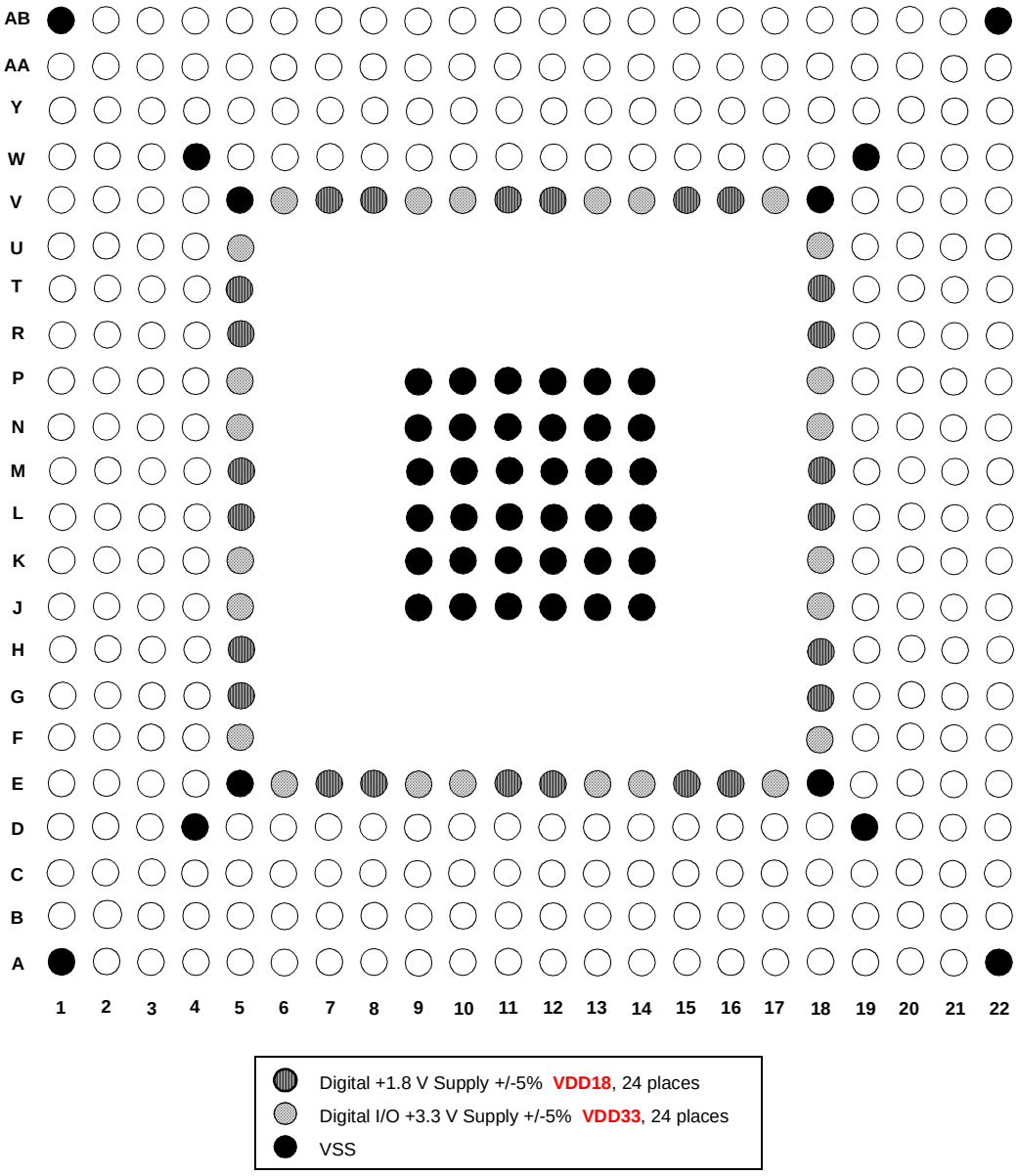
The POH Monitor will terminate all path overhead bytes of the dropped high order path containers compliant to the latest ITU/ETSI/ANSI standards. Additionally, the received raw POH overhead bytes are stored in on-chip memory and output on the POH port interface for external processing (except for BIP where the error mask is calculated). The remote information, RDI and REI, is output on the external and internal path ring port interfaces for ring applications.

Finally, the high order path data is output on the Drop Telecom Bus interface.

In the transmit direction, the high order path data is input from the ADD telecom bus interface. The POH Generator will optionally insert all path overhead bytes. The POH overhead bytes can be inserted from on-chip memory or the POH port interface. The remote information, RDI and REI, can be inserted from the internal or external ring port interface. This selection can be made on a per high order path basis.

For Test purposes, a PRBS pattern can be generated and inserted on a particular path by the PHAST-12N. PRBS can be analyzed for bit errors on the receive side.

5.0 LEAD DIAGRAM



Note: This is the bottom view. The leads are solder balls. See Figure 55 for package information.
This view is rotated relative to the bottom view in Figure 55.
Some signal Symbols have been abbreviated to fit the space available.
The Symbols are shown in full in the Lead Descriptions section.

Figure 4. PHAST-12N TXC-06312B 376-Lead Plastic Ball Grid Array Package Lead Diagram

6.0 LEAD DESCRIPTIONS

In the I/O/P column of the following tables, I = Input, O = Output, P = Power, T = Tristateable during normal operation. Entries in the Type column are defined in the Input, Output and Input/Output Parameters section.

All single-ended inputs (= LVTTL inputs) that are not used, must be connected to a low level.

Differential inputs (= LVPECL and LVDS inputs) that are not used can be left floating. They must be left in power-down mode, which is the default mode of these pads, after reset.

POWER SUPPLY, GROUND, AND NO CONNECT LEADS

Symbol	Lead No.	I/O/P	Name/Function
VDD18	E7, E8, E11, E12, E15, E16, G5, G18, H5, H18, L5, L18, M5, M18, R5, R18, T5, T18, V7, V8, V11, V12, V15, V16	P	**Digital Core 1.8V supply:** +1.8V +/-5%
VDDA18RPA	AB15, W16	P	Rx PLL / Clock Recovery & Rx LVPECL analog 1.8V supply
VDDA18TPA	AB13, Y9	P	Tx PLL / Clock Synthesis & Tx LVPECL analog 1.8V supply
VDD33	E6, E9, E10, E13, E14, E17, F5, F18, J5, J18, K5, K18, N5, N18, P5, P18, U5, U18, V6, V9, V10, V13, V14, V17	P	**Digital I/O 3.3V supply:** +3.3V +/-5%
VDDA33LVPCDRV	AB11, W10	P	LVPECL driver analog 3.3V supply
VDDA33LVPCIO	AA17, W11	P	LVPECL pre-drive analog 3.3V supply
VSS	A1, A22, AB1, AB22, D19, D4, E18, E5, J10, J11, J12, J13, J14, J9, K10, K11, K12, K13, K14, K9, L10, L11, L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, V18, V5, W19, W4	P	Digital Core 1.8V & Digital I/O 3.3V returns
VSSA18RPA	AA16, AB16	P	Rx PLL / Clock Recovery & Rx LVPECL analog 1.8V return
VSSA18TPA	AA8, AB12	P	Tx PLL / Clock Synthesis & Tx LVPECL analog 1.8V return
VSSA33LVPCPST	AA14, AA15	P	LVPECL driver & pre-drive analog 3.3V returns

Symbol	Lead No.	I/O/P	Name/Function
NC	A10, A13, A15, A16, A18, A19, A6, A7, A8, A9, AA9, B10, B13, B14, B15, B17, B6, B7, B8, B9, C10, C13, C14, C16, C7, C8, C9, D10, D11, D12, D13, D3, D8, D9, F19, Y20		**No Connect:** These leads are not to be connected, and must be left floating. Connection of an NC lead may impair performance or cause damage to the device. NC leads that are currently unused may be assigned functions in a future version of the device, affecting its usability in applications which have not left them floating.
Reserved	AB7, AB17		These leads are no longer used. For all applications it is required to leave these leads unconnected.
Reserved_Low	A11, A12, A14, A17, A20, A21, B11, B12, B16, B18, B19, B20, B22, C11, C12, C15, C17, C18, C19, C20, C21, C22, D14, D15, D16, D17, D18, D20, D21, D22, E19, E20, E21, F20, G19		**For Future Use:** These leads are reserved for future use and should be tied to VSS.

REFERENCE VOLTAGES

Symbol	Lead No.	I/O/P	Type	Name/Function
VREF	W12			**1.2V Reference Voltage:** 1.2V reference voltage for all LVPECL and LVDS output drivers, and to bias the Rx and Tx PLLs.
VTERM	AB10			**1.2V Termination Voltage:** optional 1.2V termination voltage for the LVDS input buffer.

SDH/SONET RECEIVE LINE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
LINERXDATA1P LINERXDATA1N	Y14 W13	I	LVPECL	**Serial SDH/SONET Receive Data #1:** 622.08/155.52 Mbit/s bit-serial data from electro/optical transceivers. Only LINERXDATA1P/N can be used in STM-4/OC-12 mode.
LINERXDATA2P LINERXDATA2N	Y15 W14	I	LVPECL	**Serial SDH/SONET Receive Data #2:** 155.52 Mbit/s bit-serial data from electro/optical transceivers. Can not be used in STM-4/OC-12 mode.
LINERXDATA3P LINERXDATA3N	W15 Y16	I	LVPECL	**Serial SDH/SONET Receive Data #3:** 155.52 Mbit/s bit-serial data from electro/optical transceivers. Can not be used in STM-4/OC-12 mode.
LINERXDATA4P LINERXDATA4N	AB18 AB19	I	LVPECL	**Serial SDH/SONET Receive Data #4:** 155.52 Mbit/s bit-serial data from electro/optical transceivers. Can not be used in STM-4/OC-12 mode.

Symbol	Lead No.	I/O/P	Type	Name/Function
LINERXSIGDET1	AA18	I	LVTTL	**Signal Detect #1:** Signal from the optical receiver for line #1 indicating signal presence.
LINERXSIGDET2	AB20	I	LVTTL	**Signal Detect #2:** Signal from the optical receiver for line #2 indicating signal presence. Not used in STM-4/OC-12 mode.
LINERXSIGDET3	W17	I	LVTTL	**Signal Detect #3:** Signal from the optical receiver for line #3 indicating signal presence. Not used in STM-4/OC-12 mode.
LINERXSIGDET4	Y18	I	LVTTL	**Signal Detect #4:** Signal from the optical receiver for line #4 indicating signal presence. Not used in STM-4/OC-12 mode.
LINERXCLK1	AA19	O	LVCMOS 8mA	**Receive Divided Clock #1:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA1P/N. The clock rate is programmable to be either 19.44 or 77.76 MHz.
LINERXCLK2	AB21	O	LVCMOS 8mA	**Receive Divided Clock #2:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA2P/N. The clock rate is fixed to 19.44 MHz.
LINERXCLK3	W18	O	LVCMOS 8mA	**Receive Divided Clock #3:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA3P/N. The clock rate is fixed to 19.44 MHz.
LINERXCLK4	Y19	O	LVCMOS 8mA	**Receive Divided Clock #4:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA4P/N. The clock rate is fixed to 19.44 MHz.
LINERXCAP	Y17		Analog	**Capacitor for the Receive Line & APS Clock Recovery:** Optional external capacitor. Do not install.

SDH/SONET TRANSMIT LINE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
LINETXDATA1P LINETXDATA1N	AA10 Y10	O	LVPECL	**Serial SDH/SONET Transmit Data #1:** 622.08/155.52 Mbit/s bit-serial data to electro/optical transceivers. Only LINETXDATA1P/N is valid in STM-4/OC-12 mode.
LINETXDATA2P LINETXDATA2N	AA11 Y11	O	LVPECL	**Serial SDH/SONET Transmit Data #2:** 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid in STM-4/OC-12 mode.
LINETXDATA3P LINETXDATA3N	Y12 AA12	O	LVPECL	**Serial SDH/SONET Transmit Data #3:** 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid in STM-4/OC-12 mode.
LINETXDATA4P LINETXDATA4N	Y13 AA13	O	LVPECL	**Serial SDH/SONET Transmit Data #4:** 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid in STM-4/OC-12 mode.
LINETXCLK	Y7	O	LVCMOS 8mA	**Transmit Divided Clock:** Clock output derived from the synthesized transmit lock. The clock rate is programmable to be either 19.44 MHz or 77.76 MHz.
LINETXCAP	AB14		Analog	**Capacitor for the Transmit Line & APS Clock Synthesizer:** Optional external capacitor. Advised capacitor value: **STM-1/OC-3 Application**: External Timing: N/A; Line/Loop - Timing: 1.0 µF **STM-4/OC-12 Application**: External Timing: N/A; Line/Loop - Timing: 1.0 µF

RECEIVE APS PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
APSRXDATAP APSRXDATAN	W9 Y8	I	LVDS	**Serial APS Port Receive Data:** 622.08 Mbit/s bit-serial data from mate PHAST-12N.
APSRXCLK	AA6	O	LVCMOS 8mA	**Receive Divided APS Port Clock:** Clock output derived from the clock recovered from the serial APS port data stream on APSRXDATAP/N. The clock rate is programmable to be either 19.44 or 77.76 MHz.

TRANSMIT APS PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
APSTXDATAP APSTXDATAN	AA7 AB6	O	LVDS	**Serial APS Port Transmit Data:** 622.08 Mbit/s bit-serial data to mate PHAST-12N.

CLOCK/TIMING INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
REFTXCLK1	AA20	I	LVTTL	**Transmit Reference Clock #1:** Reference clock for the transmit clock synthesizer. The clock rate is programmable to be either 19.44 or 77.76 MHz. The frequency tolerance for this clock is ± 20 ppm. The maximum allowed jitter on this clock should be confined to the same limits as indicated below for the REFTXCLK2P/REFTXCLK2N leads.
REFTXCLK2P REFTXCLK2N	AB9 AB8	I	LVPECL	**Transmit Reference Clock #2:** Reference clock for the transmit clock synthesizer. The clock rate is programmable to be 19.44, 77.76 or 155.52 MHz. A 622.08 MHz clock can be provided when the Tx PLL is bypassed. The frequency tolerance for this clock is ± 20 ppm. The maximum jitter on this clock should be confined to a bandwidth of 5 kHz - 5 MHz and to the values shown below depending on the selected frequency as indicated:
REFRXCLK	W8	I	LVTTL	**Receive Reference Clock:** Optional Reference clock for the receive clock and data recovery units. This clock is required for line/loop-time applications, when REFTXCLK1 and REFTXCLK2P/N are not present. The clock rate is programmable to be either 19.44 or 77.76 MHz. The frequency tolerance for this clock is ± 100 ppm

Applied Reference Clock Frequency (MHz)	Maximum Reference Clock Jitter			
	OC-3		OC-12	
	ps RMS	ps pp	ps RMS	ps pp
19.44	40	280	8	56
77.76	40	280	8	56
155.52	40	280	8	56
622.08	40	280	8	56

Symbol	Lead No.	I/O/P	Type	Name/Function
REFONESECCLK	R1	I	LVTTL	**One Second Clock:** Optional one second reference for performance monitoring counters. This is a 1.0 Hz ± 32 ppm clock input which is asynchronous with other clock inputs/outputs, and has a minimum pulse width of 2 77.76 MHz clock cycles = 25.72 ns (because synchronized). If used, the one second counters are shadowed after detection of the rising edge of this input.
REFTXFS	R2	I	LVTTL	**Transmit Reference Frame Sync:** Optional 8 kHz reference frame sync pulse. If present, this input must be synchronous to LINETXCLK and shall be at least 1 77.76 MHz clock cycle wide = 12.86 ns.
REFSYSFS	B21	O	LVCMOS 8mA	**System Reference Frame Sync:** 8 kHz reference frame sync pulse. This output has a pulse width of 1 77.76 MHz clock cycle (= 12.86 ns) and shall be synchronous to the LINETXCLK when this last one is not divided down to 19.44 MHz.
$\overline{\text{RESET}}$	A4	I	LVTTLp	**Hardware Reset (Active Low):** The use of this lead at power-up is mandatory. Holding this lead for at least 50 ns causes all the registers in the device to be reset.

RECEIVE DCC INTERFACES

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCRXDATA1	V2	O	LVCMOS 4mA	**Receive DCC Data #1:** Bit-serial data from the TOH monitor of receive line interface #1 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXDATA2	Y1	O	LVCMOS 4mA	**Receive DCC Data #2:** Bit-serial data from the TOH monitor of receive line interface #2 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXDATA3	U4	O	LVCMOS 4mA	**Receive DCC Data #3:** Bit-serial data from the TOH monitor of receive line interface #3 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCRXDATA4	V3	O	LVCMOS 4mA	**Receive DCC Data #4:** Bit-serial data from the TOH monitor of receive line interface #4 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXCLK1	V1	O	LVCMOS 8mA	**Receive DCC Clock #1:** The DCCRXDATA1 signal is clocked out by the PHAST-12N on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA1, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA1, the frequency is 192 kHz.
DCCRXCLK2	W1	O	LVCMOS 8mA	**Receive DCC Clock #2:** The DCCRXDATA2 signal is clocked out by the PHAST-12N on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA2, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA2, the frequency is 192 kHz.
DCCRXCLK3	T4	O	LVCMOS 8mA	**Receive DCC Clock #3:** The DCCRXDATA3 signal is clocked out by the PHAST-12N on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA3, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA3, the frequency is 192 kHz.
DCCRXCLK4	U3	O	LVCMOS 8mA	**Receive DCC Clock #4:** The DCCRXDATA4 signal is clocked out by the PHAST-12N on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA4, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA4, the frequency is 192 kHz.

TRANSMIT DCC INTERFACES

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCTXDATA1	U1	I	LVTTL	**Transmit DCC Data #1:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #1. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXDATA2	R4	I	LVTTL	**Transmit DCC Data #2:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #2. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXDATA3	T3	I	LVTTL	**Transmit DCC Data #3:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #3. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXDATA4	U2	I	LVTTL	**Transmit DCC Data #4:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #4. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXCLK1	T1	O	LVCMOS 8mA	**Transmit DCC Clock #1:** The DCCTXDATA1 signal is clocked into the PHAST-12N on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA1, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA1, the frequency is 192 kHz.
DCCTXCLK2	P4	O	LVCMOS 8mA	**Transmit DCC Clock #2:** The DCCTXDATA2 signal is clocked into the PHAST-12N on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA2, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA2, the frequency is 192 kHz.
DCCTXCLK3	R3	O	LVCMOS 8mA	**Transmit DCC Clock #3:** The DCCTXDATA3 signal is clocked into the PHAST-12N on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA3, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA3, the frequency is 192 kHz.
DCCTXCLK4	T2	O	LVCMOS 8mA	**Transmit DCC Clock #4:** The DCCTXDATA4 signal is clocked into the PHAST-12N on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA4, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA4, the frequency is 192 kHz.

ADD TELECOM BUS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
CBADT	E22	I	LVTTLp	**Add Telecom Bus Timing Mode:** Selects Master or Slave timing mode on the Add Telecom Bus. If CBADT is high, Slave timing is selected: CBADCLK, CBADSPE and CBADJ0J1 are inputs. If CBADT is low, Master timing is selected: CBADCLK, CBADSPE and CBADJ0J1 are outputs.
CBADD7 CBADD6 CBADD5 CBADD4 CBADD3 CBADD2 CBADD1 CBADD0	L21 L20 K22 L19 K21 K20 J22 J21	I	LVTTL	**Add Telecom Bus Data:** Byte wide SDH/SONET data received from the Add Telecom Bus.
CBADSPE	M21	I/O(T)	LVTTL/ LVCMOS 24mA	**Add Telecom Bus SPE Indicator:** This signal is high during each byte of the High Order Path Overhead and payload bytes and low during the Transport Overhead byte times.
CBADJ0J1	M22	I/O(T)	LVTTL/ LVCMOS 24mA	**Add Telecom Bus J0J1 Indicator:** This signal represents the frame sync and optionally the position of each payload container (VC-n/STS-N SPE). This signal works in conjunction with the CBADSPE signal. The J0 pulse identifies the position of the first J0 byte when the CBADSPE signal is low. The J1 pulses identify the position of the J1 byte of each payload container (VC-n/STS-N SPE) when the CBADSPE signal is high. A V1 pulse can optionally be available on this lead.
CBADPAR	M20	I	LVTTL	**Add Telecom Bus Parity Bit:** Parity bit input signal that represents the parity calculated over CBADD[7:0], and optionally CBADSPE and CBADJ0J1. Even or odd parity can be selected.
CBADCLK	L22	I/O(T)	LVTTL/ LVCMOS 24mA	**Add Telecom Bus Clock:** This 77.76 MHz clock is used to clock in Add Telecom Bus data. In addition CBADSPE and CBADJ0J1 are clocked in in Slave timing mode. CBADSPE and CBADJ0J1 are clocked out in Master timing mode. The active clock edges can be selected.

DROP TELECOM BUS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
CBDPD7 CBDPD6 CBDPD5 CBDPD4 CBDPD3 CBDPD2 CBDPD1 CBDPD0	G22 J19 H20 G21 F22 H19 G20 F21	O(T)	LVCMOS 8mA	**Drop Telecom Bus Data:** Byte wide SDH/SONET data sent on the Drop Telecom Bus.
CBDPSPE	J20	O	LVCMOS 8mA	**Drop Telecom Bus SPE Indicator:** This signal is high during each byte of the High Order Path Overhead and payload bytes and low during the Transport Overhead byte times.
CBDPJ0J1	H22	O	LVCMOS 8mA	**Drop Telecom Bus J0J1 Indicator:** This signal represents the frame sync and optionally the position of each payload container (VC-n/STS-N SPE). This signal works in conjunction with the CBDPSPE signal. The J0 pulse identifies the position of the first J0 byte when the CBDPSPE signal is low. The J1 pulses identify the position of the J1 byte of each payload container (VC-n/STS-N SPE) when the CBDPSPE signal is high. A V1 pulse can optionally be generated on this lead.
CBDPPAR	K19	O(T)	LVCMOS 8mA	**Drop Telecom Bus Parity Bit:** Parity bit output signal that represents the parity calculated over CBDPD[7:0], and optionally CBDPSPE and CBDPJ0J1. Even or odd parity can be selected.
CBDPCLK	H21	O	LVCMOS 8mA	**Drop Telecom Bus Clock:** All Drop Telecom Bus signals are clocked out on this 77.76 MHz clock. The active clock edge can be selected.

RECEIVE LINE RING PORT/ALARM INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
LRPRXCLK	T22	O	LVCMOS 4mA	**Receive Line Ring Port Clock:** The LRPRXFS and LRPRXDATA signals are clocked out on the rising edges of this clock. Its frequency is 19.44 MHz.
LRPRXFS	R21	O	LVCMOS 4mA	**Receive Line Ring Port Frame Sync:** An active high, one LRPRXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on LRPRXDATA.
LRPRXDATA	P19	O	LVCMOS 4mA	**Receive Line Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals.

TRANSMIT LINE RING PORT/ALARM INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
LRPTXCLK	P20	I	LVTTL	**Transmit Line Ring Port Clock:** The LRPTXFS and LRPTXDATA signals are clocked in on the rising edges of this clock. Its frequency is 19.44 MHz. When this lead is not connected to LRPRXCLK of a mate PHAST-12N device, it must be tied to VSS.
LRPTXFS	N19	I	LVTTL	**Transmit Line Ring Port Frame Sync:** An active high, one LRPTXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on LRPTXDATA. When this lead is not connected to LRPRXFS of a mate PHAST-12N device, it must be tied to VSS.
LRPTXDATA	R22	I	LVTTL	**Transmit Line Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals. When this lead is not connected to LRPRXDATA of a mate PHAST-12N device, it must be tied to VSS.

RECEIVE HIGH ORDER PATH RING PORT/ALARM INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
PRPRXCLK	M19	O	LVCMOS 4mA	**Receive HO Ring Port Clock:** The PRPRXFS and PRPRXDATA signals are clocked out on the rising edges of this clock. Its frequency is 19.44 MHz.
PRPRXFS	N21	O	LVCMOS 4mA	**Receive HO Ring Port Frame Sync:** An active high, one PRPRXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on PRPRXDATA.
PRPRXDATA	N22	O	LVCMOS 4mA	**Receive HO Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals.

TRANSMIT HIGH ORDER PATH RING PORT/ALARM INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
PRPTXCLK	P22	I	LVTTL	**Transmit HO Ring Port Clock:** The PRPTXFS and PRPTXDATA signals are clocked in on the rising edges of this clock. Its frequency is 19.44 MHz. When this lead is not connected to LRPRXCLK of a mate PHAST-12N device, it must be tied to VSS.
PRPTXFS	P21	I	LVTTL	**Transmit HO Ring Port Frame Sync:** An active high, one PRPTXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on PRPTXDATA. When this lead is not connected to LRPRXFS of a mate PHAST-12N device, it must be tied to VSS.
PRPTXDATA	N20	I	LVTTL	**Transmit HO Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals. When this lead is not connected to LRPRXDATA of a mate PHAST-12N device, it must be tied to VSS.

RECEIVE TOH BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TOHRXCLK	U19	O	LVCMOS 8mA	**Receive TOH Port Clock:** The TOHRXALE, TOHRXDLE, TOHRXADDR and TOHRXDATA signals are clocked out on the falling edges of this clock. Its frequency is 77.76 MHz.
TOHRXALE	V20	O	LVCMOS 8mA	**Receive TOH Port Address Latch Enable:** An active high, 10 TOHRXCLK clock-cycle wide pulse indicating that a valid address is present on TOHRXADDR.
TOHRXADDR	W21	O	LVCMOS 8mA	**Receive TOH Port Address:** The 10 consecutive states clocked out while TOHRXALE is high form the address of the subsequent TOH byte sent on the TOHRXDATA lead.
TOHRXDLE	V21	O	LVCMOS 8mA	**Receive TOH Port Data Latch Enable:** An active high, 8 TOHRXCLK clock-cycle wide pulse indicating that valid data is present on TOHRXDATA.
TOHRXDATA	Y22	O	LVCMOS 8mA	**Receive TOH Port Data:** The 8 consecutive states clocked out while TOHRXDLE is high form the value of the TOH byte addressed by TOHRXADDR.

TRANSMIT TOH BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TOHTXCLK	W20	O	LVCMOS 16mA	**Transmit TOH Port Clock:** The TOHTXALE, TOHTXDLE and TOHTXADDR signals are clocked out on the falling edges of this clock. TOHTXDATA is clocked in on the rising edge of this clock. Its frequency is 77.76 MHz.
TOHTXALE	Y21	O	LVCMOS 8mA	**Transmit TOH Port Address Latch Enable:** An active high, 10 TOHTXCLK clock-cycle wide pulse indicating that a valid address is present on TOHTXADDR.
TOHTXADDR	AA21	O	LVCMOS 8mA	**Transmit TOH Port Address:** The 10 consecutive states clocked out while TOHTXALE is high form the address of the subsequent TOH byte requested on the TOHTXDATA lead.
TOHTXDLE	AA22	O	LVCMOS 8mA	**Transmit TOH Port Data Latch Enable:** An active high, 8 TOHTXCLK clock-cycle wide pulse indicating that valid data is present on TOHTXDATA.
TOHTXDATA	V19	I	LVTTL	**Transmit TOH Port Data:** The value of the TOH byte requested by TOHTXADDR is clocked in as the 8 consecutive states while TOHTXDLE is high. When the Transmit TOH Byte Interface is not used, this lead must be tied to VSS.

RECEIVE HIGH ORDER POH BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
POHRXCLK	W22	O	LVCMOS 8mA	**Receive HO POH Port Clock:** The POHRXALE, POHRXDLE, POHRXADDR and POHRXDATA signals are clocked out on the falling edges of this clock. Its frequency is 77.76 MHz.
POHRXALE	V22	O	LVCMOS 8mA	**Receive HO POH Port Address Latch Enable:** An active high, 8 POHRXCLK clock-cycle wide pulse indicating that a valid address is present on POHRXADDR.
POHRXADDR	U21	O	LVCMOS 8mA	**Receive HO POH Port Address:** The 8 consecutive states clocked out while POHRXALE is high form the address of the subsequent High Order POH byte sent on the POHRXDATA lead.
POHRXDLE	U20	O	LVCMOS 8mA	**Receive HO POH Port Data Latch Enable:** An active high, 8 POHRXCLK clock-cycle wide pulse indicating that valid data is present on POHRXDATA.
POHRXDATA	T19	O	LVCMOS 8mA	**Receive HO POH Port Data:** The 8 consecutive states clocked out while POHRXDLE is high form the value of the High Order POH byte addressed by POHRXADDR.

TRANSMIT HIGH ORDER POH BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
POHTXCLK	U22	O	LVCMOS 16mA	**Transmit HO POH Port Clock:** The POHTXALE, POHTXDLE and POHTXADDR signals are clocked out on the falling edges of this clock. POHTXDATA is clocked in on the rising edge of this clock. Its frequency is 77.76 MHz.
POHTXALE	T21	O	LVCMOS 8mA	**Transmit HO POH Port Address Latch Enable:** An active high, 8 POHTXCLK clock-cycle wide pulse indicating that a valid address is present on POHTXADDR.
POHTXADDR	R20	O	LVCMOS 8mA	**Transmit HO POH Port Address:** The 8 consecutive states clocked out while POHTXALE is high form the address of the subsequent High Order POH byte requested on the POHTXDATA lead.
POHTXDLE	T20	O	LVCMOS 8mA	**Transmit HO POH Port Data Latch Enable:** An active high, 8 POHTXCLK clock-cycle wide pulse indicating that valid data is present on POHTXDATA.
POHTXDATA	R19	I	LVTTL	**Transmit HO POH Port Data:** The value of the High Order POH byte requested by POHTXADDR is clocked in as the 8 consecutive states while POHTXDLE is high. When the Transmit High Order POH Byte Interface is not used, this lead must be tied to VSS.

GENERAL PURPOSE INPUT/OUTPUT

Symbol	Lead No.	I/O/P	Type	Name/Function
GPIN1	N1	I	LVTTL	**General Purpose Input #1:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPIN2	M4	I	LVTTL	**General Purpose Input #2:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPIN3	N2	I	LVTTL	**General Purpose Input #3:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPIN4	N3	I	LVTTL	**General Purpose Input #4:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.

Symbol	Lead No.	I/O/P	Type	Name/Function
GPOUT1	P1	O	LVCMOS 4mA	**General Purpose Output #1:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.
GPOUT2	P2	O	LVCMOS 4mA	**General Purpose Output #2:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.
GPOUT3	N4	O	LVCMOS 4mA	**General Purpose Output #3:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.
GPOUT4	P3	O	LVCMOS 4mA	**General Purpose Output #4:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.

HOST PROCESSOR INTERFACE SELECTION

Symbol	Lead No.	I/O/P	Type	Name/Function
MPMODE1 MPMODE0	M2 M3	I	LVTTL	**Microprocessor Interface Select:** These leads select the Host Processor interface mode:
MPINTLEVEL	A2	I	LVTTLd	**Microprocessor Interrupt Level:** This lead selects the polarity of the MPINTR lead. If MPINTLEVEL is low, the interrupt on the MPINTR lead is active low, if MPINTLEVEL is high, the interrupt on the MPINTR lead is active high. This lead is evaluated in all modes (MPMODE[1:0] = '00', '01', '10' and '11').
MPACKLEVEL	D5	I	LVTTLd	**Microprocessor Acknowledge Level:** This lead selects the polarity of the MPACK lead. If MPACKLEVEL is low, an acknowledge is indicated by a falling edge of MPACK, if MPACKLEVEL is high, an acknowledge is indicated by a rising edge of MPACK. This lead is only evaluated in Generic Intel Mode (MPMODE[1:0] = '00') and Generic Motorola Mode (MPMODE[1:0] = '01'). This lead must be tied to VSS when MPMODE[1:0] = '10' or '11'.

MPMODE1	MPMODE0	Interface
0	0	Generic Intel
0	1	Generic Motorola
1	0	Motorola MPC860
1	1	Motorola MPC8260 Local Bus

Note: The Generic Intel, Generic Motorola, Motorola MPC860 and Motorola MPC8260 Local Bus - Host Processor interfaces are shared on the same leads.

GENERIC INTEL - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Interface Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Intel notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12N for a read or write cycle. MPA13 is the most significant bit in the location's address. **Intel notation: A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12N and the host processor. MPD15 is the most significant bit. **Intel notation: D[ ]**
MPSEL	K1	I	LVTTL	**PHAST-12N Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12N through a read or write cycle. **Intel notation: CS**
MPTS	L3	I	LVTTL	**Read Strobe (Active low):** This active low lead initiates a read transfer between the host processor and the PHAST-12N. **Intel notation: RD**

Symbol	Lead No.	I/O/P	Type	Name/Function
MPWR	L2	I	LVTTL	**Write Strobe (Active Low):** This active low lead initiates a write transfer between the host processor and the PHAST-12N. **Intel notation: WR**
MPACK	L1	O(T)	LVCMOS 24mA	**Ready:** For a write access, an active edge on this lead indicates that data is written to the addressed memory location. For a read access, an active edge on this lead indicates that the data to be read from the addressed memory location is available on the data bus. Active level depends on MPACKLEVEL. **Intel notation: RDY**
MPINTR	B3	O	LVCMOS 8mA	**Interrupt:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL.

GENERIC MOTOROLA - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12N for a read or write cycle. MPA13 is the most significant bit in the location's address. **Motorola notation: A[ ]**

Symbol	Lead No.	I/O/P	Type	Name/Function
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12N and the host processor. MPD15 is the most significant bit. **Motorola notation: D[ ]**
MPSEL	K1	I	LVTTL	**PHAST-12N Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12N through a read or write cycle. **Motorola notation: CS**
MPTS	L3	I	LVTTL	**Data Strobe (Active Low):** This active low lead initiates a (read or write) transfer between the host processor and the PHAST-12N. **Motorola notation: DS**
MPWR	L2	I	LVTTL	**Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the PHAST-12N is a write transfer. **Motorola notation: R/W**
MPACK	L1	O(T)	LVCMOS 24mA	**Data Transfer Acknowledge:** For a write access, an active edge on this lead indicates that data is written to the addressed memory location. For a read access, an active edge on this lead indicates that the data to be read from the addressed memory location is available on the data bus. Active level depends on MPACKLEVEL. **Motorola notation: DSACK**
MPINTR	B3	O	LVCMOS 8mA	**Interrupt Request:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL.

MOTOROLA MPC860 - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola MPC860 notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12N for a read or write cycle. MPA13 is the most significant bit in the location's address. **Motorola MPC860 notation: A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12N and the host processor. MPD15 is the most significant bit. **Motorola MPC860 notation: D[ ]**
MPSEL	K1	I	LVTTL	**PHAST-12N Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12N through a read or write cycle. **Motorola MPC860 notation: CS**
MPTS	L3	I	LVTTL	**Transfer Start (Active Low):** This active low lead initiates a (read or write) transfer between the host processor and the PHAST-12N. It is active low only during the first cycle of the access. **Motorola MPC860 notation: TS**

Symbol	Lead No.	I/O/P	Type	Name/Function
MPWR	L2	I	LVTTL	**Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the PHAST-12N is a write transfer. **Motorola MPC860 notation: RD/WR**
MPACK	L1	O(T)	LVCMOS 24mA	**Transfer Acknowledge (Active Low):** This active low lead is used to acknowledge a host processor access. It is synchronous to the MPCLK. To acknowledge an access, MPACK is asserted during 1 MPCLK cycle. For a write access, an acknowledge indicates that data is written to the addressed memory location. For a read access, an acknowledge indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola MPC860 notation: TA**
MPINTR	B3	O	LVCMOS 8mA	**Interrupt:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL. Note: MPC860 expects active low interrupt, requiring MPINTLEVEL to be low.

MOTOROLA MPC8260 LOCAL BUS - HOST PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola MPC8260 Notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Local Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12N for a read or write cycle. MPA13 is the most significant bit in the location's address. **Motorola MPC8260 Notation: L_A[ ]**

Symbol	Lead No.	I/O/P	Type	Name/Function
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Local Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12N and the host processor. MPD15 is the most significant bit. **Motorola MPC8260 Notation: LCL_D[ ]**
MPSEL	K1	I	LVTTL	**PHAST-12N Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12N through a read or write cycle. **Motorola MPC8260 notation: CS**
MPTS	L3	I	LVTTL	**Not Applicable Input:** This lead must be tied to VSS.
MPWR	L2	I	LVTTL	**Local Bus Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the PHAST-12N is a write transfer. **Motorola MPC8260 notation: LWR**
MPACK	L1	O(T)	LVCMOS 24mA	**Local Bus GPCM Transfer Acknowledge (Active Low):** This lead is used to acknowledge a host processor access. It is synchronous to the MPCLK. To acknowledge an access, MPACK is asserted during 1 MPCLK cycle and then de-asserted during 3 MPCLK cycles before going in tristate. For a write access, an acknowledge indicates that data is written to the addressed memory location. For a read access, an acknowledge indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola MPC8260 notation: LGTA**
MPINTR	B3	O	LVCMOS 8mA	**Interrupt:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL. Note: MPC8260 Local Bus expects active low interrupt, requiring MPINTLEVEL to be low.

BOUNDARY SCAN

Symbol	Lead No.	I/O/P	Type	Name/Function
TCK	A3	I	LVTTLp	**Test Boundary Scan Clock:** This signal is used to shift data into TDI on its rising edge and out of TDO on its falling edge. The maximum clock frequency is 10 MHz.
TDI	D6	I	LVTTLp	**Test Boundary Scan Data Input:** Serial test instructions and data are clocked into this lead on the rising edge of TCK. This lead has an internal pull-up resistor.
TDO	C5	O(T)	LVCMOS 4mA	**Test Boundary Scan Data Output:** Serial test instructions and data are clocked onto this lead on the falling edge of TCK. When inactive, this lead goes into a high impedance state.
TMS	B4	I	LVTTLp	**Test Boundary Scan Mode Select:** This input lead is sampled on the rising edge of TCK. It is used to place the Test Access Port controller into various states, as defined in [IEEE 1149.1]. This lead has an internal pull-up resistor.
TRS	B5	I	LVTTLp	**Test Boundary Scan Reset:** An active low signal that asynchronously resets the Test Access Port controller. The reset must be present for a minimum of 250 ns. This lead has an internal pull-up resistor and must be tied to VSS for normal operation.

SDH/SONET RECEIVE BYPASS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
BYPRXCLK	W5	I	LVTTL	**Receive Line Bypass Clock:** For TranSwitch testing purposes. This lead must be tied to VSS.
BYPRXSEQ	AA2	I	LVTTL	**Receive Line Bypass Sequence:** For TranSwitch testing purposes. This lead must be tied to VSS.
BYPRXDATA07 BYPRXDATA06 BYPRXDATA05 BYPRXDATA04 BYPRXDATA03 BYPRXDATA02 BYPRXDATA01 BYPRXDATA00	Y4 AA3 Y3 Y2 W3 V4 AA1 W2	I	LVTTL	**Receive Line Bypass Data:** For TranSwitch testing purposes. These leads must be tied to VSS.

SDH/SONET TRANSMIT BYPASS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
BYPTXCLK	AB5	I	LVTTL	**Transmit Line Bypass Clock:** For TranSwitch testing purposes. This lead must be tied to VSS.
BYPTXC1	AB4	O	LVCMOS 8mA	**Transmit Line Bypass C1 Indication:** For TranSwitch testing purposes. This lead must be left unconnected.
BYPTXDATA07 BYPTXDATA06 BYPTXDATA05 BYPTXDATA04 BYPTXDATA03 BYPTXDATA02 BYPTXDATA01 BYPTXDATA00	W7 Y6 AA5 AB3 W6 Y5 AA4 AB2	O	LVCMOS 8mA	**Transmit Line Bypass Data:** For TranSwitch testing purposes. These leads must be left unconnected.

TEST

Symbol	Lead No.	I/O/P	Type	Name/Function
DEVHIGHZ	C4	I	LVTTLd	**Device High-Z:** For TranSwitch testing purposes. All LVCMOS outputs and all bi-dirs are tristated when this lead is high. This lead must be tied to VSS.
TEST1	C3	I	LVTTLd	**TEST1:** For TranSwitch testing purposes. This lead must be tied to VSS.
PLLBYPASS	A5	I	LVTTLd	**PLL Bypass:** For TranSwitch testing purposes. This lead must be tied to VSS.
SCANEN	D7	I	LVTTLd	**Scan Enable:** For TranSwitch testing purposes. This lead must be tied to VSS.
SCANMODE	C6	I	LVTTLd	**Scan Mode:** For TranSwitch testing purposes. This lead must be tied to VSS.

7.0 SELECTED PARAMETER VALUES

7.1 ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	V_{DD1}	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	V_{DD2}	-0.3	3.9	V	Notes 1, 4
DC input voltage	VIN	-0.5	5.5	V	Notes 1, 4, 5
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per IPC/JEDEC J-STD-020C
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114C.01.
4. Device core is 1.8V only.
5. All LVDS and LVPECL inputs, LINERXCAP and LINETXCAP are excluded.

7.2 THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		14.7		^{0}C/W	0 ft/min linear airflow

7.3 POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
VDD18	1.71	1.8	1.89	V	
IDD18			490	mA	
VDD18RPA	1.71	1.8	1.89	V	
IDD18RPA			70	mA	
VDD18TPA	1.71	1.8	1.89	V	
IDD18TPA			40	mA	
VDD33	3.15	3.3	3.45	V	
IDD33			80	mA	
VDDA33LVPCDRV	3.15	3.3	3.45	V	
IDDA33LVPCDRV			120	mA	
VDDA33LVPCIO	3.15	3.3	3.45	V	
IDDA33LVPCIO			7	mA	
VREF	1.14	1.2	1.26	V	
IREF			10	uA	
VTERM	1.14	1.2	1.26	V	
ITERM			see text		
P_{TOTAL}	1.4	1.6	1.9	W	See Note 3

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C. Maximum values are based on measurements made at maximum voltages at 85° C.
2. All four line interfaces are operational in STM-1/OC-3 mode, and the APS port is operational.
3. All measurements for the Parameter P_{TOTAL} are preliminary.

7.4 POWER SUPPLY SHARING, FILTERING AND OTHER REQUIREMENTS

VDD33 may be combined with other 3.3V card supplies.

VDDA33LVPCDRV and VDDA33LVPCIO may share a supply, but should each be filtered. VDDA33LVPCDRV must use the same supply as the Tx side of the optical transceiver(s) (also filtered), for LVPECL threshold tracking.

VREF should have an isolated 1.2V supply.

VTERM (optional) should have an isolated 1.2V supply, when used.

All VSS pins may be combined on a strong ground plane with appropriate decoupling.

The following power pins supply I/O ESD structures and must either lead other supplies or be simultaneous with other supplies: VDD33 and VDDA33LVPCIO.

Device inputs may not be driven until the core supplies are up.

The use of VREF is mandatory. It is the reference voltage for the four LVPECL Tx pads (LINETXDATA1P/N, LINETXDATA2P/N, LINETXDATA3P/N, LINETXDATA4P/N) and the LVDS Tx pad (APSTXDATAP/N). In addition, it is used to bias the Rx and Tx PLLs.

The use of VTERM is optional, and in fact not recommended: It serves as the termination voltage for the LVDS Rx pad (APSRXDATAP/N).

VTERM must only be supplied, when the potential difference between the grounds of the two PHAST-12N devices (connected using the APS port) is large and does not meet LVDS standard: [IEEE Std 1596.3-1996]. In this case, the VTERM current can get larger than 20mA. If the grounds are equal, no current will be drawn and VTERM is not needed (can be left floating).

When the APS port is not used, VTERM can be left floating as well.

VDD18 may be combined with other 1.8V card supplies, but should be each filtered.

VDDA18TPA supplies the Tx PLL / Clock Synthesis and Tx LVPECL analog supplies. VDDA18RPA supplies the Rx PLL / Clock Recovery and Rx LVPECL analog supplies. They are the most sensitive supplies in the device. Noise on these supplies result in deteriorated jitter performance at the Line side. The recommendation is to have separate 1.8V supplies for VDDA18TPA and VDDA18RPA, each one carefully filtered. The power supply noise requirement for both VDDA18TPA and VDDA18RPA is 20 mVpp max.

7.5 LVPECL I/O RECOMMENDATIONS:

LVPECL - Line Interfaces:

It is required to provide a pull-up and a pull-down resistor as close as possible to the LINERXDATAxP and LINERXDATAxN (x = 1...4) pins on the PHAST-12N:

- pull-up value (towards +3.3V) = 130 Ω
- pull-down value (towards VSS) = 82 Ω

It is required to provide a pull-up and a pull-down resistor at the LINETXDATAxP and LINETXDATAxN (x = 1...4) pins on the PHAST-12N:

- pull-up value (towards +3.3V) = 130 Ω
- pull-down value (towards VSS) = 82 Ω

The placement of these resistors should be near the PHAST-12N in AC coupled mode and near the optical transceiver in DC coupled mode.

Provide optional 0.1 µF series capacitors on all P and N lines between the PHAST-12N and each optical transceiver. This allows for both AC- and DC-coupling: 0 Ω resistors can be mounted in case of DC coupling.

At the optical transceiver side, one should carefully follow the recommendations in the data sheet of the optical transceiver. This should satisfy most vendors' data sheets:

- Provide pull-up and pull-down resistors as close as possible to the optical transceiver's Rx output, on both P and N (Usually, only pull-down resistors are required).
- Provide pull-up and pull-down resistors as close as possible to the optical transceiver's Tx input, on both P and N.
- Provide a resistor between P and N as close as possible to the optical transceiver's Tx input.
- Provide enough resistors in the schematic. Some of them may not be required, and can be treated as 'do not install'.

LVPECL - Tx Reference Clock:

It is required to provide a pull-up and a pull-down resistor as close as possible to the REFTXCLK2P & REFTXCLK2N pins on the PHAST-12N:

- pull-up value (towards +3.3V) = 130 Ω
- pull-down value (towards VSS) = 82 Ω

One should follow the recommendations in the data sheet of the oscillator.

- Typically, pull-down resistors of approx. 150 Ω on both P and N are required, close to the oscillator outputs.
- Provide enough resistors in the schematic. Some of them may not be required, and can be treated as 'do not install'.

To achieve optimal jitter performance, it is recommended to connect a differential oscillator to REFTXCLK2P/N (LVPECL), instead of a single-ended to REFTXCLK1 (LVTTL).

LVPECL - PCB guidelines:

The differential pairs (P and N) will be routed together, have a controlled impedance of 50 Ω and be the same length. Make them as short as possible and in as straight a path as possible. Vias should be avoided if practicable.

LVPECL - Unused pins:

All unused LVPECL inputs can be left floating (no resistors required).

All unused LVPECL outputs can be left floating (no resistors required).

LVDS I/O RECOMMENDATIONS:

LVDS - APS Port:

The LVDS I/O on the APS Port (APSRXDATAP/N, APSTXDATAP/N) is compliant to the LVDS standard: [IEEE Std 1596.3-1996].

The LVDS receiver (APSRXDATAP/N) has an integrated 100 Ω termination resistor between P and N. It is however recommended to provide a 100 Ω resistor on the board, between APSRXDATAP and APSRXDATAN, as close as possible to the PHAST-12N. This resistor will normally be treated as 'do not install'.

Use DC coupling (no series capacitors).

LVDS - PCB, Connector and Cable guidelines:

The differential pairs (P and N) will be routed together, have a controlled impedance of 50 Ω and be the same length. Make them as short as possible and in as straight a path as possible. Vias should be avoided if practicable.

Use high quality connectors that are qualified for an LVDS signal at 622.08 Mbit/s (311.04 MHz).

The APS Port always operates at this rate. It cannot operate at a lower rate.

When a cable is used to interconnect two PHAST-12N devices using the APS Port, it is mandatory to use a 50 Ω cable. In a careful implementation, cable length can be up to 2 meter.

It is required to have a common ground between the two PHAST-12N devices that are connected using the APS Port.

LVDS - Unused pins:

Unused LVDS inputs can be left floating (no resistors required).

Unused LVDS outputs can be left floating (no resistors required).

8.0 INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

Input/Output Parameters for LVPECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}-V_{oH}	0.99		1.114	V	
V_{DD}-V_{oL}	1.576		1.769	V	
V_{oD}	0.586		0.657	V	
V_{DD}-V_{oS}	1.283		1.44	V	
V_{iD}	0.2		**TBD**	V	
V_{iS}	1.525		2.4	V	

Notes:

a. V_{DD} is VDDA33LVPCDRV.

b. V_{oD} = Tx output differential voltage

c. V_{oS} = Tx output offset voltage

d. V_{iD} = Rx input differential voltage

e. V_{iS} = Rx input offset voltage

Input/Output Parameters for LVDS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{oH}			1.475	V	
V_{oL}	0.925			V	
V_{oD}	0.25		0.4	V	
V_{oS}	1.125		1.275	V	
R_o	40		140	Ohm	
V_i	0		1.8	V	
V_{tH}	.1			V	Differential Threshold, High
V_{tL}	-.1			V	Differential Threshold, Low
R_{iN}	80		120	Ohm	

Input Parameters for LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \le V_{DD33} \le 3.46$
V_{IL}			0.8	V	$3.14 \le V_{DD33} \le 3.46$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

Input Parameters for LVTTLpu (Internal Pull-Up Resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \le V_{DD33} \le 3.46$
V_{IL}			0.8	V	$3.14 \le V_{DD33} \le 3.46$
Input current	-90		-25	µA	$V_{IN} = V_{SS}$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$
Input capacitance		5		pF	

Input Parameters for LVTTLpd (Internal Pull-Down Resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \le V_{DD33} \le 3.46$
V_{IL}			0.8	V	$3.14 \le V_{DD33} \le 3.46$
Input current	28		85	µA	$V_{IN} = V_{DD33}$
Input leakage current	-10		10	µA	$V_{IN} = V_{SS}$
Input capacitance		5		pF	

Output Parameters for LVCMOS 24mA (Open Drain)

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		30		pF	
V_{OH}	2.4			V	$V_{DD33} = 3.15$; $I_{OH} = -24$
V_{OL}			0.4	V	$V_{DD33} = 3.15$; $I_{OL} = 24$
I_{OL}		24		mA	
I_{OH}		-24		mA	
t_{RISE}	1.17		2.25	ns	$C_{LOAD} = 30$ pF
t_{FALL}	0.87		1.77	ns	$C_{LOAD} = 30$ pF
Leakage tristate			±15	µA	0 to 3 V input

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to V_{DD33}.

Output Parameters for LVCMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		**TBD**		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -8
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 8
I_{OL}	8			mA	
I_{OH}	-8			mA	
t_{RISE}	1.78		3.38	ns	C_{LOAD} = 30 pF
t_{FALL}	1.65		3.22	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

Output Parameters for LVCMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -4
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 4
I_{OL}	4			mA	
I_{OH}	-4			mA	
t_{RISE}	2.97		5.54	ns	C_{LOAD} = 30 pF
t_{FALL}	2.95		5.66	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input
Output capacitance		5		pF	

Output Parameters for LVCMOS 16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -16
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 16
I_{OL}	16			mA	
I_{OH}	-16			mA	
t_{RISE}	1.28		2.87	ns	C_{LOAD} = 30 pF
t_{FALL}	1.04		2.65	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to V_{DD33}.

Input/Output Parameters for LVTTL/CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \le V_{DD33} \le 3.46$
V_{IL}			0.8	V	$3.14 \le V_{DD33} \le 3.46$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33}= 3.14; $I_{OH = -8 mA}$
V_{OL}			0.4	V	V_{DD33}= 3.14; $I_{OL = 8 mA}$
I_{OL}	8.0			mA	
I_{OH}	-8.0			mA	

Input/Output Parameters for LVTTL Input and LV3CMOS Output 16mA (3.3V Volt Tolerant Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD33} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD33} \le 3.45$
Input leakage current			±15	µA	0 to 3.3 V input
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33} = 3.15$; $I_{OH} = -16$
V_{OL}			0.4	V	$V_{DD33} = 3.15$; $I_{OL} = 16$
I_{OL}	16			mA	
I_{OH}	-16			mA	
t_{RISE}	1.76		2.85	ns	$C_{LOAD} = 25$ pF
t_{FALL}	1.60		2.64	ns	$C_{LOAD} = 25$ pF

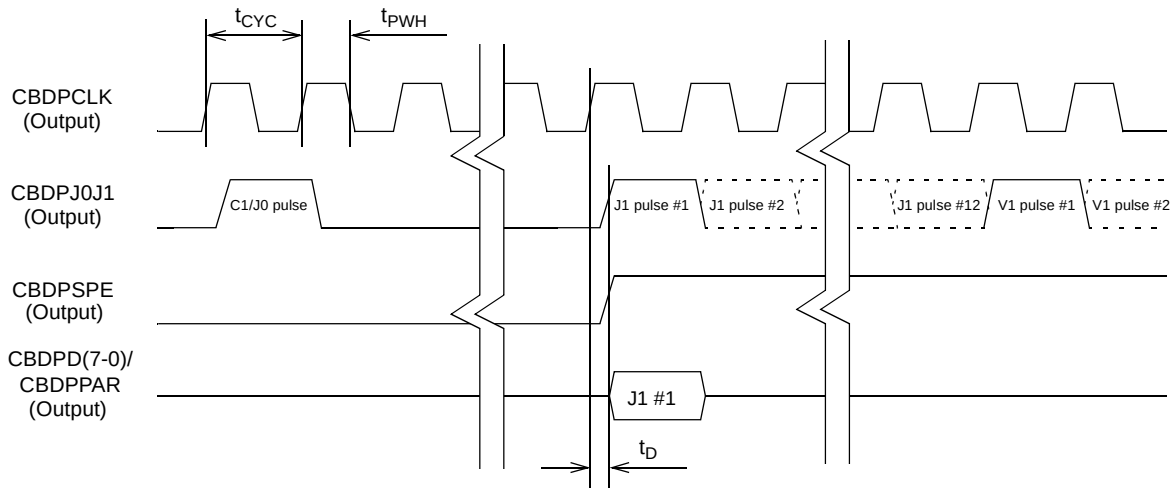
Input/Output Parameters for LVTTL Input and LV3CMOS Output 8mA (3.3V Volt Tolerant Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD33} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD33} \le 3.45$
Input leakage current			±15	µA	0 to 3.3 V input
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33} = 3.15$; $I_{OH} = -8$
V_{OL}			0.4	V	$V_{DD33} = 3.15$; $I_{OL} = 8$
I_{OL}	8			mA	
I_{OH}	-8			mA	
t_{RISE}	1.80		3.39	ns	$C_{LOAD} = 25$ pF
t_{FALL}	1.78		3.36	ns	$C_{LOAD} = 25$ pF

9.0 TIMING CHARACTERISTICS

Detailed timing diagrams for the PHAST-12N device are illustrated in Figure 5 through Figure 26 with values of the timing parameters tabulated below each waveform diagram. All outputs are measured with a maximum load capacitance of 50 pF unless otherwise stated. Timing parameters are measured at the voltage levels of $(V_{OH} + V_{OL})/2$ for output signals and $(V_{IH} + V_{IL})/2$ for input signals.

Figure 5. DROP Bus Timing



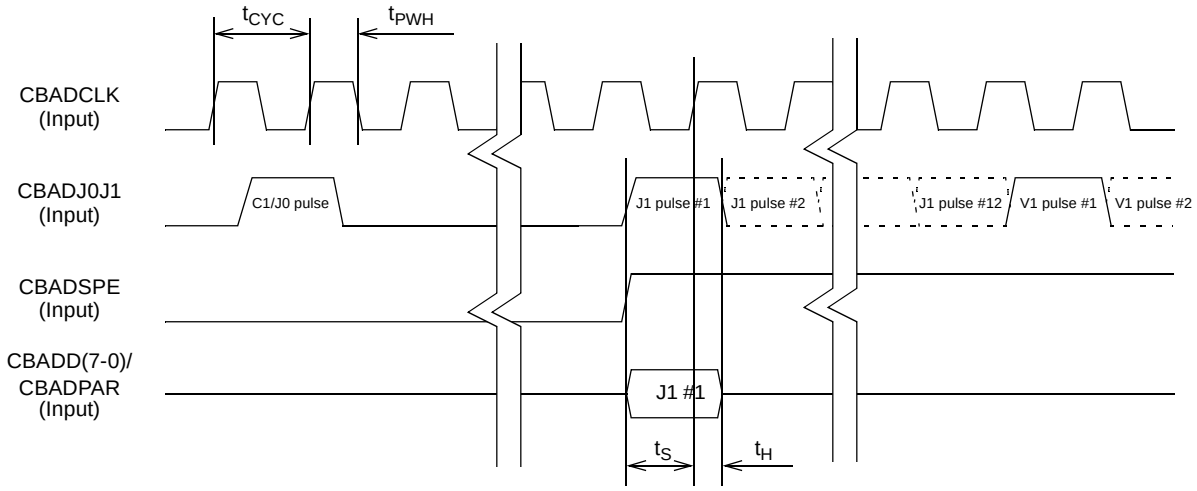
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
CBDPCLK clock period	t_{CYC}		12.86		ns
CBDPCLK duty cycle	t_{PWH}	40	50	60	$\%t_{CYC}$
CBDPD(7-0)/CBDPPAR/CBDPC0J1/CBDPSPE out valid delay from DCLK↑	t_D	1		6	ns

Notes:

1. The optional V1 pulse only occurs during the first frame of the low order multi-frame as indicated by the H4 byte. It is **always** located twelve clock cycles after the corresponding J1 pulse.
2. The active CBDPCLK clock edge on which the data/parity and timing signals are clocked out can be selected, see "Drop Bus Interface" on page 131. The waveforms shown correspond to the positive clock edge selection.
3. An additional delay of 0 up to 15 extra CBDPCLK clock cycles can be inserted between the Drop bus data/parity and the Drop bus timing signals, CBDPJ0J1 and CBDPSPE, see "Drop Bus Delay" on page 132. The waveforms shown correspond to a delay of 0 clock cycles.

Figure 6. Add Bus Timing (ADD Slave Mode: Timing Signals Are Inputs)



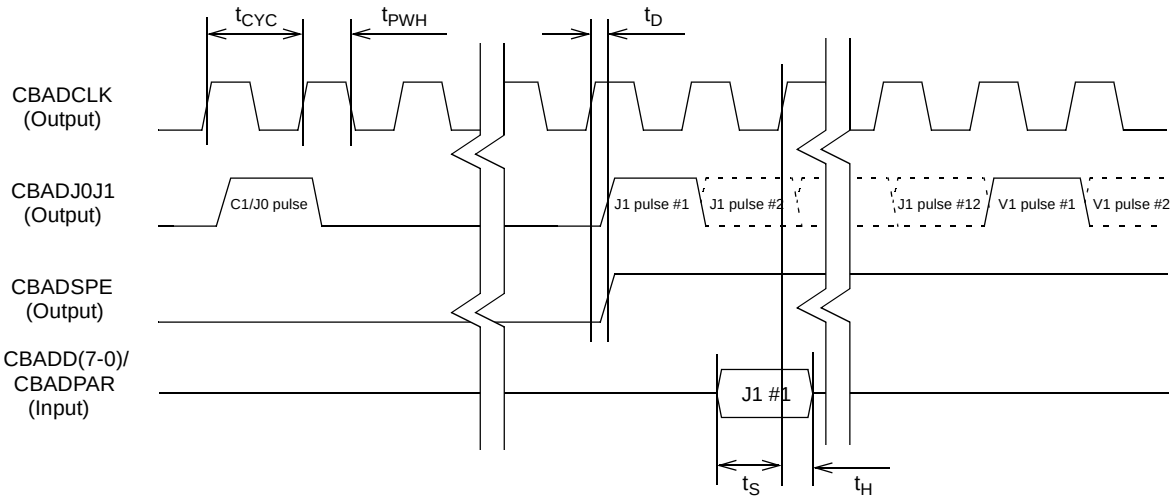
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
CBADCLK clock period	t_{CYC}		12.86		ns
CBADCLK duty cycle	t_{PWH}	40	50	60	$\%t_{CYC}$
CBADJ0J1/CBADSPE/CBADD(7-0)/CBADPAR setup time to CBADCLK↑	t_S	3			ns
CBADJ0J1/CBADSPE/CBADD(7-0)/CBADPAR hold time after CBADCLK↑	t_H	0			ns

Notes:

1. The optional V1 pulse only occurs during the first frame of the low order multi-frame as indicated by the H4 byte. It is **always** located twelve clock cycles after the corresponding J1 pulse.
2. The CBADCLK clock edge on which the data/parity and timing signals are clocked in can be selected, see "Add Bus Interface" on page 132. The waveforms shown correspond to the positive clock edge selection.
3. An additional delay of 0 up to 15 extra CBADCLK clock cycles can be inserted between the Add bus timing signals, CBADJ0J1 and CBADSPE, and the Add bus data/parity, see "Add Bus Delay" on page 134. The waveforms shown correspond to a delay of 0 clock cycles.

Figure 7. ADD Bus Timing (ADD Master Mode: Timing Signals Are Outputs)



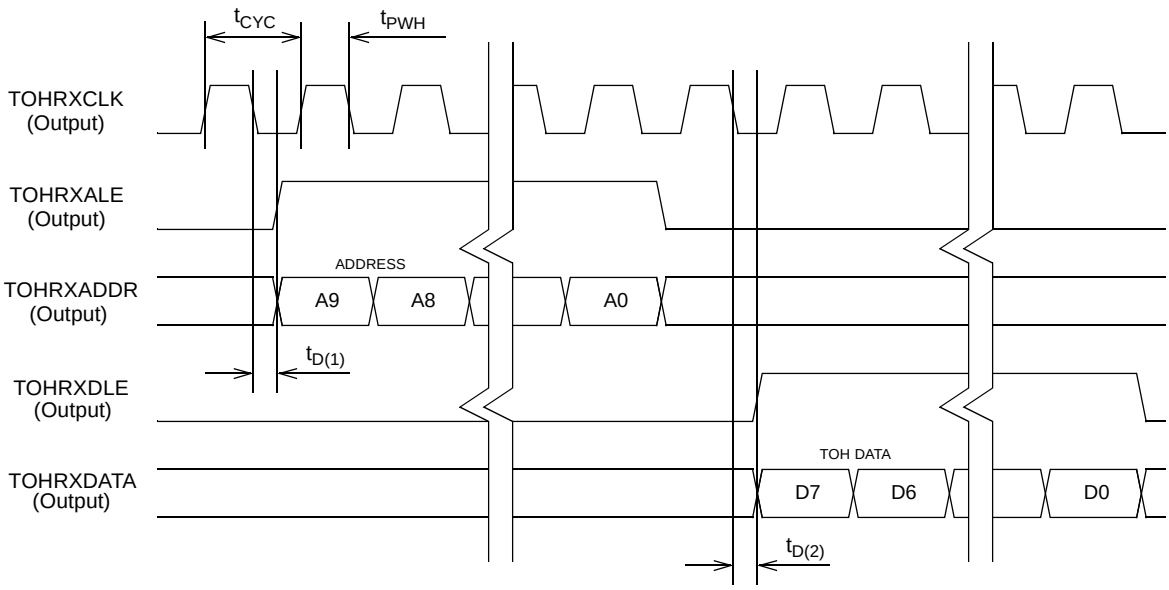
50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
CBADCLK clock period	t_{CYC}		12.86		ns
CBADCLK duty cycle	t_{PWH}	40	50	60	$\%t_{CYC}$
CBADD(7-0)/CBADPAR setup time before CBADCLK↑	t_S	5			ns
CBADD(7-0)/CBADPAR hold time after CBADCLK↑	t_H	0			ns
CBADJ0J1/CBADSPE out valid delay from CBADCLK↑	t_D	1		6	ns

Notes:

1. The optional V1 pulse only occurs during the first frame of the low order multi-frame as indicated by the H4 byte. It is **always** located twelve clock cycles after the corresponding J1 pulse.
2. The CBADCLK clock edge on which the data/parity signals are clocked in can be selected, see "Add Bus Interface" on page 132. The waveforms shown correspond to the positive clock edge selection.
3. The active CBADCLK clock edge on which the timing signals are clocked out can be selected, see "Add Bus Interface" on page 132. The waveforms shown correspond to the positive clock edge selection.
4. An additional delay of 0 up to 15 extra CBADCLK clock cycles can be inserted between the Add bus timing signals, CBADJ0J1 and CBADSPE, and the Add bus data/parity, see "Add Bus Delay" on page 134. The waveforms shown correspond to a delay of 1 clock cycle.

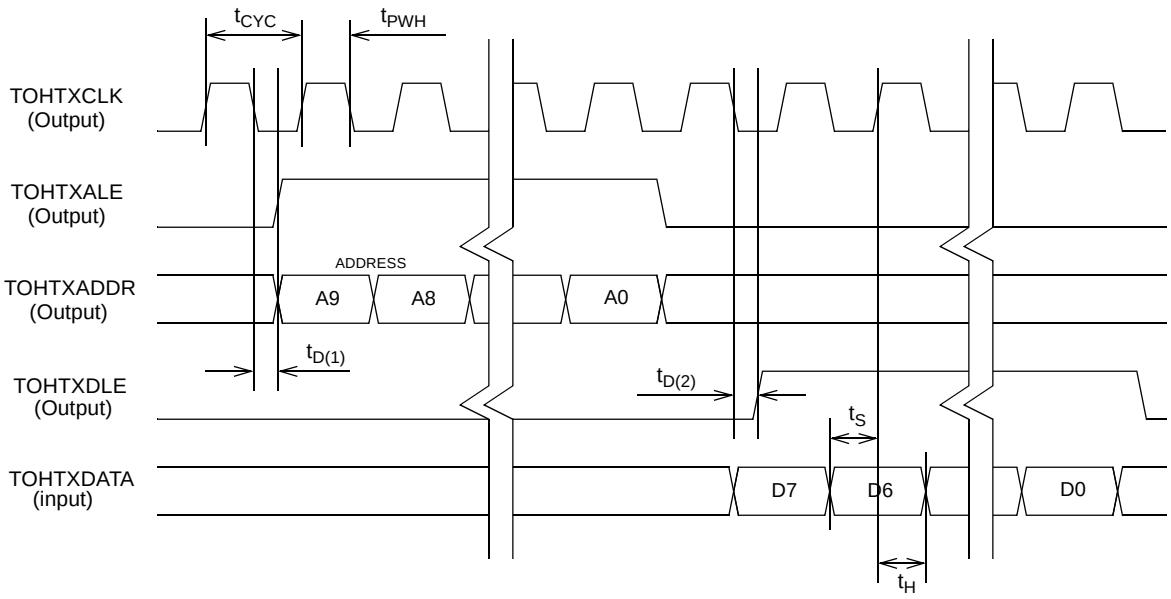
Figure 8. RX TOH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
TOHRXCLK clock period	t_{CYC}		12.86		ns
TOHRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
TOHRXALE/TOHRXADDR out valid delay from TOHRXCLK↓	$t_{D(1)}$	1		4	ns
TOHRXDLE/TOHRXDATA out valid delay from TOHRXCLK↓	$t_{D(2)}$	1		4	ns

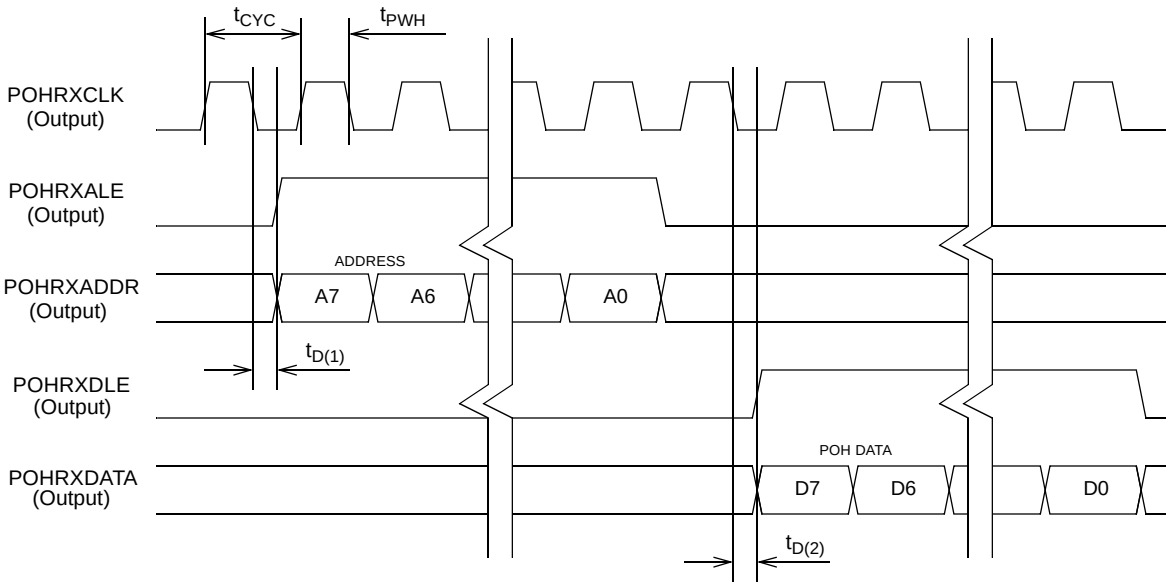
Figure 9. TX TOH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
TOHTXCLK clock period	t_{CYC}		12.86		ns
TOHTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
TOHTXALE/TOHTXADDR out valid delay from TOHTXCLK↓	$t_{D(1)}$	1		4	ns
TOHTXDLE out valid delay from TOHTXCLK↓	$t_{D(2)}$	1		4	ns
TOHTXDATA setup time before TOHTXCLK↑	t_S	6			ns
TOHTXDATA hold time after TOHTXCLK↑	t_H	0			ns

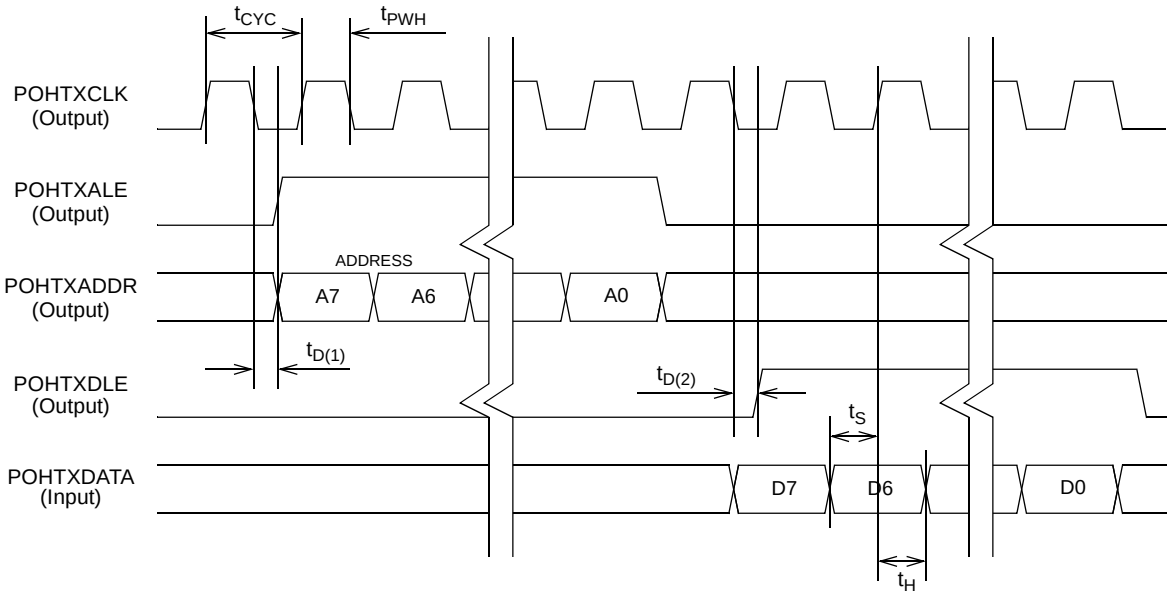
Figure 10. RX High Order POH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHRXCLK clock period	t_{CYC}		12.86		ns
POHRXCLK clock pulse width	t_{PWH}	40	50	60	%t_{CYC}
POHRXALE/POHRXADDR out valid delay from POHRXCLK↓	$t_{D(1)}$	1		4	ns
POHRXDLE/POHRXDATA out valid delay from POHRXCLK↓	$t_{D(2)}$	1		4	ns

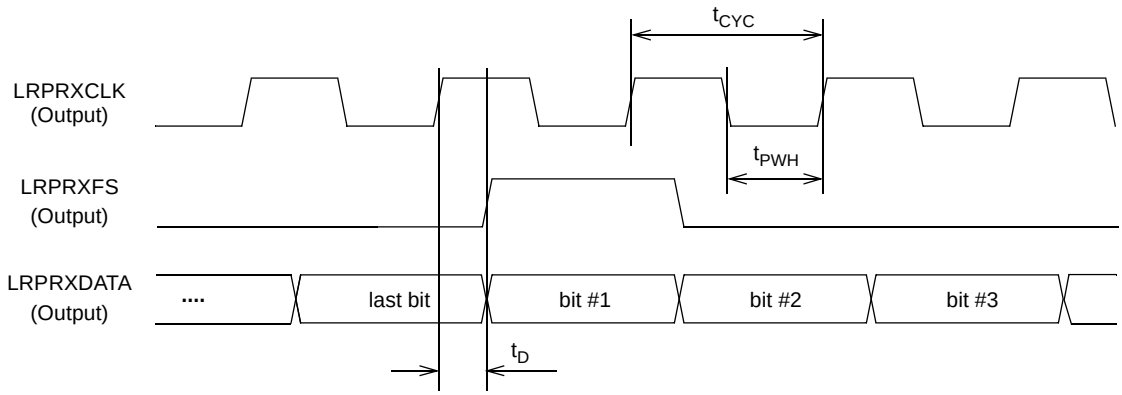
Figure 11. TX High Order POH Byte Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHTXCLK clock period	t_{CYC}		12.86		ns
POHTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
POHTXALE/POHTXADDR out valid delay from POHTXCLK↓	$t_{D(1)}$	1		4	ns
POHTXDLE out valid delay from POHTXCLK↓	$t_{D(2)}$	1		4	ns
POHTXDATA setup time before POHTXCLK↑	t_S	6			ns
POHTXDATA hold time after POHTXCLK↑	t_H	0			ns

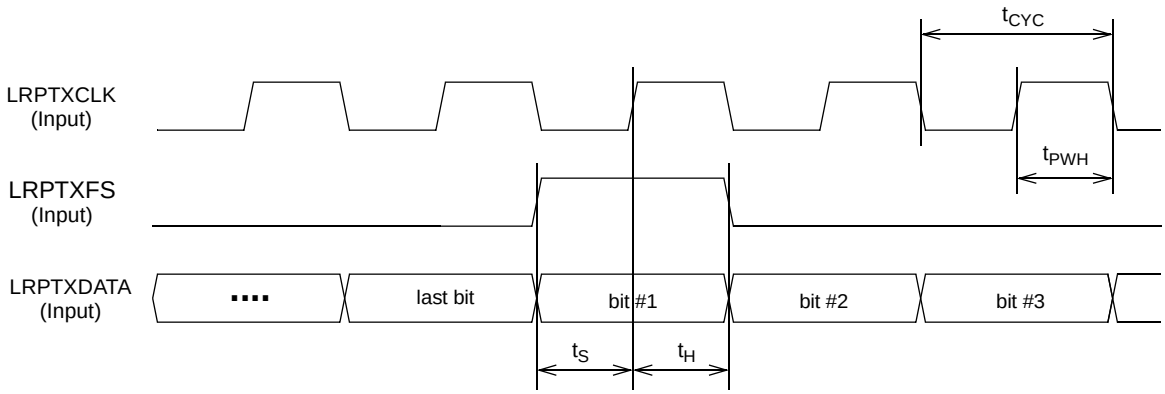
Figure 12. RX Line Ring Port Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
LRPRXCLK clock period	t_{CYC}		51.44		ns
LRPRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
LRPRXFS/LRPRXDATA out valid delay from LRPRXCLK↑	t_D	1		6	ns

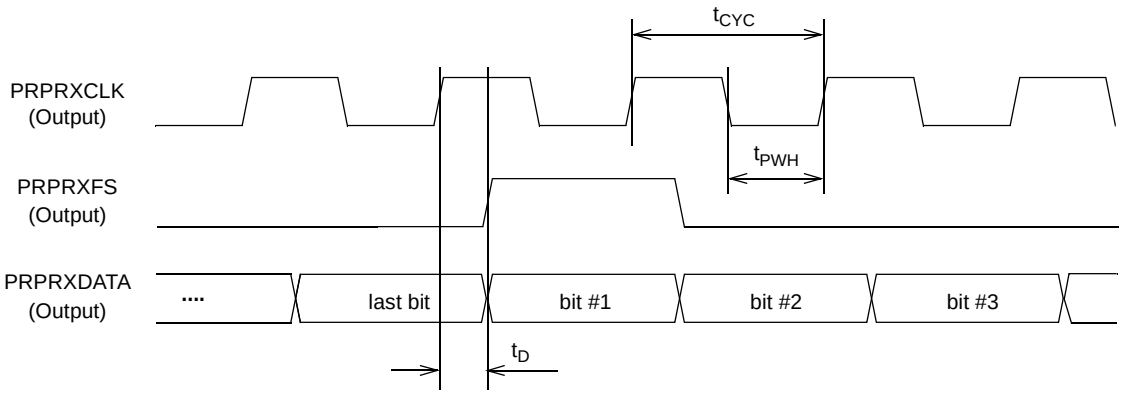
Figure 13. TX Line Ring Port Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
LRPTXCLK clock period	t_{CYC}		51.44		ns
LRPTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
LRPTXFS/LRPTXDATA setup time before LRPTXCLK↑	t_S	30			ns
LRPTXFS/LRPTXDATA hold time after LRPTXCLK↑	t_H	0			ns

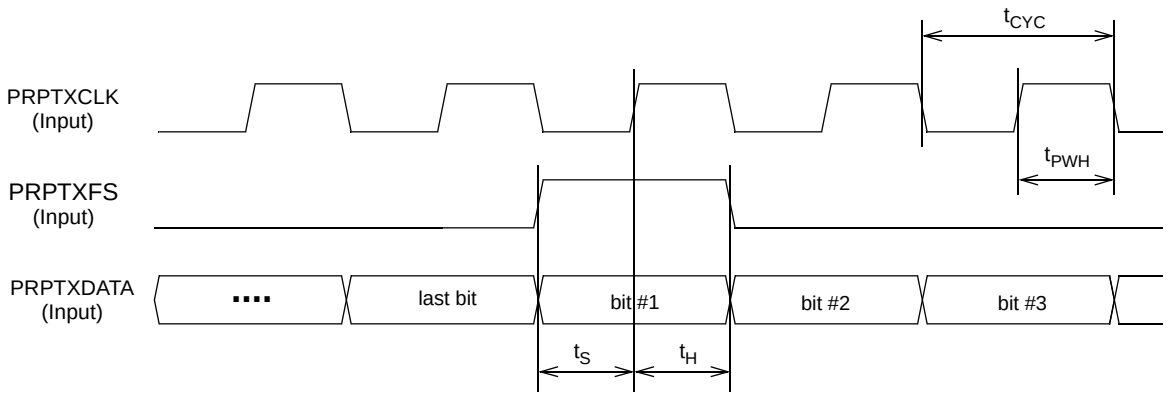
Figure 14. RX Path Alarm Indication Port Interface



50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
PRPRXCLK clock period	t_{CYC}		51.44		ns
PRPRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
PRPRXFS/PRPRXDATA out valid delay from PRPRXCLK↑	t_D	1		6	ns

Figure 15. TX Path Alarm Indication Port Interface

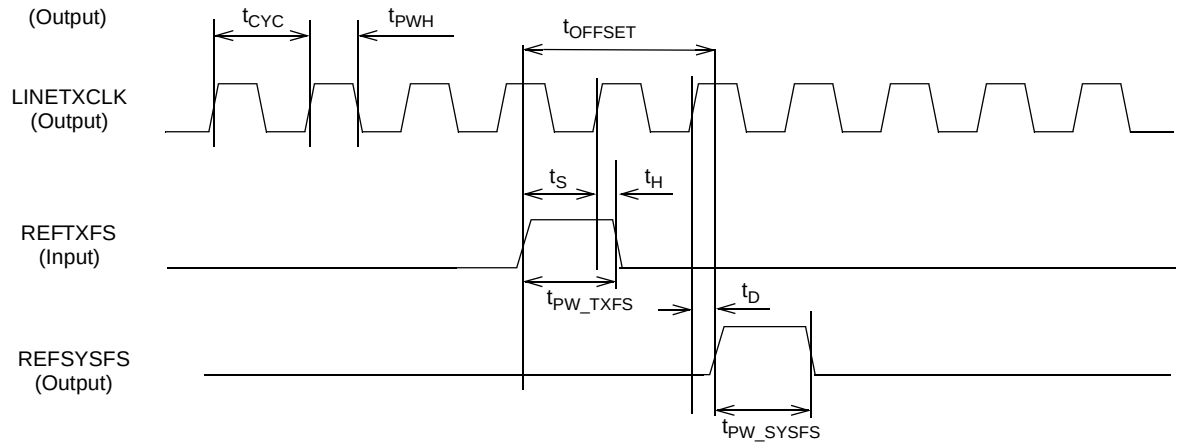


50 pF Load

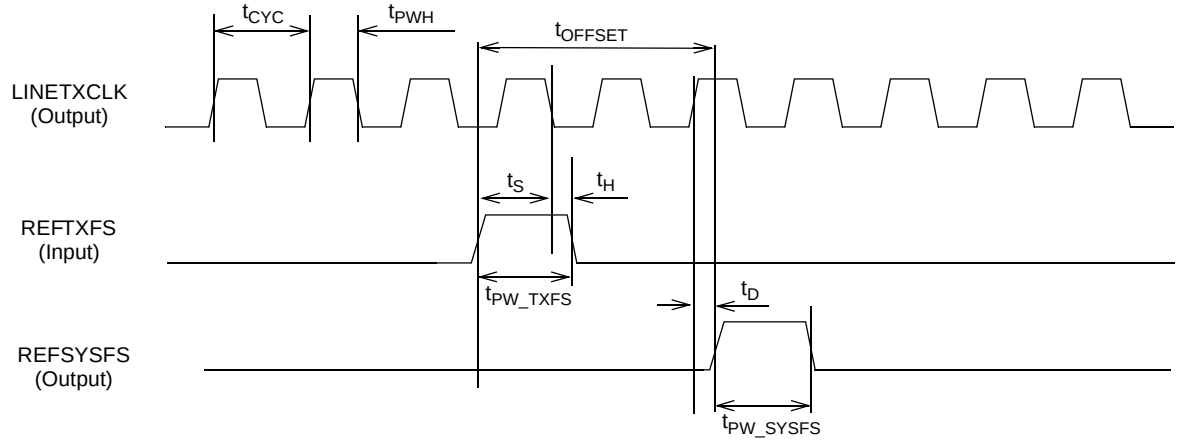
Parameter	Symbol	Min	Typ	Max	Unit
PRPTXCLK clock period	t_{CYC}		51.44		ns
PRPTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
PRPTXFS/PRPTXDATA setup time before PRPTXCLK↑	t_S	35			ns
PRPTXFS/PRPTXDATA hold time after PRPTXCLK↑	t_H	0			ns

Figure 16. Relationship Between the External Frame Reference Pulse (REFTXFS) and the Generated Internal Frame Reference Pulse (REFSYSFS)

a. REFTXFS synchronous to rising edge of LINETXCLK (at 77.76 MHz)



b. REFTXFS synchronous to falling edge of LINETXCLK (at 77.76 MHz)

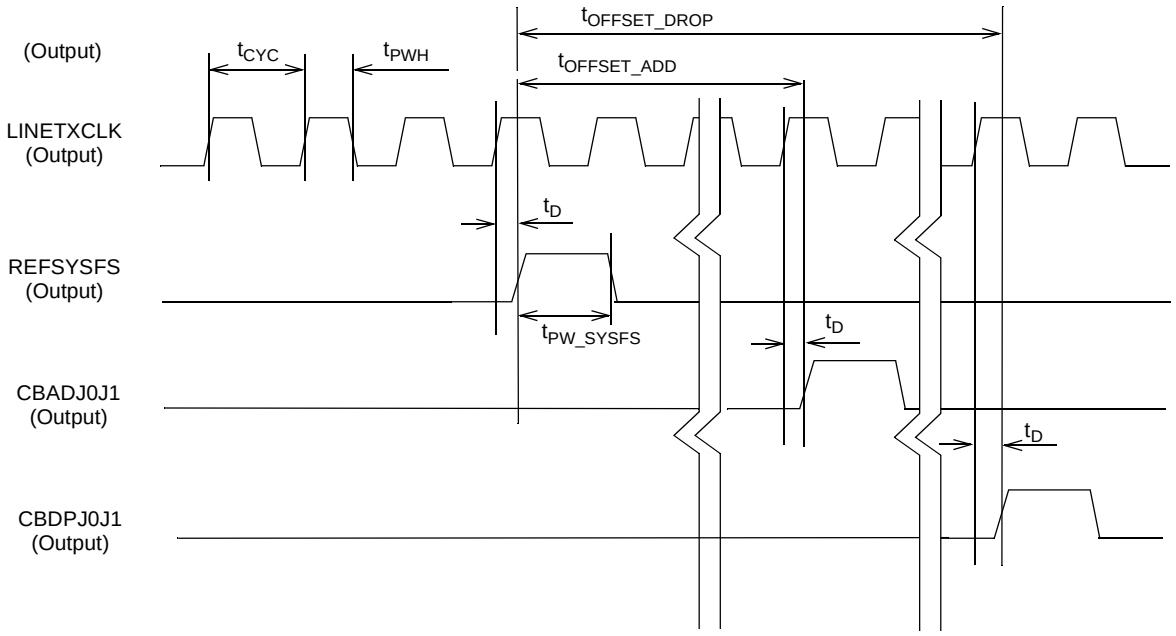


Parameter	Symbol	Min	Typ	Max	Unit
LINETXCLK	t_{CYC}		12.86		ns
LINETXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
REFTXFS pulse width	t_{PW_TXFS}	12.86			ns
REFSYSFS pulse width	t_{PW_SYSFS}		12.86	12.86	ns
REFTXFS synchronous to LINETXCLK↑ (at 77.76 MHz): offset between REFTXFS↑ and REFSYSFS↑	t_{OFFSET}		2		t_{CYC}
REFTXFS synchronous to LINETXCLK↓ (at 77.76 MHz): offset between REFTXFS↑ and REFSYSFS↑	t_{OFFSET}	1.5	2.5		t_{CYC}

Notes:

1. The relationship between the External Frame Reference pulse input (REFTXFS lead) and System Frame Reference Pulse is only useful when LINETXCLK is configured to 77.76 MHz. Because of this the period of LINETXCLK used in the timing diagrams above is 12.86 ns.
2. An additional offset of 0 to 9719 clock cycles (77.76 MHz clock) can be inserted between REFTXFS and REFSYSFS by configuring **ExtFramePulseOffset**, see "Locking on External Frame Reference Pulse" on page 113. The waveforms shown correspond to a delay of 0 clock cycles
3. The External Frame Reference Pulse input (REFTXFS lead) can be sampled at both positive or negative clock edge of LINETXCLK (when at 77.76 MHz). The sample edge is configured by setting **ExtFramePulseNegEdge**, see "Retimer Common Configuration (T_RT_Common_Config)" on page 173. when REFTXFS is synchronous to the rising edge of LINETXCLK, the offset between REFTXFS and REFSYSFS is always equal to (2 + ExtFramePulseOffset) clock cycles (77.76 MHz clock), independent from the value of ExtFramePulseNegEdge. When REFTXFS is synchronous to the falling edge of LINETXCLK, the offset between REFTXFS and REFSYSFS is equal to (1.5 + ExtFramePulseOffset) clock cycles when ExtFramePulseNegEdge = 0, and (2.5 + ExtFramePulseOffset) clock cycles (77.76 MHz) when ExtFramePulseNegEdge = 1.

Figure 17. Relationship Between REFSYSFS, Add and Drop Telecom Bus Timing Signals

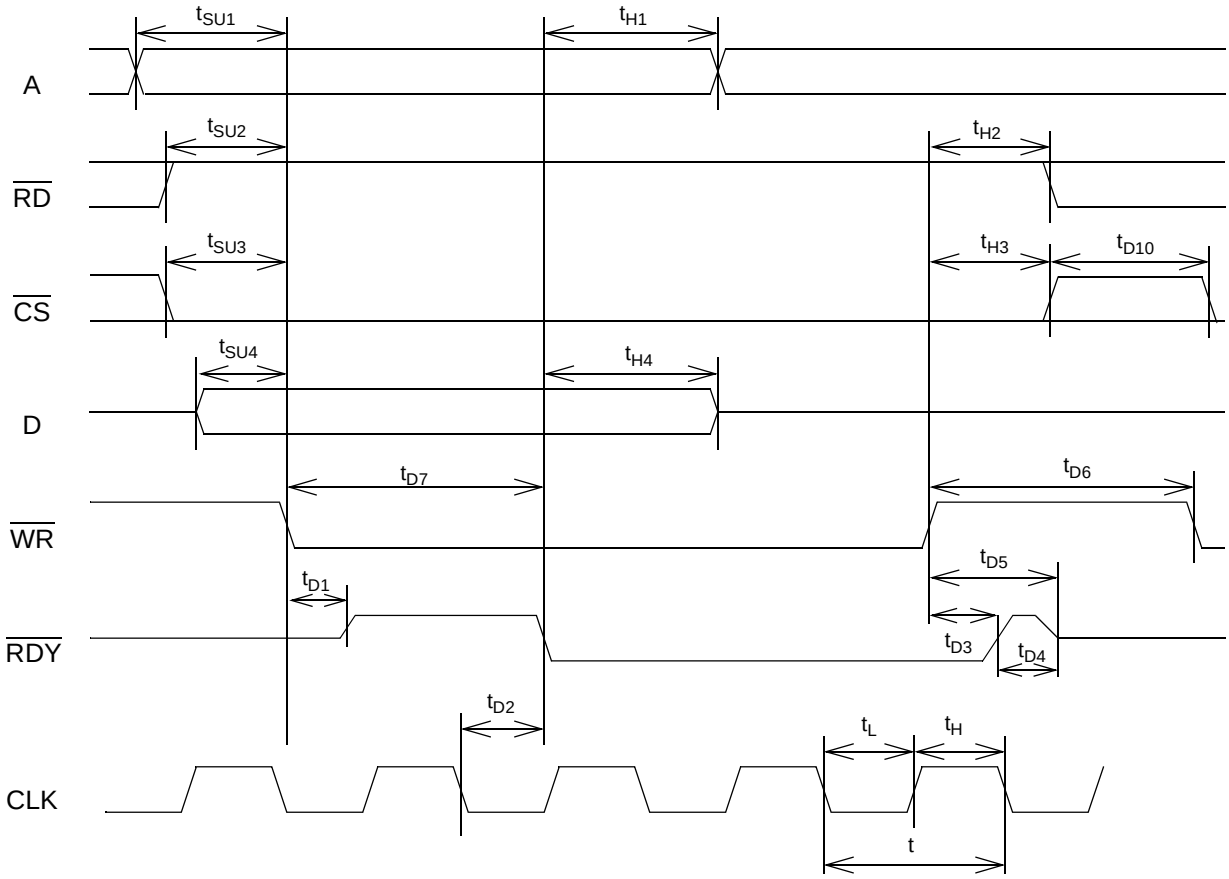


Parameter	Symbol	Min	Typ	Max	Unit
LINETXCLK	t_{CYC}		12.86		ns
LINETXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
REFSYSFS pulse width	t_{PW_SYSFS}		12.86	12.86	ns
REFSYSFS↑ to CBADJ0J1↑	t_{OFFSET_ADD}	7	22	22	t_{CYC}
REFSYSFS↑ to CBDPJ0J1↑	t_{OFFSET_DROP}		26		t_{CYC}

Notes:

1. The relationship represented between CBADJ0J1 and REFSYSFS is only valid for the Add Telecom Bus operating in master mode.
2. For the Add Telecom Bus, an additional delay of 0 up to 15 clock cycles (see also Figure 7) can be inserted between the Add Bus Timing and Add Bus Data/Parity signals (see also "Add Bus Delay" on page 134). When TimingDelay = 0, t_{OFFSET_ADD} = 22, when TimingDelay = 15, t_{OFFSET_ADD} = 7.

Figure 18. Microprocessor Interface: Generic Intel Mode Write Cycle[1]



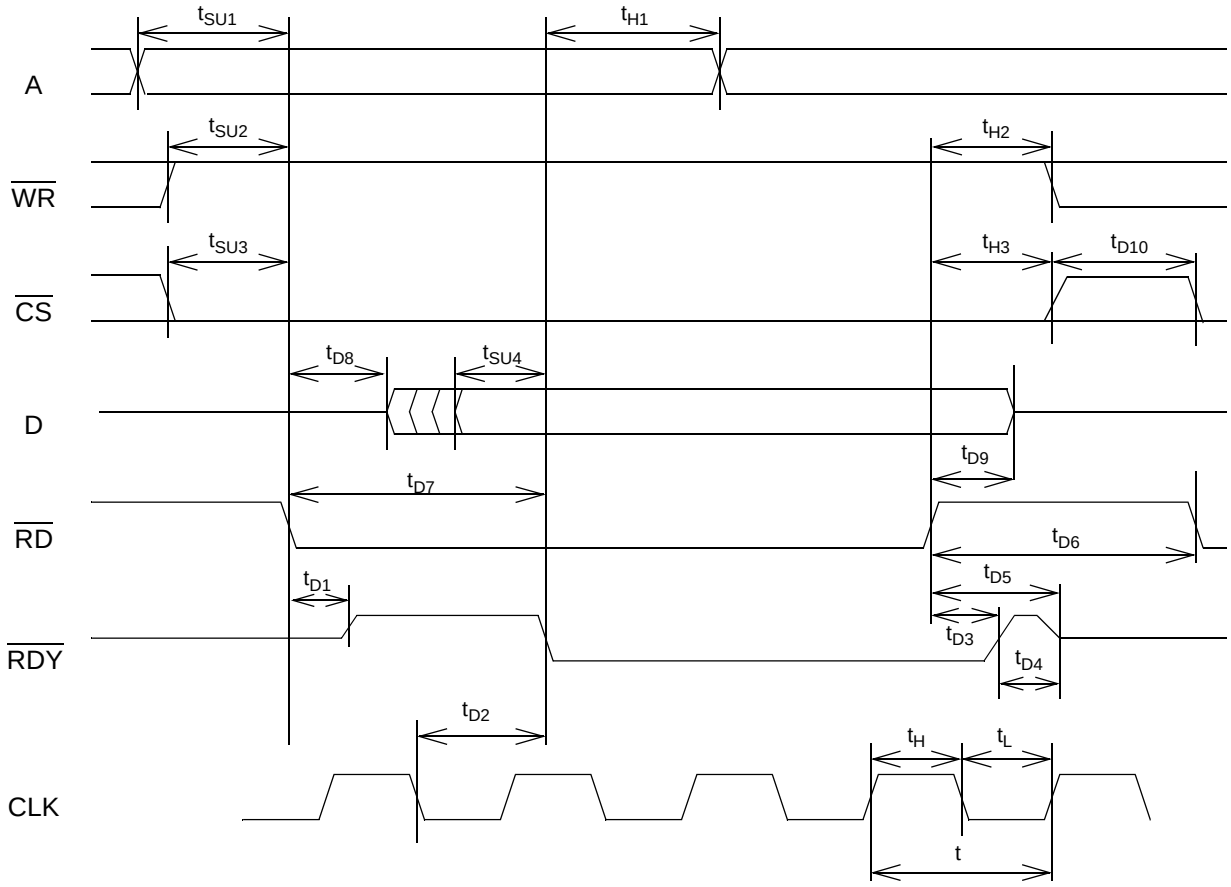
Note: MPACK ($\overline{RDY}$) is shown active low. This corresponds to MPACKLEVEL being tied low.

1. See the Lead Descriptions table on Generic Intel - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{WR}$
t_{SU2}[a]	0 ns	-	Setup time of $\overline{RD}$ to falling edge $\overline{WR}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{WR}$
t_{SU4}	-0.9t	-	Setup time of D to falling edge $\overline{WR}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{RDY}$
t_{H2}[c]	t	-	Hold time of $\overline{RD}$ to rising edge $\overline{WR}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{WR}$
t_{H4}	0 ns	-	Hold time of D to active edge $\overline{RDY}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{WR}$ to $\overline{RDY}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{RDY}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{WR}$ to inactive edge $\overline{RDY}$
t_{D4}	4 ns	-	Delay from $\overline{RDY}$ going inactive to $\overline{RDY}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{WR}$ to $\overline{RDY}$ going in tristate
t_{D6}	t	-	$\overline{WR}$ inactive pulse width
t_{D7}	TBD	TBD	Response latency
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. $\overline{CS}$ applies if a write access is preceded by a read access.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a write access is followed by a read access.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{WR}$ are defined. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals.

Figure 19. Microprocessor Interface: Generic Intel Mode Read Cycle[1]



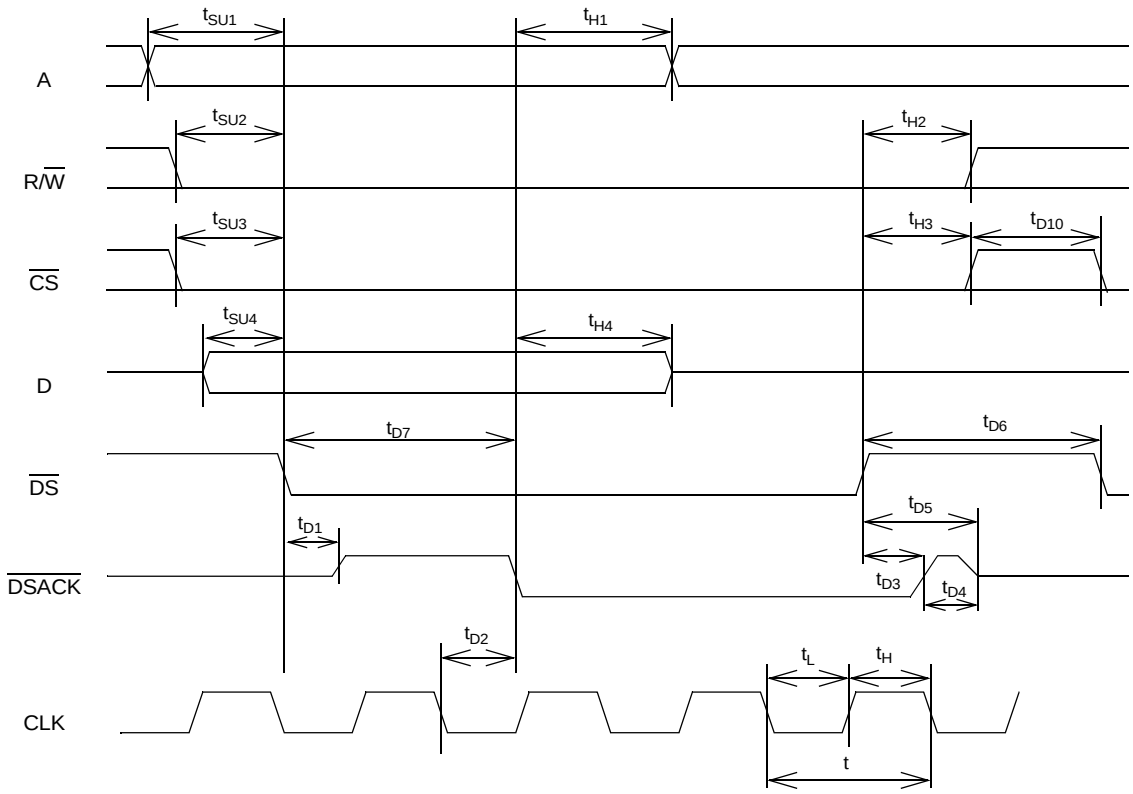
Note: MPACK ($\overline{RDY}$) is shown active low. This corresponds to MPACKLEVEL being tied low.

1. See the Lead Description table on Generic Intel - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{RD}$
t_{SU2}[a]	0 ns	-	Setup time of $\overline{WR}$ to falling edge $\overline{RD}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{RD}$
t_{SU4}	0.7t	-	Setup time of D to active edge $\overline{RDY}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{RDY}$
t_{H2}[c]	t	-	Hold time of $\overline{WR}$ to rising edge $\overline{RD}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{RD}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{RD}$ to $\overline{RDY}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{RDY}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{RD}$ to inactive edge $\overline{RDY}$
t_{D4}	4 ns	-	Delay from $\overline{RDY}$ going inactive to $\overline{RDY}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{RD}$ to $\overline{RDY}$ going in tristate
t_{D6}	t	-	$\overline{RD}$ inactive pulse width
t_{D7}	TBD	TBD	Response latency
t_{D8}	0 ns	12 ns	Delay from falling edge $\overline{RD}$ to D driving
t_{D9}	0 ns	12 ns	Delay from rising edge $\overline{RD}$ to D going in tristate
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. Only applies if a read access is preceded by a write access.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a read access is followed by a write access.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{RD}$ are defined. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals.

Figure 20. Microprocessor Interface: Generic Motorola Mode Write Cycle[1]



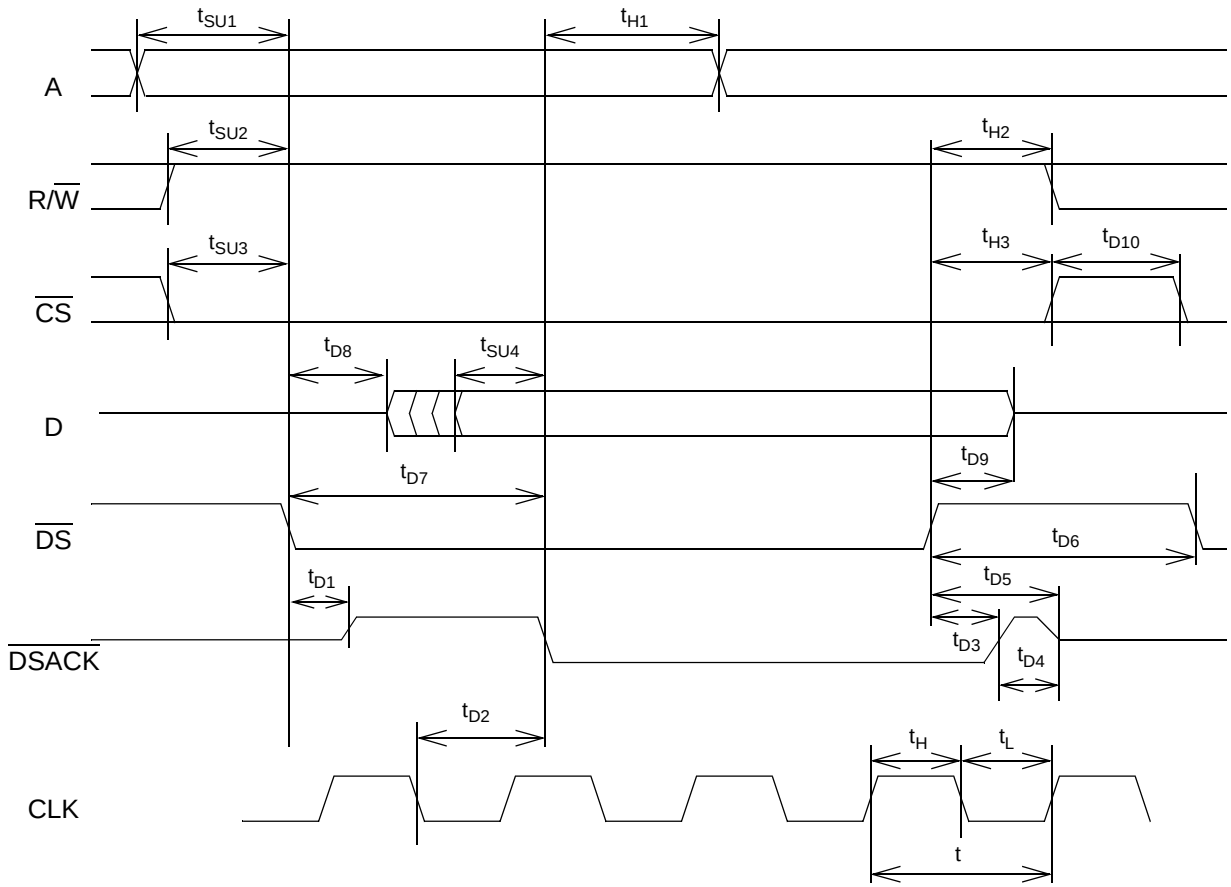
Note: MPACK (DSACK) is shown active low. This corresponds to MPACKLEVEL being tied low.

1. See the Lead Description table on Generic Motorola - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{DS}$
t_{SU2}[a]	0 ns	-	Setup time of R/$\overline{W}$ to falling edge $\overline{DS}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{DS}$
t_{SU4}	-0.9t	-	Setup time of D to falling edge $\overline{DS}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{DSACK}$
t_{H2}[c]	0 ns	-	Hold time of R/$\overline{W}$ to rising edge $\overline{DS}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{DS}$
t_{H4}	0 ns	-	Hold time of D to active edge $\overline{DSACK}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{DS}$ to $\overline{DSACK}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{DSACK}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{DS}$ to inactive edge $\overline{DSACK}$
t_{D4}	4 ns	-	Delay from $\overline{DSACK}$ going inactive to $\overline{DSACK}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{DS}$ to $\overline{DSACK}$ going in tristate
t_{D6}	t	-	$\overline{DS}$ inactive pulse width
t_{D7}	TBD	TBD	Response latency
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. Only applies if a write access is preceded by a read access. R/$\overline{W}$ may stay low between 2 successive write accesses.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a write access is followed by a read access. R/$\overline{W}$ may stay low between 2 successive write accesses.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{DS}$ are defined, since no such relationship is defined in the MC68360 data sheet. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals.

Figure 21. Microprocessor Interface: Generic Motorola Mode Read Cycle[1]



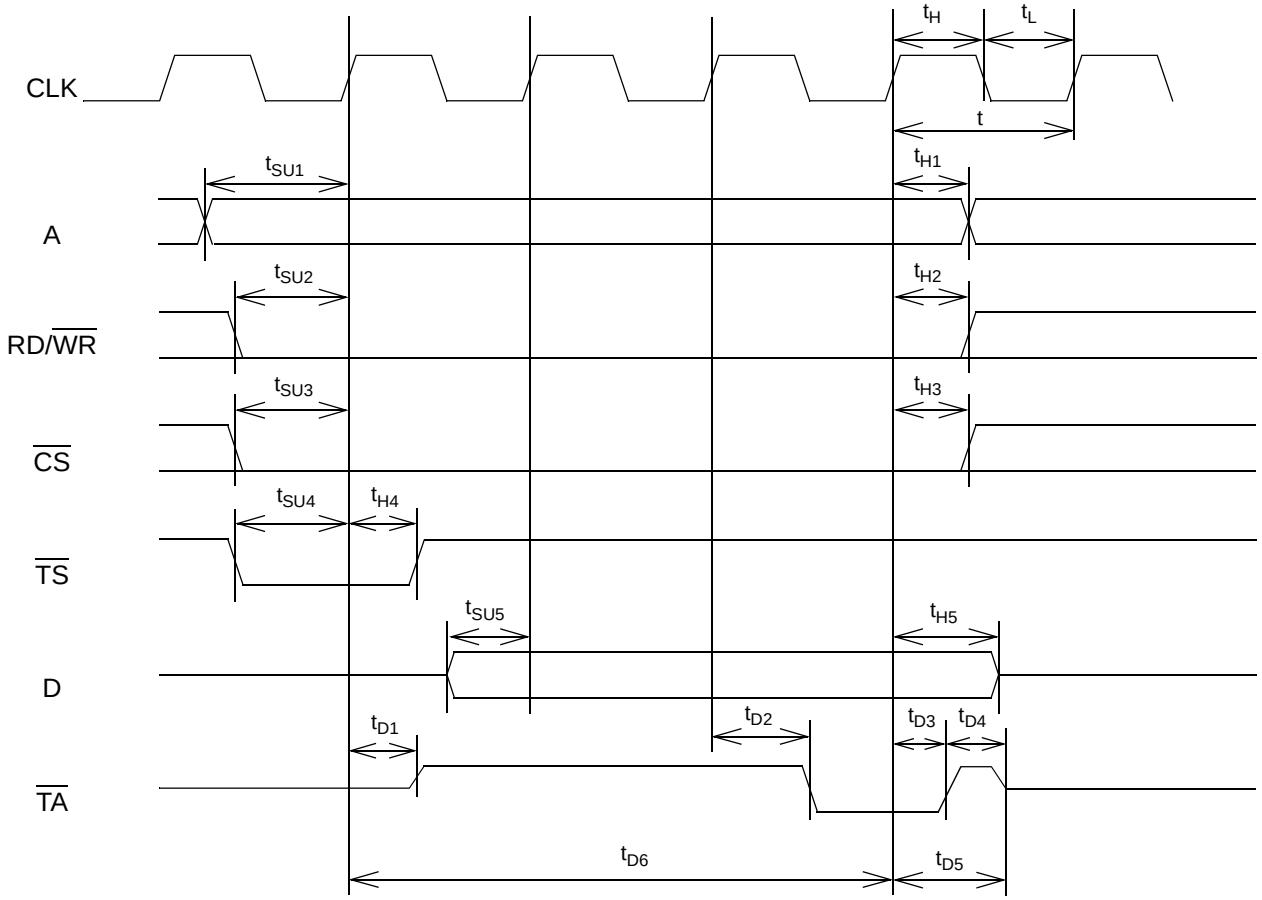
Note: MPACK (DSACK) is shown active low. This corresponds to MPACKLEVEL being tied low.

1. See the Lead Description table on Generic Motorola - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{DS}$
t_{SU2}[a]	0 ns	-	Setup time of R/$\overline{W}$ to falling edge $\overline{DS}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{DS}$
t_{SU4}	0.7t	-	Setup time of D to active edge $\overline{DSACK}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{DSACK}$
t_{H2}[c]	0 ns	-	Hold time of R/$\overline{W}$ to rising edge $\overline{DS}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{DS}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{DS}$ to $\overline{DSACK}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{DSACK}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{DS}$ to inactive edge $\overline{DSACK}$
t_{D4}	4 ns	-	Delay from $\overline{DSACK}$ going inactive to $\overline{DSACK}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{DS}$ to $\overline{DSACK}$ going in tristate
t_{D6}	t	-	$\overline{DS}$ inactive pulse width
t_{D7}	TBD	TBD	Response latency
t_{D8}	0 ns	12 ns	Delay from falling edge $\overline{DS}$ to D driving
t_{D9}	0 ns	12 ns	Delay from rising edge $\overline{DS}$ to D going in tristate
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. Only applies if a read access is preceded by a write access. R/$\overline{W}$ may stay high between 2 successive read accesses.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a read access is followed by a write access. R/$\overline{W}$ may stay high between 2 successive read accesses.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{DS}$ are defined, since no such relationship is defined in the MC68360 data sheet. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals.

Figure 22. Microprocessor Interface: Motorola MPC860 Mode Write Cycle[1]

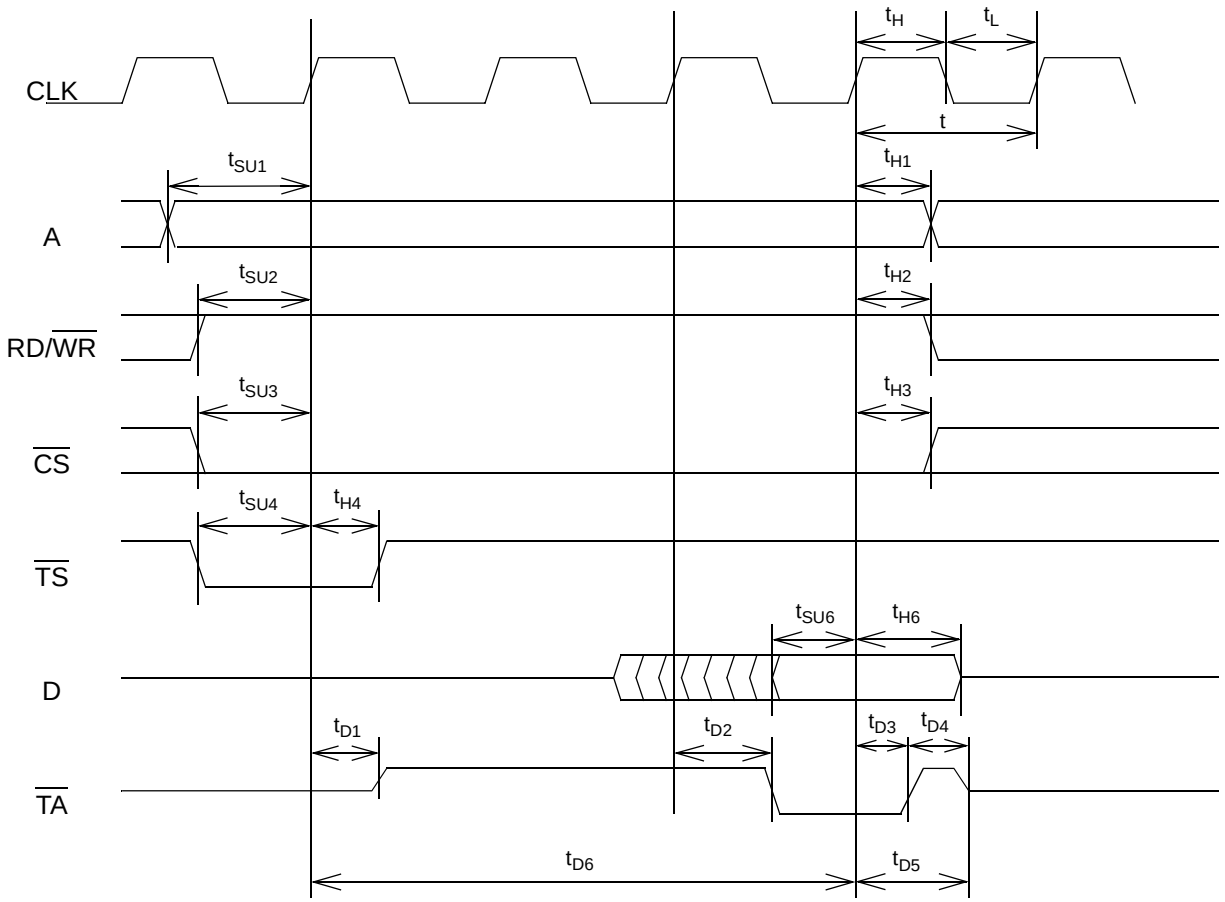


1. See the Lead Description table on Motorola MPC860 - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of RD/$\overline{WR}$ to rising edge CLK
t_{SU3} [a, c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{SU4}	6 ns	-	Setup time of falling edge $\overline{TS}$ to rising edge CLK
t_{SU5} [d]	0 ns	-	Setup time of D to rising edge CLK
t_{H1} [e]	0 ns	-	Hold time of A to rising edge CLK
t_{H2} [e, f]	0 ns	-	Hold time of RD/$\overline{WR}$ to rising edge CLK
t_{H3} [e, c]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{H4}	4 ns	-	Hold time of $\overline{TS}$ to rising edge CLK
t_{H5} [e]	0 ns	-	Hold time of D to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{TA}$ driving
t_{D2} [g]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{TA}$
t_{D3} [e]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{TA}$
t_{D4}	4 ns	-	Delay from $\overline{TA}$ going inactive to $\overline{TA}$ going in tristate
t_{D5} [e]	-	20 ns	Delay from rising edge CLK to $\overline{TA}$ going in tristate
t_{D6}	TBD	TBD	Maximum response latency

a. Timing is relative to the rising edge of CLK during which TS is asserted.
b. Only applies if a write access is preceded by a read access. RD/$\overline{WR}$ may stay low between 2 successive write accesses to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.
d. Timing is relative to next rising edge after the one during which $\overline{TS}$ is asserted.
e. Timing is relative to the rising edge of CLK during which $\overline{TA}$ is asserted.
f. Only applies if a write access is followed by a read access. RD/$\overline{WR}$ may stay low between 2 successive write accesses to the same peripheral.
g. Timing is relative to the rising edge before the one during which $\overline{TA}$ is asserted.

Figure 23. Microprocessor Interface: Motorola MPC860 Mode Read Cycle[1]

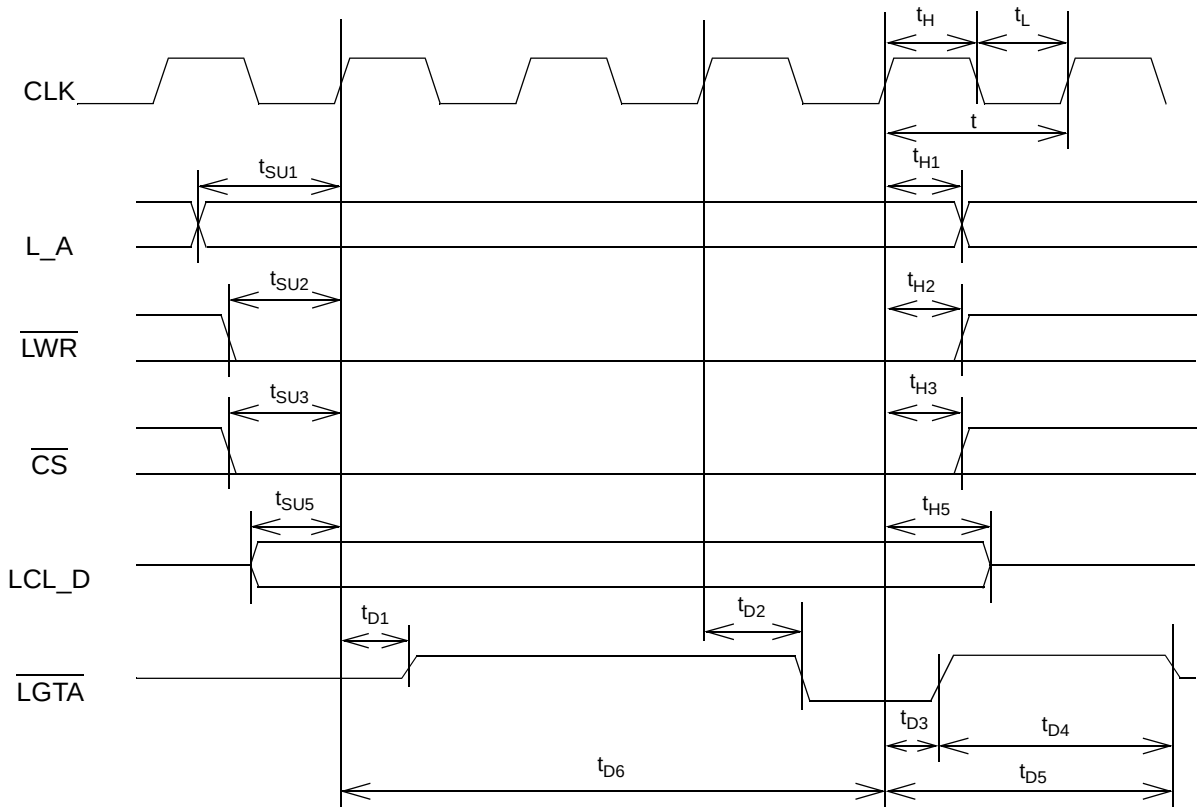


1. See the Lead Description table on Motorola MPC860 - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of RD/$\overline{WR}$ to rising edge CLK
t_{SU3} [a, c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{SU4}	6 ns	-	Setup time of falling edge $\overline{TS}$ to rising edge CLK
t_{H1} [d]	0 ns	-	Hold time of A to rising edge CLK
t_{H2} [d, e]	0 ns	-	Hold time of RD/$\overline{WR}$ to rising edge CLK
t_{H3} [c, d]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{H4}	4 ns	-	Hold time of $\overline{TS}$ to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{TA}$ driving
t_{D2} [f]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{TA}$
t_{D3} [d]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{TA}$
t_{D4}	4 ns	-	Delay from $\overline{TA}$ going inactive to $\overline{TA}$ going in tristate
t_{D5} [d]	-	20 ns	Delay from rising edge CLK to $\overline{TA}$ going in tristate
t_{D6}	TBD	TBD	Maximum response latency
t_{SU6} [d]	t	-	Setup time of D to rising edge CLK
t_{H6} [d]	1 ns	12 ns	Hold time of D going in tristate to rising edge CLK

a. Timing is relative to the rising edge of CLK during which $\overline{TS}$ is asserted.
b. Only applies if a read access is preceded by a write access. RD/$\overline{WR}$ may stay high between 2 successive read accesses to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.
d. Timing is relative to the rising edge of CLK during which $\overline{TA}$ is asserted.
e. Only applies if a read access is followed by a write access. RD/$\overline{WR}$ may stay high between 2 successive read accesses to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{TA}$ is asserted.

Figure 24. Microprocessor Interface: Motorola MPC8260 Local Bus Mode Write Cycle[1]

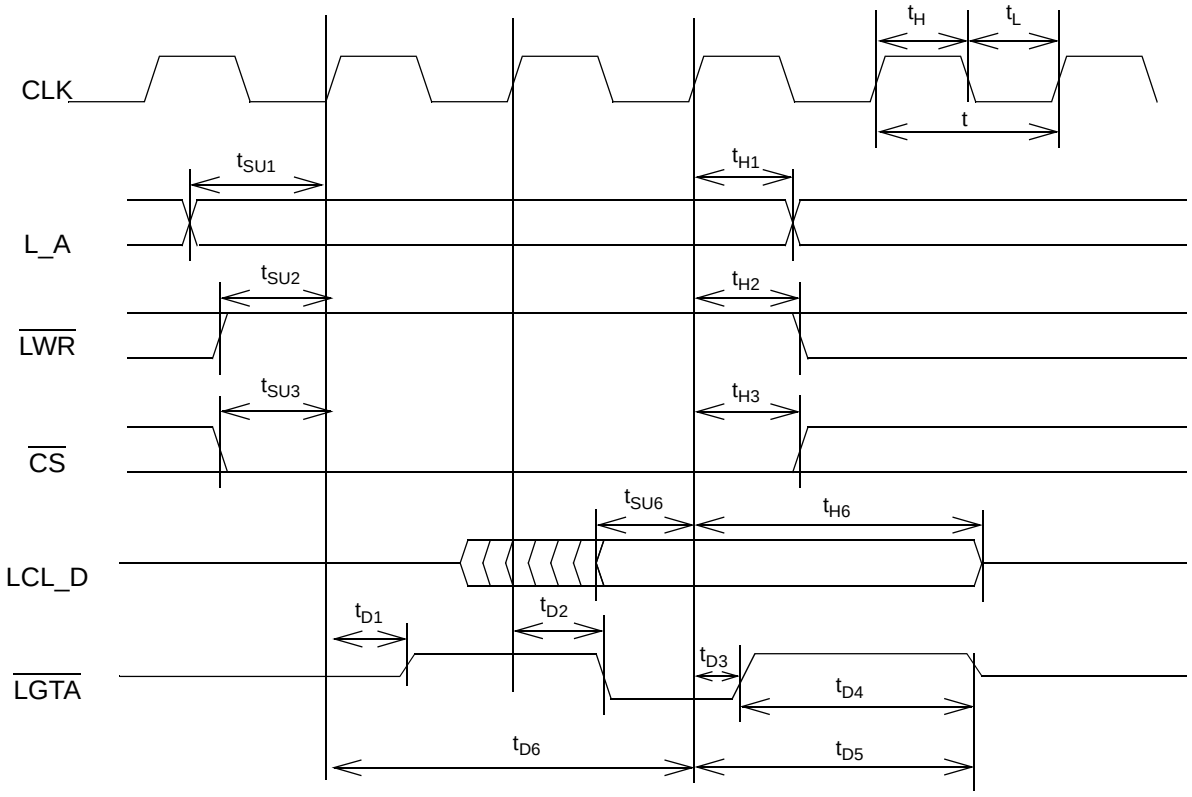


1. See the Lead Description table on Motorola MPC8260 Local Bus - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of L_A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of $\overline{LWR}$ to rising edge CLK
t_{SU3} [c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{SU5} [a]	0 ns	-	Setup time of LCL_D to rising edge CLK
t_{H1} [d]	0 ns	-	Hold time of L_A to rising edge CLK
t_{H2} [d, e]	0 ns	-	Hold time of $\overline{LWR}$ to rising edge CLK
t_{H3} [c, d]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{H5} [d]	0 ns	-	Hold time of LCL_D to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{LGTA}$ driving
t_{D2} [f]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{LGTA}$
t_{D3} [d]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{LGTA}$
t_{D4}	3t + 4 ns	-	Delay from $\overline{LGTA}$ going inactive to $\overline{LGTA}$ going in tristate
t_{D5} [d]	3t	3t + 20 ns	Delay from rising edge CLK to $\overline{LGTA}$ going in tristate
t_{D6}	TBD	TBD	Maximum response latency

a. Timing is relative to the first rising edge of the access during which $\overline{CS}$ is asserted.
b. Only applies if a write access is preceded by a read access. $\overline{LWR}$ may stay low if 2 successive write accesses are done to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral, as long as the other setup times are respected for the 2nd access. If $\overline{CS}$ remains low between accesses, the second access starts after the first is terminated.
d. Timing is relative to the rising edge during which $\overline{LGTA}$ is asserted.
e. Only applies if a write access is followed by a read access. $\overline{LWR}$ may stay low if 2 successive write accesses are done to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{LGTA}$ is asserted.

Figure 25. Microprocessor Interface: Motorola MPC8260 Local Bus Mode Read Cycle[1]

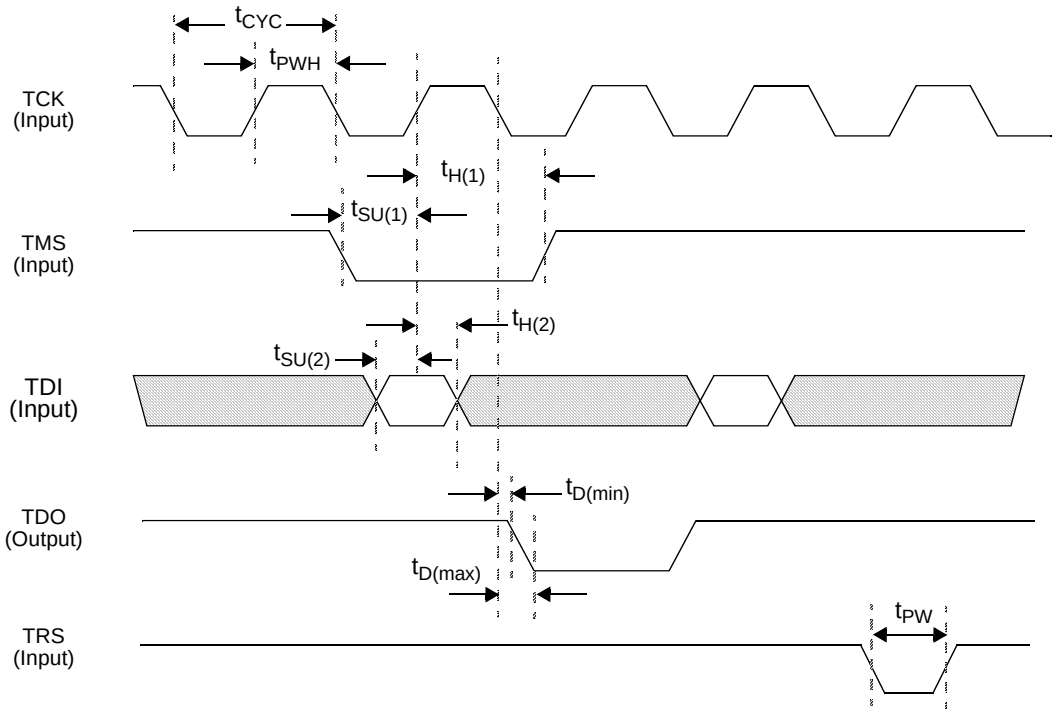


1. See the Lead Description table on Motorola MPC8260 Local Bus - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of L_A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of $\overline{LWR}$ to rising edge CLK
t_{SU3} [c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{H1} [d]	0 ns	-	Hold time of L_A to rising edge CLK
t_{H2} [d, e]	0 ns	-	Hold time of $\overline{LWR}$ to rising edge CLK
t_{H3} [c, d]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{LGTA}$ driving
t_{D2} [f]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{LGTA}$
t_{D3} [d]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{LGTA}$
t_{D4}	3t + 4 ns	-	Delay from $\overline{LGTA}$ going inactive to $\overline{LGTA}$ going in tristate
t_{D5} [d]	3t	3t + 20 ns	Delay from rising edge CLK to $\overline{LGTA}$ going in tristate
t_{D6}	TBD	TBD	Maximum response latency
t_{SU6} [d]	t	-	Setup time D to rising edge CLK
t_{H6} [d]	3t + 1 ns	3t + 12 ns	Hold time of D going in tristate to rising edge CLK

a. Timing is relative to the first rising edge of the access during which $\overline{CS}$ is asserted.
b. Only applies if a read access is preceded by a write access. $\overline{LWR}$ may stay high if 2 successive read accesses are done to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral, as long as the other setup times are respected for the 2nd access. If $\overline{CS}$ remains low between accesses, the second access starts after the first is terminated.
d. Timing is relative to the rising edge during which $\overline{LGTA}$ is asserted.
e. Only applies if a read access is followed by a write access. $\overline{LWR}$ may stay high if 2 successive read accesses are done to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{LGTA}$ is asserted.

Figure 26. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock period	t_{CYC}	50		ns
TCK clock duty cycle $t_{PWH/tCYC}$		40	60	%
TMS setup time to TCK↑	$t_{SU(1)}$	3.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	15		ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	15		ns
TDO delay from TCK↓	t_D	4.0	20	ns
$\overline{TRS}$ pulse width	t_{PW}	250		ns

10.0 OPERATION

10.1 MODES

10.1.1 Line Interface Mode

The PHAST-12N supports either one STM-4/OC-12 line interface, or four STM-1/OC-3 line interfaces.

In STM-4/OC-12 mode line interfaces #2 to #4 will not be used.

STM4_Mode	Description
0 (Default)	STM-1/OC-3 Mode: • Line interfaces #1 to #4 are 155.52 Mbit/s signals.
1	STM-4/OC-12 Mode: • Line interface #1 is a 622.08 Mbit/s signal. • Line interfaces #2 to #4 are not used.

10.1.2 SDH/SONET Mapping

The PHAST-12N supports the SDH/SONET structures presented in Figure 1. The mapping of receive and transmit line interfaces, receive and transmit APS port interfaces, and receive and transmit terminal side interfaces is independent. All mapping configurations default to all AU-4/VC-4 resp. STS-3c.

In STM-4/OC-12 mode the line interface transports a single AUG-4. A standard AUG-4 consists either of a single VC-4-4c/STS-12c SPE or four AUG-1's. To support non-standard VC-4-2c/STS-6c SPE and VC-4-3c/STS-9c SPE contiguous concatenated containers a **TimeSlotIsConcatenated** register is provided per AUG-1 time slot.

TimeSlotIsConcatenated$_{[aug1]}$	Description
0 (Default)	The AUG-1 time slot is either not part of a contiguous concatenated container, or it is the master time slot (i.e., it carries the POH column) of a VC-4-Xc resp. STS-Nc contiguous concatenated container.
1	The AUG-1 time slot is a slave (i.e., it does not carry the POH column) of a VC-4-Xc resp. STS-Nc contiguous concatenated container.

The following table lists all valid contiguous concatenation settings:

Contiguous Concatenation Structure				TimeSlotIsConcatenated[aug1]			
				0	**1**	**2**	**3**
AUG-1	AUG-1	AUG-1	AUG-1	0	0	0	0
AUG-1	AUG-1	VC-4-2c/STS-6c SPE		0	0	0	1
AUG-1	VC-4-2c/STS-6c SPE		AUG-1	0	0	1	0
AUG-1	VC-4-3c/STS-9c SPE			0	0	1	1
VC-4-2c/STS-6c SPE		AUG-1	AUG-1	0	1	0	0
VC-4-2c/STS-6c SPE		VC-4-2c/STS-6c SPE		0	1	0	1
VC-4-3c/STS-9c SPE			AUG-1	0	1	1	0
VC-4-4c/STS-12c SPE				0	1	1	1

Each AUG-1 time slot that is not part of a contiguous concatenated container, can independently be configured to consist of a single VC-4/STS-3c SPE or three VC-3/STS-1's SPE. A **Has_AU3** register per AUG-1 time slot determines the structure of that time slot.

Has_AU3[aug1]	Description
0 (Default)	The AUG-1 time slot consists of a single AU-4/VC-4 resp. STS-3c container
1	The AUG-1 time slot consists of three AU-3/VC-3 resp. STS-1 containers

In STM-1/OC-3 mode each line interface transports a single AUG-1. With the **Has_AU3** register each AUG-1 can independently be configured to consist of a single VC-4/STS-3c SPE or three VC-3/STS-1's SPE. In STM-1/OC-3 mode, it is mandatory that the **TimeSlotIsConcatenated** registers are set to the default master mode.

Another set of configuration registers is available for the Add and Drop Combus interfaces when the AUG-1 contains AU-4's. Four bits, **Is_TUG_Structured**, specify whether the corresponding VC-4 contains TUG-3's or C-4. This register is only applicable for the Combus configuration and is a don't care when the corresponding AUG-1 is part of a non-standard concatenated structure or when the AUG-1 contains three AU-3's.

Is_TUG_Structured[aug1]	Description
0	C-4 is mapped in the VC-4
1 (Default)	Three TUG-3's are mapped in the VC-4

When TUG-3 is mapped in VC-4/AU-4 or VC-3 is mapped in AU-3 an extra register is provided to specify whether these containers contain TUG-2 or not. These configuration bits are don't care for the VC-4's containing C-4.

Is_TUG_Structured[timeslot]	Description
0	• C-3 is mapped in VC-3 (AU-3 mode) • TU-3 is mapped in TUG-3 (AU-4 mode)
1 (Default)	• TUG-2 is mapped in VC-3 (AU-3 mode) • TUG-2 is mapped in TUG-3 (AU-4 mode)

Note 1: These **Is_TUG_Structured** configuration registers need only be specified for the Add and the Drop Telecombus interfaces and are don't care for all other interfaces.

Note 2: V1 pulses will be enabled on the Telecombus interfaces when the structures contain TUG-2's (see Telecom Bus Interface section).

10.2 CLOCK ARCHITECTURE

The PHAST-12N's internal Transmit Clock synthesizer generates, using a selectable Tx timebase, a high-speed Transmit Clock, running at 622.08 MHz.

The System Clock, running at 77.76 MHz, is a divided-down version of this high-speed Transmit Clock.

Telecom Bus clocks:

- The Drop Telecom Bus clock output lead, CBDPCLK, is actually the System Clock
- The Add Telecom Bus clock lead, CBADCLK, is an output in master timing mode. It is actually the System Clock
- The Add Telecom Bus clock lead, CBADCLK, is an input in slave timing mode. It gets retimed to the System Clock in the Retimer

The System Clock is available on an output lead: LINETXCLK, optionally divided down to 19.44 MHz.

The PHAST-12N's internal Clock Recovery units, operating on the four SDH/SONET Receive Line interfaces and the Receive APS Port generate five recovered clocks: one for each channel.

Internally, these units require a high-speed Receive Clock, which is synthesized using a selectable Rx timebase.

The recovered data from the four SDH/SONET Receive Lines and from the Receive APS Port is retimed to the System Clock, before entering the Cross Connect.

Divided-down versions of each recovered clock are available on output leads: LINERXCLK1 (19.44 or 77.76 MHz), LINERXCLK2 (19.44 MHz), LINERXCLK3 (19.44 MHz), LINERXCLK4 (19.44 MHz), and APSRXCLK (19.44 or 77.76 MHz).

The Tx timebase can be selected using control bits:

- Either one of the two external Transmit Clock sources: REFTXCLK1 or REFTXCLK2P/N (External Timing) (control field **TxRefSelect**, see Table 55 of the Memory Maps and Bit Descriptions)
- The recovered 622.08 MHz Receive APS Port clock (External Timing) (control field: **LineTimingChannel** and **TimingMode**, see Table 55 of the Memory Maps and Bit Descriptions)

- The recovered 622.08 MHz clock in STM-4/OC-12 application (Line/Loop - Timing) (control field: **LineTimingChannel** and **TimingMode**, see Table 55 of the Memory Maps and Bit Descriptions)
- Any of the four recovered 155.52 MHz clocks in STM-1/OC-3 application (Line/Loop - Timing) (control field: **LineTimingChannel** and **TimingMode**, see Table 55 of the Memory Maps and Bit Descriptions)

The frequency of REFTXCLOCK1 is selectable:

- 19.44 MHz
- 77.76 MHz

The frequency of REFTXCLOCK2P/N is selectable:

- 19.44 MHz
- 77.76 MHz
- 155.52 MHz
- 622.08 MHz (bypass mode)

The Rx timebase can be selected using control bits:

- Either one of the two external Tx clock sources: REFTXCLK1 or REFTXCLK2P/N (External Timing) (control field **TxRefSelect**, see Table 55 of the Memory Maps and Bit Descriptions)
- The external Rx clock source: REFRXCLOCK (Line/Loop - Timing) (control field **RxRefSelect**, see Table 55 of the Memory Maps and Bit Descriptions)

In case REFTXCLOCK2P/N is used as Rx timebase, the 622.08 MHz frequency (bypass mode) is not supported.

In Line/Loop - Timing mode, it is mandatory to provide an external Rx clock source at REFRXCLK. Its frequency is selectable:

- 19.44 MHz
- 77.76 MHz

Figure 27 shows the relation between synthesized/recovered clocks and the reference clocks.

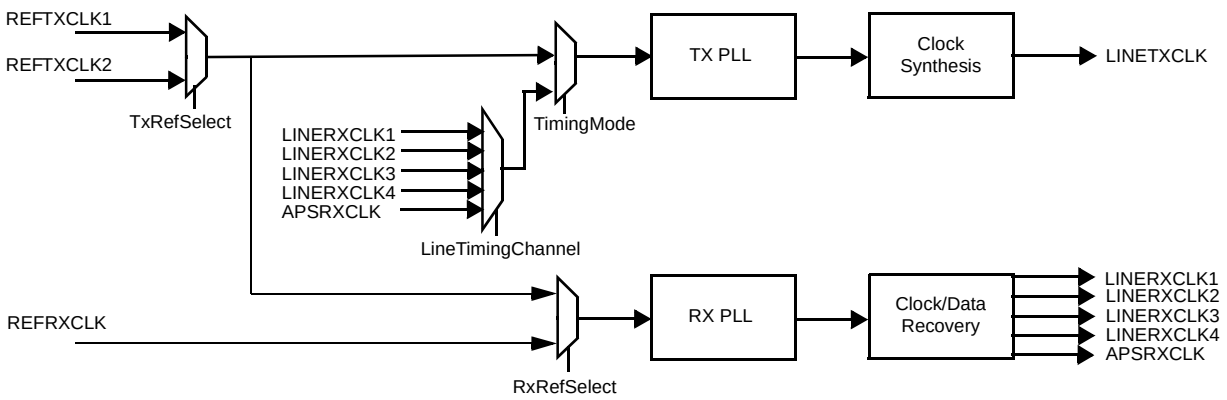
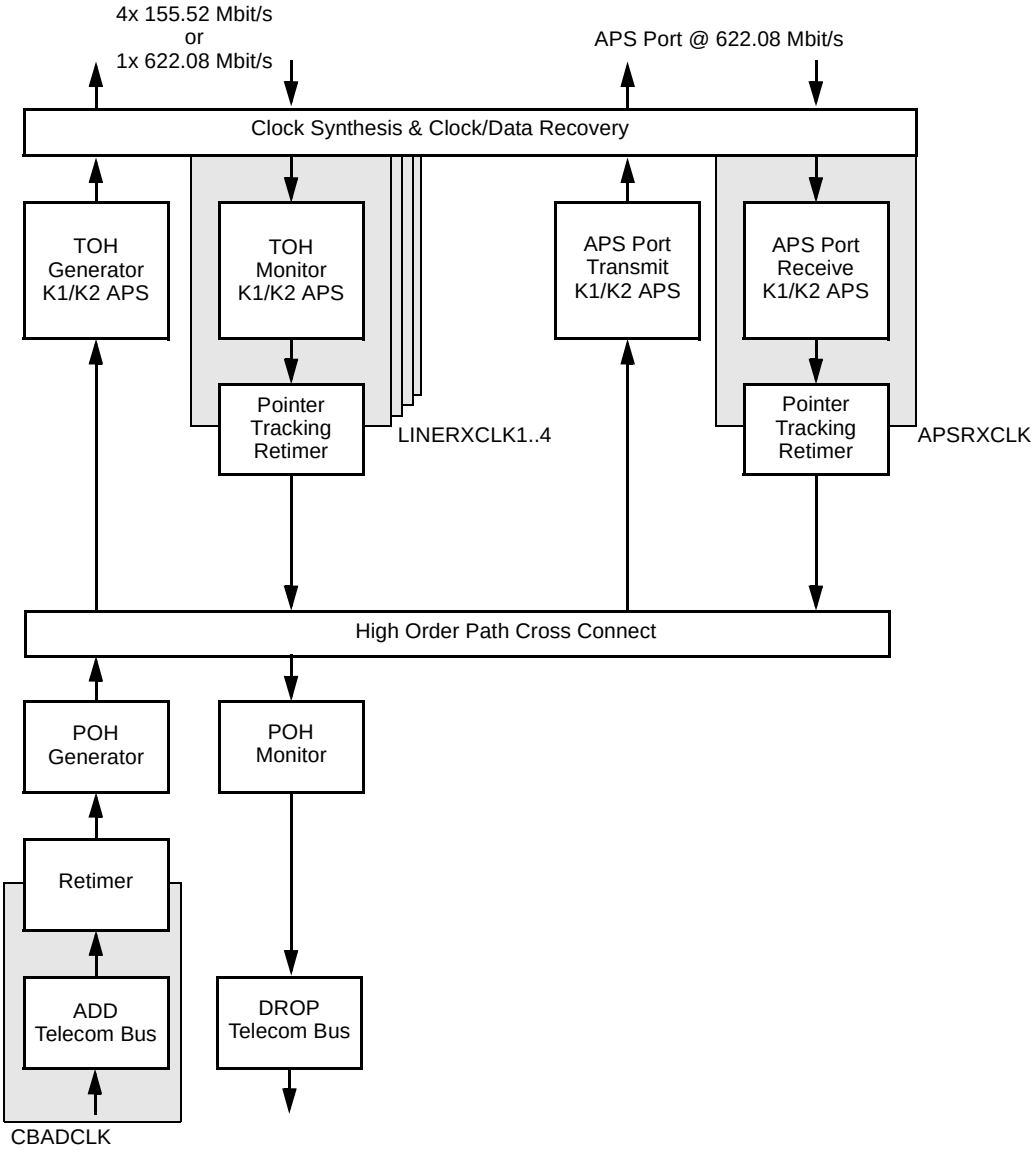


Figure 27. Clock Recovery/Clock Synthesis

10.2.1 Clocks and Software-Access



Following table gives an overview of the different clock domains which are necessary in order to access a particular block (see Memory Maps and Bit Descriptions).

Clock Domain	Blocks
MPCLK	Global Control Reset Generator Interrupt Clock Recovery/Clock Synthesis/SerDes JTAG Master
MPCLK System Clock (=LINETXCLK)	Line Ring Port/Alarm Interface Transmit APS Port POH Generator TOH Generator TOH and DCC Port High Order Pointer Tracker and Retimer - Rx Line Interface High Order Pointer Tracker and Retimer - Rx APS Interface Retimer Cross Connect High Order Path Ring Port/Alarm Interface Drop Telecom Bus POH Monitor - Rx Line Interface POH Monitor - Rx APS Interface POH Monitor - Terminal Side Add Telecom Bus (Master mode) PRBS Generator/Analyzer
MPCLK System Clock (=LINETXCLK) LINERXCLK1	TOH Monitor - Rx Line 1 (STM-1 / STM-4 mode)
MPCLK System Clock (=LINETXCLK) LINERXCLK2	TOH Monitor - Rx Line 2 (STM-1 mode only)
MPCLK System Clock (=LINETXCLK) LINERXCLK3	TOH Monitor - Rx Line 3 (STM-1 mode only)
MPCLK System Clock (=LINETXCLK) LINERXCLK4	TOH Monitor - Rx Line 4 (STM-1 mode only)
MPCLK System Clock (=LINETXCLK) APSRXCLK	Receive APS Port
MPCLK System Clock (=LINETXCLK) CBADCLK	Add Telecom Bus (Slave mode)

10.2.2 Loss of Clock Detection

All clocks, except the microprocessor clock, are monitored for Loss of Clock. The clock to be monitored is divided by **LocDivider** + 1.

Loss of Clock is detected as follows:

- Entry: when **LOC_EntryThreshold** microprocessor clock cycles have passed without transitions on the divided clock to be monitored.
- Exit: when **LOC_ExitThreshold** transitions are detected the divided clock

Note: The Loss of Clock detector can only operate correctly if the optical transceiver generates a constant output (no transitions) on the receive side when there is no valid incoming optical signal.

10.3 RESET

10.3.1 External Lead Controlled Hardware Reset

Hardware Reset (Active Low): The use of this lead at power-up is mandatory. Holding this lead low for at least 50ns causes all the registers in the device to be reset.

10.3.2 Microprocessor Controlled Hardware Reset (RESETH)

When written with the value 0x91H all registers in the device will be reset but with a few exceptions.

The registers in the following blocks will not be reset:

- Microprocessor interface
- Global control
- Reset generator
- Interrupt
- Clock recovery / clock synthesis / SerDes
- JTAG Master

These are the registers that operate in the microprocessor clock domain.

10.3.3 Microprocessor Controlled Reset Per Clock Domain

There are 5 major interfaces. For each of these there is a separate microprocess controlled reset available. Reset is activated by writing the value 0x91 H to the corresponding register.

- AddCombus_Reset: Reset in the Add Combus clock domain
- RxLine1_Reset ... RxLine4_Reset: Reset in the RxLine 1 ... 4 clock domain

These software resets may only be asserted when RESETH is equal to 0x91. They may be deasserted at anytime.

10.4 POWERUP, INITIALIZATION AND STARTUP

After powerup and external reset of the device, no internal clocks are active. This section describes the way the necessary clocks need to be brought up and the initialization of the device.

The first clock present in the device is the external microprocessor clock. The registers which are needed to bring up the internal clocks are located in the clock domain from this external microprocessor clock.

The clock domains which must be brought up next are:

- System Clock
- Rx Line 1 Clock
- Rx Line 2 Clock
- Rx Line 3 Clock
- Rx Line 4 Clock
- Rx APS Clock

In case the Add Telecombus is operating in Slave Mode, this is an external clock domain. The external clock must be running in order to access the registers in this domain. If the Add Telecombus is in Master Mode, this is a part of the System Clock domain.

At this stage of the process, the hardware interrupt can be enabled through the **HINTEN** field (see Table 7 of Memory Maps and Bit Descriptions section). The interrupt masks must be properly disabled here.

It is advised to unmask the Global Control Interrupt now. In the Global Control block, the Loss of System Clock and Loss of Clock for the active lines must be unmasked to enable the hardware interrupt for events on the Loss of Clock detection.

After this, the Clock Recovery/Clock Synthesis block must be configured and powered up (see section Powerup of the CDR/CS). If the General Purpose Outputs are used to control the lasers, those must also be powered up.

It is recommended to leave **RESETH** (see Table 6) asserted until this point. Once **RESETH** is deasserted, the device will start a reset sequence for all of its internal RAMs. The **RamResetDone** record in the Global Control block (see Table 2) indicates which clock domains have finished resetting their RAMs.

Once all the necessary clock domains are powered up, and the corresponding RAMs are reset, the device will not yet be operational. Operation is halted so the device can be configured in a clean way. Once the configuration is done, **DeviceInitialized** field in Global Control can be set to 1 and the device will start its normal operation.

10.4.1 Powerup of the CDR/CS

A startup sequence for the Clock and Data Recovery / Clock Synthesis part of the PHAST-12N is given below (all registers can be found in the CDR/CS section of the Memory Map):

- Set device in software reset: Write 0x91 to **RESETH** (Address 0x00A0). Other clock domains can also be set in reset now (See Memory Map).
- Write 0x0000 to **IndirectAccessMode** (Address 0x3A26), followed by writing 0x0017 to **IndiretAccessData** (Address 0x3A5E)

- Write 0x0008 to **IndirectAccessMode** (Address 0x3A26), followed by writing 0x5000 to **IndiretAccessData** (Address 0x3A5E)
- Configure System Loopback (Address 0x3A22) or Facility Loopback (Address 0x3A24) if desirable
- Configure the **CDRTune** and **PLLTune** parameters (Addresses 0x3A74-0x3A7C and 0x3A7E)
  Refer to the Memory Map section for recommended values.
- Configure the PLL's for External or Line Timing as follows:

Register	External Timing		Line Timing	
TimingMode (Address 0x3A60)	0x0		0x1	
LineTimingChannel (Address 0x3A62)	N/A		Select timing mode channel	
TxRefSelect (Address 0x3A64)	Select Tx Reference Clock		N/A	
RxRefSelect (Address 0x3A66)	Select Rx Reference Clock		Select Rx Reference Clock	
TxPLL_Cap_Enable (Address 0x3A68)	Enable/Disable External Capacitor for Tx PLL		Enable/Disable External Capacitor for Tx PLL	
RxPLL_Cap_Enable (Address 0x3A6A)	Enable/Disable External Capacitor for Rx PLL		Enable/Disable External Capacitor for Rx PLL	
TxRefFreq (Address 0x3A6C)	Select Tx PLL Reference Clock Frequency		N/A	
RxRefFreq (Address 0x3A6E)	Select Rx PLL Reference Clock Frequency		Select Rx PLL Reference Clock Frequency	
TxPLL_PowerDown (Address 0x3A70)	0x0		0x0	
RxPLL_PowerDown (Address 0x3A72)	0x0		0x0	
LineRate (Address 0x3A52)	N/A		Select Line Rate of Reference Channel	
OC3NotOC12 (Address 0x3A5A)	STM-1/OC-3 Mode	STM-4/OC-12 Mode	STM-1/OC-3 Mode	STM-4/OC-12 Mode
	0x0F	0x0E	0x0F	0x0E

- Write 0x00 to **TxRefClock2 PadPowerDown** register (Address 0x3A34) if REFTXCLK2 is used as reference clock

- Power up the Rx pads: **RxPadPowerDown** register (Address 0x3A30)
- Write 0x00 to **RxPowerDown1** register (Address 0x3A54)
- Write 0x00 to **RxPowerDown2** register (Address 0x3A56)
- Write 0x00 to **TxPowerDown** register (Address 0x3A50)
- Write 0x00 to **ToplevelPowerDown** register (Address 0x3A58)
- Write 0x01 to **SerDes_LoadConfig** register (Address 0x3A20). This will cause the previous settings to be transferred to the CDR/CS/SerDes part (See Note below)
- Wait until the **SerDes_LoadConfig** register (Address 0x3A20) is reset to 0x00 by the device
- Power up the Tx pads: **TxPadPowerDown** register (Address 0x3A32)
- Take away the Software reset by writing 0x0000 to the **RESETH** register (Address 0x00A0). Other software resets can also be deasserted if any.

Note: Some CDR/CS configurations are transferred to the CDR/CS part only after a software command. Following settings will not have effect before transferring them:

CDR_CS_Setup.TxPowerDown

CDR_CS_Setup.RxPowerDown1

CDR_CS_Setup.RxPowerDown2

CDR_CS_Setup.ToplevelPowerDown

CDR_CS_Setup.OC3NotOC12

PLL_Control.TxPLL_Cap_Enable

PLL_Control.RxPLL_Cap_Enable

PLL_Control.TxPLL_PowerDown

PLL_Control.RxPLL_PowerDown

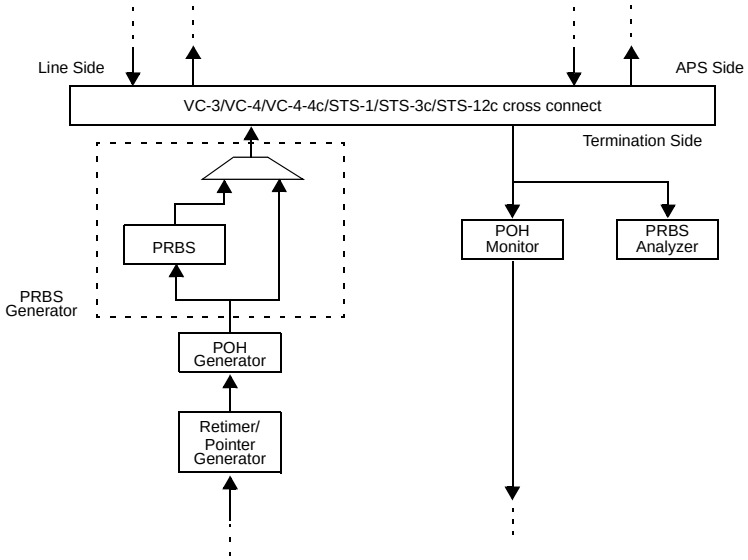
PLL_Control.CDRTune

PLL_Control.PLLTune

All configurations done via the indirect access register (IndirectAccessData and IndirectAccessMode)

After configuration of these fields, one has to set **SerDes_LoadConfig** to 0x1 in order to make these settings effective. A transfer of the above mentioned configuration records will start. **SerDes_LoadConfig** will be reset automatically by the device after the transfer is completed (approx. 420 microprocessor clockcycles). Note however settings to other addresses than those before mentioned are still possible during this transfer. The configured registers will not be reset after transfer.

10.5 PRBS GENERATOR AND PRBS ANALYZER



The PHAST-12N has a built-in PRBS generator and analyzer for test purposes. PRBS can be inserted on one path of the Terminal Side input port of the cross connect (port #3). This way PRBS can be routed through the cross connect to each of its three output ports. The PRBS analyzer is situated on the Terminal Output of the cross connect (port #3). The PRBS polynomial is $2^{23} - 1$. The output of the PRBS generator and the input of the PRBS analyzer can optionally be inverted. In order to use the PRBS generator/analyzer functionality the **AUG1_Mode_Config** record in the CDR/CS block has to be configured properly. This record is a don't care if the PRBS functionality is not used. Configuration of the PRBS generator and analyzer is done in the **XConnectPRBSControl** registers.

The PRBS analyzer will lock on the incoming PRBS data after 24 consecutive correct bits. This is reported in the **Status_Unlatched** register. Once in lock the PRBS analyzer will stay in lock and count the received bit errors. These are accessible via the **PRBSBitErrorCounter**, which is reset each time a (software) read access is done to this register (clear-on-read).

The state machines are reset when disabling the PRBS generator/analyzer, so make sure to disable the PRBS generator and analyzer before (re-)configuring them.

Important Notes:

1. Although the PRBS bit error counter is mapped in the memory map of the CDR/CS block, the System clock (LINETXCLK) must be available when reading this counter.
2. B3 may contain errors as it is not recalculated on the PRBS data.

10.6 LINE INTERFACE

Four serial line interfaces with differential input/output and integrated clock recovery and synthesis are provided.

The device supports two modes: either a single STM-4/OC-12 signal, or four STM-1/OC-3 signals.

- Line Interface #1 can handle 622.08 Mbit/s or 155.52 Mbit/s data rate for STM-4/OC-12, STM-1/OC-3 applications respectively
- Line Interfaces #2 - #4 can handle 155.520 Mbit/s data rate for STM-1/OC-3 applications

The device's System Clock is the time base for the transmit SDH/SONET line output(s).

Each individual line interface can be powered down via a memory mapped register.

Frame alignment is recovered from the A1-A2 bytes of the received signals.

The OOF anomaly and the dLOF defect will be detected according to the latest ITU/ETSI/ ANSI standards.

The following additional functions are provided:

- Four (one for each line interface) active high status inputs to monitor the external optical transceivers for low power status
- Four (one for each line interface) output control signals under microprocessor command to control each individual external optical transceiver
- Four (one for each line interface) reference clocks derived from the received signal. The rate of these reference clocks will be selectable per line

AIS will be inserted per line on detection of dLOF, on detection of dLOS, optionally on the externally detected Signal Detect or under software control.

$$\begin{aligned} aAIS &= \text{not SignalDetect}_{[line]} * \text{not SignalDetect\_AIS\_Insert\_Disable}_{[line]} \\ &+ \text{dLOS}_{[line]} * \text{not LOS\_AIS\_Insert\_Disable}_{[line]} \\ &+ \text{dLOF}_{[line]} * \text{not LOF\_AIS\_Insert\_Disable}_{[line]} \\ &+ \text{Framer AIS Force}_{[line]} \end{aligned}$$

10.7 APS INTERFACE

The APS Port transports the payload and APS signaling between two mate devices. The APS finite state machine itself needs to be implemented by the external host software. The resulting bridge and switch requests are performed by configuring the cross connect.

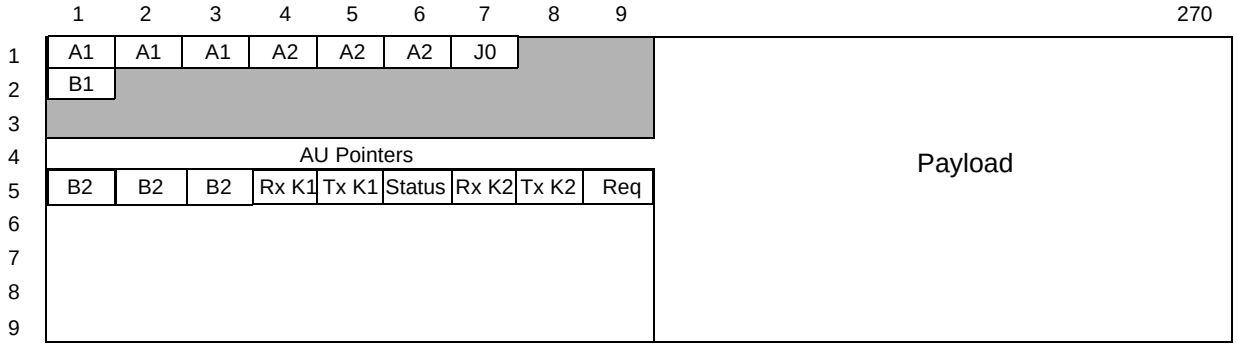
A single 622.08 Mbit/s LVDS serial APS interface with differential input/output is provided. Clock recovery and synthesis are integrated.

The device's System Clock is the time base for the transmit APS interface output.

The APS port interface can be powered down via a memory mapped register.

The APS Interface characteristic information consists of:

- A1, A2, J0, and B1 overhead bytes similar to the STM-4/OC-12 RS (section) overhead
- The high order path data for four STM-1/OC-3 signals or one STM-4/OC-12 signal
- The received and transmitted K1/K2 APS signal for up to four lines
- Signal fail and signal degrade indications for up to four lines



10.7.1 APS Interface Generator

The PHAST-12N generates the APS interface overhead bytes.

- The SDH/SONET frame alignment signal will be inserted in the A1-A2 bytes
- The signal will be scrambled, except for the first SOH row
  - Software will be able to disable scrambling for test purposes
- A single byte Trail Trace Identifier (TTI) will be inserted in the J0 byte
- A fixed value (0xCC) will be inserted in the Z0 bytes. Remark the inserted value is different from 0x00 to avoid LOS detection.
- BIP-8 will be calculated over all bits of the preceding STM-4 like APS frame after scrambling and will be inserted in the B1 byte of the current frame before scrambling
- BIP-96 will be calculated over all bits of the preceding STM-4 frame except the first three SOH rows and will be inserted in the B2 bytes of the current frame. The software configurable B2 bytes have a special behavior, in that the filled in bytes are used as an error-mask to corrupt the calculated B2 bytes.
- Rx K1, Tx K1, Rx K2, Tx K2, Status and Request are inserted according to the APS protocol
- AU Pointer bytes are passed
- Unused bytes are set to 0x00

10.7.2 APS Interface Monitor

The PHAST-12N terminates the APS interface overhead bytes.

- Loss of Lock (LOL) of the on-chip clock and data recovery will be reported
- Frame alignment is recovered from the A1-A2 bytes of the received signals
- Errors in the frame alignment signal will be detected and reported as OOF

- The signal will be descrambled, except for the first SOH row
  - Software will be able to disable descrambling for test purposes
- The single byte Trail Trace Identifier (TTI) in the J0 byte will be compared to an expected value and the TTI Mismatch defect (TIM) will be detected
- The accepted Trail Trace Identifier will be reported
- The Z0 bytes are ignored
- BIP-8 will be calculated over all bits of the preceding STM-4 like APS frame before descrambling and will be compared to the B1 byte of the current frame after descrambling
- B1 BIP-8 errored blocks will be counted in a one second performance counter
- 3 subsequent frames with B1 BIP-8 errored blocks will be reported as a degraded signal (**B1_Error**) alarm, 5 subsequent non-errored frames will clear the **B1_Error** alarm. Remark the B1 BIP-8 errored blocks continues to count the errored frames on incoming SSF. As a consequence B1_Error will also be declared. Note:
  - B1_Error is not a standard SONET/SDH defect. No consequent actions are defined for it.
  - APS is a dedicated interface and the only reason for incoming SSF is Loss Of Frame (which indicates there is something wrong in the APS connection).
  - In the Line RSOH monitor the B1 counter is frozen on incoming SSF.
- B2 bytes are ignored.
- Rx K1, Tx K1, Rx K2, Tx K2, Status and Request are monitored according to the APS protocol
- All other (unused) bytes are ignored.

10.8 REGENERATOR SECTION (SECTION) OVERHEAD PROCESSING

The PHAST-12N device complies to the latest ITU/ETSI/ANSI standards and features regarding the generation and monitoring of the Regenerator Section Overhead bytes.

10.8.1 Regenerator Section Overhead Generator

The PHAST-12N generates the Regenerator Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- The frame alignment signal will be inserted in the A1-A2 bytes
- The signal will be scrambled, except for the first SOH row
  - software will be able to disable scrambling for test purposes.
- A single or 16 byte Trail Trace Identifier will be inserted in the J0 byte
- The interleave depth coordinate can be inserted in the Z0 bytes for backwards compatibility. Note the Z0 bytes need to be carefully chosen in order to guarantee enough transitions on the first TOH row.
- BIP-8 will be calculated over all bits of the preceding STM-n frame after scrambling and will be inserted in the B1 byte of the current frame before scrambling. The software configurable B1 byte has a special behavior, in that the filled in byte is used as an error-mask to corrupt the calculated B1 byte.
- The D1-D3 bytes will optionally be inserted from

- the transmit DCC interface, if the latter is configured for RS DCC
- the TOH byte interface
- the transmit TOH RAM

- The E1, F1, user bytes and MDB bytes will optionally be inserted from
  - the transmit TOH byte interface
  - the transmit TOH RAM

10.8.2 Regenerator Section Overhead Monitor

The PHAST-12N terminates the Regenerator Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- The signal will be descrambled, except for the first SOH row
  - Software will be able to disable descrambling for test purposes
- The single or 16 byte Trail Trace Identifier in the J0 byte will be compared to an expected value and the dTIM defect will be detected
  - Software will be able to disable the TTI mismatch process
  - AIS insertion upon dTIM detection will be configurable
- The accepted Trail Trace Identifier will be reported
- BIP-8 will be calculated over all bits of the preceding STM-n frame before descrambling and will be compared to the B1 byte of the current frame after descrambling. The software readable B1 byte has a special behavior, in that the transmitted byte represents the error mask (difference between calculated and received byte)
- The D1-D3 bytes will be forwarded to the receive DCC interface, if the latter is configured for RS DCC
- The D1-D3, E1, user bytes and MDB bytes will be written to the receive TOH RAM
- The D1-D3, E1, user bytes and MDB bytes will be forwarded to the receive TOH byte interface
- Near End Defect Second: Occurrence of aTSF will result in a Near End Defect Second. This register is cleared on the one-second boundary, after it has been copied to its shadow register (software readable)

The PHAST-12N RSOH Monitor will insert AIS per line interface towards the MSOH Monitor according to the following expression:

$$aAIS_{[line]} = dTIM_{[line]} * \text{not } TIM\_AIS\_Insert\_Disable_{[line]} + RSOH\_AIS\_Force_{[line]}$$

10.9 MULTIPLEX SECTION (LINE) OVERHEAD PROCESSING

The PHAST-12N device is compliant to the latest ITU/ETSI/ANSI standards and features regarding the generation and monitoring of the Multiplex Section Overhead bytes.

10.9.1 Multiplex Section Overhead Generator

The PHAST-12N generates the Multiplex Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- BIP-nx24 will be calculated over all bits of the preceding STM-n frame except the first three SOH rows and will be inserted in the B2 bytes of the current frame. The software configurable B2 bytes have a special behavior, in that the filled in bytes are used as an error-mask to corrupt the calculated B2 bytes
- Per line the internal or the external ring port can be selected as source for the REI and RDI indications
- The REI will be inserted into the M1 byte
- The RDI will be inserted into the K2 byte
- The MSP APS signal will be inserted into the K1-K2 bytes from
  - The receive APS Port
  - The transmit receive TOH RAM
- The D4-D12 bytes will optionally be inserted from
  - The transmit DCC interface, if the latter is configured for MS DCC
  - The transmit TOH byte interface
  - The transmit TOH RAM
- The E2 byte will optionally be inserted from
  - The transmit TOH byte interface
  - The transmit TOH RAM
- The synchronization status message will be inserted into the S1 byte. The sources are
  - The transmit TOH byte interface
  - The transmit TOH RAM

10.9.2 Multiplex Section Overhead Monitor

The PHAST-12N terminates the Multiplex Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- BIP-nx24 will be calculated over all bits of the preceding STM-n frame except the first three SOH rows and will be compared to the B2 bytes of the current frame. The software readable B2 bytes have a special behavior, in that the transmitted bytes represent the error mask (difference between calculated and received bytes).
  - An errored near-end block nN_B will be counted for performance monitoring if one or more errors in a STM-n frame are detected by the BIP-nx24. Optionally bit errors will be counted
  - The error count per frame will be forwarded to the internal and external line ring ports as REI indication for the mate TOH generator

  - The dDEG and dEXC defects will be detected for both bursty and Poisson error distributions based on (block) error thresholds
- The errored far-end blocks will be counted for performance monitoring based on the REI value retrieved from the M1 byte. Optionally bit errors will be counted
- The dAIS and dRDI defects will be detected
- The MSP APS signal will be retrieved from the K1-K2 bytes and
  - Written to the receive TOH RAM
  - Forwarded to the receive TOH byte interface
  - Forwarded to the transmit APS Port
- The D4-D12 bytes will be forwarded to the receive DCC interface, if the latter is configured for MS DCC
- The D4-D12, E2 and S1 bytes will be written to the receive TOH RAM
- The D4-D12, E2 and S1 bytes will be forwarded to the receive TOH byte interface
- The synchronization status message accepted from the S1 byte will be reported
- The S1 byte will be monitored for changes in the accepted synchronization status message
- Far End Defect Second: Occurrence of dRDI will result in a Far End Defect Second. This register is cleared on the one-second boundary, after it has been copied to its shadow register (software readable).

Per line AIS will be inserted on detection of dAIS or dEXC on that line or under software control.

Per line RDI will be forwarded to the internal and external line ring ports for the mate TOH generator.

The signal degrade (dDEG) and signal fail indications will be forwarded to the transmit APS port.

The PHAST-12N MSOH Monitor will insert AIS per line interface towards the pointer tracker according to the following expression:

$$\begin{aligned} aAIS_{[line]} &= dAIS_{[line]} * \text{not } AIS\_AIS\_Insert\_Disable_{[line]} \\ &+ dEXC_{[line]} * \text{not } EXC\_AIS\_Insert\_Disable_{[line]} \\ &+ dSSF_{[line]} * \text{not } SSF\_AIS\_Insert\_Disable_{[line]} \\ &+ MSOH\_AIS\_Force_{[line]} \end{aligned}$$

The PHAST-12N MSOH Monitor will insert RDI per line interface towards the RX Line Ring Port according to the following expression:

$$\begin{aligned} aRDI_{[line]} &= dAIS_{[line]} * \text{not } AIS\_RDI\_Insert\_Disable_{[line]} \\ &+ dEXC_{[line]} * \text{not } EXC\_RDI\_Insert\_Disable_{[line]} \\ &+ dSSF_{[line]} * \text{not } SSF\_RDI\_Insert\_Disable_{[line]} \\ &+ MSOH\_AIS\_Force_{[line]} \end{aligned}$$

10.10 HIGH ORDER CROSS CONNECT

The PHAST-12N provides a high order SDH/SONET path cross connect function. Each VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE path at the cross connect outputs will be able to serve as connection destination point. Each VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE path at the cross connect inputs will be able to serve as connection source point.

The cross connect function will support uni-directional connections between source points at any of its inputs to destination points at any of its outputs.

The cross connect function will support multicasting of a single source point to any number of destination points.

The cross connect function will source the appropriate unequipped signal at not connected destination points.

At power up or reset, the cross connect will default all destination points to not connected.

The cross connect will be able to squelch or insert AIS at each destination point.

The cross connect function will be non-blocking.

For each output time slot the following parameters will be configurable by the user:

- The connection source point (input bus and time slot)
- Concatenation indication according to the SDH/SONET mapping mode
- Forced unequipped signal insertion (if no connection active)

Force_Uneq$_{[bus][ts]}$	**Description**
0	Output time slot [ts] on bus [bus] is connected to the SourceBus/SourceTs channel.
1 (Default)	Output time slot [ts] on bus [bus] is forced to unequipped.

- Forced AIS insertion (for APS squelching)

Force_AIS$_{[bus][ts]}$	**Description**
0 (Default)	Output time slot [ts] on bus [bus] is connected to the SourceBus/SourceTs channel.
1	Output time slot [ts] on bus [bus] is forced to AIS.

The PHAST-12N high order cross connect function will support three input buses and three output buses.

- Line interface
- APS Port
- POH Termination

Each bus will transport synchronous payload containers equivalent to a STM-4/OC-12 rate, i.e., up to 12 AU-3/VC-3/STS-1's, up to four VC-4/STS-3c's SPE, up to two STS-6c's, one STS-9c, one VC-4-4c/STS-12c, SPE or combinations thereof.

10.11 AUTOMATIC PROTECTION SWITCHING

10.11.1 Single Device Operation

The PHAST-12N device will support two 1+1, two 1:1 or one 1:n (n=2-3) protection groups within a single PHAST-12N device in STM-1/OC-3 mode. The incoming K1/K2 APS will be monitored by the TOH Monitor block. The outgoing K1/K2 APS will be generated by the TOH Generator block. The high order path cross connect will support bridge and switch operation. Figure 28 shows a 1:3 APS in idle state and in bridge/switch state after a failure of working line #2.

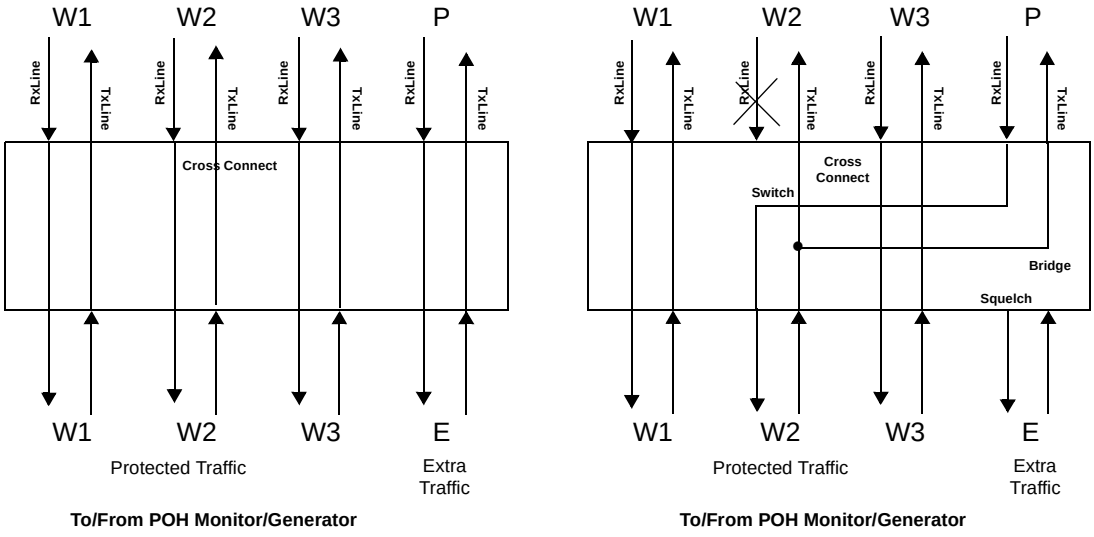


Figure 28. STM-1/OC-3, 1:3 APS with one PHAST-12N

10.11.2 Dual Device Operation

When two PHAST-12N devices are connected through the APS Port Interface, the following protection schemes are supported:

- 1+1, 1:1 or 1:n (n<=7) in STM-1/OC-3 mode
- 1+1 or 1:1 in STM-4/OC-12 mode

The APS Port interface will transport payload data and the APS finite state machine (FSM) indications between the two participating PHAST-12N devices. The interface consists of two point-to-point interfaces: one will transport payload data and FSM indications from the worker lines to the protection line, the other will transport payload data and FSM indications from the protection line to the worker lines.

The FSM indications include:

- RxAPS: the K1/K2 APS code received from the receive line interface
- TxAPS: the K1/K2 APS code which needs to be sent on the transmit line interface
- Status: the status of the received line, including the signal failure and signal degrade conditions

- Request: actions requested by the finite state machine, including switch and bridge requests

The high order path cross connect will support bridge and switch operation.

10.11.3 APS Port Architecture

Figure 29 shows the Receive and Transmit APS Port interface in relation to the Receive and Transmit Line interface and high order cross connect function.

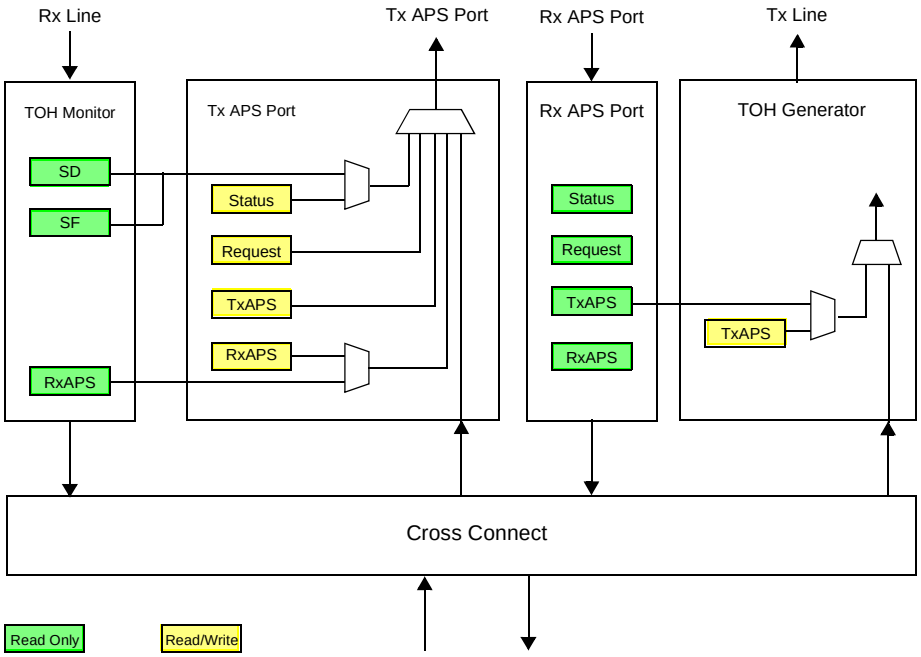


Figure 29. APS Port Architecture

The Tx APS Port interface sends the synchronous payload data from this PHAST-12N to its mate PHAST-12N.

It also allows the in-band forwarding of RxAPS, TxAPS, Status and Request:

- RxAPS: forwarded from the receive line interface, or optionally under software control
- TxAPS: under software (APS finite state machine) control
- Status: forwarded from the receive line interface, or optionally under software control
- Request: under software (APS finite state machine) control

The Rx APS Port interface receives the synchronous payload data from the mate PHAST-12N. It will also monitor the in-band forwarded of RxAPS, TxAPS, Status and Request indications. The TxAPS will be forwarded to the TOH Generator. The latter will have an option to insert the transmitted K1/K2 APS autonomously from the TxAPS on the Rx APS Port or from software controlled registers.

The functionality of the APS Interfaces described in "APS Interface" on page 96, the presence of the AU Pointer Tracker and the STM-4 like APS frame makes the APS port can be used as a STM-4 SONET Lite Port. Important limitation to know about this: the incoming B2 bytes are NOT processed by the APS Monitor. Remark also the APS port has LVDS I/Os while the Line Ports has LVPECL I/Os.

10.11.4 Example: STM-4/OC-12 Mode, 1+1 APS Protection

Figure 30 shows an example of a 1+1 APS protection architecture in STM-4/OC-12 mode. One PHAST-12N device handles the Worker line (W) while a second PHAST-12N handles the Protection line (P). Both devices are interconnected through the full bandwidth of APS Port interface. The cross connects of both devices setup a permanent bridge from the Worker Transmit line to the Protection Transmit line over one of the APS Port interfaces. The received protection payload is available on the other APS Port interface.

When the APS FSM detects a failure of the Worker line the cross connect of the Worker PHAST-12N performs the protection switch. It connects the receive protected traffic to the Receive APS Port interface which transports the payload of the received Protection line.

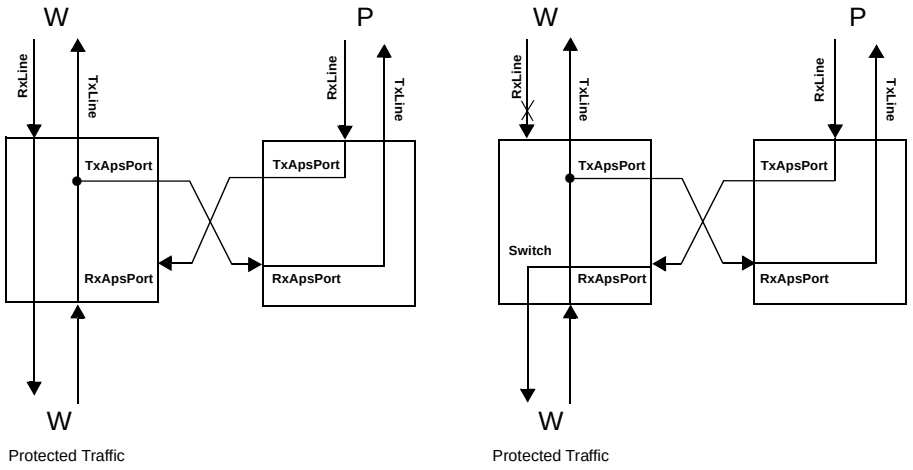


Figure 30. STM-4/OC-12, 1+1 APS

10.11.5 Example: STM-4/OC-12 Mode, 1:1 APS Protection

Figure 31 shows an example of a 1:1 APS protection architecture in STM-4/OC-12 mode. The setup is similar to the 1+1 case without the permanent bridge. This allows unprotected extra traffic to be transported over the Protection line while there is no protection request active.

When the APS FSM detects a failure of the Worker line the cross connect of the Protection PHAST-12N performs a protection bridge connecting the transmit protected traffic to the transmit Protection line. The Worker PHAST-12N performs the protection switch. It connects the protected traffic to the Receive APS Port interface which transports the payload of the received Protection line. The unprotected extra traffic is no longer available and will be squelched.

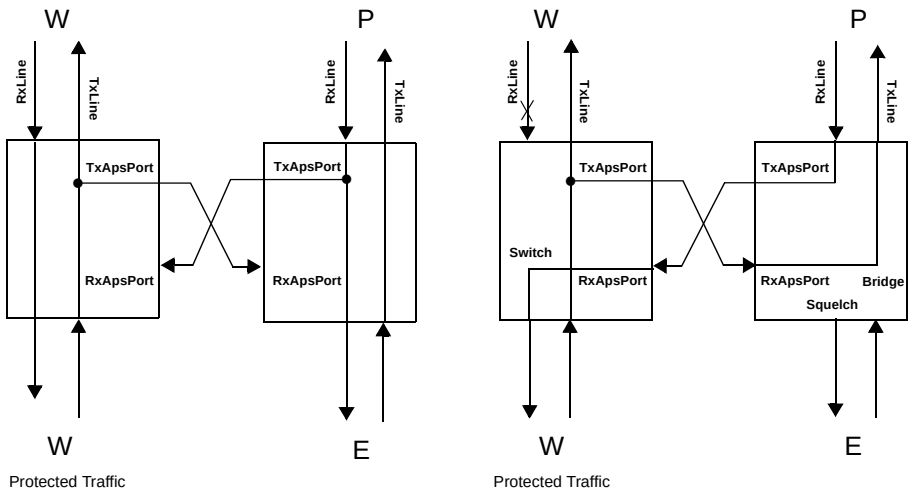


Figure 31. STM-4/OC-12, 1:1 APS

10.11.6 Example: STM-1 Mode, 1+1 APS Protection

Figure 32 shows an example of a 1+1 APS protection architecture in STM-1/OC-3 mode using two PHAST-12N devices. One PHAST-12N device handles up to four Worker lines (W) while a second PHAST-12N handles the associated Protection lines (P). Both devices are interconnected through the APS Port interface, using one fourth of the bandwidth per STM-1/OC-3 protection group. The cross connects of both devices setup permanent bridges from the Worker Transmit lines to their Protection Transmit lines over one of the APS Port interfaces. The received protection payload of the four lines is available on the other APS Port interface.

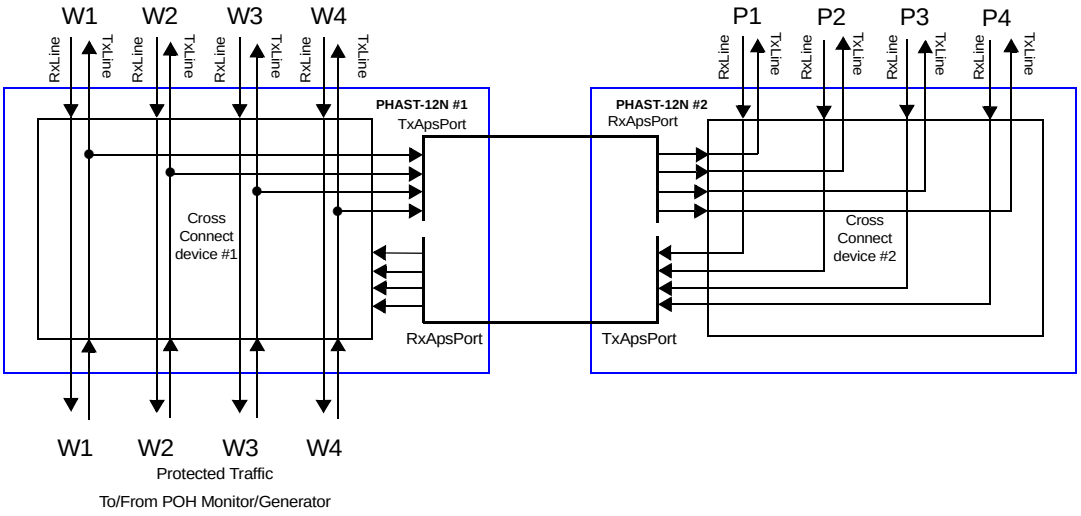


Figure 32. STM-1/OC-3, 1+1 APS Idle State

When the APS FSM detects a failure of one of the Worker lines, e.g., line #2 in Figure 33, the cross connect of the Worker PHAST-12N performs the protection switch. It connects the receive protected traffic of the failed line to the payload of its associated received Protection line available at the Receive APS Port interface.

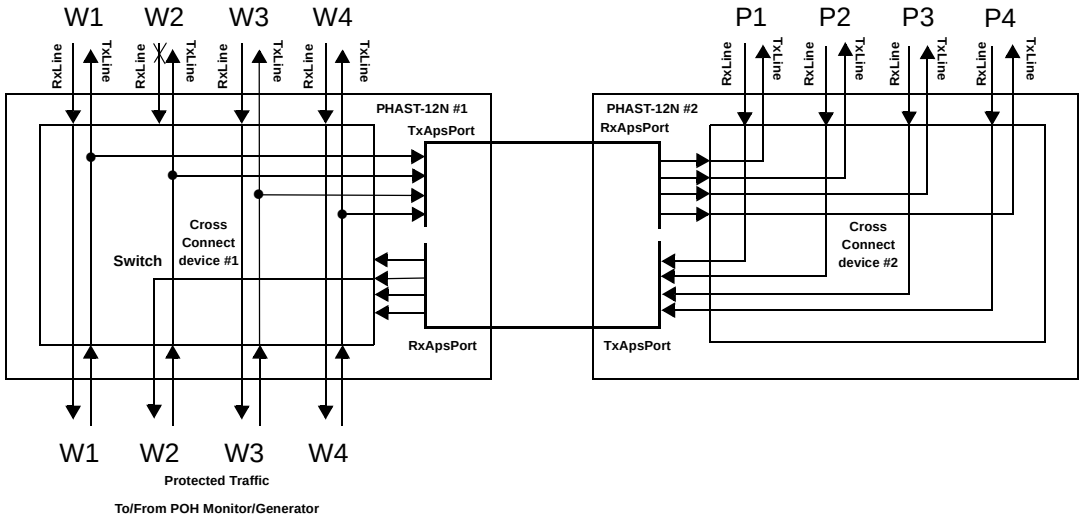


Figure 33. STM-1/OC-3, 1+1 APS Switch State

10.11.7 Example: STM-1 Mode, 1:1 APS Protection

Figure 34 shows an example of a 1:1 APS protection architecture in STM-1/OC-3 mode using two PHAST-12N devices. The setup is similar to the 1+1 case without the permanent bridge. This allows unprotected extra traffic to be transported over a Protection line while there is no protection request active at that line.

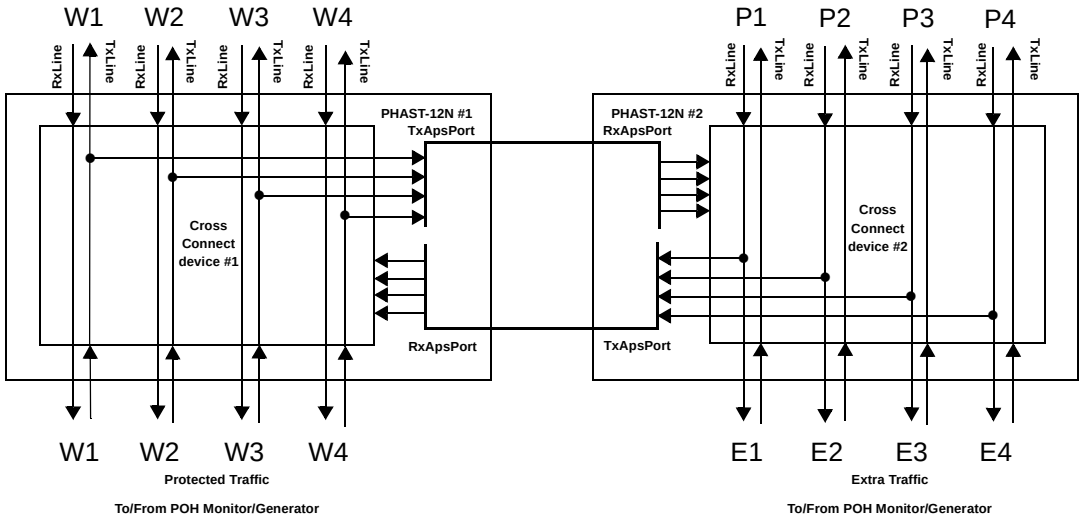


Figure 34. STM-1/OC-3, 1:1 APS Idle State

When the APS FSM detects a failure of one of the Worker lines, e.g., line #2 in Figure 35, the cross connect of the Protection PHAST-12N performs a protection bridge connecting the transmit protected traffic of the failed line to the transmit Protection line. The Worker PHAST-12N performs the protection switch. It connects the protected traffic of the failed line to the payload of its associated received Protection line available at the Receive APS Port interface. The unprotected extra traffic of that Protection line is no longer available and will be squelched.

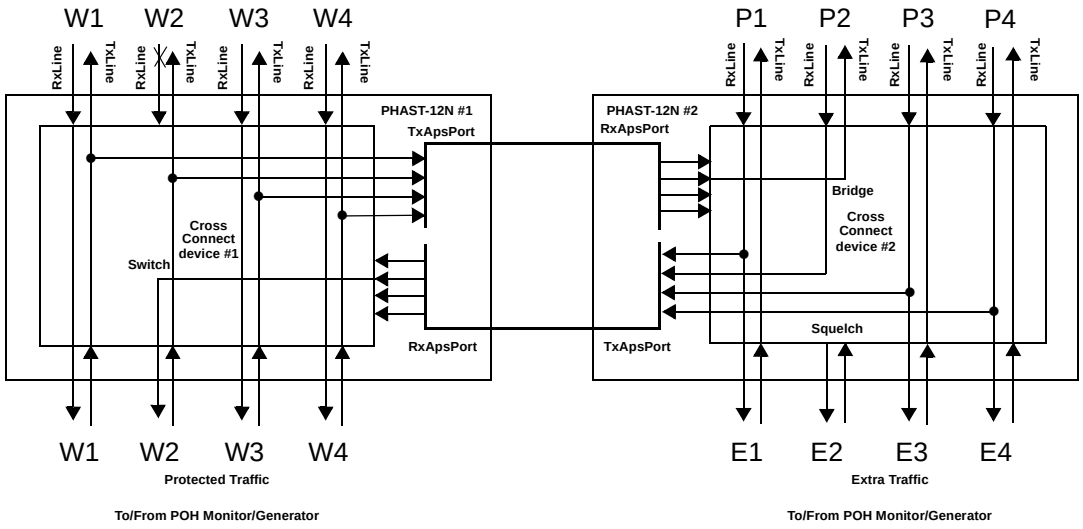


Figure 35. STM-1/OC-3, 1:1 APS Switch State

10.11.8 Example: STM-1 Mode, 1:n APS Protection

Figure 36 shows an example of a 1:n (n=7) APS protection architecture in STM-1/OC-3 mode using two PHAST-12N devices.

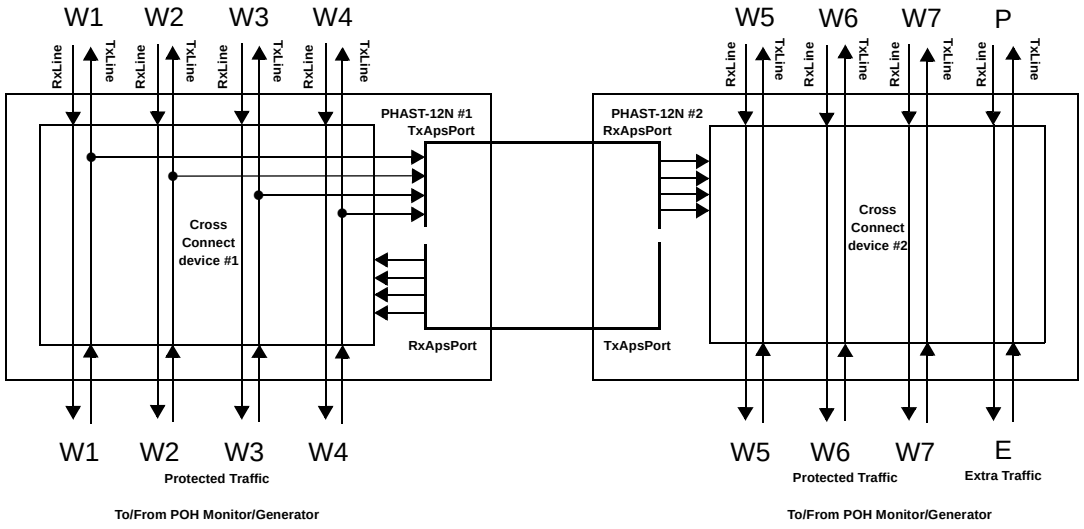


Figure 36. STM-1/OC-3, 1:7 APS Idle State

When the APS FSM detects a failure of one of the Worker lines, e.g., line #2 in Figure 37, the cross connect of PHAST-12N #2 performs a protection bridge connecting the transmit protected traffic of the failed line to the transmit Protection line. PHAST-12N #1 performs the protection switch. It connects the protected traffic of the failed line to the payload of its associated received Protection line available at the Receive APS Port interface. The unprotected extra traffic of that Protection line is no longer available and will be squelched.

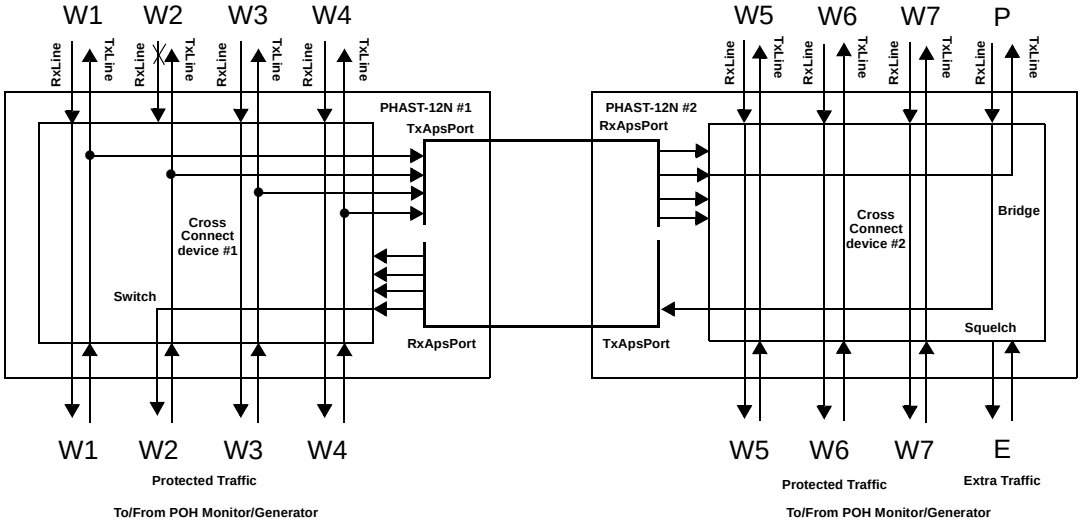


Figure 37. STM-1/OC-3, 1:7 APS Switch State

In case the failed line is terminated in PHAST-12N #2 itself, the cross connect of that PHAST-12N #2 will perform the protection switch without use of the APS port.

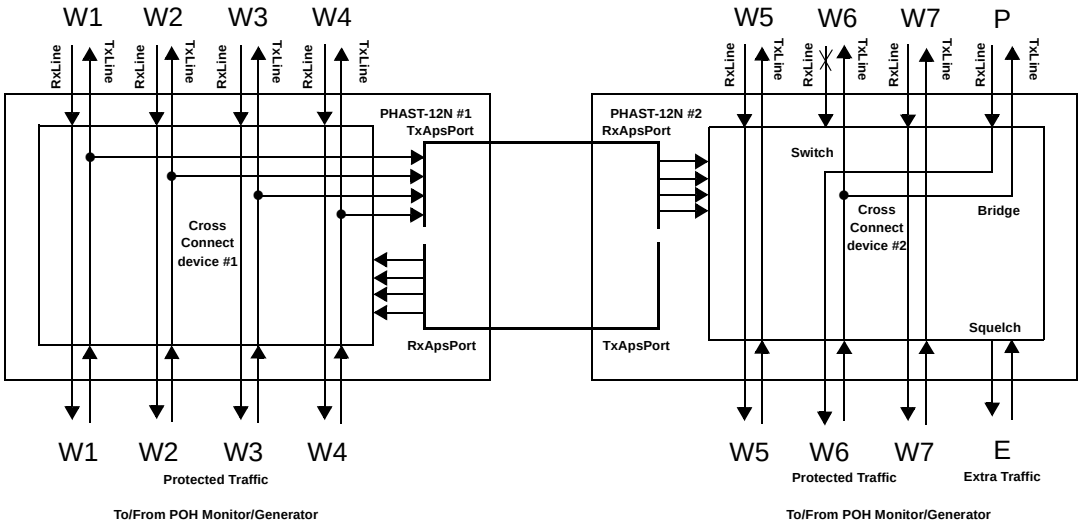


Figure 38. STM-1/OC-3, 1:7 APS Switch State

11.0 HIGH ORDER POINTER TRACKING, RETIMING AND POINTER GENERATION

11.1 LINE AND APS SIDE POINTER TRACKING, RETIMING AND POINTER GENERATION

The PHAST-12N will perform high order pointer processing and retiming on the H1/H2 pointer bytes from the received lines and from the APS Port.

The pointer tracking process will be performed according to the generic requirements for a SDH/SONET pointer tracker based on ETSI/ITU-T/ANSI standards.

The retiming process will retime the incoming OC-12/4*OC-3 lines and the received APS signal to the System Clock.

The path AIS (dAIS), loss of pointer (dLOP) and FifoError defect will be detected per high order path.

The PHAST-12N pointer tracker and retimer will insert AIS per high order path towards the high order cross connect according to the following expression:

$$
\begin{aligned}
aAIS_{[path]} \;=\; & dAIS_{[path]} * \text{not AU\_AIS\_AIS\_Insert\_Disable} \\
+\; & dLOP_{[path]} * \text{not LOP\_AIS\_Insert\_Disable} \\
+\; & dTSF_{[path]} * \text{not TSF\_AIS\_Insert\_Disable} \\
+\; & FifoError_{[path]} * \text{not FifoError\_AIS\_Insert\_Disable} \\
+\; & AIS\_Force_{[path]}
\end{aligned}
$$

Incoming and outgoing pointer increments and decrements will be counted for performance monitoring.

Received SS bits are reported by the pointer tracking process. SS bits to be generated by the retiming process are configurable.

11.2 DETECTION OF CONCATENATED STRUCTURES

The incoming pointer bytes are analyzed for concatenation indicators (Y1*). A Concatenation configuration is set up and locked after four identical configurations. A (latched) indication is given to software when a new configuration has been detected and the entire detected configuration is reported by 12 bits. A '1' means a concatenation indication (Y1*) has been detected on the pointer bytes of the corresponding timeslot.

Important note: This concatenation detector only detects the concatenation indicators of the incoming pointer bytes. The detected configuration only serves as status, reported to software and is never used to configure the pointer tracking process.

11.3 FRAME REFERENCE PULSES

A Frame Reference Pulse is necessary wherever timing has to be (re)generated in the PHAST-12N. The PHAST-12N can lock on an externally provided Frame Reference Pulse, making it possible to align with other devices, or generate the Frame Reference Pulse internally.

The (generated) System Frame Reference Pulse is available via the REFSYSFS lead.

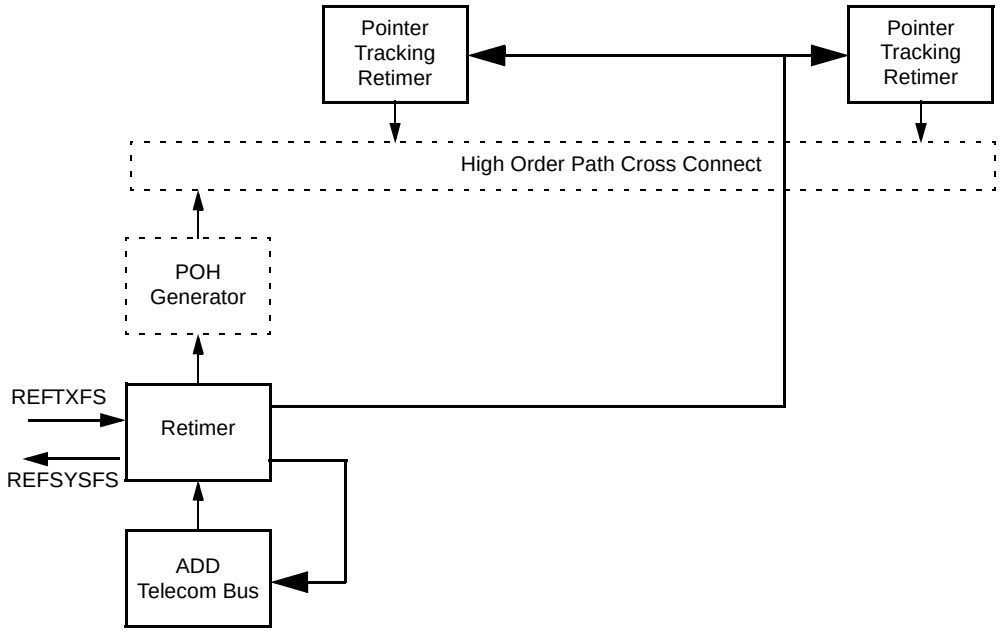


Figure 39. Frame Reference Pulse Generation

11.3.1 Generation of Frame Reference Pulse

A System Frame Reference Pulse is generated every 125 us (8 kHz) when **ExtFramePulseExpected** is deasserted. The generated System Frame Reference Pulse can be monitored or used by other devices in order to align with the PHAST-12N via the REFSYSFS lead. For the relationship between the System Frame Reference Pulse and the Add and Drop Telecom Bus timing, see Figure 17.

11.3.2 Locking on External Frame Reference Pulse

When **ExtFramePulseExpected** is asserted, the PHAST-12N will lock on an external Frame Reference Pulse (REFTXFS lead) and will generate a System Frame Reference Pulse. When the distance between two consecutive Frame Reference Pulses is not exactly 125 us, a Loss Of Frame defect (LOF) will be generated.

This LOF defect is cleared as soon as two consecutive pulses with a distance of 125 us have been received. The System Frame Reference Pulse will still be generated during LOF state, locked on previously accepted Frame Pulse.

Sampling of the Frame Reference Pulse is configurable on the positive or the negative System Clock edge (**ExtFramePulseNegEdge**).

Optionally an offset between the external Frame Reference Pulse and the internal System Frame Reference Pulse can be provided (**ExtFramePulseOffset**).

The generated System Frame Reference Pulse can be monitored via the REFSYSFS lead.

The relationship between REFTXFS and REFSYSFS is represented in Figure 16.

11.4 TERMINAL SIDE RETIMING AND POINTER GENERATION

The Add Telecom Bus interface has two operational modes: Master mode and Slave mode.

When the Add Telecom Bus interface is operating in slave mode, the SDH/SONET stream has to be retimed from the CBADCLK to the System Clock. This retiming is performed in the Retimer block. Therefore the setting **COMBUS_Bypass** has to be deasserted in the Retimer block.

No retiming is necessary when the Add Telecom Bus interface is operating in master mode. Sourced VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE channels will have a AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c pointer value fixed to 0 or 522 in this case. This value has to be configured both in the Add Telecom Bus interface and in the Terminal Pointer Generator. **COMBUS_Bypass** has to be asserted in this mode.

SS bits are configurable in both cases.

11.5 RETIMER FIFO LEAK REGISTERS

All Retimers in PHAST-12N are able to reduce the number of pointer justifications to reduce jitter on AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c pointers.

To provide this ability, the FIFO size is 29 words and the filling level of the FIFO is divided into several zones, as depicted in Figure 40.

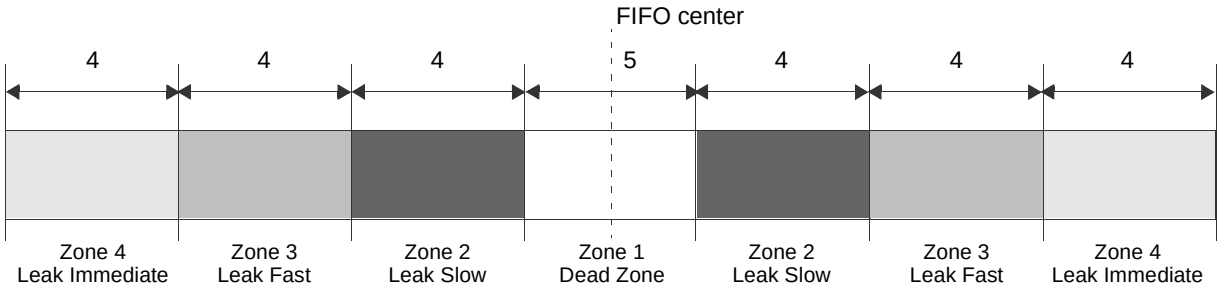


Figure 40. Retimer FIFO Filling Levels

The center zone is called Dead Zone and is 5 words wide. In this zone, the FIFO is at half filling and no pointer adjustments will be made.

If the FIFO is almost empty or almost full, immediate action is required. These filling levels are called Immediate Leak Zone. This zone is 4 words wide at each end of the filling level. If the

FIFO filling level is in one of these zones, as much pointer justifications as allowed will be generated to adjust the filling level towards the dead zone, resulting in one justification generated every four SDH/SONET frames.

The remaining zones are the Slow Leak Zone and the Fast Leak Zone. Each of these zones is also 4 words wide. These are the zones that allow smoothing out jitter on the AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c pointer values. The mechanism used to obtain this uses a Justification Spacing counter per timeslot. This counter maintains a fixed distance between two consecutive Pointer Justifications and is used as long as the FIFO filling level is situated inside the Slow or Fast leak zones. The initial value for these countdown counters is set to the value provided by **SlowLeakRegister** or **FastLeakRegister**, according to the current zone.

Efficient smoothing out of the jitter can be obtained by providing accurate values for **SlowLeakRegister** and **FastLeakRegister**.

11.6 HIGH ORDER PATH OVERHEAD PROCESSING

The PHAST-12N device is compliant to the latest ITU/ETSI/ANSI standards and features regarding the generation and monitoring of the high order Path Overhead bytes.

11.6.1 High Order Path Overhead Generator

The PHAST-12N generates the high order path overhead bytes of all sourced VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c channels.

- A single, 16 or 64 byte Trail Trace Identifier stored in the transmit POH RAM will be inserted in the J1 byte. Note that in case of a single or 16 byte Trail Trace Identifier the message must be repeated respectively 64 or 4 times.
- BIP-8 will be calculated over all bits of the preceding VC-n frame and will be inserted in the B3 byte of the current frame. The B3 byte in the transmit POH RAM is used as an errormask to corrupt the calculated B3 byte.
- The TSL signal label stored in the transmit POH RAM will be inserted in the C2 byte
- Per high order path the REI can be sourced from
  - The transmit POH RAM
  - The transmit POH byte interface
  - The internal or external ring port
- The REI will be inserted into the G1 byte
- Per high order path the RDI can be sourced from
  - The transmit POH RAM
  - The transmit POH byte interface
  - The internal or external ring port

- The internal or external ring port can be selected as source for RDI/E-RDI.
  If **OneBitRDI** is deasserted, E-RDI will be encoded as follows (ordered from high to low priority):

E-RDI indication	b5	b6	b7
Server	1	0	1
Connectivity	1	1	0
Payload	0	1	0
None	0	0	1

If **OneBitRDI** is asserted, RDI will be generated as follows:

E-RDI indication	b5	b6	b7
Server	1	0	0
Connectivity	1	0	0
Payload	0	0	0
None	0	0	0

- The RDI will be inserted into the G1 byte
- Per high order path the G1 spare bit can be sourced from
  - The transmit POH RAM
  - The transmit POH byte interface
- If the unidirectional option is active, 0x00 will be inserted in the G1 byte
- The F2 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- The H4 byte will be
  - Inserted from the transmit POH RAM
  - Inserted from the transmit POH byte interface
  - Passed
  - Generated based on incoming multiframe index
- The F3 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- The K3 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface

- The N1 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- Optionally insertion of VC-AIS, resulting in the insertion of all 1's in the entire VC
- Optionally insertion of Unequipped, resulting in the insertion of all 0's in the entire VC
- Optionally insertion of Supervisory Unequipped, resulting in the insertion of all 0's in the entire VC except for the POH bytes J1, B3 and G1
- Optionally bypass the POH generation: the entire high order path is just passed through

11.6.2 High Order Path Overhead Monitor

The PHAST-12N monitors the high order path overhead bytes on all incoming high order channels and terminates the path overhead bytes on all dropped channels.

- Optionally the single, 16 or 64 byte Trail Trace Identifier in the J1 byte will be monitored and the dTIM and dTTIZERO defects will be detected. For more information about the TTI process see "Trail Trace Identifier Process" on page 137
- Optionally the accepted Trail Trace Identifier and stable indications will be reported for one configurable high order path. For more information about the reporting of TTI see "Trail Trace Identifier Process" on page 137
- BIP-8 will be calculated over all bits of the preceding VC-n frame and will be compared to the B3 byte of the current frame
  - If one or more errors are detected, both a NearEndDefect_BlockCounter (1 block = 1 frame with 1 or more bit errors) and a NearEndDefect_BitCounter will be updated
  - The error counter per frame will be forwarded to the internal and external ring ports as REI indication
  - The dDEG defect will be detected for bursty or Poisson error distributions. For more information about these processes see "BER Supervision for B2/B3" on page 134
  - The dEXC defect will be detected for Poisson error distribution. For more information about this process see "BER Supervision for B2/B3" on page 134
  - During incoming SSF, the counters are not updated and the value 0 is forwarded to the ring ports
- Received C2 is debounced on a 5 frames basis
  - Accepted C2 is reported
  - Changes in accepted C2 are reported
  - The dUNEQ defect will be detected when the accepted C2 equals the unequipped activation pattern 0x00
  - The dAIS defect will be detected when the accepted C2 equals the AIS activation pattern 0xff
  - The dPLM defect will be detected when the accepted C2 does not equal the expected TSL code or the "equipped non-specific" 0x01
- If one or more errors are indicated by the REI G1, the FarEndDefect_Counter will be updated.
  - Optionally bit errors will be counted

- During incoming SSF, the counter is not updated

- Received RDI (3 bit) is debounced on a configurable number of frames basis (ETSI: 3, 5 Telcordia: 10)
  - The dRDI, E-RDI Server, E-RDI Connectivity and E-RDI Payload defects will be detected according to the following table:

b5	b6	b7	Defects
0	0	0	No defect
0	0	1	No defect
0	1	0	dRDI-P
0	1	1	No defect
1	0	0	dRDI and dRDI-S
1	0	1	dRDI and dRDI-S
1	1	0	dRDI and dRDI-C
1	1	1	dRDI and dRDI-S

  - During incoming SSF or when the unidirectional option is active, all RDI defects are cleared
- Optionally the H4 byte is be monitored for the low order multiframe sequence
  - The dLOM defect will be detected in case a low order multiframe is expected
- Received K3 is debounced on a 3 frame basis
  - Accepted K3 is reported
  - Changes in accepted K3 are reported
- AIS will be inserted per high order path according to the following expression:

$$\begin{aligned} aTSF_{[path]} &= dAIS_{[path]} * \text{not AIS\_AIS\_Insert\_Disable} \\ &+ dSSF_{[path]} * \text{not SSF\_AIS\_Insert\_Disable} \\ &+ dEXC_{[path]} * \text{not EXC\_AIS\_Insert\_Disable} \\ &+ dUNEQ_{[path]} * \text{not UNEQ\_AIS\_Insert\_Disable} \\ &+ dTIM_{[path]} * \text{not TIM\_AIS\_Insert\_Disable}_{[path]} \end{aligned}$$

$$\begin{aligned} aAIS_{[path]} &= AI\_TSF_{[path]} \\ &+ dPLM_{[path]} * \text{not PLM\_AIS\_Insert\_Disable} \\ &+ dLOM_{[path]} * \text{not LOM\_AIS\_Insert\_Disable} \\ &+ AIS\_Force_{[path]} \end{aligned}$$

- RDI will be inserted per high order path according to the following expressions:

$$aE\text{-}RDI\text{-}S_{[path]} = dSSF_{[path]} * \text{not SSF\_RDI\_Insert\_Disable}$$

$$aE\text{-}RDI\text{-}C_{[path]} = dUNEQ_{[path]} * \text{not UNEQ\_RDI\_Insert\_Disable} + dTIM_{[path]} * \text{not TIM\_RDI\_Insert\_Disable}$$

$$aE\text{-}RDI\text{-}P_{[path]} = dPLM_{[path]} * \text{not PLM\_RDI\_Insert\_Disable}$$

$$aRDI_{[path]} = aE\text{-}RDI\text{-}S_{[path]} + aE\text{-}RDI\text{-}C_{[path]}$$

- The defect correlations are applied as follows:

$$cSSF_{[path]} = dSSF_{[path]} + dAIS_{[path]} * \text{not AIS\_SSF\_Contribution\_Disable}$$

$$cAIS_{[path]} = dAIS_{[path]}$$

$$cUNEQ_{[path]} = dUNEQ_{[path]} * (\text{not } dSSF_{[path]} + \text{SSF\_UNEQ\_Inhibit\_Disable}) * (dTTIZERO_{[path]} + \text{TTIZERO\_UNEQ\_Contribution\_Disable}) * (dTIM_{[path]} + \text{TIM\_UNEQ\_Contribution\_Disable})$$

$$cTIM_{[path]} = dTIM_{[path]} * (\text{not } dSFF_{[path]} + \text{SSF\_TIM\_Inhibit\_Disable}) * (\text{not } dUNEQ_{[path]} * \text{not UNEQ\_TIM\_Inhibit\_Disable} + \text{not } dTTIZERO_{[path]} * \text{not TTIZERO\_TIM\_Inhibit\_Disable} + \text{UNEQ\_TIM\_Inhibit\_Disable} * \text{TTIZERO\_TIM\_Inhibit\_Disable})$$

$$cTTIZERO_{[path]} = dTTIZERO_{[path]} * (\text{not } dSSF_{[path]} + SSF\_TTIZERO\_Inhibit\_Disable)$$

$$cDEG_{[path]} = dDEG_{[path]} * (\text{not } dSSF_{[path]} + SSF\_DEG\_Inhibit\_Disable) * (\text{not } dTIM_{[path]} + TIM\_DEG\_Inhibit\_Disable)$$

$$cEXC_{[path]} = dEXC_{[path]} * (\text{not } dSSF_{[path]} + SSF\_EXC\_Inhibit\_Disable) * (\text{not } dTIM_{[path]} + TIM\_EXC\_Inhibit\_Disable)$$

$$cPLM_{[path]} = dPLM_{[path]} * (\text{not } AI\_TSF_{[path]} + TSF\_PLM\_Inhibit\_Disable)$$

$$cLOM_{[path]} = dLOM_{[path]} * (\text{not } AI\_TSF_{[path]} + TSF\_LOM\_Inhibit\_Disable) * (\text{not } dPLM_{[path]} + PLM\_LOM\_Inhibit\_Disable)$$

$$cE\text{-}RDI(-S)(-C)(-P)_{[path]} = dE\text{-}RDI(-S)(-C)(-P)_{[path]} * (\text{not } dSSF_{[path]} + SSF\_RDI\_Inhibit\_Disable) * (\text{not } dUNEQ_{[path]} * \text{not } UNEQ\_RDI\_Inhibit\_Disable + \text{not } dTTIZERO_{[path]} * \text{not } TTIZERO\_RDI\_Inhibit\_Disable + UNEQ\_RDI\_Inhibit\_Disable * TTIZERO\_RDI\_Inhibit\_Disable) * (\text{not } dTIM_{[path]} + TIM\_RDI\_Inhibit\_Disable)$$

- Optionally bypass the POH monitor: the entire high order path is passed through without processing.
  Note: The High order POH Monitor should be bypassed for unused high-order paths.

11.7 TOH PORT INTERFACE

The transmit TOH port interface allows insertion of the RSOH and MSOH bytes into the TOH.

All received TOH bytes are output on the receive TOH port interface.

Each interface consists of clock, data, data enable, address and address enable lines.

The address is a 10-bit word according to the (a, b, c) format specified by ITU-T G.707/Y.1322 clause 9.2.1 and Figure 9-1:

<table>
<tr><th>A9</th><th>A8</th><th>A7</th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Line Interface Mode</th></tr>
<tr><td colspan="4">Row number
a-1
(range 0 to 8)</td><td colspan="4">(Multi-)Column number
b-1
(range 0 to 8)</td><td colspan="2">STM-1/OC-3 Line
(range 0 to 3)</td><td>STM-1/OC-3 Mode</td></tr>
<tr><td colspan="4" rowspan="2"></td><td colspan="4" rowspan="2"></td><td colspan="2">Multi-Column Interleave Depth
c-1
(range 0 to 3)</td><td>STM-4/OC-12 Mode</td></tr>
</table>

11.7.1 Transmit TOH Port Interface

This port interface allows insertion of the RSOH and MSOH bytes into the TOH. The TOH port interface is used to request any of the TOH bytes for either one STM-4 or four STM-1 frames from the outside world. Note the BIP bytes (B1, B2) have a special meaning, these can be used as an error mask on the calculated BIP.

The Transmit TOH Port consists of following leads:

- Output Transmit TOH Port Clock TOHTXCLK
- Output Transmit TOH Port Address Latch Enable TOHTXALE
- Output Transmit TOH Port Address TOHTXADDR
- Output Transmit TOH Port Data Latch Enable TOHTXDLE
- Input Transmit TOH Port Data TOHTXDATA

The transmit TOH Port protocol is as follows (see Figure 9):

1. The 10-bit address for the requested byte is output on TOHTXADDR, most significant bit first. During this time the Address Latch Enable TOHTXALE is asserted.
2. A one cycle gap is left open.
3. The Data Latch Enable TOHTXDLE is asserted and the 8-bit data word is sampled on the input TOHTXDATA, most significant bit first.

Note: Configuration of the Transmit TOH Port interface is done in the memory map of the TOH Generator (see **Table 29**). Selection of the TOH Port as source for a TOH byte is done in the TOH bytes internal memory by setting the most significant bit of the corresponding memory entry to '1'.

11.7.2 Receive TOH Port Interface

All received RSOH and MSOH bytes are sent over a serial Receive TOH Port interface. The values sent out on this interface are the raw, unprocessed values, except for B1 and B2, where an error mask is calculated (ones indicate the errored bits).

The Receive TOH Port consists of following leads:

- Output Receive TOH Port Clock TOHRXCLK
- Output Receive TOH Port Address Latch Enable TOHRXALE
- Output Receive TOH Port Address TOHRXADDR
- Output Receive TOH Port Data Latch Enable TOHRXDLE
- Output Receive TOH Port Data TOHRXDATA

The Receive TOH Port protocol is as follows (see Figure 8):

1. The 10-bit address for the transmitted byte is output on TOHRXADDR, most significant bit first. During this time the Address Latch Enable TOHRXALE is asserted.
2. A one cycle gap is left open.
3. The 8-bit data of the transmitted TOH byte is output on TOHRXDATA. During this time the Data Latch Enable TOHRXDLE is asserted.

Note: Configuration of the Receive TOH Port interface is done in the memory map of the TOH and DCC Port (see Table 32). The Receive TOH Port interface has to be enabled by the **TOH_Port_Enable** setting. No bytes will be sent out when this port is disabled.

11.8 DCC PORT INTERFACE

The Transmit and the Receive DCC Port interfaces provide an interface to the RS or MS DCC bytes. The interface is a constant bit-rate serial interface, each consisting of a clock and a data line.

11.8.1 Transmit DCC Port Interface

The Transmit DCC ports are constant bit-rate ports that provide a possible source for either the RS or the MS DCC bytes in the outgoing STM-4 or the four STM-1 frames. In STM-4 mode, only the first DCC Port is active.

Each Transmit DCC port can be configured for RS DCC bytes or MS DCC bytes:

RSOH_DCC_Select	Mode
0 (Default)	MS DCC bytes mode: the Transmit DCC port will request the MS DCC bytes.
1	RS DCC bytes mode: the Transmit DCC port will request the RS DCC bytes.

The Transmit DCC Port consists of following leads:

- Inputs Transmit DCC Data DCCTXDATA1..4
- Outputs Transmit DCC Clock DCCTXCLK1..4

The index indicates the port, one per transmit line. The Transmit DCC Clocks DCCTXCLK1..4 have a constant frequency and depend on the configured mode, as indicated in following table:

RSOH_DCC_Select	DCCTXCLK frequency (kHz)
0	576
1	192

Note: Configuration of the Transmit DCC Port interface is done in the memory map of the TOH Generator (see Table 29). The Transmit DCC port has to be enabled by the **DCC_Port_Enable** setting. If the Transmit DCC Port is disabled, the Transmit Port Clock DCCTXCLK output will be held low.

11.8.2 Receive DCC Port Interface

The Receive DCC ports are constant bit-rate ports that provide either the received RS DCC bytes or the received MS from the incoming STM-4 or the four STM-1 frames. In STM-4 mode, only the first DCC Port is active.

Each Receive DCC port can be configured for RS DCC bytes or MS DCC bytes:

RSOH_DCC_Select	Mode
0 (Default)	MS DCC bytes mode: the Receive DCC port will send the MS DCC bytes.
1	RS DCC bytes mode: the Receive DCC port will send the RS DCC bytes.

The Receive DCC Port consists of following leads:

- Outputs Receive DCC Data DCCRXDATA1..4
- Outputs Receive DCC Clock DCCRXCLK1..4

The index indicates the port, one per receive line. The Receive DCC Clocks DCCRXCLK1..4 have a constant frequency and depend on the configured mode, as indicated in following table:

RSOH_DCC_Select	DCCTXCLK frequency (kHz)
0	576
1	192

Note: Configuration of the Receive DCC Port interface is done in the memory map of the TOH and DCC Port (see Table 32). The Receive DCC port has to be enabled by the **DCC_Port_Enable** setting. If the Receive DCC Port is disabled, the Receive Port Clock DCCRXCLK output will be held low.

11.9 LINE ALARM INDICATION (RING) PORT INTERFACE

The Line Alarm Indication (Ring) Port Interface transports the Remote Information (RI) from the TOH sink/monitor to the TOH source/generator. The Remote Information consists of the REI and RDI values to be inserted by the TOH generator.

The TOH monitors send the Remote Information of all SDH/SONET lines to the Receive Line Alarm Indication (Ring) Port Interface. This port multicasts the information internally to the POH generator and externally to the Receive Alarm Indication (Ring) Port Interface.

The source for the Remote Information can be selected in the TOH generator, per SDH/ SONET line. When the Remote Information is taken from the Transmit Line Alarm Indication (Ring) Port Interface, it is possible to configure the Line Alarm Indication (Ring) Port Interface to use the internally or externally available information.

11.9.1 Internal Line Alarm Indication (Ring) Port Interface

When sink and source are handled on one device, the internal ring port can be used (**ExternalSourceSelect** deasserted). The Transmit Line Alarm Indication (Ring) Port Interface leads must then be connected to VSS.

Figure 41 shows the use of the internal Line Alarm Indication (Ring) Port Interface.

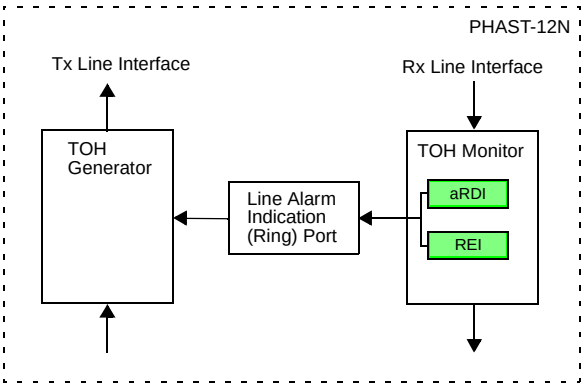


Figure 41. Internal Line Alarm Indication (Ring) Port Interface

11.9.2 External Line Alarm Indication (Ring) Port Interface

The external Line Alarm Indication (Ring) Port Interface is necessary when sink and source are processed on two different devices. The Receive Line Ring Port / Alarm Interface of the sink has to be connected to the Transmit Line Ring Port / Alarm Interface of the source and the external source mode has to be selected (**ExternalSourceSelect** asserted).

Figure 42 shows the use of the external Line Alarm Indication (Ring) Port Interface.

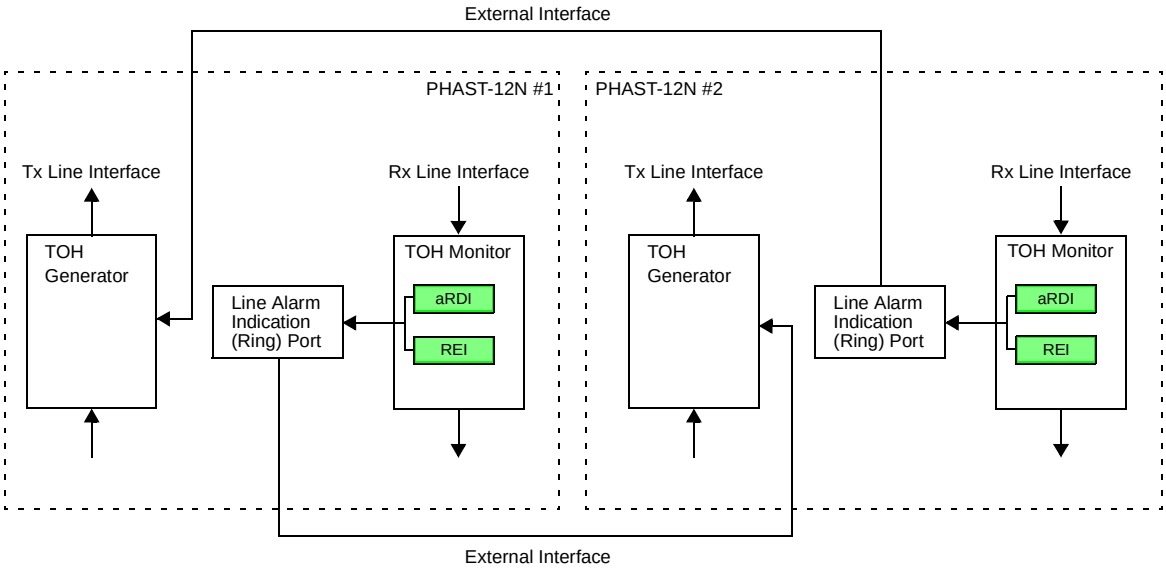


Figure 42. External Line Alarm Indication (Ring) Port Interface

The external interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the Line Alarm Indication (Ring) Port data frame.

The Receive Line Alarm Indication (Ring) Port Interface consists of following leads:

- Output Receive Line Alarm Indication (Ring) Port clock LRPRXCLK
- Output Receive Line Alarm Indication (Ring) Port frame sync LRPRXFS
- Output Receive Line Alarm Indication (Ring) Port data LRPRXDATA

The Transmit Line Alarm Indication (Ring) Port Interface consists of following leads:

- Input Transmit Line Alarm Indication (Ring) Port clock LRPTXCLK
- Input Transmit Line Alarm Indication (Ring) Port frame sync LRPTXFS
- Input Transmit Line Alarm Indication (Ring) Port data LRPTXDATA

Refer to Figure 12 and Figure 13 for timing diagrams.

11.10 HIGH ORDER POH PORT INTERFACE

The transmit POH port interface allows insertion of the POH bytes.

All received High Order POH bytes are output on the receive High Order POH port interface.

Each interface consists of clock, data, data enable, address and address enable lines.

The address is an 8-bit word with following format:

A7	A6	A5	A4	A3	A2	A1	A0
High Order path number				POH byte identification			

The least significant nibble identifies the POH byte on the High Order POH Port Interface:

A3	A2	A1	A0	POH Byte
0	0	0	0	J1
0	0	0	1	B3
0	0	1	0	C2
0	0	1	1	G1
0	1	0	0	F2
0	1	0	1	H4
0	1	1	0	F3
0	1	1	1	K3
1	0	0	0	N1

The most significant nibble identifies the High Order path number:

A7	A6	A5	A4	Assigned to
0	0	0	0	VC-3/STS-1 SPE #1 or VC-4/STS-3c SPE #1
0	0	0	1	VC-3/STS-1 SPE #2
0	0	1	0	VC-3/STS-1 SPE #3
0	0	1	1	VC-3/STS-1 SPE #4 or VC-4/STS-3c SPE #2
0	1	0	0	VC-3/STS-1 SPE #5
0	1	0	1	VC-3/STS-1 SPE#6
0	1	1	0	VC-3/STS-1 SPE #7 or VC-4/STS-3c SPE #3
0	1	1	1	VC-3/STS-1 SPE #8
1	0	0	0	VC-3/STS-1 SPE #9
1	0	0	1	VC-3/STS-1 SPE #10 or VC-4/STS-3c SPE #4
1	0	1	0	VC-3/STS-1 SPE #11
1	0	1	1	VC-3/STS-1 SPE #12

A7	A6	A5	A4	Assigned to
1	1	0	0	NA
1	1	0	1	NA
1	1	1	0	NA
1	1	1	1	NA

Note the address corresponding to the master VC is used for concatenated structures. E.g., when mapping four VC-4/STS-3c's SPE in a STM-4/OC-12, only 0x0, 0x3, 0x6 and 0x9 will be valid values for A[7:4].

11.10.1 Transmit High Order POH Port Interface

The transmit High Order POH port interface allows inserting most High Order Path Overhead bytes into the High Order POH. J1 and C2 cannot be selected from the transmit High Order POH port interface, while the B3 BIP-8 can be used as error mask on the calculated BIP-8 for test purposes.

The Transmit POH Port consists of following leads:

- Output Transmit POH Port Clock POHTXCLK
- Output Transmit POH Port Address Latch Enable POHTXALE
- Output Transmit POH Port Address POHTXADDR
- Output Transmit POH Port Data Latch Enable POHTXDLE
- Input Transmit TOH Port Data POHTXDATA

The Transmit POH Port protocol is as follows (see Figure 11):

1. The 8-bit address for the requested byte is output on POHTXADDR, most significant bit first. During this time the Address Latch Enable POHTXALE is asserted.
2. A one cycle gap is left open.
3. The Data Latch Enable POHTXDLE is asserted and the 8-bit data word is sampled on the input POHTXDATA, most significant bit first.

Note: No configuration is necessary for the Transmit POH Port. The source of the POH bytes can be configured in the memory map of the POH Generator (see Table 82).

11.10.2 Receive High Order POH Port Interface

All received High Order Path Overhead bytes are sent over a serial Receive POH Port interface. The values sent out on this interface are the raw, unprocessed values, except for B3, where an error mask is calculated (ones indicates the errored bits).

The Receive POH Port consists of following leads:

- Output Receive POH Port Clock POHRXCLK
- Output Receive POH Port Address Latch Enable POHRXALE
- Output Receive POH Port Address POHRXADDR
- Output Receive POH Port Data Latch Enable POHRXDLE
- Output Receive POH Port Data POHRXDATA

The Receive POH Port protocol is as follows (see Figure 10):

1. The 8-bit address for the transmitted byte is output on POHRXADDR, most significant bit first. During this time the Address Latch Enable POHRXALE is asserted.
2. A one cycle gap is left open.
3. The 8-bit data of the transmitted TPOH byte is output on POHRXDATA. During this time the Data Latch Enable POHRXDLE is asserted.

Note: No configuration is necessary for this POH Port.

11.11 HIGH ORDER ALARM INDICATION (RING) PORT INTERFACE

The High Order Alarm Indication (Ring) Port Interface transports the Remote Information (RI) from the High Order POH sink/monitor to the POH source/generator. The Remote Information consists of the REI and (enhanced) RDI values to be inserted by the POH generator.

The High Order POH monitor sends the Remote Information of all High Order path channels to the Receive High Order Alarm Indication (Ring) Port Interface. This port multicasts the information internally to the POH generator and externally to the Receive Alarm Indication (Ring) Port Interface.

The source for the Remote Information can be selected in the POH generator, per high order path. When the Remote Information is taken from the Transmit High Order Alarm Indication (Ring) Port Interface, it is possible to configure the High Order Alarm Indication (Ring) Port Interface to use the internally or externally available information.

When the **ExtendRDI** option is asserted, the RDI insertion will be extended to minimum 20 frames.

11.11.1 Internal High Order Alarm Indication (Ring) Port Interface

When sink and source are handled on one device, the internal ring port can be used (**SelectExternalSource** deasserted). The Transmit High Order Alarm Indication (Ring) Port Interface leads must then be connected to VSS.

Figure 43 shows the use of the internal High Order Alarm Indication (Ring) Port Interface.

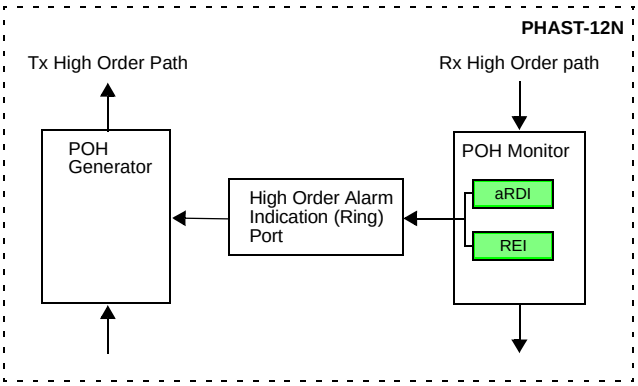


Figure 43. Internal High Order Alarm Indication (Ring) Port Interface

11.11.2 External High Order Alarm Indication (Ring) Port Interface

The external High Order Alarm Indication (Ring) Port Interface is necessary when sink and source are processed on two different devices. The Receive High Order Path Ring Port / Alarm Interface of the sink has to be connected to the Transmit High Order Path Ring Port / Alarm Interface of the source and the external source mode has to be selected (**SelectExternalSource** asserted).

Figure 44 shows the use of the external High Order Alarm Indication (Ring) Port Interface.

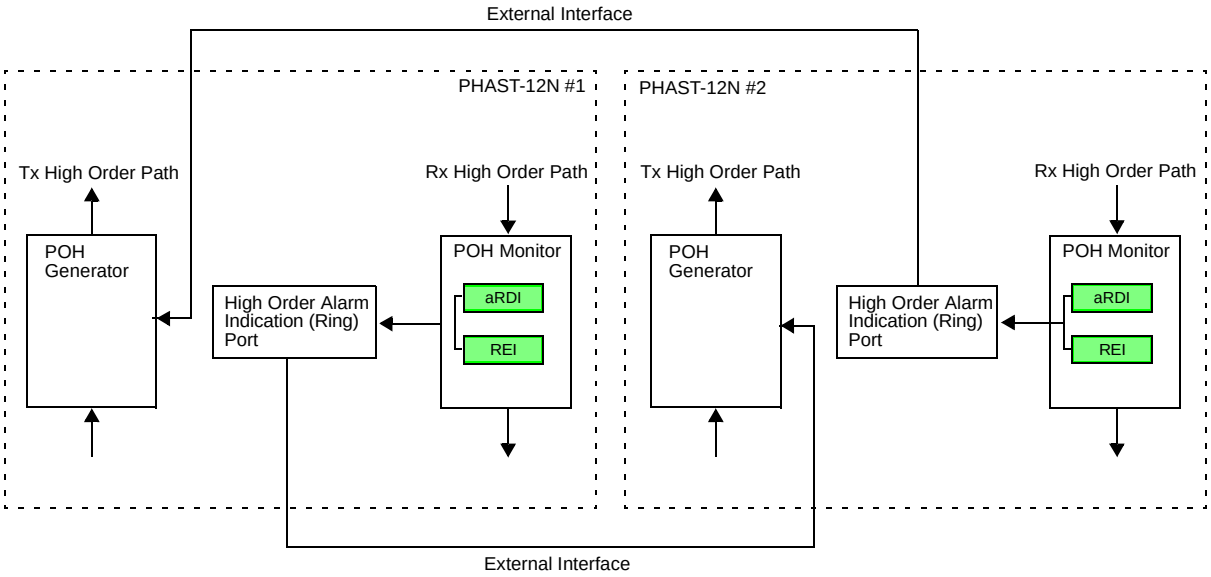


Figure 44. External High Order Alarm Indication (Ring) Port Interface

The external interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the High Order Alarm Indication (Ring) Port data frame.

The Receive High Order Alarm Indication (Ring) Port Interface consists of following leads:

- Output Receive High Order Alarm Indication (Ring) Port clock PRPRXCLK
- Output Receive High Order Alarm Indication (Ring) Port frame sync PRPRXFS
- Output Receive High Order Alarm Indication (Ring) Port data PRPRXDATA

The Transmit High Order Alarm Indication (Ring) Port Interface consists of following leads:

- Input Transmit High Order Alarm Indication (Ring) Port clock PRPTXCLK
- Input Transmit High Order Alarm Indication (Ring) Port frame sync PRPTXFS
- Input Transmit High Order Alarm Indication (Ring) Port data PRPTXDATA

Refer to Figure 13 and Figure 14 for timing diagrams.

12.0 TELECOM BUS

12.1 DROP BUS INTERFACE

The Drop bus consists of the following leads:

- Output data CBDPD(7-0)
- Output parity CBDPPAR
- Output clock CBDPCLK
- Output J0, J1, and optional V1 marker pulses CBDPJ0J1
- Output payload indication CBDPSPE

J0 and J1 marker pulses are always present on the CBDPJ0J1 lead. A V1 marker pulse will be present when TUG-2 is mapped in the SDH/SONET stream (see "SDH/SONET Mapping" on page 85). i.e., when lower-order is mapped in the SDH/SONET traffic.

The Drop bus always outputs all bytes on the bus. The H1/H2 pointer bytes are always inserted. Other TOH bytes are don't cares and must be ignored.

The most significant bit (MSB) of the output data is assigned to CBDPD7. The MSB is defined as the first bit received in a SDH/SONET byte. The bus rate is 77.76 MHz.

The active CBDPCLK clock edge on which the data and timing signals are clocked out can be selected.

Output_SelectNegativeClockEdge (see Table 80)	Active CBDPCLK clock edge
0	Output signals are clocked out on positive CBDPCLK clock edge.
1	Output signals are clocked out on negative CBDPCLK clock edge.

12.1.1 Drop Bus Parity Selection

The parity selection for the Drop bus is according to the following table. The calculated parity is output on the CBDPPAR lead.

ParityEven (see Table 80)	ParityIncludesTiming (see Table 80)	Drop Bus Parity Selection
0	0	Odd parity is calculated for the data output leads CBDPD(7-0).
0	1	Odd parity is calculated for the data and timing output leads, CBDPD(7-0), CBDPJ0J1 and CBDPSPE.

ParityEven (see Table 80)	ParityIncludesTiming (see Table 80)	Drop Bus Parity Selection
1	0	Even parity is calculated for the data output leads CBDPD(7-0).
1	1	Even parity is calculated for the data and timing output leads, CBDPD(7-0), CBDPJ0J1 and CBDPSPE.

12.1.2 Drop Bus Delay

With control field **TimingDelay**, see Table 80 of the Memory Maps and Bit Descriptions section, an additional delay of 0 up to 15 extra CBDPCLK clock cycles can be inserted between the Drop bus data/parity and the Drop bus timing signals, CBDPJ0J1 and CBDPSPE. All Drop bus outputs are delayed one clock cycle when control field **TimingDelay** is set to 1.

12.1.3 Drop Bus High Impedance

The Drop Telecom Bus interface can tristate each type of container it carries:

- **AUG-1**: The data and parity corresponding to an AUG-1 can be forced into a high impedance state by setting control field **AUG1_HighZ_Config** (see Table 81 of the Memory Maps and Bit Descriptions) to high for the particular AUG-1. (4 bits, LSB corresponds to AUG-1 #1). Each AUG-1 can be configured independently. When an AUG-1 is not tristated all its subcontainers (AU-4, AU-3) are also automatically out of tristate. In concatenated mode (e.g., VC4-4c, VC4-2c), the AUG1 HighZ configuration for the master AUG1 is copied to the slave AUG1's. This is done to avoid user errors in the configuration, which would result in useless behaviour since, e.g., a VC4-4c with half it's timeslots in tristate wouldn't make sense.

- **AU-4/STS-3c**: For this type of container, also the **AUG1_HighZ_Config** (see above) must be used.

- **AU-3/STS-1**: When operating in AU-3/STS-1 mode, the data and parity corresponding to individual AU-3/STS-1 can be forced into a high impedance state by setting register **VC3_TUG3_HighZ** (see Table 79 of the Memory Maps and Bit Descriptions) to 1. This control field is indirect accessible meaning that the control field **Config_Channel** (see Table 80 of the Memory Maps and Bit Descriptions) inside the same Drop Telecom Bus must also be set to indicate the desired AU-3/STS-1 timeslot.

12.2 ADD BUS INTERFACE

The Add bus consists of the following leads:

- Input data CBADD(7-0)
- Input parity CBADPAR

The timing information can be input or output:

- Input/Output clock CBADCLK
- Input/Output J0, J1, and optional V1 marker pulses CBADJ0J1
- Input/Output payload indication CBADSPE

J0 and J1 marker pulses are always expected on the CBADJ0J1 lead. A V1 pulse is expected when the SDH/SONET traffic contains lower-order (see "SDH/SONET Mapping" on page 85).

The most significant bit (MSB) of the output data is assigned to CBADD7. The MSB is defined as the first bit received in a SDH/SONET byte. The bus rate is 77.76 MHz.

The CBADCLK clock edge on which the data (and optionally timing) signals are clocked in can be selected.

Sample_SelectNegativeClockEdge (see Table 70)	Active CBADCLK clock edge
0	Input signals are sampled on positive CBADCLK clock edge.
1	Input signals are sampled on negative CBADCLK clock edge.

The active CBADCLK clock edge on which the timing signals are clocked out can be selected.

Output_SelectNegativeClockEdge (see Table 70)	Active CBADCLK clock edge
0	Output signals are clocked out on positive CBADCLK clock edge.
1	Output signals are clocked out on negative CBADCLK clock edge.

12.2.1 Add Bus Timing Modes

The CBADT lead selects the Master (timing signals are output) or Slave (timing signals are input) timing mode on the Add bus interface.

Lead CBADT	Add Bus Timing Mode
Low	Master Timing Mode: The Add bus timing leads, CBADCLK, CBADJ0J1, and CBADSPE, are Outputs. Refer to Figure 7.
High	Slave Timing Mode: The Add bus timing leads, CBADCLK, CBADJ0J1, and CBADSPE, are Inputs. Refer to Figure 6.

12.2.2 Add Bus Parity Selection

The parity selection for the Add bus is according to the following table. The calculated parity is compared to the value of the CBADPAR input lead. A parity error is indicated by the ParityError alarm, see Table 68. Other than an alarm indication, no action is taken by the PHAST-12N.

ParityEven (see Table 70)	ParityIncludesTiming (see Table 70)	Drop Bus Parity Selection
0	0	Odd parity is calculated for the data input leads CBADD(7-0).
0	1	Odd parity is calculated for the data and timing input leads, CBADD(7-0), CBADJ0J1 and CBADSPE (CBADT is high).
1	0	Even parity is calculated for the data input leads CBADD(7-0).
1	1	Even parity is calculated for the data and timing input leads, CBADD(7-0), CBADJ0J1 and CBADSPE (CBADT is high).

12.2.3 Add Bus Delay

With control field **TimingDelay**, see Table 70 of the Memory Maps and Bit Descriptions section, an additional delay of 0 up to 15 extra CBADCLK clock cycles can be inserted between the Add bus timing signals, CBADJ0J1 and CBADSPE, and the Add bus data/parity. All Add bus inputs are delayed one clock cycle when control field **TimingDelay** is set to 1, for all timing modes.

12.3 BER SUPERVISION FOR B2/B3

The PHAST-12N supports detection of the degraded signal (dDEG) and the excessive error (dEXC) defects for both line (B2 BIP-96 in STM-4/OC-12 mode, B2 BIP-24 in STM-1/OC-3 mode) and path (B3 BIP-8).

The assumed distribution of errors needs to be configured:

PoissonErrorCheck	Description
0 (Default)	Bursty distribution of errors is assumed (SDH).
1	Poisson distribution of errors is assumed (SONET).

12.3.1 Bursty Distribution of Errors

If a bursty distribution of errors is assumed, the excessive error defect is assumed to be false. The degraded signal defect detection is based on one second performance monitoring block error count.

Two sets of configuration registers are provided: one for setting the defect, one for clearing (to allow some hysteresis).

The degraded signal defect (dDEG) is declared if **DEG_DetectionWindowSize** consecutive bad intervals are detected - an interval is the one second period used for performance monitoring. For B2 (MSOH) an interval is declared bad if the number of errored blocks in that interval is greater than or equal to **DEG_DetectionErrorThreshold**. For B3 (POH) an interval is declared bad if the number of errored blocks in that interval is greater than **DEG_DetectionErrorThreshold**. Remark the slight difference between the B2 (MSOH) and B3 (POH) detectors configuration!

The degraded signal defect (dDEG) is cleared if **DEG_RecoveryWindowSize** consecutive good intervals are detected. An interval is declared good if the number of errored blocks in that interval is smaller than **DEG_RecoveryErrorThreshold**.

The parameters **DEG_DetectionWindowSize** and **DEG_RecoveryWindowSize** are provisionable in the range 2 to 10.

The threshold parameters **DEG_DetectionErrorThreshold** and **DEG_RecoveryErrorThreshold** are to be provisioned as a number of errored blocks in the range of 0 < threshold <= Number of blocks in the interval.

12.3.2 Poisson Distribution of Errors

If a Poisson distribution of errors is assumed, both the degraded signal and the excessive error defects need to be detected based on the accumulated BIP errors during intervals of configurable duration.

For each defect, two sets of configuration registers are provided: one for setting the defect, one for clearing (to allow some hysteresis).

The monitoring intervals for the degraded signal defect (dDEG) can be configured in steps of time base T. The value of time base T can be set to 500 µs or 125 µs via the **DEG_Use125usCounter** configuration.

The degraded signal defect (dDEG) is declared if the accumulated BIP error count since the start of the detection interval is greater than or equal to **DEG_DetectionErrorThreshold** errors. The interval duration is **DEG_DetectionWindowSize** * T.

The degraded signal defect (dDEG) is cleared if the accumulated BIP error count during the clearing interval is less than **DEG_RecoveryErrorThreshold** errors. The interval duration is **DEG_RecoveryWindowSize** * T.

The monitoring intervals for the excessive error defect (dEXC) can be configured in steps of time base T. The value of time base T can be set to 500 µs or 125 µs via the **EXC_Use125usCounter** configuration.

The excessive signal defect (dEXC) is declared if the accumulated BIP error count since the start of the detection interval is greater than or equal to **EXC_DetectionErrorThreshold** errors. The interval duration is **EXC_DetectionWindowSize** * T.

The excessive signal defect (dEXC) is cleared if the accumulated BIP error count during the clearing interval is less than **EXC_RecoveryErrorThreshold** errors. The interval duration is **EXC_RecoveryWindowSize** * T.

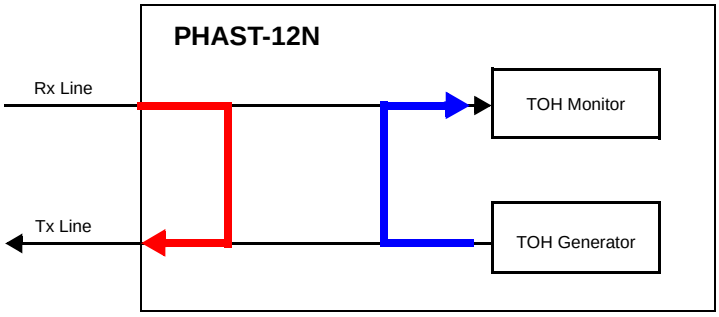
The Poisson detector can be configured to work in **BurstProtection** mode, in that case the configured error threshold needs to be exceeded during 2 consecutive intervals before the defect is declared. This way one can protect the state machine against a burst of BER errors.

For B3 (POH) the BIP error counters have a overflow behaviour (instead of saturation). For those counters a large DetectionErrorThreshold combined with a large DetectionWindowSize can lead to an overflow and avoid correct detection of the DEG/EXC signal defects. DetectionErrorThreshold and DetectionWindowSize (both for DEG and EXC detection) must always be configured in such way no overflow of the BIP error counter can occur. For B2 (TOH) the BIP error counters have a saturating behaviour and are thus not vulnerable to this.

12.4 LOOPBACKS

The PHAST-12N provides the following diagnostic loopbacks:

- Receive line interface looped back to the transmit line interface
- Transmit line interface looped back to the receive line interface



12.5 PERFORMANCE COUNTERS

The PHAST-12N supports the following performance counters:

- RS/section counters per line interface:
  - B1 error count, configurable to count either BIP errors or errored frames
- RS/section counters APS interface:
  - B1 errored frame count
- MS/line counters per line interface:
  - B2 near-end errored BIP count
  - B2 near-end Errored frame count
  - M1 far-end error count, configurable to count either REI errors or errored blocks
  - Near-end defect second
  - Far-end defect second
- Pointer adjustment counters per high order path:
  - Incoming positive pointer adjustment count
  - Incoming negative pointer adjustment count
  - Outgoing positive pointer adjustment count
  - Outgoing negative pointer adjustment count
- POH counters per high order path:
  - B3 near-end errored BIP count
  - B3 near-end errored block count
  - G1 far-end error count, configurable to count either REI errors or errored blocks
  - Near-end defect second
  - Far-end defect second

All performance counters are one second shadow counters: at the one second boundary the contents of each performance counter is latched into its one second shadow register, after which the performance counter is cleared. These one second shadow registers will hold their value during the entire period between two subsequent one second boundaries.

The one second shadow registers are available for software read-only access.

All errored BIP and block counters are dimensioned to cover the maximum count value during a one second interval meaning they can never reach saturation.

The one second boundary is generated by the internal one second clock which is either derived from the PHAST-12N System Clock or from the external REFONESECCLK input lead.

The performance counters can be reset by writing 0x91 into the **ResetCounters** register.

12.6 TRAIL TRACE IDENTIFIER PROCESS

12.6.1 TTI Formats

The following TTI formats or modes are supported:

- 16-byte trace message: 16-byte repeating pattern consisting of a 15-byte APId preceded by a one byte header. The most significant bits of the TTI bytes form a 16-bit TFAS with a 1 in the most significant bit of the first TTI byte (header byte) and a 0 in the most significant bit of the APId bytes.
- 64-byte trace message: a 64-byte repeating pattern consisting of a 63-byte APId preceded by a one byte header. The most significant bits of the TTI bytes form a 64-bit TFAS with a 1 in the most significant bit of the first TTI byte (header byte) and a 0 in the most significant bit of the APId bytes.
- 64-byte trace message with CR/LF: a 64-byte repeating pattern consisting of a 62-byte APId followed by a two byte trailer. The trailer consists of the <CR> and <LF> ASCII characters.
- repeating non-specific byte: a repeating single byte with fixed (constant), but unspecified value.
- repeating specific byte: a repeating single byte with fixed (constant) value. The remote end user knows in advance which value is expected.

Note: *The user has to specify TFAS, CRC or CR/LF both for monitoring (mismatch detection) and generation.

*The repeating specific byte is handled as a 16-byte trace message without TFAS.

The following TTI message types are supported:

J0	Repeating non-specific byte
	Repeating specific byte
	16-byte trace message
J1	Repeating non-specific byte
	16-byte trace message
	64-byte trace message with TFAS
	64-byte trace message with CR/LF

12.6.2 TTI Mismatch Process

The TTI framer frames on TFAS or CR/LF. The framer freewheels when not locked to allow mismatch detection when expecting a repeating specific byte.

The TIM defect is set when the received TTI does not match the format or value of the expected TTI during a configurable number of consecutive multiframes[1]. The TIM defect is cleared when the received TTI has the same format and value as the expected TTI during a configurable number of consecutive multiframes.

In case of repeating non-specific byte mode, the defined expected value will be ignored. Comparisons are made with the previous samples.

12.6.3 TTI Report Process

The received TTI value is accepted when 3 subsequent identical 16 respectively 64 byte multiframes are received. Note that when both 16-byte and 64-byte trace message modes are supported as is the case for path overhead monitoring (J1), the received 16-byte trace message is only accepted when 4 subsequent identical 16 byte multiframes are received. This condition when the received TTI equals the accepted TTI is indicated as stable.

If the new multiframe TTI message is the same as the previously accepted message, only 1 multiframe is required to assert the Stable_1 indication. For the Stable_64 indication, 3 multiframes are needed and for the Stable_16 indication, 3 multiframes are needed in case no 64-byte trace message mode is supported, otherwise 4 multiframes are needed.

Latched registers are provided for the Stable indications. This guarantees consistency when the reported TTI message is being read out by software:

1. Clear the Stable indication latch (clear-on-write-1)
2. Read out the reported TTI message
3. The Stable indication latch must still be deasserted. If not, the stable indication (and the reported message) may have changed during software read accesses.

Note 1: Stable_1 is the inverse of TIM1.

Note 2: Stable_16 will inhibit Stable_64.

Note 3: Stable_16 will also indicate stable one byte messages. In this case software has to compare the reported message bytes.

12.7 DEFECTS AND INTERRUPTS

12.7.1 Unlatched Defects (Correlated)

Defects representing the current status of the device are correlated to fault causes (correlated defects). This inhibition process avoids the unnecessary generation of interrupts, when a defect that is at an high hierarchy leads to the generation of multiple lower order defects. Unlatched defects are read-only.

1. A multiframe is 16 or 64 frames, depending on the TTI format.

12.7.2 Latched Defects

Changes in the state of defects are latched by the PHAST-12N. The edge on which latching occurs is configurable through the **LatchForIntCtrl** control register:

- Both rising and falling edges are latched (default)
- Only rising edges are latched, or
- Only falling edges are latched

Latched defects are cleared by a clear-on-write-1 mechanism (COW-1). This way software/ firmware can clear a defect when it will be handled. Software must never write a '1' to a latched defect that was previously read to be '0', because between the read and the write the defect may become active and will be cleared without software knowing it was active.

12.7.3 Defects Mask

Each latched defect can optionally contribute to the device hardware interrupt. The contribution of each individual latched defect can be enabled/disabled by clearing/setting the corresponding mask[1] :

Summary $\leftarrow \Sigma$ ($Defect\_Latch_i$ AND not $Defect\_Mask_i$)

12.7.4 Interrupts

The contribution of groups of latches can in turn be combined into a summary latch with associated mask, forming an interrupt tree:

device interrupt $\leftarrow \Sigma$ ($Summary_i$ AND not $Summary\_Mask_i$)

At the device top level, the general interrupt summary latches and the APS interrupt summary latches contribute to the interrupt:

HINT $\leftarrow \Sigma$ ($General\_Interrupt_i$ AND not $General\_Mask_i$)

OR

Σ ($APS\_Interrupt_k$ AND not APS_Mask_k)

The hardware interrupt capability is enabled by setting the **HINTEN** control bit. While disabled, the hardware interrupt indication INT/$\overline{IRQ}$ output lead is inactive. When enabled, the device top level hardware interrupt is

INT/$\overline{IRQ}$ output lead $\leftarrow$ (**HINT** AND **HINTEN**).

12.8 ALARM INTERRUPT TREE

Following legend is used:

[dim] = array of dimension "dim", directly accessible

{dim} = array of dimension "dim", which has to be accessed indirectly

(i) = the i'th element of the array (direct access)

1. Σ (x) is used to indicate a logical 'OR' of a number of logical expressions (x).

+ = OR

& = AND

~ = NOT

index ranges:

ho = range 0 to 11 (= #VCs)

li = range 0 to 3 (= #lines)

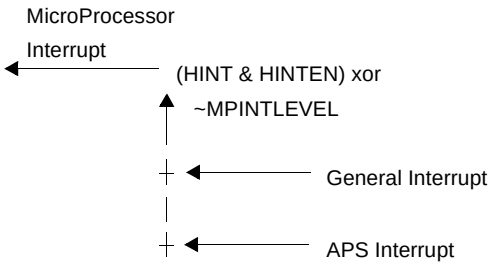


Figure 45. HINT

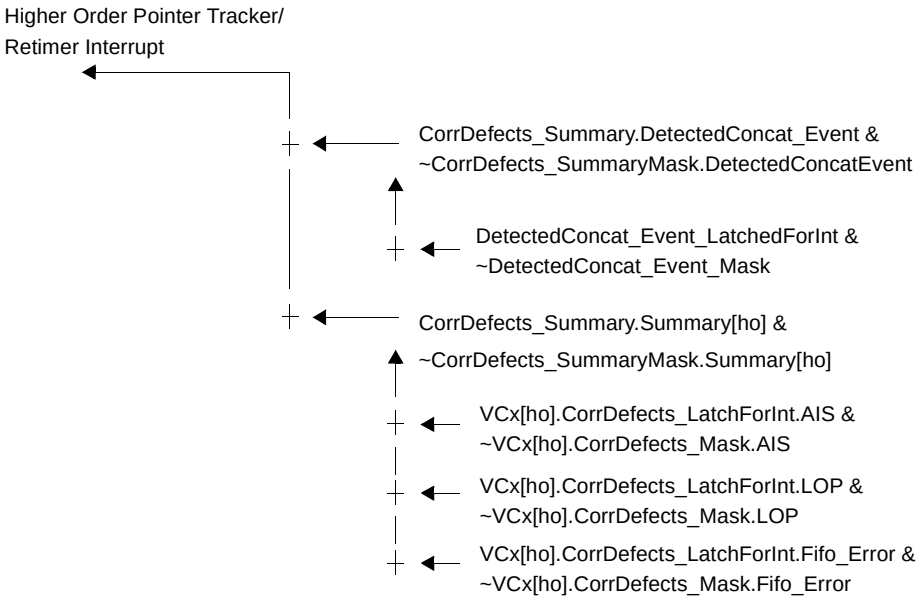


Figure 46. High Order Point Tracker Retimer Interrupt Tree

Figure 47. POH Monitor Interrupt Tree

Figure 48. TOH Monitor Interrupt Tree

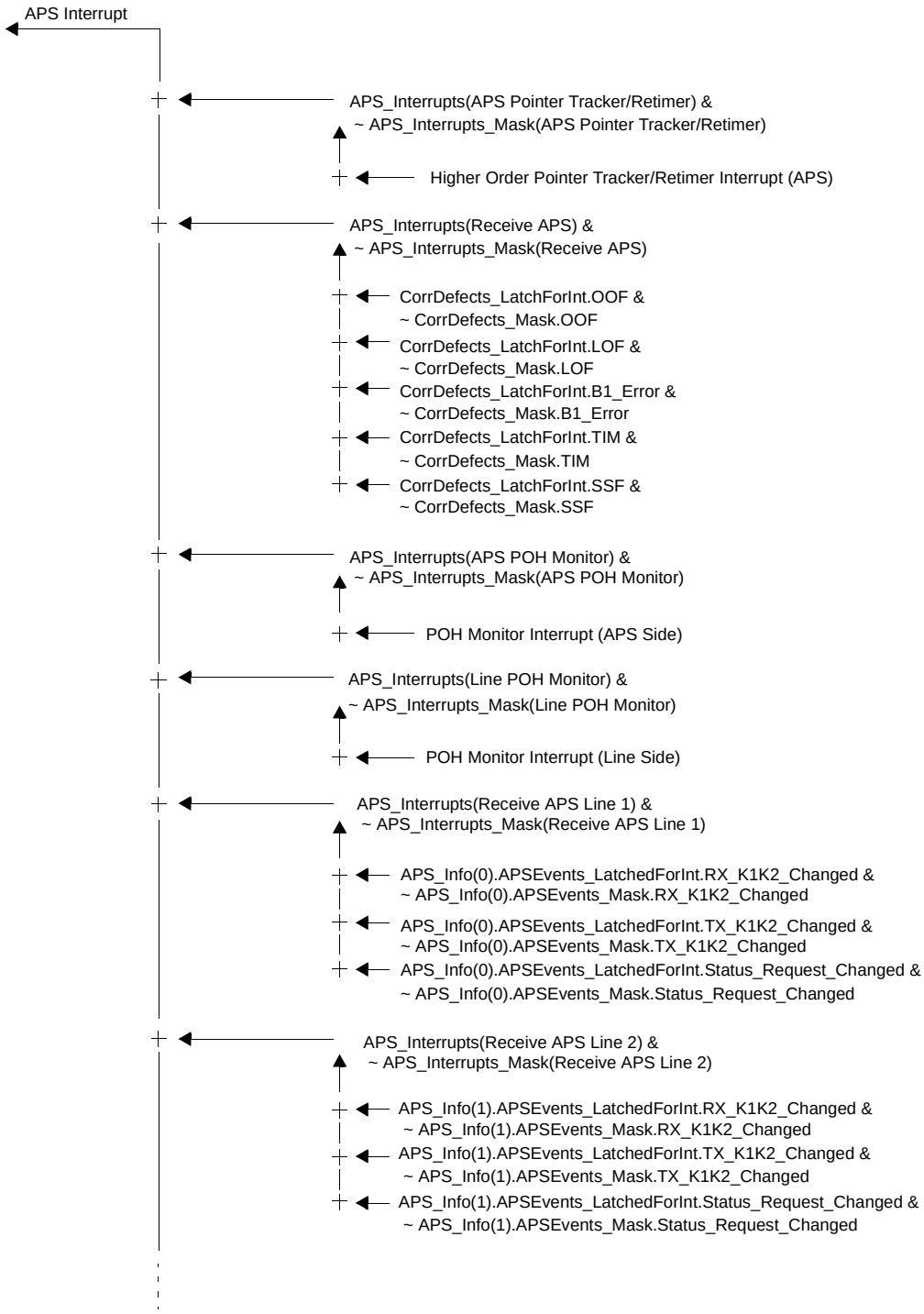


Figure 49. APS Interrupt Tree (part 1)

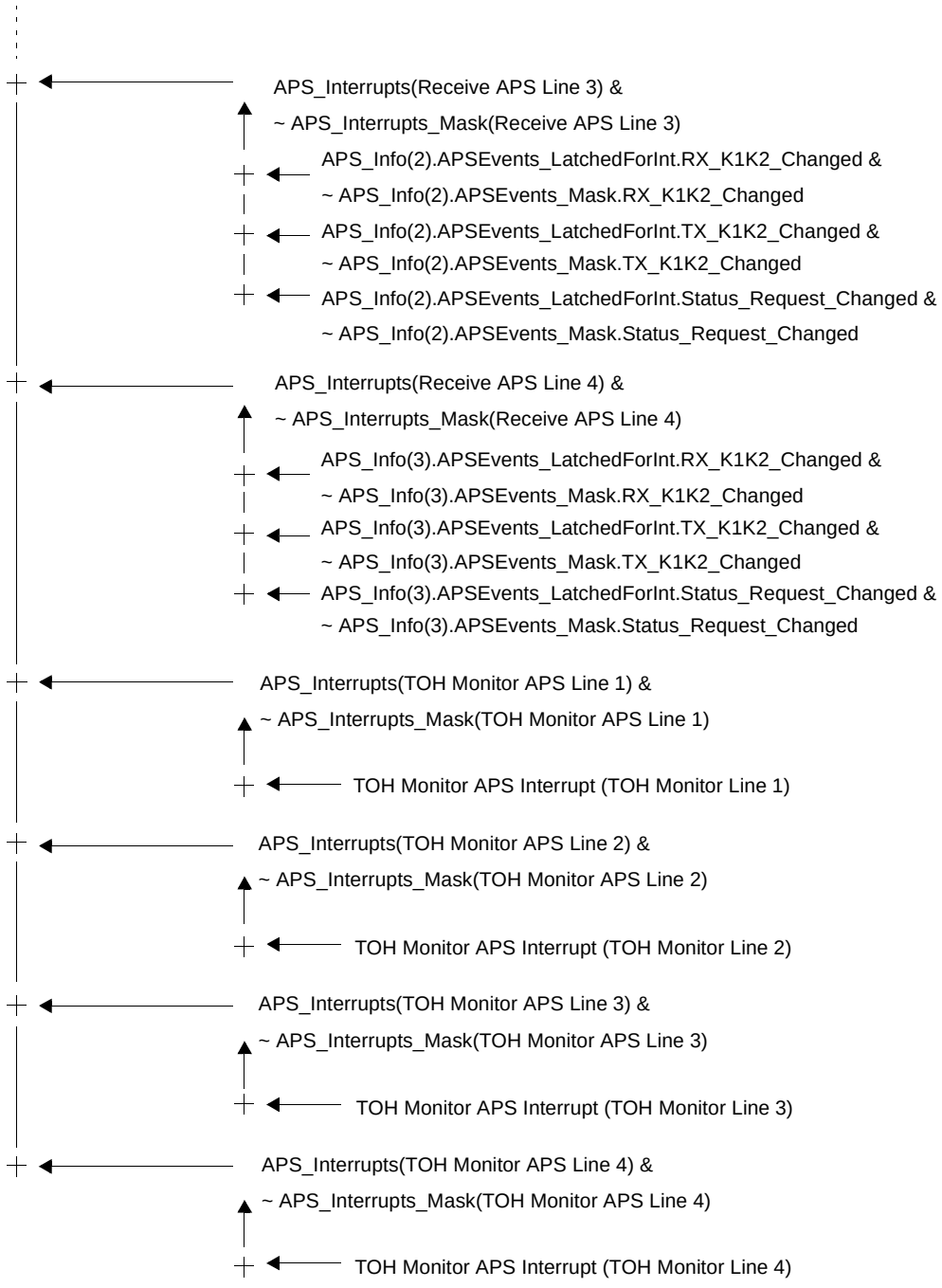


Figure 50. APS Interrupt Tree (part 2)

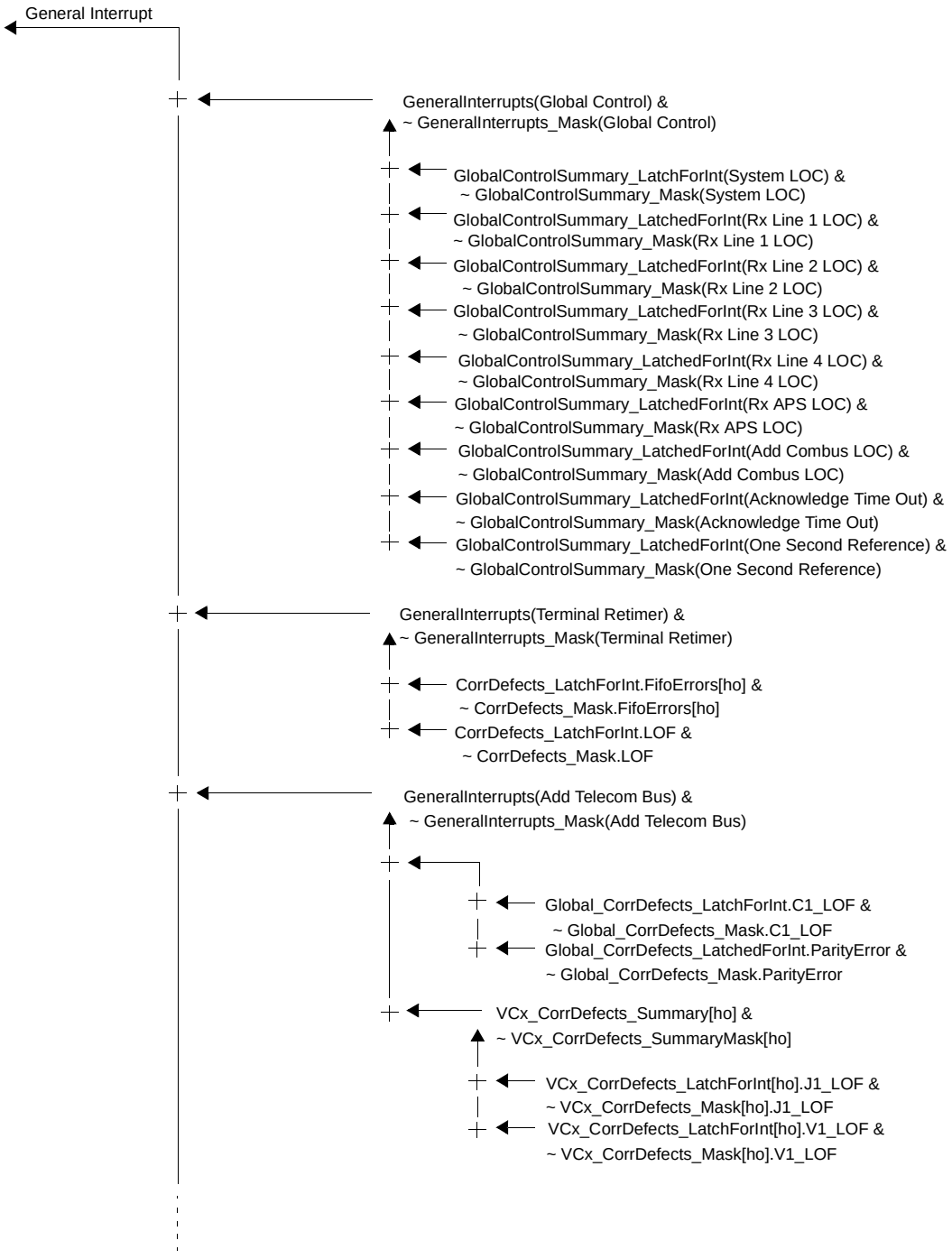


Figure 51. General Interrupt Tree (part 1)

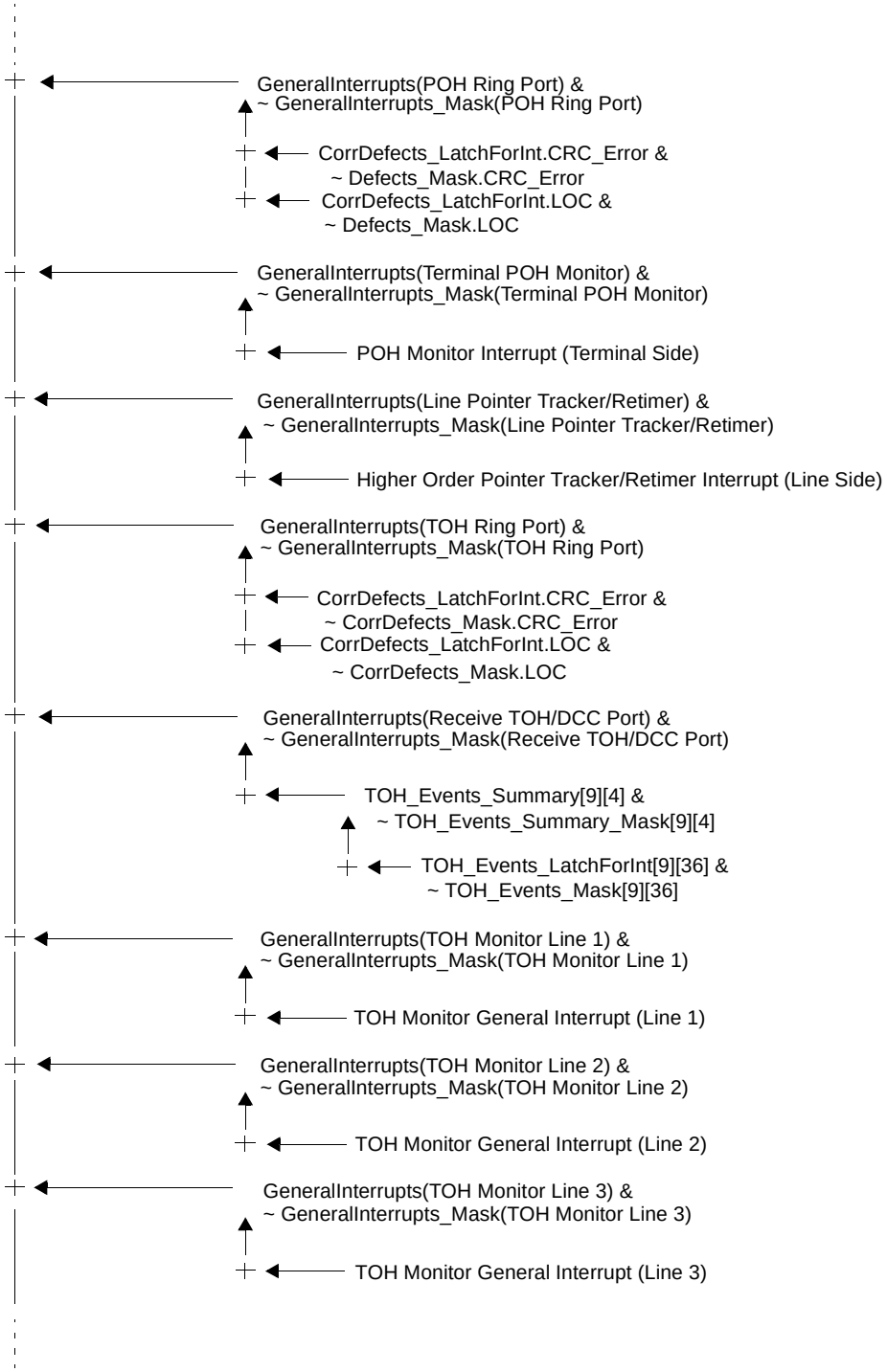


Figure 52. General Interrupt Tree (part 2)

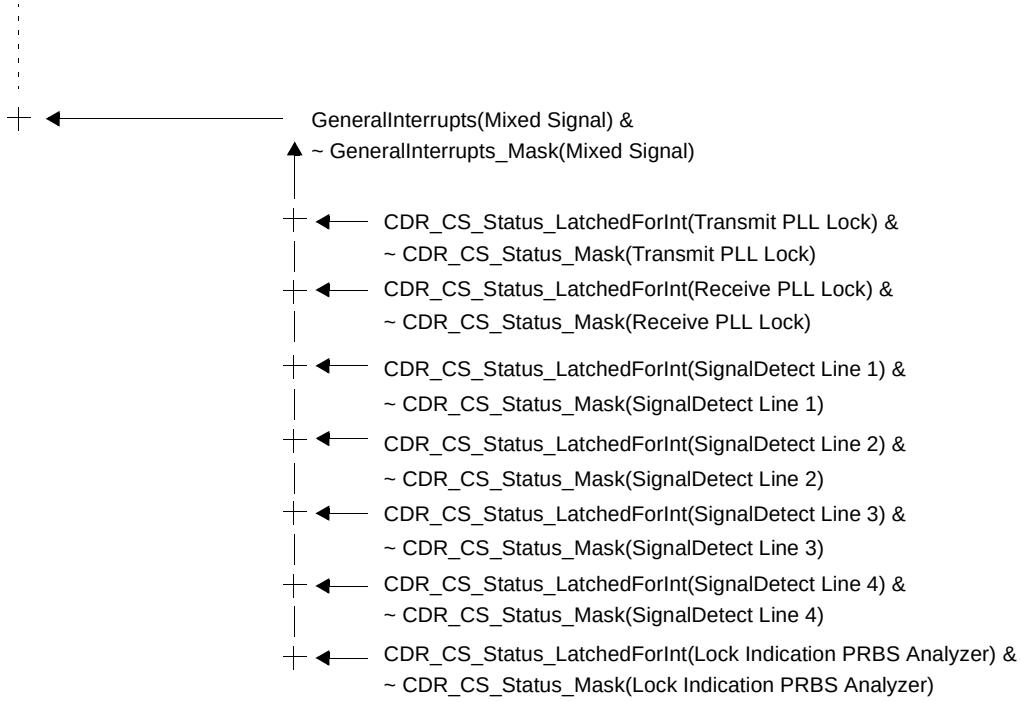


Figure 53. General Interrupt Tree (part 3)

12.9 BOUNDARY SCAN

12.9.1 Introduction

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 54, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 26.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 54.

The boundary scan function can be reset and disabled by holding lead $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the PHAST-12N device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

12.9.2 Boundary Scan Operation

The maximum frequency the PHAST-12N device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 54.

The instruction register contains three bits. The PHAST-12N device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the PHAST-12N device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the PHAST-12N boundary scan and instruction registers.

12.9.3 Boundary Scan Reset

Specific control of the $\overline{\text{TRS}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the PHAST-12N. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value must be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the 'Input, Output and Input/Output Parameters' section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

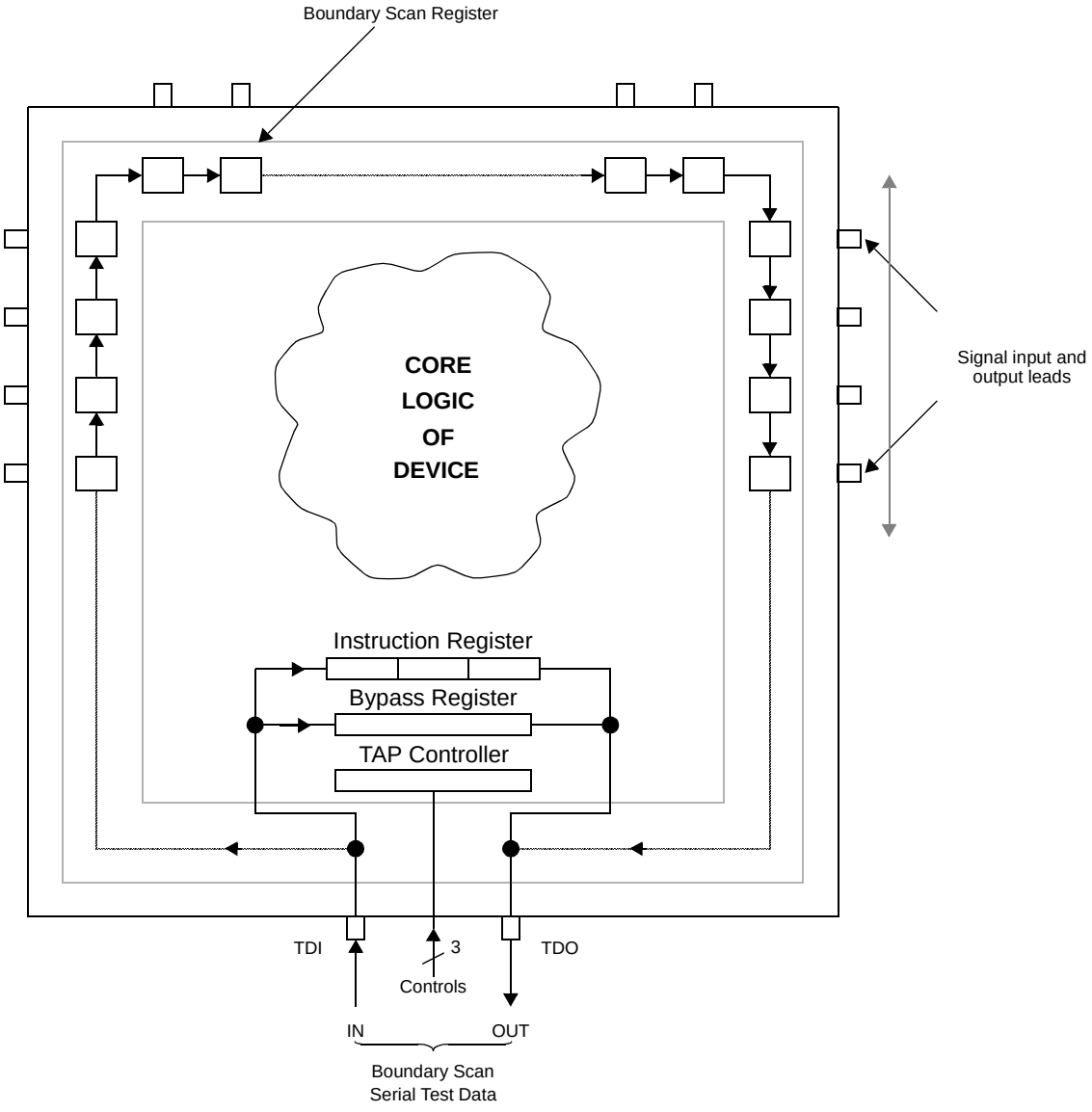


Figure 54. Boundary Scan Schematic

12.9.4 Boundary Scan Chain

A boundary scan description language (BSDL) source file is available via the Products page of the TranSwitch Internet World Wide Web site at www.transwitch.com.

13.0 MEMORY MAPS AND BIT DESCRIPTIONS

This section contains the address map of the internal memory locations of the PHAST-12N. The Access columns of the tables specify the access types as Read-only (ro), Read-Write (rw) or Clear-On-Write-1 (cow_1).

All addresses and offsets are byte addresses.

13.1 OVERVIEW

Table 1: Memory Map Overview

Offset	Description
0x0000	Global Control (See page 151)
0x0080	Line Ring Port/Alarm Interface (See page 153)
0x00A0	Reset Generator (See page 153)
0x00B0	Interrupt (See page 154)
0x00C0	Transmit APS Port (See page 156)
0x0200	POH Generator (See page 157)
0x0400	TOH Monitor - Rx Line 1 (See page 160)
0x0500	TOH Monitor - Rx Line 2 (See page 160)
0x0600	TOH Monitor - Rx Line 3 (See page 160)
0x0700	TOH Monitor - Rx Line 4 (See page 160)
0x0800	TOH Generator (See page 165)
0x1000	TOH and DCC Port (See page 167)
0x1800	High Order Pointer Tracker and Retimer - Rx Line Interface (See page 170)
0x1C00	High Order Pointer Tracker and Retimer - Rx APS Interface (See page 170)
0x3800	Retimer (See page 173)
0x3A00	Clock Recovery/Clock Synthesis/SerDes (See page 175)
0x3B00	Receive APS Port (See page 180)
0x3C00	Cross Connect (See page 182)
0x3D00	Add Telecom Bus (See page 183)
0x3E80	High Order Path Ring Port/Alarm Interface (See page 185)
0x3F00	JTAG Master (See page 186)
0x3F80	Drop Telecom Bus (See page 187)
0x4000	POH Monitor - Rx Line Interface (See page 188)
0x4800	POH Monitor - Rx APS Interface (See page 188)
0x5000	POH Monitor - Terminal Side (See page 188)

13.2 GLOBAL CONTROL

Table 2: Global Control (T_GLOBAL_CONTROL)

Offset	Bits	Name	Init	Access	Description
0x0000		DeviceIdentification		ro	T_DeviceIdentification (See page 152) Device identification.
0x0010	0	STM4_Mode	0x0	rw	STM-4/OC-12 Mode when 0x1: line 1 is a 622.08 Mbit/s signal, lines 2 to 4 are not used. STM-1/OC-3 Mode when 0x0: lines 1 to 4 are 155.52 Mbit/s signals.
0x0012	0	Reserved	0x1	rw	Reserved.
0x0014	0	Reserved	0x1	rw	Reserved.
0x0016	8 - 0	TimeOutCount	0x1FF	rw	Range 0 to 511 Acknowledge Time Out Count. Specifies the Time Out after which an Acknowledge is generated if a request hasn't been acknowledged. Timebase is the microprocessor clock period (MPCLK).
0x0018	0	AckOnTimeOut	0x1	rw	Acknowledge on Time Out. An Acknowledge will be generated upon failed accesses after a period specified by TimeOutCount when 0x1. No Acknowledge will be generated upon failed accesses when 0x0.
0x001A	15 - 0	LastAddress	0x0	ro	Last Address. Indicates the address of the last timed-out request. Note: the address returned is a word address.
0x001C	0	CBADT	0x0	ro	Add Combus Timing Slave. Indicates the value on the CBADT input pad (this pad configures the Add Telecombus in master or slave mode).
0x001E	15 - 0	LocDivider	0x4	rw	Range 0 to 65535 Loss Of Clock Divider. The clock to be monitored is divided by this number + 1 for LOC detection.
0x0020	15 - 0	LocEntryThreshold	0x20	rw	Range 1 to 65535 Loss Of Clock Entry Threshold. Specifies the time without divided clock transition before declaring LOC. Timebase is the microprocessor clock period (MPCLK).
0x0024	15 - 0	LocExitThreshold	0x2	rw	Range 1 to 65535 Loss Of Clock Exit Threshold. LOC is deasserted when this many divided clock transitions were detected. Detection occurs in the microprocessor clock domain (MPCLK).
0x0028	0	External1secRef_Select	0x0	rw	External One Second Reference Select. The one second reference on the REFONESECCLK is used when 0x1. The one second reference is generated internally when 0x0.
0x002C	0	DeviceInitialized	0x0	rw	The device processes incoming data when this value is set to 0x1. The software must set this value to 0x1 as soon as it has finished the configuration of the device.
0x0030	3 - 0	GP_Input	0x0	ro	General purpose input (GPIN4..GPIN1).
0x0034	3 - 0	GP_Output	0x0	rw	General purpose output (GPOUT4..GPOUT1).

Table 2: Global Control (T_GLOBAL_CONTROL)

Offset	Bits	Name	Init	Access	Description
0x0038	6 - 0	RamResetDone	0x0	ro	For every bit in the list, 0x1 means the RAMs of the corresponding clock domain are initialized, 0x0 the RAMs are not initialized. • bit 0: System Clock domain • bit 1: Rx Line 1 Clock domain • bit 2: Rx Line 2 Clock domain • bit 3: Rx Line 3 Clock domain • bit 4: Rx Line 4 Clock domain • bit 5: Rx APS Clock domain • bit 6: Add Combus Clock domain
0x003A	10 - 0	GlobalControlSummary_Unlatched	0x0	ro	Global Control Interrupt Summary. • bit 0: Loss of System Clock • bit 1: Loss of Rx Line 1 Clock • bit 2: Loss of Rx Line 2 Clock • bit 3: Loss of Rx Line 3 Clock • bit 4: Loss of Rx Line 4 Clock • bit 5: Loss of Rx APS Clock • bit 6: Reserved • bit 7: Reserved • bit 8: Loss of Add Combus Clock • bit 9: Acknowledge Time Out • bit 10: One Second Reference
0x003C	10 - 0	GlobalControlSummary_LatchForInt	0x0	cow_1	Global Control Interrupt Summary. See GlobalControlSummary_Unlatched for details.
0x003E	10 - 0	GlobalControlSummary_Mask	0x7FF	rw	Global Control Interrupt Summary Mask. See GlobalControlSummary_Unlatched register for details.
0x0040		ScratchPad	All 0x0	rw	Array (32) of two_bytes Offset between two elements = 0x2. Array index indicates the scratch pad address. Scratch pad: general purpose read/write memory which can be used as scratch pad by the device driver.

Table 3: Device Identification (T_DeviceIdentification)

Offset	Bits	Name	Init	Description
0x0000	10 - 0	ManufacturerIdentity	0x6B	Manufacturer Identity, assigned by the Solid State Products Engineering Council (JEDEC) to the TranSwitch Corporation (0x06B = "0001101011").
0x0002	15 - 0	PartNumber	0x18A8	Part Number (06312).
0x0004	3 - 0	Version	0x0	Version or revision level. The initial version will be 0x0. The version register will be incremented with each new revision of the part.
0x0006	Growth_Mask			
	3 - 0	MaskLevel	0x0	Indicates the Mask Level.
	7 - 4	GrowthField	0x0	Indicates the Growth Field.
0x0008	12 - 0	Reserved	0x0	Reserved.

13.3 LINE RING PORT/ALARM INTERFACE

Table 4: Ring Port/Alarm Interface (T_TOH_RING_PORT)

Offset	Bits	Name	Init	Access	Description
0x0000		ExternalSourceSelect	All 0x0	rw	Array (4) of boolean Offset between two elements = 0x2. Array index indicates the line (= line number - 1). Selection of external ring port interface. The internal ring port interface is used when 0x0, the external port is used when 0x1.
0x0008	0	CRC_Error_Insert	0x0	rw	Insert CRC errors. All CRC bits are inverted when 0x1 (for test purposes only).
0x000A		CorrDefects_Unlatched		ro	T_TOH_RING_PORT_Defects (See page 153) Correlated defects.
0x000C		CorrDefects_LatchForInt		cow_1	T_TOH_RING_PORT_Defects (See page 153) Correlated defects latched for interrupt.
0x000E		CorrDefects_Mask		rw	T_TOH_RING_PORT_Defects (See page 153) Correlated defects masks.

Table 5: Ring Port/Alarm Interface Defects (T_TOH_RING_PORT_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	CRC_Error	0x1	CRC error on external Ring Port interface.
	1	LOC	0x1	Loss of clock on external Ring Port interface.

13.4 RESET GENERATOR

Table 6: Reset Generator (T_RGEN)

Offset	Bits	Name	Init	Access	Description
0x0000	7 - 0	RESETH	0x0	rw	Microprocessor Controlled Reset. Writing the value 0x91 to this register generates a reset in all clock domains, except the microprocessor clock domain (MPCLK). Reset is active as long as this register contains the value 0x91.
0x0002	7 - 0	Reserved	0x0	rw	Reserved.
0x0004	7 - 0	AddCombus_Reset	0x0	rw	Microprocessor Controller Reset for Add Combus. Writing the value 0x91 to this register generates a reset in the Add Combus clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.
0x0006	7 - 0	Reserved	0x0	rw	Reserved

Table 6: Reset Generator (T_RGEN)

Offset	Bits	Name	Init	Access	Description
0x0008	7 - 0	RxLine1_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 1. Writing the value 0x91 to this register generates a reset in the Receive Line 1 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.
0x000A	7 - 0	RxLine2_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 2. Writing the value 0x91 to this register generates a reset in the Receive Line 2 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.
0x000C	7 - 0	RxLine3_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 3. Writing the value 0x91 to this register generates a reset in the Receive Line 3 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.
0x000E	7 - 0	RxLine4_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 4. Writing the value 0x91 to this register generates a reset in the Receive Line 4 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.

13.5 INTERRUPT

Table 7: Interrupt (T_INTERRUPT)

Offset	Bits	Name	Init	Access	Description
0x0000	11 - 0	APS_Interrupts_Mask	0xFFF	rw	APS Interrupts Mask. See APS_Interrupts register for details.
0x0004		IntCtrl_Config		rw	T_InterruptCtrl_Config (See page 155) Interrupt and performance configuration.
0x0006	0	HINT	0x0	ro	Global device interrupt (HINT = Hardware INTerrupt).
0x0008	0	HINTEN	0x0	rw	The global device interrupt is enabled when 0x1, no interrupt will be generated when 0x0 (HINTEN = Hardware INTerrupt ENable).

Table 7: Interrupt (T_INTERRUPT)

Offset	Bits	Name	Init	Access	Description
0x000A	15 - 0	GeneralInterrupts	0x0	ro	General Interrupts Register: • bit 0: Global Control Interrupt • bit 1: Terminal Retimer • bit 2: Add Telecombus • bit 3: Reserved • bit 4: Reserved • bit 5: Reserved • bit 6: POH Ring Port • bit 7: Terminal POH Monitor • bit 8: Line Pointer Tracker/Retimer • bit 9: TOH Ring Port • bit 10: Receive TOH/DCC Port • bit 11: TOH Monitor Line 1 • bit 12: TOH Monitor Line 2 • bit 13: TOH Monitor Line 3 • bit 14: TOH Monitor Line 4 • bit 15: Mixed Signal
0x000C	11 - 0	APS_Interrupts	0x0	ro	APS Interrupts Register: • bit 0: APS Pointer Tracker/Retimer • bit 1: Receive APS • bit 2: APS POH Monitor • bit 3: Line POH Monitor • bit 4: Receive APS Line 1 • bit 5: Receive APS Line 2 • bit 6: Receive APS Line 3 • bit 7: Receive APS Line 4 • bit 8: TOH Monitor APS Line 1 • bit 9: TOH Monitor APS Line 2 • bit 10: TOH Monitor APS Line 3 • bit 11: TOH Monitor APS Line 4
0x000E	15 - 0	GeneralInterrupts_Mask	0xFFFF	rw	General Interrupts Mask. See GeneralInterrupts register for details.

Table 8: Interrupt Configuration (T_InterruptCtrl_Config)

Offset	Bits	Name	Init	Description
0x0000	7 - 0	ResetCounters	0x0	All performance counters are reset when the value 0x91 is written to this register. Reset is active as long this register contains the value 0x91.
	9 - 8	LatchForIntCtrl	0x3	0x0 = INT_LEVEL 0x1 = INT_RISING_EDGE 0x2 = INT_FALLING_EDGE 0x3 = INT_BOTH_EDGES Field to control on which edges the unlatched defects are latched for interrupts.
	10	Reserved	0x0	Reserved.

13.6 TRANSMIT APS PORT

Table 9: Transmit APS Port (T_TX_APS)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_TX_APS_Common_Config (See page 156) General configuration.
0x0020		MSP		rw	Array (4) of T_TX_APS_Config (See page 156) Offset between two elements = 0x8. Array index indicates the line (= line number - 1). Multiplex Section Protection configuration.

Table 10: Transmit APS Port Configuration (T_TX_APS_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	Functionality			
	0	AIS_Force	0x0	Insertion of line AIS is forced when 0x1.
	1	Scrambler_Disable	0x0	Scrambling is disabled when 0x1.
0x0002	Setting			
	7 - 0	B1_Mask	0x0	Mask used on the B1 byte, set to default value for normal operation.
	15 - 8	J0_Insert	0x0	J0 byte. Used as a form of simple connection identification.
0x0004		B2_Mask	All 0x0	Array (12) of byte Offset between two elements = 0x2. Mask used on the B2 byte, set to the default value for normal operation.

Table 11: Transmit APS Port Line Configuration (T_TX_APS_Config)

Offset	Bits	Name	Init	Description
0x0000	Enable			
	0	K1K2_ForwardEnable	0x0	Rx K1 K2 APS signal are forwarded from MSOH monitor when 0x1, Rx K1 K2 APS signal are inserted from register when 0x0. (RX_K1K2_Data).
	1	SignalFail_ForwardEnable	0x0	Signal fail indication is forwarded from MSOH monitor when 0x1, signal fail indication is inserted from register (StatusRequest) when 0x0. Positioned at the LSB of the status-byte.
	2	SignalDegrade_ForwardEnable	0x0	Signal degrade indication is forwarded from MSOH monitor when 0x1, signal degrade indication is inserted from register (StatusRequest) when 0x0. Positioned at the 2nd LSB of the status-byte.
0x0002	15 - 0	RX_K1K2_Data	0x0	Register that contains the values for Rx K1 and Rx K2. Rx K1 is located in MSB, Rx K2 is located in LSB.
0x0004	15 - 0	TX_K1K2_Data	0x0	Register that contains the values for Tx K1 and Tx K2. Tx K1 is located in MSB, Tx K2 is located in LSB.
0x0006	15 - 0	StatusRequest	0x0	Register that contains the values for Status and Request. Status is located in MSB, Request is located in LSB.

13.7 POH GENERATOR

Table 12: POH Generator (T_POH_GENERATOR)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_VCXPG_Common_Config (See page 157) General configuration.
0x0100		VC_Config		rw	T_VCXPG_VC_Config (See page 158) High order path configuration. The high order path to be configured is selected by indirect access. See the Config_Channel register in the Common_Config record to select the desired high order path.

Table 13: POH Generator Common Configuration (T_VCXPG_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	Config_Channel	0x0	Range 0 to 11 High order path for which configuration can be done in VC_Config.
0x0002		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.

Table 14: AUG-1 Mode Configuration (T_AUG1_Mode_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	TimeslotIsConcatenated	0x0	Concatenation setting, one bit per AUG-1. Each bit has following meaning (Least significant bit represents the first AUG-1. Don't care for line side in STM-1 mode): The corresponding AUG-1 is either an independent AUG-1 or the first AUG-1 of a larger concatenated structure when '0' (e.g., AU4-4c). The corresponding AUG-1 is part of a larger concatenated structure (but not the first one) when '1'. Note: The least significant bit must be '0' (the first AUG-1 is always master). This bit will be forced to '0', no matter what has been written to it.
	7 - 4	Has_AU3	0x0	Selection between AU-3 and AU-4 mapping for independent AUG-1's, one bit per AUG-1. Each bit has following meaning (Least significant bit represents the first AUG-1. For the line side: least significant bit represents the first AUG-1 in STM-4 mode or the first line in STM-1 mode): The corresponding AUG-1 contains an AU-4 when '0', the corresponding AUG-1 contains three AU-3's when '1'. Note the configuration is a don't care for AUG-1's which are part of a larger concatenated structure. It is advisable to fill in the default value.
	11 - 8	Is_TUG_Structured	0xF	For AUG-1 containing AU-4 format, one bit per AUG-1. Each bit has following meaning (least significant bit represents the first AUG-1): The corresponding VC-4 contains C-4 when '0', the corresponding VC-4 contains three TUG-3's when '1'.

Table 15: POH Generator Path Configuration (T_VCXPG_VC_Config)

Offset	Bits	Name	Init	Description
0x0000		RAM		T_VCXPG_RAMBytes (See page 158) Configuration of the POH RAM bytes.
0x0090		Mode		T_VCXPG_Mode_record (See page 158) Mode Configuration.
0x0092		Control		T_VCXPG_Control_record (See page 159) Source selection for the POH bytes.

Table 16: Transmit POH Byte RAM (T_VCXPG_RAMBytes)

Offset	Bits	Name	Init	Description
0x0000		J1	All 0x0	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. TTI-message for insertion in the J1 location. • bytes 0-15 for 16 byte TTI message • bytes 0-63 for 64 byte TTI message
0x0080	7 - 0	B3_ErrorMask	0x0	Mask used on the B3 byte, set to default value for normal operation.
0x0082	7 - 0	C2	0x0	Signal label to be inserted.
0x0084	7 - 0	G1	0x0	Value used when G1 is inserted out of RAM.
0x0086	7 - 0	F2	0x0	Value used when F2 is inserted out of RAM.
0x0088	7 - 0	H4	0x0	Value used when H4 is inserted out of RAM.
0x008A	7 - 0	F3	0x0	Value used when F3 is inserted out of RAM.
0x008C	7 - 0	K3	0x0	Value used when K3 is inserted out of RAM.
0x008E	7 - 0	N1	0x0	Value used when N1 is inserted out of RAM.

Table 17: POH Generator Path Mode (T_VCXPG_Mode_record)

Offset	Bits	Name	Init	Description
0x0000	0	Force_AIS	0x0	AIS insertion is forced in the corresponding high order path when 0x1.
	1	Force_Uneq	0x0	Unequipped is forced in the corresponding high order path when 0x1.
	2	Force_SupUneq	0x0	Supervisory Unequipped is forced in the corresponding high order path when 0x1.
	3	UniDirectional	0x0	Uni-directional option is activated (G1 byte will be filled with 0x00, regardless the byte provided from the selected source) when 0x1.
	4	OneBitRDI	0x0	RDI is encoded in one bit when 0x1, in three bits (Enhanced RDI) when 0x0.
	5	Bypass	0x0	The incoming high order path is passed untouched when 0x1.

Table 18: POH Byte Source Control (T_VCXPG_Control_record)

Offset	Bits	Name	Init	Description
0x0000	1 - 0	REI_Control	0x0	0x0 = VCXPG_RAM_RI 0x1 = VCXPG_POH_INTF_RI 0x2 = VCXPG_PR_RI Selects the source of the G1 REI field. • VCXPG_RAM_RI = Use RAM as source • VCXPG_POH_INTF_RI = Use POH Port Interface as source • VCXPG_PR_RI = Use Ring port Interface as source
	3 - 2	RDI_Control	0x0	0x0 = VCXPG_RAM_RI 0x1 = VCXPG_POH_INTF_RI 0x2 = VCXPG_PR_RI Selects the source of the G1 RDI value. • VCXPG_RAM_RI = Use RAM as source • VCXPG_POH_INTF_RI = Use POH Port Interface as source • VCXPG_PR_RI = Use Ring port Interface as source
	4	SPARE_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the G1 SPARE bit. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	5	F2_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the F2 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	7 - 6	H4_Control	0x0	0x0 = VCXPG_RAM_H4 0x1 = VCXPG_POH_INTF_H4 0x2 = VCXPG_PASS_H4 0x3 = VCXPG_GENERATE_H4 Selects the source of the H4 Byte. • VCXPG_RAM_H4 = Use RAM as source • VCXPG_POH_INTF_H4 = Use POH Port Interface as source • VCXPG_PASS_H4 = Pass H4 • VCXPG_GENERATE_H4 = Generate H4
	8	F3_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the F3 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	9	K3_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the K3 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	10	N1_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the N1 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source

13.8 TOH MONITOR

Table 19: TOH Monitor (T_TOH_MONITOR)

Offset	Bits	Name	Init	Access	Description
0x0000		TTI_ExpectedMessage	All 0x0	rw	Array (16) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Expected TTI message: • 16 byte TTI message: specify all sixteen bytes. • 1 byte specific TTI message: write all bytes with the same value. This register is only used when NonSpecificMessage is 0x0 (see J0 TTI Configuration).
0x0040		TTI_ReportedMessage	All 0x0	ro	Array (16) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Reported TTI message.
0x0080		PerfCounters_Shadow		ro	T_TOH_MONITOR_Performance_Counters (See page 160) RSOH/MSOH Performance counters.
0x00A0		Line_Status		ro/cow_1	T_TOH_MONITOR_Line_Status (See page 161) Line Status. Note: Latched bits are clear-on-write-1, all others are read-only.
0x00B0		CorrDefects_LatchForInt		cow_1	T_TOH_MONITOR_Defects (See page 161) Correlated defects latched for interrupt.
0x00B4		APS_Defects_Mask		rw	T_TOH_MONITOR_APS_Defects (See page 162) Defects for APS handling mask.
0x00B8		APS_Defects_LatchForInt		cow_1	T_TOH_MONITOR_APS_Defects (See page 162) Defects for APS handling latched for (APS) interrupt.
0x00BC		CorrDefects_Unlatched		ro	T_TOH_MONITOR_Defects (See page 161) Correlated defects.
0x00BE		CorrDefects_Mask		rw	T_TOH_MONITOR_Defects (See page 161) Correlated defects mask.
0x00C0		Common_Config		rw	T_TOH_MONITOR_Common_Config (See page 162) General configuration.

Table 20: TOH Monitor Performance Counters (T_TOH_MONITOR_Performance_Counters)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	B1_BIP_Errors	0x0	B1 BIP error counter. Configurable as bit or block count.
0x0002	15 - 0	B2_BIP_BitErrors_LSB	0x0	B2 BIP bit error counter, least significant bits.
0x0004	3 - 0	B2_BIP_BitErrors_MSB	0x0	B2 BIP bit error counter, most significant bits.
0x0006	12 - 0	B2_BIP_BlockErrors	0x0	B2 BIP block error counter.
0x0008	15 - 0	REI_BIP_Errors	0x0	REI BIP Counter. Configurable as bit or block count.
0x000A	DefectSeconds			
	0	NearEndDefectSec	0x0	TSF one second latch.
	1	FarEndDefectSec	0x0	RDI defect one second latch.

Table 21: TOH Monitor Status (T_TOH_MONITOR_Line_Status)

Offset	Bits	Name	Init	Description
0x0000	TTI_StableIndications			
	0	TTI_Stable1	0x0	TTI 1 byte message stable indication.
	1	TTI_Stable16	0x0	TTI 16 byte message stable indication.
	2	TTI_Stable16_Latched	0x0	Latched TTI 16 byte message stable indication. This field is clear-on-write-1.
0x0002	15 - 0	Debounced_K1K2	0x0	Debounced value of K1/K2 bytes (most significant byte is K1, least significant byte is K2).
0x0004	7 - 0	Debounced_S1	0x0	Debounced value of S1 nibbles.

Table 22: TOH Monitor Events/Defects (T_TOH_MONITOR_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	SignalDetect	0x1	SignalDetect from optical transceiver. SignalDetect is active high. (this is LINERXSIGDET when SignalDetect_ActiveLow is 0x0 and not LINERXSIGDET when SignalDetect_ActiveLow is 0x1).
	1	OOF	0x1	Out Of Frame.
	2	LOF	0x1	Loss Of Frame.
	3	LOS	0x1	Loss Of Signal.
	4	RSOHM_CI_SSF	0x1	Incoming SSF on RSOH Monitor.
	5	B1_Error	0x1	B1 BIP Error.
	6	TIM	0x1	Trail Identifier Mismatch.
	7	MSOHM_CI_SSF	0x1	Incoming SSF on MSOH Monitor.
	8	DEG	0x1	Degraded signal.
	9	EXC	0x1	Excessive error.
	10	RDI	0x1	Remote Defect Indication.
	11	AIS	0x1	Line AIS detected on K2.
	12	SF	0x1	Signal Fail.
	13	K1K2_Event	0x1	New (debounced) K1K2 value accepted.
	14	S1_Event	0x1	New (debounced) S1 value accepted.

Table 23: TOH Monitor APS Events/Defects (T_TOH_MONITOR_APS_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	DEG	0x1	Signal Degrade.
	1	SF	0x1	Signal Fail.
	2	K1K2_Event	0x1	New K1K2 value accepted.

Table 24: TOH Monitor Configuration (T_TOH_MONITOR_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	General_Config			
	0	B1_BIP_PerformanceCounter_Bit Count	0x0	B1 BER performance counter reports bit errors when 0x1, block errors when 0x0.
	1	REI_BIP_PerformanceCounter_Bit Count	0x0	REI BIP performance counter reports bit errors when 0x1, block counter when 0x0.
	2	SignalDetect_ActiveLow	0x0	SignalDetect input from transceiver (LINERXSIGDET) is active low when 0x1, active high when 0x0.
	3	LOS_Detection_Disable	0x0	LOS detection is disabled when 0x1.
	4	Descrambler_Disable	0x0	Descrambling is disabled when 0x1. Descrambling must be enabled in normal operation.
	5	Debounce_K2_LSB_Separately	0x1	Debouncing of K1/K2 bytes: the three least significant bits of K2 are debounced separately when 0x1. All sixteen bits are debounced when 0x0.
	6	SignalDetect_LOF_Inhibit_Disable	0x1	Inhibition of LOF by SignalDetect is disabled when 0x1.
	7	LOS_LOF_Inhibit_Disable	0x0	Inhibition of LOF by LOS is disabled when 0x1.
	8	SSF_AIS_Inhibit_Disable	0x0	Inhibition of K2 Line AIS by incoming SSF is disabled when 0x1.
0x0002		TTI_Config		T_TOH_MONITOR_TTI_Config (See page 163) TTI Configuration.
0x0006		B2_Config		T_TOH_MONITOR_BIP_Detector_Config (See page 164) Configuration for B2 DEG/EXC detection.

Table 24: TOH Monitor Configuration (T_TOH_MONITOR_Common_Config)

Offset	Bits	Name	Init	Description
0x0022	AIS_RDI_Config			
	0	AIS_RDI_Insert_Disable	0x0	Insertion of RDI on K2 Line AIS is disabled when 0x1.
	1	SSF_RDI_Insert_Disable	0x0	Insertion of RDI on SSF (incoming SSF in MSOH Monitor) is disabled when 0x1.
	2	EXC_RDI_Insert_Disable	0x0	Insertion of RDI on EXC is disabled when 0x1.
	3	SignalDetect_AIS_Insert_Disable	0x1	Insertion of Line AIS on SignalDetect is disabled when 0x1.
	4	LOS_AIS_Insert_Disable	0x0	Insertion of Line AIS on LOS defect detected in the A1/A2 Framer is disabled when 0x1.
	5	LOF_AIS_Insert_Disable	0x0	Insertion of Line AIS on LOF defect is disabled when 0x1.
	6	TIM_AIS_Insert_Disable	0x0	Insertion of Line AIS on TIM defect is disabled when 0x1.
	7	AIS_AIS_Insert_Disable	0x0	Insertion of Line AIS on K2 line AIS detection is disabled when 0x1.
	8	SSF_AIS_Insert_Disable	0x0	Insertion of Line AIS on SSF (incoming SSF in MSOH Monitor) is disabled when 0x1.
	9	EXC_AIS_Insert_Disable	0x0	Insertion of Line AIS on B2 EXC defect is disabled when 0x1.
	10	Framer_AIS_Force	0x0	Forces Line AIS insertion after Framing when 0x1.
	11	RSOH_AIS_Force	0x0	Forces Line AIS insertion after Regenerator Section Overhead Monitoring when 0x1.
	12	MSOH_AIS_Force	0x0	Forces Line AIS insertion after Multiplex Section Overhead Monitoring when 0x1.

Table 25: J0 TTI Configuration (T_TOH_MONITOR_TTI_Config)

Offset	Bits	Name	Init	Description
0x0000	Config			
	0	TIM_Enable	0x0	TIM detection is enabled when 0x1.
	1	NonSpecificMessage	0x0	Ignore expected TTI message and assume non-specific repeating byte message when 0x1. When 0x0 the TTI message has to match the specified expected message (16 byte TTI message or repeating specific byte message).
0x0002	Counters			
	3 - 0	MultiFramesToSet_TIM	0x5	Range 2 to 15 Number of multiframes to set TIM alarm.
	7 - 4	MultiFramesToReset_TIM	0x3	Range 2 to 15 Number of multiframes to reset TIM alarm.

Table 26: Section BER Detection Configuration (T_TOH_MONITOR_BIP_Detector_Config)

Offset	Bits	Name	Init	Description
0x0000	0	PoissonErrorCheck	0x0	Assume Poisson error distribution when 0x1, bursty distribution when 0x0.
0x0002		PoissonDetector_Config		T_BIP_PoissonDetector_Config (See page 164) Configuration for DEG/EXC detection, assuming Poisson distribution of errors.
0x0014		BurstyDetector_Config		T_Line_BIP_BurstyDetector_Config (See page 165) Configuration for DEG detection, assuming bursty distribution of errors.

Table 27: Poisson Distribution BER Detection (T_BIP_PoissonDetector_Config)

Offset	Bits	Name	Init	Description
0x0000	PoissonCommon_Config			
	0	DEG_Use125usCounter	0x0	Use 125 us interval length for DEG detection when 0x1, otherwise 500 us interval length.
	1	EXC_Use125usCounter	0x0	Use 125 us interval length for EXC detection when 0x1, otherwise 500 us interval length.
	2	BurstProtection	0x0	Enables Burst Protection when 0x1.
0x0002	15 - 0	DEG_DetectionErrorThreshold	0xFFFF	Range 1 to 65535 Minimum number of bit errors within a window for DEG detection.
0x0004	15 - 0	DEG_DetectionWindowSize	0xFFFF	Range 1 to 65535 Window size for DEG detection in 125/500 us intervals.
0x0006	15 - 0	DEG_RecoveryErrorThreshold	0xFFFF	Range 1 to 65535 Allowed number of bit errors within a window for DEG recovery (error threshold for which the DEG state will not be exited).
0x0008	15 - 0	DEG_RecoveryWindowSize	0x1	Range 1 to 65535 Window size for DEG recovery in 125/500 us intervals.
0x000A	15 - 0	EXC_DetectionErrorThreshold	0xFFFF	Range 1 to 65535 Minimum number of bit errors within a window for EXC detection.
0x000C	15 - 0	EXC_DetectionWindowSize	0xFFFF	Range 1 to 65535 Window size for EXC detection in 125/500 us intervals.
0x000E	15 - 0	EXC_RecoveryErrorThreshold	0xFFFF	Range 1 to 65535 Maximum allowed number of bit errors within a window for EXC recovery (error threshold for which the EXC state will not be exited).
0x0010	15 - 0	EXC_RecoveryWindowSize	0x1	Range 1 to 65535 Window size for EXC recovery in 125/500 us intervals.

Table 28: Section Bursty Distribution BER Detection (T_Line_BIP_BurstyDetector_Config)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	DEG_DetectionErrorThreshold_ LSB	0xFFFF	integer range 0 to 768000 (two addresses) Least significant bits of Detection Error Threshold. An (one second) interval is bad if the number of detected errored bits in that interval is greater than or equal to this threshold.
0x0002	Detection_Config			
	3 - 0	DEG_DetectionWindowSize	0xA	range 2 to 10 Number of consecutive bad intervals before DEG is declared.
	7 - 4	DEG_DetectionErrorThreshold_ MSB	0xF	integer range 0 to 768000 (two addresses) Most significant bits of Detection Error Threshold. An (one second) interval is bad if the number of detected errored bits in that interval is greater than or equal to this threshold.
0x0004	15 - 0	DEG_RecoveryErrorThreshold_ LSB	0xFFFF	range 0 to 768000 (two addresses) Least significant bits of Recovery Error Threshold. An (one second) interval is a good interval when the number of errored bits in this interval does not exceed this threshold.
0x0006	Recovery_Config			
	3 - 0	DEG_RecoveryWindowSize	0x2	range 2 to 10 Number of consecutive good intervals before DEG is cleared.
	7 - 4	DEG_RecoveryErrorThreshold_ MSB	0xF	range 0 to 768000 (two addresses) Most significant bits of Recovery Error Threshold. An (one second) interval is a good interval when the number of errored bits in this interval does not exceed this threshold.

13.9 TOH GENERATOR

Table 29: TOH Generator (T_TOH_GENERATOR)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_TOHG_Common_Config (See page 166) General configuration.
0x0100		Line_Config		rw	Array (4) of T_TOHG_Line_Config (See page 167) Offset between two elements = 0x8. Array index indicates the line (= line number - 1). Configuration.
0x0200		TTI_Contents	All 0x0	rw	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. This array contains the TTI sequence for the four lines: • bytes 0-15: TTI message for line 1 • bytes 16-31: TTI message for line 2 • bytes 32-47: TTI message for line 3 • bytes 48-63: TTI message for line 4 Note: Bytes 16 to 63 are not used in STM-4 mode.

Table 29: TOH Generator (T_TOH_GENERATOR)

Offset	Bits	Name	Init	Access	Description
0x0400		TOH_Contents	See desc.	rw	Array (324) of nine_bits Offset between two elements = 0x2. Array index indicates the TOH byte number. This array contains the TOH for a single STM-4 or 4 times STM-1. Each TOH byte is represented by a nine bit word. The most significant bit determines the source of the corresponding byte (0x0 = internal memory, 0x1 = TOH Port Interface). This way of determining the source of a byte is the default behavior. For certain bytes (DCC-bytes, M1, K1, K2), other sources than internal memory or TOH-Port can be selected by extra settings which override this default behavior. The least significant byte contains the byte value when this bytes has to be inserted from memory. The order in which bytes are mapped in memory is the same order as these bytes appear in the TOH. For STM-1 mode the columns are byte interleaved: column #1 corresponds to line 1, column 2 to line 2, etc. The byte number can easily be calculated as follows: byte number = (a-1)x36 + (b-1)x4 + c-1 where • a = row number (1 to 3, 5 to 9) • b = multi-column number (1 to 9) • c, for STM-4 mode = depth of the interleave within the multi-column (1-4) • c, for STM-1 mode = line number (1-4) See also [ITU-T G.707/Y.1322] for the TOH bytes locations. Note 1: Space is also reserved for the administrative Unit Pointer bytes (a = 4) but these bytes are not used. Note 2: K1/K2 can not be sourced from this internal memory. Separate sixteen bit registers are provided for these bytes to guarantee that K1 and K2 are kept together. Note 3: B1 and B2 byte locations serve as an error mask which will be EXORed with the calculated BIP. These locations must be 0x00 for normal operation. Note 4: A1 bytes (bytes 0-11) are initialized to 0xF6, A2 bytes (bytes 12-23) are initialized to 0x28. All other entries are initialized to 0x00.

Table 30: Transmit TOH Port Configuration (T_TOHG_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	TOH_Port_Enable	0x0	Enables TX side TOH port when 0x1.

Table 31: TOH Configuration (T_TOHG_Line_Config)

Offset	Bits	Name	Init	Description
0x0000	Sources			
	0	RSOH_DCC_Select	0x0	Select mode for DCC port. The DCC port requests RS DCC bytes (D1-D3) when 0x1 and MS DCC bytes (D4-D12) when 0x0. Only valid when DCC port is enabled.
	1	DCC_Port_Enable	0x0	The DCC port is enabled when 0x1 and RSOH_DCC_Port_Select setting determines which set of DCC bytes will be filled in from the DCC port (RS DCC or MS DCC). For the other set, default behavior applies (see TOH_Contents). Default behavior applies both for RSOH and MSOH DCC bytes when 0x0.
	2	REI_Ring_Port_Enable	0x1	REI, in M1. M1 contents is taken from Ring Port when 0x1, default behavior applies when 0x0.
	4 - 3	K1K2_Source	0x0	Source for K1 and K2 bytes: • 0x0 = Register • 0x1 = TOH Port • 0x2 = Rx APS • 0x3 = Reserved
	6 - 5	RDI_Source	0x2	Source for RDI, in K2 (b6-b8). • 0x0 = Register • 0x1 = TOH Port • 0x2 = Ring Port • 0x3 = None
0x0002	15 - 0	K1K2_Value	0x0	Values for K1 and K2 bytes, used when Source is Register. K1 is least significant byte, K2 is most significant byte.
0x0004	2 - 0	RDI_Value	0x0	RDI value used to overwrite b1-b3 of K2 when RDI Source = Register.
0x0006	0	Scrambling_Disable	0x0	Scrambling is disabled when 0x1. Scrambling must be enabled in normal operation.

13.10 TOH AND DCC PORT

Table 32: Receive TOH and DCC Port (T_RX_TOH_DCC_PORT)

Offset	Bits	Name	Init	Access	Description
0x0000		TOH_Events_Mask	All 0x1	rw	Array (36) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH byte events. Masks for the corresponding events. Refer to TOH_Events_LatchForInt descriptions for the layout of the bits.
0x0200		Common_Config		rw	T_RXTDP_Common_Config (See page 169) General configuration.
0x0240		Line_Config		rw	Array (4) of T_RXTDP_Line_Config (See page 169) Offset between two elements = 0x2. Array index indicates the line (= line number - 1). DCC port configuration.

Table 32: Receive TOH and DCC Port (T_RX_TOH_DCC_PORT)

Offset	Bits	Name	Init	Access	Description
0x0280		TOH_Events_Summary	All 0x0	ro	Array (4) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH_Events_LatchedForInt bits. Each bit corresponds to the summary of one entry in TOH_Events_LatchForInt. Each entry of this array corresponds to the summaries of all TOH byte events for the bytes with the same interleave depth (STM-4 mode), or with the same line number (STM-1 mode). The array index and the bit position can be calculated as follows: Array index = c-1 The correlation between bit position and TOH_Events_LatchForInt entry is as follows: A bit p corresponds to the summary of TOH Events entry (px4) + c. where • a = row number (1 to 9) • b = multi-column number (1 to 9) • c, for STM-4 mode = depth of the interleave within the multi-column (1-4) • c, for STM-1 mode = line number (1-4) • p = bit position (0 to 8, least significant bit is 0) See also [ITU-T G.707/Y.1322] for the TOH bytes locations.
0x02C0		TOH_Events_Summary_Mask	All 0x1	rw	Array (4) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH_Events_LatchedForInt bits. Summary mask of TOH Events. Refer to TOH_Events_Summary descriptions for the layout of the bits.
0x0300		TOH_Events_LatchForInt	All 0x0	cow_1	Array (36) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH byte events. Latched events on TOH bytes. Events occur if the TOH byte content has a different value as the one in the previous frame. The array index and the bit position within the corresponding entry can be calculated as follows: Array index = (a-1)x4 + c-1 Bit position = b-1 where • a = row number (1 to 9) • b = multi-column number (1 to 9) • c, for STM-4 mode = depth of the interleave within the multi-column (1-4) • c, for STM-1 mode = line number (1-4) See also [ITU-T G.707/Y.1322] for the TOH bytes locations.

Table 32: Receive TOH and DCC Port (T_RX_TOH_DCC_PORT)

Offset	Bits	Name	Init	Access	Description
0x0400		TOH_Contents	All 0x0	ro	Array (324) of byte Offset between two elements = 0x2. Array index indicates the TOH byte number. Received TOH bytes (raw, unprocessed values, except B1/B2). The order in which bytes are mapped in memory is the same order as these bytes appear in the TOH. For STM-1 mode the columns are byte interleaved: column #1 corresponds to line 1, column 2 to line 2, etc. The byte number can easily be calculated as follows: byte number = (a-1)x36 + (b-1)x4 + c-1 where • a = row number (1 to 9) • b = multi-column number (1 to 9) • c, for STM-4 mode = depth of the interleave within the multi-column (1-4) • c, for STM-1 mode = line number (1-4) See also [ITU-T G.707/Y.1322] for the TOH bytes locations. Note: B1 and B2 locations contain the EXOR of the calculated BIP with the received BIP.

Table 33: Receive TOH Port Configuration (T_RXTDP_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	TOH_Port_Enable	0x0	TOH Port is enabled when 0x1.

Table 34: Receive DCC Port Configuration (T_RXTDP_Line_Config)

Offset	Bits	Name	Init	Description
0x0000	0	RSOH_DCC_Select	0x0	Select mode for DCC port. The DCC port sends RS DCC bytes (D1-D3) when 0x1 and MS DCC bytes (D4-D12) when 0x0. Only valid when the DCC port is enabled.
	1	DCC_Port_Enable	0x0	The DCC port is enabled when 0x1 and the RSOH_DCC_Port_Select setting determines which set of DCC bytes will be sent out on the DCC port (RS DCC or MS DCC).

13.11 HIGH ORDER POINTER TRACKER AND RETIMER

Table 35: Pointer Tracker and Retimer (T_HO_PTR_RETIMER)

Offset	Bits	Name	Init	Access	Description
0x0000	0	DetectedConcat_Event_Mask	0x1	rw	Detected Concatenation event mask.
0x0040	0	DetectedConcat_Event_Latch ForInt	0x0	cow_1	Detected Concatenation event latched for interrupt.
0x0080		CorrDefects_SummaryMask		rw	T_HOPTRRT_Defects_Summary (See page 170) Summary mask.
0x00C0		CorrDefects_Summary		ro	T_HOPTRRT_Defects_Summary (See page 170) Summary.
0x0100		Reserved	0x0	ro	Reserved.
0x0140		Reserved	0x0	ro	Reserved.
0x0180		Common_Config		rw	T_HOPTRRT_Common_Config (See page 171) General configuration.
0x01C0		AUG1_Mode_Config		rw	T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.
0x01E0	11 - 0	DetectedConcat	0x0	ro	Detected concatenation in the Pointer Tracker. A '1' means a concatenation indication (Y1*) has been detected on the pointer bytes of the corresponding timeslot (least significant bit corresponds to the first timeslot).
0x0200		VCx			Array (12) of T_HOPTRRT_VCx (See page 171) Offset between two elements = 0x20. Array index indicates the high order path. Configuration and status.

Table 36: Pointer Tracker and Retimer Defect/Event Summary (T_HOPTRRT_Defects_Summary)

Offset	Bits	Name	Init	Description
0x0000	11 - 0	Summary	0xFFF	Defects summary, one bit per high order path. Least significant bit corresponds to the first high order path.
	12	DetectedConcat_Event	0x1	Event telling detected concatenation has changed.

Table 37: Pointer Tracker and Retimer Common Configuration (T_HOPTRRT_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	AIS_Config			
	0	AU_AIS_AIS_Insert_Disable	0x0	Insertion of AU AIS on AU AIS detection by the Pointer Tracker is disabled when 0x1.
	1	LOP_AIS_Insert_Disable	0x0	Insertion of AU AIS on Loss Of Pointer is disabled when 0x1 by the Pointer Tracker.
	2	TSF_AIS_Insert_Disable	0x0	Insertion of AU AIS on TSF is disabled when 0x1.
	3	FifoError_AIS_Insert_Disable	0x0	Insertion of AU AIS on a FIFO Error is disabled when 0x1.
0x0002	0	Reserved	0x0	Reserved.

Table 38: Pointer Tracker and Retimer Per Path (T_HOPTRRT_VCx)

Offset	Bits	Name	Init	Access	Description
0x0000		VC3_TUG3_Config		rw	T_HOPTRRT_VC3_TUG3_Config (See page 171) Per VC-3/TUG-3 configuration.
0x0006		VCx_Status		ro	T_HOPTR_VCx_Status (See page 172) Pointer Tracker Status.
0x0008		PerfCounters_Shadow		ro	T_HOPTRRT_PerfCounters (See page 172) Performance counters.
0x000C		CorrDefects_Mask		rw	T_HOPTRRT_Defects (See page 172) Correlated defects mask.
0x000E		CorrDefects_Unlatched		ro	T_HOPTRRT_Defects (See page 172) Correlated defects.
0x0010		CorrDefects_LatchForInt		cow_1	T_HOPTRRT_Defects (See page 172) Correlated defects latched for interrupt.
0x0012		Reserved	0x0	cow_1	Reserved.
0x0014		Reserved	0x0	ro	Reserved.
0x0016		Reserved	0x0	ro	Reserved.

Table 39: Pointer Tracker and Retimer Path Configuration (T_HOPTRRT_VC3_TUG3_Config)

Offset	Bits	Name	Init	Description
0x0000	General_Config			
	0	AIS_Force	0x0	Insertion of AU AIS (after the Retimer) is forced when 0x1.
	2 - 1	SS_bits	0x2	SS bits to be used in the Pointer Generator.

Table 39: Pointer Tracker and Retimer Path Configuration (T_HOPTRRT_VC3_TUG3_Config)

Offset	Bits	Name	Init	Description
0x0002	15 - 0	SlowLeakRegister	0x10	Slow Leak Register (consult documentation).
0x0004	15 - 0	FastLeakRegister	0x10	Fast Leak Register (consult documentation).

Table 40: Pointer Tracker Path Status (T_HOPTR_VCx_Status)

Offset	Bits	Name	Init	Description
0x0000	1 - 0	Reported_SS_Bits	0x0	Received SS bits reported by the Pointer Tracker.

Table 41: Pointer Justification Counters (T_HOPTRRT_PerfCounters)

Offset	Bits	Name	Init	Description
0x0000	IncomingJustifications			
	7 - 0	Incoming_PJ	0x0	range 0 to 0xFE Positive Justifications as counted by the Pointer Tracker.
	15 - 8	Incoming_NJ	0x0	range 0 to 0xFE Negative Justifications as counted by the Pointer Tracker.
0x0002	OutgoingJustifications			
	7 - 0	Outgoing_PJ	0x0	range 0 to 0xFE Positive Justifications as generated by the Pointer Generator.
	15 - 8	Outgoing_NJ	0x0	range 0 to 0xFE Negative Justifications as generated by the Pointer Generator.

Table 42: Pointer Tracker and Retimer Defects (T_HOPTRRT_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	AIS	0x1	AIS, detected by the Pointer Tracker.
	1	LOP	0x1	Loss of Pointer.
	2	Fifo_Error	0x1	Retimer FIFO Error.

13.12 RETIMER

Table 43: Retimer (T_RETIMER)

Offset	Bits	Name	Init	Access	Description
0x0000		AUG1_Mode_Config		rw	T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.
0x0010		CorrDefects_Mask		rw	T_RT_Defects (See page 173) Correlated defects mask.
0x0020		CorrDefects_Unlatched		ro	T_RT_Defects (See page 173) Correlated defects.
0x0030		CorrDefects_LatchForInt		cow_1	T_RT_Defects (See page 173) Correlated defects latched for interrupt.
0x0040		Common_Config		rw	T_RT_Common_Config (See page 173) General configuration.
0x0080		VCx			Array (12) of T_RT_VCx (See page 174) Offset between two elements = 0x8. Array index indicates the high order path. Configuration and status.

Table 44: Retimer Defects (T_RT_Defects)

Offset	Bits	Name	Init	Description
0x0000	11 - 0	FIFO_Errors	0xFFF	FIFO Errors, one bit per high order path. Least significant bit corresponds to the first high order path.
	12	LOF	0x1	Loss Of Frame defect on external reference frame sync (REFTXFS).

Table 45: Retimer Common Configuration (T_RT_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	Reserved	0x0	Reserved.
0x0002	0	COMBUS_Bypass	0x0	No retiming is done when 0x1. It is mandatory to set this field to 0x0 when the Add Telecombus operates in slave mode.
0x0004	0	ExtFramePulseExpected	0x0	Lock on external reference frame sync (REFTXFS) when 0x1.
0x0006	0	ExtFramePulseNegEdge	0x0	Sample external reference frame sync (REFTXFS) on negative clockedge when 0x1.
0x0008	13 - 0	ExtFramePulseOffset	0x0	Range 0 to 9719 Offset between external reference frame sync (REFTXFS) and system reference frame sync.
0x000A	13 - 0	Reserved	0x25E4	Reserved.
0x000C	13 - 0	Reserved	0x25E1	Reserved.

Table 46: Retimer Per Path (T_RT_VCx)

Offset	Bits	Name	Init	Access	Description
0x0000		VC3_TUG3_Config		rw	T_RT_VC3_TUG3_Config (See page 174) High order path configuration.
0x0006		PerfCounters_Shadow		ro	T_RT_PerfCounters (See page 174) Performance Counters.

Table 47: Retimer Path Configuration (T_RT_VC3_TUG3_Config)

Offset	Bits	Name	Init	Description
0x0000	1 - 0	SS_bits	0x2	SS bits to be used in the Pointer Generator.
0x0002	15 - 0	SlowLeakRegister	0x10	Slow Leak Register (consult documentation).
0x0004	15 - 0	FastLeakRegister	0x10	Fast Leak Register (consult documentation).

Table 48: Retimer Performance Counters (T_RT_PerfCounters)

Offset	Bits	Name	Init	Description
0x0000	OutgoingJustifications			
	7 - 0	Outgoing_PJ	0x0	range 0 to 0xFE Positive Justifications, as generated by the pointer generator.
	15 - 8	Outgoing_NJ	0x0	range 0 to 0xFE Negative Justifications, as generated by the pointer generator.

13.13 CLOCK RECOVERY/CLOCK SYNTHESIS/SERDES

Table 49: Clock Recovery/Clock Synthesis/SerDes (T_ANALOG)

Offset	Bits	Name	Init	Access	Description
0x0000		TestControl		rw	T_TestControl (See page 176) Configuration of the PRBS generator/analyzer at the cross connect.
0x0020		Common_Config		rw	T_ANALOG_Common_Config (See page 177) Loopback selection routes input or output data to different output/inputs for test purposes.
0x0030		PadPowerDown		rw	T_PadPowerDown (See page 178) Powerdown for each LVPECL and LVDS pad.
0x0040	11 - 0	Status_Unlatched	0x0	ro	Unlatched Status. • bit 0: reserved • bit 1: reserved • bit 2: reserved • bit 3: reserved • bit 4: reserved • bit 5: Lock indication Transmit PLL • bit 6: Lock indication Receive PLL • bit 7: SignalDetect Line 1 • bit 8: SignalDetect Line 2 • bit 9: SignalDetect Line 3 • bit 10: SignalDetect Line 4 • bit 11: Lock indication PRBS analyzer
0x0044	11 - 0	Status_LatchForInt	0x0	cow_1	Status Latched for Interrupt, see Unlatched Status
0x0048	11 - 0	Status_Mask	0xFFF	rw	Status Mask, see Unlatched Status
0x004C	2 - 0	DivideClocks	0x0	rw	Divide clocks by 4. For every bit in the list, 0x1 divides the corresponding clock by 4. • bit 0: Line 1 receive clock • bit 1: APS receive clock • bit 2: Transmit clock Note: The undivided APS receive clock and Transmit Clock are always 77.76 MHz. Line 1 receive clock frequency depends on the operational mode (77.76 MHz in STM-4 mode, 19.44 MHz in STM-1 mode.
0x0050		CDR_CS_Setup		rw	T_CDR_CS_Setup (See page 178) Setup and initialization of the Clock Recovery, Serializer and Deserializer (CDR/CS).
0x0060		PLL_Control		rw	T_PLL_Control (See page 179) Control of the PLL's in Clock Recovery, Serializer and Deserializer (CDR/CS).

Table 50: Test Configuration (T_TestControl)

Offset	Bits	Name	Init	Description
0x0000	0	Reserved	0x0	Reserved.
0x0002	0	Reserved	0x0	Reserved.
0x0004	3 - 0	Reserved	0x0	Reserved.
0x0006	0	Reserved	0x0	Reserved.
0x0008	3 - 0	Reserved	0x0	Reserved.
0x000A	0	Reserved	0x0	Reserved.
0x000C		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration for the PRBS generator/analyzer at the cross connect.
0x000E		XConnectPRBSControl		T_XConnectPRBSControl (See page 176) Configuration of the PRBS generator/analyzer in the cross connect.

Table 51: PRBS Configuration (T_XConnectPRBSControl)

Offset	Bits	Name	Init	Description
0x0000	0	EnablePRBSGenerator	0x0	The PRBS generator at the cross connect is enabled when 0x1, disabled when 0x0.
	4 - 1	PRBSGeneratorChannel	0x0	range 0 to 11 Path on which PRBS is inserted.
	5	InvertPRBSGeneratorOutput	0x1	The output of the PRBS generator is inverted when 0x1.
	6	EnablePRBSAnalyzer	0x0	The PRBS analyzer at the cross connect is enabled when 0x1, disabled when 0x0.
	10 - 7	PRBSAnalyzerChannel	0x0	range 0 to 11 Path on which PRBS is received.
	11	InvertPRBSAnalyzerOutput	0x1	The received bits are inverted before they are analyzed by the PRBS analyzer when 0x1.

Table 52: CDR/CS Configuration (T_ANALOG_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	SerDes_LoadConfig	0x0	Writing 0x1 to this register will start the transmission of the control signals to the SerDes. When the transmission is finished this register is reset to its default value. Writing 0x0 to the register is ignored. The following settings are transmitted: • CDR_CS_Setup.TxPowerDown • CDR_CS_Setup.RxPowerDown1 • CDR_CS_Setup.RxPowerDown2 • CDR_CS_Setup.ToplevelPowerDown • CDR_CS_Setup.OC3NotOC12 • PLL_Control.TxPLL_Cap_Enable • PLL_Control.RxPLL_Cap_Enable • PLL_Control.TxPLL_PowerDown • PLL_Control.RxPLL_PowerDown • PLL_Control.CDRTune[4:0] • PLL_Control.PLLTune • All settings configured via the indirect access register (CDR_CS_Setup.Indirect_AccessData and Common_Config.IndirectAccessMode)
0x0002	4 - 0	SysLoop	0x0	System Loopback Select, it routes the serialized transmit output to the deserializer receive input. Each bit controls a line. The corresponding LIU is in normal operation when 0x0 and is looped back when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0004	4 - 0	FacLoop	0x0	Facility Loopback Select, it routes the receive serial input back to the transmit serial output. Each bit controls a line. The corresponding LIU is in normal operation when 0x0 and is looped back when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0006	5 - 0	IndirectAccessMode	0x0	Selects the mode for the IndirectAccessData register. • 0x0: Mode0 • 0x8: Mode1 • All others: Reserved

Table 53: High Speed Interface Power Down (T_PadPowerDown)

Offset	Bits	Name	Init	Description
0x0000	4 - 0	RxPAD	0x1F	Power Down for the Receive Line and APS pads. Each bit controls a receive pad. The corresponding pad is powered down when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0002	4 - 0	TxPAD	0x1F	Power Down for the Transmit Line and APS pads. Each bit controls a transmit pad. The corresponding pad is powered down when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0004	0	TxRefClock2	0x1	Power Down for the Transmit Reference Clock Pad, REFTXCLK2. The pad is powered down when 0x1.

Table 54: Setup of Clock Recovery/Clock Synthesis/SerDes (T_CDR_CS_Setup)

Offset	Bits	Name	Init	Description
0x0000	9-0	TxPowerDown	0x3FF	Power down for the SerDes transmit section. Must be set to 0x0 at power-up.
0x0002	0	LineRate	0x0	Indicates the line rate for the selected line when line timing is used. Line rate is 155.52 Mbit/s when 0x0, 622.08 Mbit/s when 0x1. Note: This setting is only applicable for the line selected by LineTimingChannel when TimingMode is 0x1.
0x0004	13-0	RxPowerDown1	0x3FFF	Power down for the SerDes receive section. Must be set to 0x0 at power-up.
0x0006	14-0	RxPowerDown2	0x7FFF	Power down for the SerDes receive section. Must be set to 0x0 at power-up.
0x0008	0	ToplevelPowerDown	0x1	Power down for the toplevel SerDes bias module. Must be set to 0x0 at power-up.
0x000A	4 - 0	OC3NotOC12	0x1F	Line Rate Configuration • 0x0E: STM-4 Mode • 0x0F: STM-1 Mode • All others: Reserved
0x000C	15 - 0	PRBSBitErrorCounter	0x0	Bit Error counter of the PRBS analyzer at the cross connect. This (read-only) counter is clear-on-read.
0x000E	15 - 0	IndirectAccessData	0x0	Indirect Access Data register. When a write is done to this register, the field specified by the IndirectAccessMode will be configured. Following values need to be set when initializing the CDR/CS: • 0x0017 to IndirectAccessMode Mode0 • 0x5000 to IndirectAccessMode Mode1

Table 55: PLL Control (T_PLL_Control)

Offset	Bits	Name	Init	Description
0x0000	0	TimingMode	0x0	External/Line timing mode selection for the transmit PLL. External timing mode is selected when 0x0, TxRefSelect selects the external source. Line-Timing mode is selected when 0x1, LineTimingChannel selects the line timing channel.
0x0002	2 - 0	LineTimingChannel	0x0	range 0 to 4 Line timing mode channel selection. This field is only used when TimingMode is '1'. The value indicates the line. • 0x0: Line 1 • 0x1: Line 2 • 0x2: Line 3 • 0x3: Line 4 • 0x4: APS
0x0004	0	TxRefSelect	0x0	Transmit reference clock external source selection for the PLL in the transmit section. This field is only valid when TimingMode is '0'. • 0x0: REFTXCLK1 is used as reference clock • 0x1: REFTXClK2 is used as reference clock
0x0006	0	RxRefSelect	0x0	Receive reference clock external source selection for the PLL in the receive section. • 0x0: REFRXCLK is used as reference clock • 0x1: REFTXCLK1/REFTXCLK2 is used as reference clock, the selection between the transmit reference clocks is made using the TxRefSelect field
0x0008	0	TxPLL_Cap_Enable	0x0	Enables the external capacitor in the Transmit PLL when 0x1.
0x000A	0	RxPLL_Cap_Enable	0x0	Reserved. Must be set to 0.
0x000C	1 - 0	TxRefFreq	0x0	Transmit PLL reference clock frequency. Indicates the frequency of the reference clock for the PLL. • 0x0: 19.44 MHz, REFTXCLK1 or REFTXCLK2 • 0x1: 77.76 MHz, REFTXCLK1 or REFTXCLK2 • 0x2: 155.52 MHz, REFTXCLK2 • 0x3: 622.04 MHz, REFTXCLK2. In this mode the Transmit PLL must be bypassed. Mind the Transmit PLL is actually still working then, although it' s output is never used.
0x000E	1 - 0	RxRefFreq	0x0	Receive PLL reference clock frequency. Indicates the frequency of the reference clock for the PLL. • 0x0: 19.44 MHz, REFRXCLK or REFTXCLK1 or REFTXCLK2 • 0x1: 77.76 MHz, REFRXCLK or REFTXCLK1 or REFTXCLK2 • 0x2: 155.52 MHz, REFTXCLK2 • 0x3: Reserved
0x0010	4-0	TxPLL_PowerDown	0x1F	Power Down for the Transmit PLL modules. Must be set to 0x0 at power-up.
0x0012	4-0	RxPLL_PowerDown	0x1F	Power Down for the RxPLL modules. Must be set to 0x0 at power-up.
0x0014		CDRTune		Array (5) of T_CDRTune (See page 180) Offset between two elements = 0x2. Array index indicates the interface. • Array index 0: Line 1 • Array index 1: Line 2 • Array index 2: Line 3 • Array index 3: Line 4 • Array index 4: APS
0x001E		PLLTune		T_PLLTune (See page 180)

Table 56: CDR Tuning Configuration (T_CDRTune)

Offset	Bits	Name	Init	Description
0x0000	2 - 0	PhaseInterpolator	0x4	Reserved. Set to 0x4 for STM-4/OC-12 application Set to 0x1 for STM-1/OC-3 application
	12 - 3	DigitalLoopFilter	0x4A	Reserved. Set to 0x4a for STM-4/OC-12 application Set to 0x5c for STM-1/OC-3 application

Table 57: PLL Tuning Configuration (T_PLLTune)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	TxPLL_ChargePump	0x4	Reserved. Set to 0x1 for External Timing. Set to 0x4 for Line/Loop Timing and STM-4/OC-12 application Set to 0x8 for Line/Loop Timing and STM-1/OC-3 application
	6 - 4	TxPLL_VCO	0x4	Reserved. Set to 0x1
	10 - 7	RxPLL_ChargePump	0x4	Reserved. Set to 0x4
	13 - 11	RxPLL_VCO	0x4	Reserved Set to 0x1

13.14 RECEIVE APS PORT

Table 58: Receive APS Port (T_RX_APS)

Offset	Bits	Name	Init	Access	Description
0x0000	7 - 0	Reported_TTI_Message	0x0	ro	Received J0 byte.
0x0010		Common_Config		rw	T_RX_APS_Common_Config (See page 181) General configuration.
0x0018	7 - 0	Expected_TTI_Message	0x0	rw	Expected J0 byte.
0x0020		CorrDefects_Unlatched		ro	T_RX_APS_Defects (See page 181) Correlated defects.
0x0028		CorrDefects_LatchForInt		cow_1	T_RX_APS_Defects (See page 181) Correlated defects latched for interrupt.
0x0030		CorrDefects_Mask		rw	T_RX_APS_Defects (See page 181) Correlated defects mask.
0x0038	15 - 0	B1_PM_Counter	0x0	ro	B1 performance counter.
0x0040		APS_Info			Array (4) of T_RX_APS_APSInfo (See page 181) Offset between two elements = 0x10. Array index indicates the line (= line number - 1). Received APS information.

Table 59: Receive APS Port Common Configuration (T_RX_APS_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	LOF_AIS_Insert_Disable	0x0	Insertion of AIS on Loss of Frame defect is disabled when 0x1.
	1	Framer_AIS_Force	0x0	AIS insertion is forced after framing when 0x1.
	2	Descrambler_Disable	0x0	Descrambling is disabled when 0x1.
	3	TIM_AIS_Insert_Disable	0x0	Insertion of AIS on Trail Trace Identifier Mismatch defect is disabled when 0x1.
	4	SSF_AIS_Insert_Disable	0x0	Insertion of AIS on incoming Server Signal Fail is disabled when 0x1.
	5	APS_AIS_Force	0x0	AIS insertion is forced after APS monitoring when 0x1.

Table 60: Receive APS Port Defects (T_RX_APS_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	OOF	0x1	Out of Frame.
	1	LOF	0x1	Loss of Frame.
	2	B1_Error	0x1	B1 BIP error.
	3	TIM	0x1	J0 Trail Trace Identifier mismatch.
	4	SSF	0x1	Incoming SSF (Server Signal Fail).

Table 61: Receive APS Port Per Line (T_RX_APS_APSInfo)

Offset	Bits	Name	Init	Access	Description
0x0000		APS_Bytes		ro	T_RX_APS_APSBytes_Status (See page 181) Received APS information.
0x0006		APSEvents_Unlatched		ro	T_RX_APS_APSBytes_Event (See page 182) Events on APS bytes.
0x0008		APSEvents_LatchForInt		cow_1	T_RX_APS_APSBytes_Event (See page 182) Events on APS bytes latched for interrupt.
0x000A		APSEvents_Mask		rw	T_RX_APS_APSBytes_Event (See page 182) Events on APS bytes mask.

Table 62: Receive APS Port Status (T_RX_APS_APSBytes_Status)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	RX_K1K2	0x0	Received K1/K2 bytes (most significant byte is K1, least significant byte is K2).
0x0002	15 - 0	TX_K1K2	0x0	K1/K2 bytes to transmit (most significant byte is K1, least significant byte is K2).
0x0004	15 - 0	Status_Request	0x0	Received SF and SD indications and indications for switch/bridge requests (most significant byte is status (bit 0 is SF and bit 1 is SD), least significant byte is switch/bridge request).

Table 63: Receive APS Port Events (T_RX_APS_APSBytes_Event)

Offset	Bits	Name	Init	Description
0x0000	0	RX_K1K2_Changed	0x1	Receive K1/K2 changed.
	1	TX_K1K2_Changed	0x1	Transmit K1/K2 changed.
	2	Status_Request_Changed	0x1	Status/Request information changed.

13.15 CROSS CONNECT

Table 64: Cross Connect (T_VC_XCONNECT)

Offset	Bits	Name	Init	Access	Description
0x0000		Termination_Config		rw	T_XC_Bus_Config (See page 182) Configuration for the Terminal interface bus.
0x0040		Line_Config		rw	T_XC_Bus_Config (See page 182) Configuration for the Line interface bus.
0x0060		APS_Config		rw	T_XC_Bus_Config (See page 182) Configuration for the APS Port bus.

Table 65: Cross Connect Bus Configuration (T_XC_Bus_Config)

Offset	Bits	Name	Init	Description
0x0000		AUG1		T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.
0x0002		Timeslot		Array (12) of T_XConnect_Config (See page 183) Offset between two elements = 0x2. Array index indicates the high order path. cross connect configuration.

Table 66: Cross Connect Time Slot Configuration (T_XConnect_Config)

Offset	Bits	Name	Init	Description
0x0000	8 - 0	SourceTimeslot	0x0	Range 0 to 11 Source time slot for this output slot.
	10 - 9	SourceBus	0x0	Range 0 to 2 Source bus for this output slot. • 0x0 = Line Interface • 0x1 = APS Interface • 0x2 = Terminal Interface
	13 - 11	Reserved	0x0	Reserved.
	14	Force_AIS	0x0	The AIS pattern is inserted in this timeslot when 0x1.
	15	Force_Uneq	0x1	The Uneq pattern is inserted in this timeslot when 0x1.

13.16 ADD TELECOM BUS

Table 67: Add Telecom Bus (T_DI_COMBUS)

Offset	Bits	Name	Init	Access	Description
0x0000		Global_CorrDefects_Mask		rw	T_DICB_Global_CorrDefects (See page 184) Correlated global defects mask.
0x0004		VCx_CorrDefects_Summary		ro	T_DICB_VCx_CorrDefects_Summary (See page 184) Defects summary.
0x0008		VCx_CorrDefects_SummaryMask		rw	T_DICB_VCx_CorrDefects_Summary (See page 184) Defects summary mask.
0x000C		Global_CorrDefects_Unlatched		ro	T_DICB_Global_CorrDefects (See page 184) Correlated global defects.
0x000E		Global_CorrDefects_LatchForInt		cow_1	T_DICB_Global_CorrDefects (See page 184) Correlated global defects latched for interrupt.
0x0010		Common_Config		rw	T_DICB_Common_Config (See page 184) General configuration.
0x0020		VCx_CorrDefects_Unlatched		ro	Array (12) of T_DICB_VCx_CorrDefects (See page 185) Offset between two elements = 0x2. Array index indicates the high order path. Correlated defects.
0x0040		VCx_CorrDefects_LatchForInt		cow_1	Array (12) of T_DICB_VCx_CorrDefects (See page 185) Offset between two elements = 0x2. Array index indicates the high order path. Correlated defects latched for interrupt.
0x0060		VCx_CorrDefects_Mask		rw	Array (12) of T_DICB_VCx_CorrDefects (See page 185) Offset between two elements = 0x2. Array index indicates the high order path. Correlated defects mask.

Table 68: Add Bus Common Defects (T_DICB_Global_CorrDefects)

Offset	Bits	Name	Init	Description
0x0000	0	C1_LOF	0x1	C1 Loss Of Frame.
	1	ParityError	0x1	Parity Error on the Telecom Bus.

Table 69: Add Bus Defect Summary (t_dicb_VCx_CorrDefects_Summary)

Offset	Bits	Name	Init	Description
0x0000	11 - 0	Summary	0xFFF	Defect Summary, one bit per high order path. Least significant bit corresponds to the first high order path.

Table 70: Add Bus Common Configuration (T_DICB_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	ClockEdge_Config			
	0	Sample_SelectNegativeClock Edge	0x0	Configure the edge on which the timing and data signals are sampled. Negative clock edge when 0x1, positive clock edge when 0x0.
	1	Output_SelectNegativeClock Edge	0x0	Configure the edge on which the timing signals are clocked out. Negative clock edge when 0x1, positive clock edge when 0x0.
0x0002	3 - 0	TimingDelay	0x0	Range 0 to 15 Configure expected Delay between Timing and Data on Combus.
0x0004	Parity_Config			
	0	ParityIncludesTiming	0x0	Calculate Parity over Data only, or over Data and Timing. Timing is included when 0x1.
	1	ParityEven	0x0	Even parity when 0x1, odd parity when 0x0.
0x0006	0	Reserved	0x1	Reserved.
0x0008	9 - 0	AU_PointerValue	0x0	Integer 0, 522 Sets the fixed AU pointer value used for generating Master mode timing.
0x000A		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.
0x000C		VC3_TUG3_Mode_Config		T_VC3_TUG3_Mode_Config (See page 184) Configuration of the VC-3/TUG-3 modes.

Table 71: Telecom Bus Path Configuration (T_VC3_TUG3_Mode_Config)

Offset	Bits	Name	Init	Description
0x0000	11 - 0	Is_TUG_Structured	0xFFF	Contents of VC-3 / TUG-3, one bit per timeslot. Each bit has following meaning (least significant bit represents the first VC-3 / TUG-3, most significant bit the last VC-3 / TUG-3): The corresponding VC-3 (when AU-3 is mapped in AUG-1) or TUG-3 (when AU-4 is mapped in AUG-1) contains TUG-2 when '1'. VC-3 / TUG-3 contains C-3 / TU-3 respectively when '0'.
0x0002	11 - 0	Reserved	0x0	Reserved.

Table 72: Add Bus Path Defects (T_DICB_VCx_CorrDefects)

Offset	Bits	Name	Init	Description
0x0000	0	J1_LOF	0x1	J1 Loss Of Frame.
	1	V1_LOF	0x1	V1 Loss Of Frame.

13.17 HIGH ORDER PATH RING PORT/ALARM INTERFACE

Table 73: Path Ring Port/Alarm Interface (T_HO_POH_RING_PORT)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_HOPR_Common_Config (See page 185) General configuraton.
0x0008		CorrDefects_Unlatched		ro	T_HOPR_Defects (See page 185) Correlated defects.
0x0010		CorrDefects_LatchForInt		cow_1	T_HOPR_Defects (See page 185) Correlated defects latched for interrupt.
0x0018		Defects_Mask		rw	T_HOPR_Defects (See page 185) Correlated defects mask.
0x0020		VC_Config		rw	Array (16) of T_HOPR_VC_Config (See page 186) Offset between two elements = 0x2. Array index indicates the high order path. High order path configuration.

Table 74: Path Ring Port/Alarm Interface Common Configuration (T_HOPR_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	InsertCRCError	0x0	Insert CRC errors. All CRC bits are inverted when 0x1 (for test purposes only).

Table 75: Path Ring Port/Alarm Interface Defects (T_HOPR_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	CRC_Error	0x1	CRC error on external Ring Port interface.
	1	LOC	0x1	Loss of clock on external Ring Port interface.

Table 76: Path Ring Port/Alarm Interface Path Configuration (T_HOPR_VC_Config)

Offset	Bits	Name	Init	Description
0x0000	0	SelectExternalSource	0x0	Select external ring port when 0x1. Internal ring port is used when 0x0.
	1	ResetVC	0x0	Resets an entire VC information when 0x1.
	2	ExtendRDI	0x0	Extends RDI for 20 frames when 0x1.

13.18 JTAG MASTER

Table 77: JTAG Master (T_JTAG_MASTER)

Offset	Bits	Name	Init	Access	Description
0x0000	0	Bit_wise_control	0x0	rw	This bit selects if direct microprocessor control bits will be used, instead of the FIFO's.
0x0004	1 - 0	TDI_TMS_bit	0x0	rw	The microprocessor driven TDI and TMS bit values (bit 0 = TMS, bit 1 = TDI).
0x0008	0	TCK_bit	0x0	rw	The microprocessor driven TCK clock bit value.
0x000C	0	TDO_bit	0x0	ro	The microprocessor read TDO bit value.
0x0010	7 - 0	TCK_DIVIDER	0x0	rw	A clock divider number to create an appropriate 10 MHz TCK clock using the current System Clock.
0x0012	5 - 0	Counter	0x0	rw	6-bit shift count register.
0x0014	7 - 0	TDI_Fifo_B0	0x0	rw	FIFO containing TDI data to send to TAP (byte 0).
0x0016	7 - 0	TDI_Fifo_B1	0x0	rw	FIFO containing TDI data to send to TAP (byte 1).
0x0018	7 - 0	TDI_Fifo_B2	0x0	rw	FIFO containing TDI data to send to TAP (byte 2).
0x001A	7 - 0	TDI_Fifo_B3	0x0	rw	FIFO containing TDI data to send to TAP (byte 3).
0x001C	7 - 0	TDI_Fifo_B4	0x0	rw	FIFO containing TDI data to send to TAP (byte 4).
0x001E	7 - 0	TMS_Fifo_B0	0x0	rw	FIFO containing TMS data to send to TAP (byte 0).
0x0020	7 - 0	TMS_Fifo_B1	0x0	rw	FIFO containing TMS data to send to TAP (byte 1).
0x0022	7 - 0	TMS_Fifo_B2	0x0	rw	FIFO containing TMS data to send to TAP (byte 2).
0x0024	7 - 0	TMS_Fifo_B3	0x0	rw	FIFO containing TMS data to send to TAP (byte 3).
0x0026	7 - 0	TMS_Fifo_B4	0x0	rw	FIFO containing TMS data to send to TAP (byte 4).
0x0028	7 - 0	TDO_Fifo_B0	0x0	ro	FIFO containing TDO data received from the TAP (byte 0).
0x002A	7 - 0	TDO_Fifo_B1	0x0	ro	FIFO containing TDO data received from the TAP (byte 1).
0x002C	7 - 0	TDO_Fifo_B2	0x0	ro	FIFO containing TDO data received from the TAP (byte 2).
0x002E	7 - 0	TDO_Fifo_B3	0x0	ro	FIFO containing TDO data received from the TAP (byte 3).
0x0030	7 - 0	TDO_Fifo_B4	0x0	ro	FIFO containing TDO data received from the TAP (byte 4).
0x0032	0	Start	0x0	rw	Start bit. Is set to trigger a transfer between microprocessor & TAP. This bit clears the Done and Error bits.
0x0034	1 - 0	Done	0x0	ro	When the transfer is completed, these bits are set: • bit 0 = 'Done' • bit 1 = 'Error'

Table 77: JTAG Master (T_JTAG_MASTER)

Offset	Bits	Name	Init	Access	Description
0x0036	0	JM_TRSTN	0x0	rw	The value of TRSTN driven by the microprocessor interface.
0x0038	0	TDI_LoopBack	0x0	rw	This bit loops back the TDI FIFO output, back into the TDO FIFO Input (Used for test).
0x003A	0	TMS_LoopBack	0x0	rw	This bit loops back the TMS FIFO output, back into the TDO FIFO Input (Used for test).
0x003C	0	TRSTN_Sample	0x0	ro	This bit samples what the microprocessor interface is driving into the TAP.
0x003E	0	uProcessor_CNTRL	0x1	rw	This bit switches the TAP control over to the microprocessor.

13.19 DROP TELECOM BUS

Table 78: Drop Telecom Bus (T_DO_COMBUS)

Offset	Bits	Name	Init	Access	Description
0x0000		Reserved	0x7	rw	Reserved.
0x0008		Reserved	0x0	ro	Reserved.
0x000C		Reserved	0x0	cow_1	Reserved.
0x0010		VC3_TUG3_Config		rw	T_DOCB_VC3_TUG3_Config (See page 187) Per VC-3/TUG-3 configuration.
0x0020		Common_Config		rw	T_DOCB_Common_Config (See page 187) General configuration.

Table 79: Drop Bus Path Configuration (T_DOCB_VC3_TUG3_Config)

Offset	Bits	Name	Init	Description
0x0000	0	HighZ	0x1	The data of the selected VC-3/TUG-3 is tristated when 0x1.
0x0002		Reserved	0x7F	Reserved.
0x0004		Reserved	0xFFFF	Reserved.

Table 80: Drop Bus Common Configuration (T_DOCB_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	ClockEdge_Config			
	0	Reserved	0x0	Reserved.
	1	Output_SelectNegativeClockEdge	0x0	Configure the edge on which the timing and data are clocked out. Negative clock edge when 0x1, positive clock edge when 0x0.
0x0002	3 - 0	TimingDelay	0x0	Configure the delay between data and timing on the Add Combus.
0x0004	0	Reserved	0x1	Reserved.
0x0006	11 - 0	Reserved	0x0	Reserved.

Table 80: Drop Bus Common Configuration (T_DOCB_Common_Config)

Offset	Bits	Name	Init	Description
0x0008	Parity_Config			
	0	ParityIncludesTiming	0x0	Calculate parity over data only, or over Data and Timing. Timing is included when 0x1.
	1	ParityEven	0x0	Even parity when 0x1, odd parity when 0x0.
0x000A	2 - 0	Reserved	0x7	Reserved.
0x000C		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.
0x000E		AUG1_HighZ_Config		T_DOCB_AUG1_Config (See page 188) Configuration of HighZ per AUG1.
0x0010		VC3_TUG3_Mode_Config		T_VC3_TUG3_Mode_Config (See page 184) Configuration of the VC-3/TUG-3 modes.
0x0014	3 - 0	Config_Channel	0x0	VC-3/TUG-3 for which configuration can be done in VC3_TUG3_Config.

Table 81: Drop Bus AUG-1 Configuration (T_DOCB_AUG1_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	HighZ	0xF	AUG-1 HighZ configuration, one bit per AUG-1. The data of the selected AUG-1 is tristated when '1'. Least significant bit corresponds to the first AUG-1.

13.20 POH MONITOR

Table 82: POH Monitor (T_VC_POH_MONITOR)

Offset	Bits	Name	Init	Access	Description
0x0000		VC_Config		rw	T_VCXPM_Config (See page 189) High order path configuration. The high order path to be configured is selected by indirect access. See the Config_Channel register in the Common_Config record to select the desired high order path.
0x0200		Common_Config		rw	T_VCXPM_Common_Config (See page 191) General configuration.
0x0300		Common_Status		ro/cow_1	T_VCXPM_Common_Status (See page 193) General status. Note: Latched bits are clear-on-write-1, all others are read-only.
0x0400		VC_Status		ro/cow_1	Array (12) of T_VCXPM_Status (See page 193) Offset between two elements = 0x40. Array index indicates the high order path. High order path status. Note: Latched bits are clear-on-write-1, all others are read-only.

Table 83: POH Monitor Path Configuration (T_VCXPM_Config)

Offset	Bits	Name	Init	Description
0x0000	ModeTTIConfig			
	0	Bypass	0x0	No processing is done on this high order path when 0x1. Use this bypass for unused paths.
	1	AIS_Force	0x0	AIS insertion is forced when 0x1.
	2	Unidirectional	0x0	Enables the uni-directional option when 0x1. When the uni-directional option is active, the FarEndBlockErrorCounter will report 0 and the RDI defect is cleared.
	3	TTI_ExTiMessage	0x0	Ignore expected TTI message and assume non-specific repeating byte message when 0x0. When 0x1 the TTI message has to match the specified expected message (16 or 64 byte TTI message).
	4	TTI_ExTi64	0x0	64 byte trace message when 0x1, 16 byte trace message when 0x0. This setting is only valid when TTI_ExTiMessage is 0x1.
	5	TTI_TimEnable	0x0	TIM detection is enabled when 0x1.
	6	TIM_AIS_Insert_Disable	0x0	AIS insertion on Trail Trace Identifier Mismatch defect is disabled when 0x1.
0x0002		ExpectedBytes	All 0x0	T_VCXPM_ExpectedBytes (See page 190) Expected bytes.
0x0084		B3_Config		T_BIP_Detector_Config (See page 190) Configuration for B3 BIP detector (DEG/EXC).
0x00A0	BytesConfig			
	3 - 0	G1_AcceptNoOfIntervals	0x5	Integer 3, 5 (ETSI) or 10 (Telcordia) Number of consecutive frames to debounce G1.
	4	G1_CountBitErrors	0x0	REI bit errors are reported when 0x1, block errors when 0x0.
	6 - 5	H4_Multiframe_Type	0x0	0x0 = H4_MF_NONE 0x1 = H4_MF_LO 0x2 = Reserved 0x3 = Reserved Enables monitoring of H4 byte. • H4_MF_NONE = H4 monitoring disabled • H4_MF_LO = Low Order Multiframe tracking
	10 - 7	H4_MsToSetLOM	0x5	Number of ms that the OOM state must persist to declare the LOM defect.
0x00A2		CorrDefects_Mask		T_VCXPM_Defects (See page 191) Correlated defects mask.

Table 84: POH Monitor Expected J1/C2 (T_VCXPM_ExpectedBytes)

Offset	Bits	Name	Init	Description
0x0000		Expected_TTI_Message	All 0x0	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Expected TTI message. • bytes 0-15 for 16 byte TTI message • bytes 0-63 for 64 byte TTI message This register is only used when TTI_ExTiMessage is 0x1 (see VC_Config).
0x0080	7 - 0	Expected_C2	0x0	Expected C2 Byte.

Table 85: BER Detection Configuration (T_BIP_Detector_Config)

Offset	Bits	Name	Init	Description
0x0000	0	PoissonErrorCheck	0x0	Assume Poisson error distribution when 0x1, bursty distribution when 0x0.
0x0002		PoissonDetector_Config		T_BIP_PoissonDetector_Config (See page 164) Configuration for DEG/EXC detection, assuming Poisson distribution of errors.
0x0014		BurstyDetector_Config		T_BIP_BurstyDetector_Config (See page 190) Configuration for DEG detection, assuming bursty distribution of errors.

Table 86: Path Bursty Distribution BER Detection (T_BIP_BurstyDetector_Config)

Offset	Bits	Name	Init	Description
0x0000	12 - 0	DEG_DetectionErrorThreshold	0x1F40	Range 0 to 8000 An (one second) interval is bad if the number of detected errored blocks in that interval is greater than or equal to this threshold.
0x0002	3 - 0	DEG_DetectionWindowSize	0xA	Range 2 to 10 Number of consecutive bad intervals before DEG is declared.
0x0004	12 - 0	DEG_RecoveryErrorThreshold	0x1F40	Range 0 to 8000 An (one second) interval is a good interval when the number of errored blocks in this interval does not exceed this threshold.
0x0006	3 - 0	DEG_RecoveryWindowSize	0x2	Range 2 to 10 Number of consecutive good intervals before DEG is cleared.

Table 87: POH Monitor Defects (T_VCXPM_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	SSF	0x1	Incoming SSF (Server Signal Fail).
	1	TIM	0x1	J1 Trail Trace Identifier Mismatch.
	2	TTIZERO	0x1	J1 Trail Trace Identifier Zero.
	3	DEG	0x1	Degraded signal.
	4	EXC	0x1	Excessive error.
	5	UNEQ	0x1	Unequipped.
	6	AIS	0x1	VC-AIS detected on C2.
	7	RDI	0x1	Remote Defect Indication.
	8	RDI_S	0x1	Enhanced Remote Defect Indication (E-RDI) Server.
	9	RDI_C	0x1	Enhanced Remote Defect Indication (E-RDI) Connectivity.
	10	RDI_P	0x1	Enhanced Remote Defect Indication (E-RDI) Payload.
	11	PLM	0x1	Payload Mismatch.
	12	LOM	0x1	Loss of Multiframe.
	13	K3_APS	0x1	Event on K3 APS byte.
	14	C2_Changed	0x1	Event on C2 byte.

Table 88: POH Monitor Common Configuration (T_VCXPM_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	Config_Channel	0x0	Range 0 to 11 High order path for which configuration can be done in VC_Config.
0x0002		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 157) AUG-1 mode configuration.
0x0004	TTIConfig			
	0	TTI_Report_Enable	0x0	Enables J1 TTI message reporting when 0x1. TTI_Report_Channel indicates the high order path for which reporting is enabled.
	4 - 1	TTI_Report_Channel	0x0	Range 0 to 11 High order path for which J1 reporting is done.
	5	SSF_TIM_Inhibit_Disable	0x0	Inhibition of TIM defect by incoming SSF is disabled when 0x1.
	6	UNEQ_TIM_Inhibit_Disable	0x0	Inhibition of TIM defect by UNEQ defect is disabled when 0x1.
	7	TTIZERO_TIM_Inhibit_Disable	0x0	Inhibition of TIM defect by TTIZERO defect is disabled when 0x1.
	8	SSF_TTIZERO_Inhibit_Disable	0x0	Inhibition of TTIZERO defect by SSF defect is disabled when 0x1.

Table 88: POH Monitor Common Configuration (T_VCXPM_Common_Config)

Offset	Bits	Name	Init	Description
0x0006	TTISettings			
	3 - 0	TTI_FramesToSetTim	0x5	Range 2 to 15 Number of consecutive mismatched multiframes to set TIM.
	7 - 4	TTI_FramesToResetTim	0x3	Range 2 to 15 Number of consecutive match multiframes to clear TIM.
0x0008	AISRDIInsertion			
	0	SSF_AIS_Insert_Disable	0x0	Insertion of AIS on incoming Server Signal Fail is disabled when 0x1.
	1	AIS_AIS_Insert_Disable	0x0	Insertion of AIS on AIS defect is disabled when 0x1.
	2	EXC_AIS_Insert_Disable	0x0	Insertion of AIS on EXC defect is disabled when 0x1.
	3	UNEQ_AIS_Insert_Disable	0x0	Insertion of AIS on unequipped defect is disabled when 0x1.
	4	PLM_AIS_Insert_Disable	0x0	Insertion of AIS on Payload mismatch defect is disabled when 0x1.
	5	LOM_AIS_Insert_Disable	0x0	Insertion of AIS on Loss of Multiframe defect is disabled when 0x1.
	6	SSF_RDI_Insert_Disable	0x0	Insertion of RDI on incoming Server Signal Fail is disabled when 0x1.
	7	UNEQ_RDI_Insert_Disable	0x0	Insertion of RDI on unequipped defect is disabled when 0x1.
	8	TIM_RDI_Insert_Disable	0x0	Insertion of RDI on Trail Trace Identifier Mismatch defect is disabled when 0x1.
	9	PLM_RDI_Insert_Disable	0x0	Insertion of RDI on Payload mismatch defect is disabled when 0x1.
	10	Reserved	0x0	**Reserved. This field must be set to 0x1.**
0x000A	AlarmInhibition			
	0	SSF_UNEQ_Inhibit_Disable	0x0	Inhibition of UNEQ defect by incoming SSF is disabled when 0x1.
	1	TTIZERO_UNEQ_Contribution_Disable	0x0	Contribution of TTIZERO to UNEQ defect is disabled when 0x1.
	2	TIM_UNEQ_Contribution_Disable	0x0	Contribution of TIM to UNEQ defect is disabled when 0x1.
	3	SSF_EXC_Inhibit_Disable	0x0	Inhibition of EXC defect by incoming SSF is disabled when 0x1.
	4	TIM_EXC_Inhibit_Disable	0x0	Inhibition of EXC defect by TIM defect is disabled when 0x1.
	5	SSF_DEG_Inhibit_Disable	0x0	Inhibition of DEG defect by incoming SSF is disabled when 0x1.
	6	TIM_DEG_Inhibit_Disable	0x0	Inhibition of DEG defect by TIM defect is disabled when 0x1.
	7	SSF_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by incoming SSF is disabled when 0x1.
	8	UNEQ_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by UNEQ defect is disabled when 0x1.
	9	TTIZERO_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by TTIZERO defect is disabled when 0x1.
	10	TIM_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by TIM defect is disabled when 0x1.
	11	AIS_SSF_Contribution_Disable	0x0	Contribution of AIS defect to SSF defect is disabled when 0x1.
	12	TSF_PLM_Inhibit_Disable	0x0	Inhibition of PLM defect by TSF indication is disabled when 0x1.
	13	TSF_LOM_Inhibit_Disable	0x0	Inhibition of LOM defect by TSF indication is disabled when 0x1.
	14	PLM_LOM_Inhibit_Disable	0x0	Inhibition of LOM defect by PLM defect is disabled when 0x1.
0x000C	11 - 0	Summary_Mask	0xFFF	Summary mask, one bit per high order path. Least significant bit corresponds to the first high order path.

Table 89: POH Monitor Status (T_VCXPM_Common_Status)

Offset	Bits	Name	Init	Description
0x0000		Reported_TTI64_Message	All 0x0	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Accepted Stable 64 byte TTI message.
0x0080		Reported_TTI16_Message	All 0x0	Array (16) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Accepted Stable 16 byte TTI message.
0x00A0		ReportStatus		T_VCXPM_Report (See page 193) Reporting status.
0x00A2	11 - 0	Summary_LatchForInt	0x0	Defects summary, one bit per high order path. Least significant bit corresponds to the first high order path.
0x00A4	11 - 0	Reserved	0x0	Reserved.
0x00A6	11 - 0	Reserved	0x0	Reserved.

Table 90: J1 TTI Stable (T_VCXPM_Report)

Offset	Bits	Name	Init	Description
0x0000	0	Stable_1	0x0	TTI 1 byte message stable indication.
	1	Stable_16	0x0	TTI 16 byte message stable indication.
	2	Stable_64	0x0	TTI 64 byte message stable indication.
	3	Stable_16_Latched	0x0	Latched TTI 16 byte message stable indication. This field is clear-on-write-1.
	4	Stable_64_Latched	0x0	Latched TTI 64 byte message stable indication. This field is clear-on-write-1.

Table 91: POH Monitor Per Path (T_VCXPM_Status)

Offset	Bits	Name	Init	Description
0x0000		POH_Status		T_VCXPM_POH_Status (See page 194) POH Status: status of received and accepted POH bytes.
0x0016		PerfMon		T_VCXPM_PM (See page 194) Performance counters.
0x001E		CorrDefects_Unlatched		T_VCXPM_Defects (See page 191) Correlated defects.
0x0020		CorrDefects_LatchForInt		T_VCXPM_Defects (See page 191) Correlated defects latched for interrupt.
0x0022		Reserved	0x0	Reserved.
0x0024		Reserved	0x0	Reserved.
0x0026		Reserved	0x0	Reserved.

Table 92: POH Monitor Path Status (T_VCXPM_POH_Status)

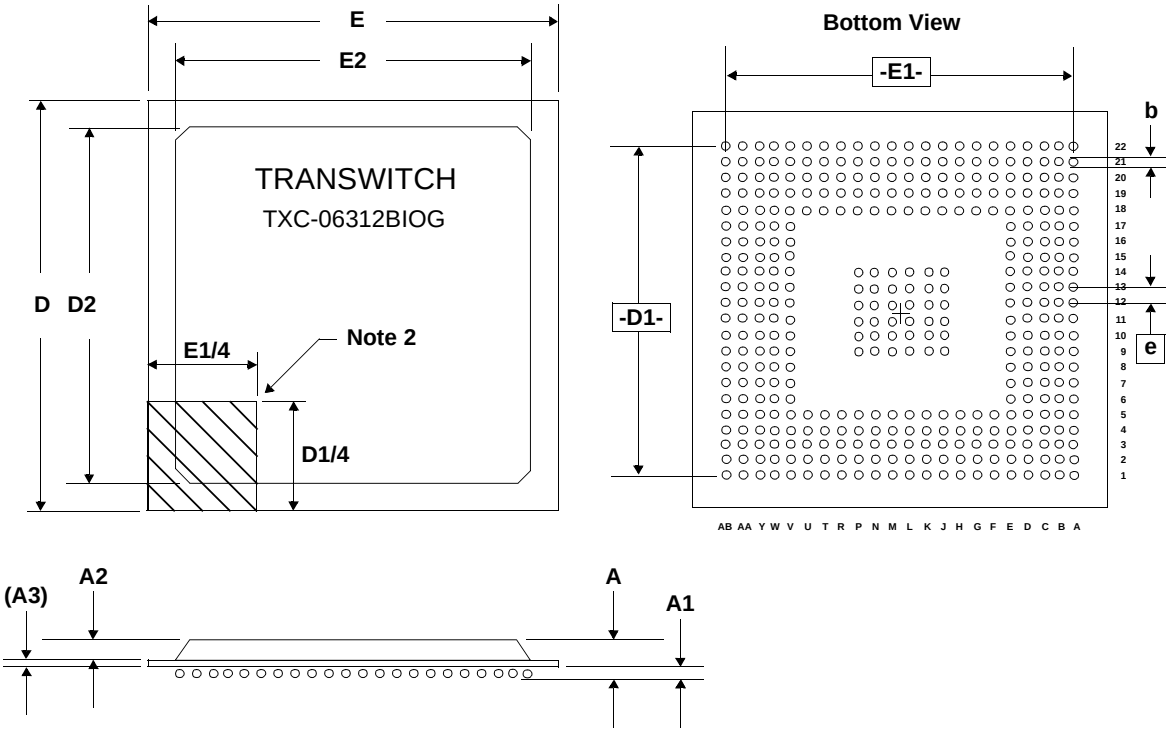
Offset	Bits	Name	Init	Description
0x0000	7 - 0	Received_J1	0x0	J1 byte of the previously received frame.
0x0002	7 - 0	Received_B3_error	0x0	Errored bit positions in B3 byte of the previously received frame.
0x0004	7 - 0	Received_C2	0x0	C2 byte of the previously received frame.
0x0006	7 - 0	Received_G1	0x0	G1 byte of the previously received frame.
0x0008	7 - 0	Received_F2	0x0	F2 byte of the previously received frame.
0x000A	7 - 0	Received_H4	0x0	H4 byte of the previously received frame.
0x000C	7 - 0	Received_F3	0x0	F3 byte of the previously received frame.
0x000E	7 - 0	Received_K3	0x0	K3 byte of the previously received frame.
0x0010	7 - 0	Received_N1	0x0	N1 byte of the previously received frame.
0x0012	7 - 0	Accepted_TSL	0x0	Accepted C2 byte.
0x0014	7 - 0	Accepted_K3	0x0	Accepted K3 byte.

Table 93: POH Monitor Performance Counters (T_VCXPM_PM)

Offset	Bits	Name	Init	Description
0x0000	12 - 0	NearEndDefect_BlockCounter	0x0	Near end block error counter (B3).
0x0002	15 - 0	NearEndDefect_BitCounter	0x0	Near end bit error counter (B3).
0x0004	15 - 0	FarEndDefect_Counter	0x0	Far end error counter (G1). Configurable as bit or block count.
0x0006	DefectSec			
	0	NearEndDefectSec	0x0	TSF one second latch.
	1	FarEndDefectSec	0x0	RDI defect one second latch.

PACKAGE INFORMATION

The PHAST-12N device is packaged in a 376-lead, 23 mm x 23 mm, plastic ball grid array package suitable for surface mounting, as illustrated in Figure 55.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 22 x 22, JEDEC code MO-151.

Dimension (Note 1)	Min	Max
A A1 A2	2.02 0.40 1.12	2.44 0.60 1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	23.00	
D1 (Nom)	21.00	
D2	19.45	20.20
E	23.00	
E1 (Nom)	21.00	
E2	19.45	20.20
e (Ref.)	1.00	

Figure 55. PHAST-12N TXC-06312B 376-Lead Plastic Ball Grid Array Package

APPLICATION EXAMPLES

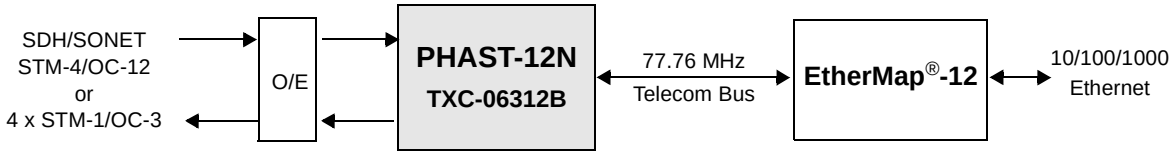


Figure 56. STM-4/OC-12 or 4 x STM-1/OC-3 Terminal Mux

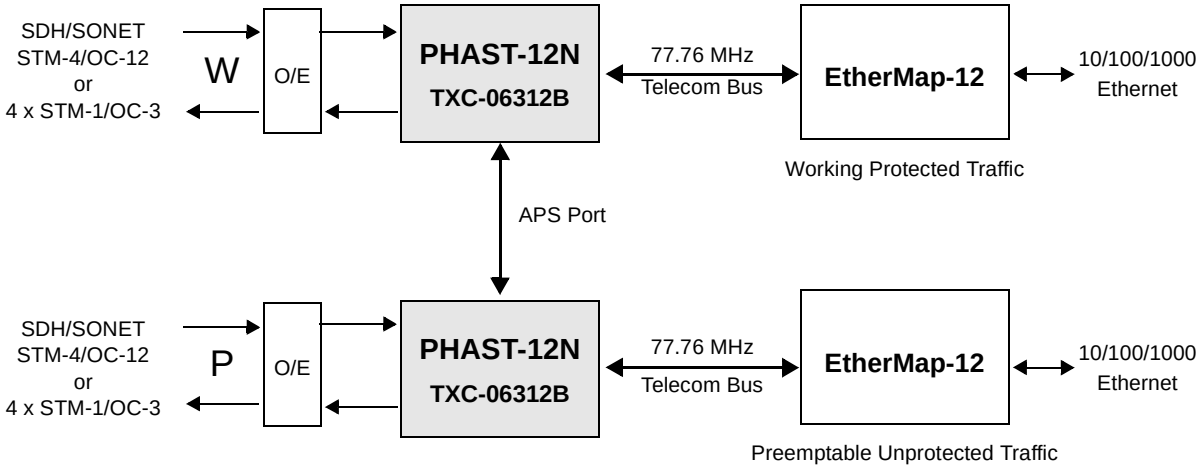
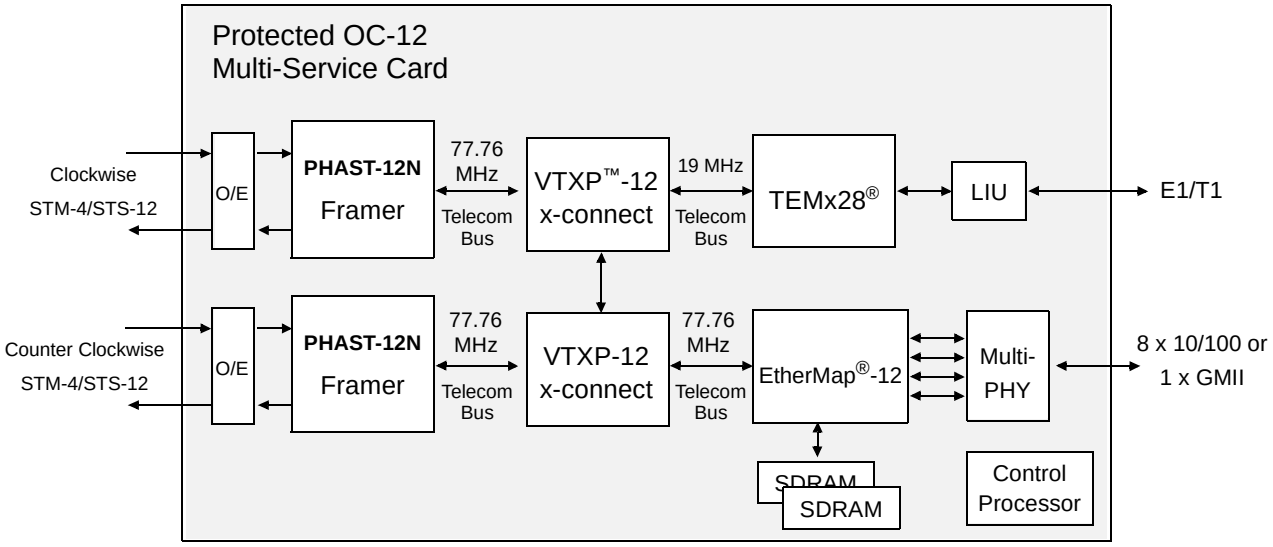


Figure 57. STM-4/OC-12 or 4 x STM-1/OC-3 1+1, 1:1 APS Terminal Mux



Multi-Service EoS and TDM Card combines line and tributary mapping functions with full TU/VT cross connect for protection applications

Figure 58. STM-4/OC-12 or 4 x STM-1/OC-3 Ethernet and TDM Terminal Mux

ORDERING INFORMATION

Part Number: TXC-06312BIOG376-Lead Plastic Ball Grid Array Package

RELATED PRODUCTS

TL3M Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. A 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is 19.44 MHz Telecom Bus, a byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

EtherMap-12 Device (OC-12 SDH/SONET Ethernet Mapper). The EtherMap-12 Device is a highly integrated, OC-12 rate SDH/SONET device, for mapping of high and low order Ethernet payloads to SDH/SONET (10/100/1000 Mbps Ethernet).

TEMx28 Device (28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU playloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

EtherMap-3 *Plus* Device (OC-3 Ethernet over SONET Mapper with Rapid Restoration). The EtherMap-3 *Plus* Device is a highly integrated EoS device that provides for mapping of 10/100/1000 Mbit/s Ethernet into SONET/SDH STS-3/STM-1 Transport payloads. The device supports connection for up to eight 10/100 Mbit/s Ethernet ports, using SMII interfaces, or a single 1000 Mbit/s Ethernet port, using a GMII interface.

PHAST-3N Device (SDH/SONET STM-1, STS-3 or STS-3c Overhead Terminator). This PHAST-3N device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

PHAST-12E Device (Programmable, High Performance ATM/PPP/TDM SDH/SONET Terminator for Level 12 with Enhanced Features). The PHAST-12E is a highly integrated SDH/SONET terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STM-1 or STS-3c lines or a single STM-4/4c or STS-12/12c line.

PHAST-12P Device (STM-4/OC-12 SDH/SONET Overhead Terminator with CDB/PPP UTOPIA/POS-PHY Interface). A highly integrated SDH/SONET overhead terminator device designed for ATM cell or PPP packet payload mappings. A single PHAST-12P can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line. Each SDH/SONET terminator has a line interface block that performs clock synthesis and clock recovery for four 155 Mbit/s signals or a single 622 Mbit/s serial signal.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office
Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office
Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007
Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.
Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland
Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834
Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094
Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221
Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157
Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

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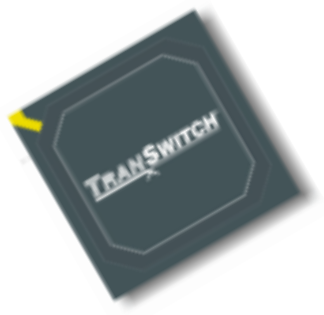

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