Stratix PCI Development Board

September 2003, ver. 2.0 Data Sheet

Introduction

This data sheet describes the features and technical details of the Stratix™ PCI development board. Slightly different versions of the board are included in the following development kits:

- PCI Development Kit, Stratix Edition (ordering code PCI-BOARD/S25). This data sheet refers to the board shipped with this kit as the Starter Board.
- PCI High-Speed Development Kit, Stratix Professional Edition (ordering code PCI-BOARD/S60). This data sheet refers to the board shipped with this kit as the Professional Board.

This data sheet indicates whenever a component or functionality is unique to either the Starter Board or the Professional Board.

Features

The Stratix PCI development board is an evaluation and development platform for high-speed interfaces including PCI, PCI-X, double data rate (DDR) SDRAM, and 10/100 Ethernet, as well as high-speed differential interfaces (HSDI) such as the HyperTransport™ interface, the RapidIO™ interface, System Packet Interface Level 4 Phase 2 (SPI-4.2), and any LVDS-based interface.

Components

- Supports the following members of the Stratix device family:
  - EP1S25F1020 (Starter Board)
  - EP1S60F1020 (Professional Board)
- Short-form universal PCI (3.3 or 5.0 V) card
  - 32-bit or 64-bit PCI at 33 or 66 MHz
  - 100-MHz PCI-X Revision 2.0 mode 1
  - 133-MHz PCI-X Revision 2.0 mode 1 (Starter Board)
- Memory
  - 256-MByte PC333 DDR SDRAM (SODIMM)
  - 64-Mbit AMD DL-type, boot-block flash
- FPGA device configuration
  - User-selectable on power-up via flash memory and the EPM3256ATC144 device
  - Via ByteBlaster™ II download cable

- Flexible clocking options
  - Socketed 33-MHz system clock oscillator
  - Socketed 100-MHz high-speed clock oscillator
  - SMA connector clock input

Expansion Interfaces

- HSDI port A: 8-bit interface with Samtec QTE connector and Broadcom standard pin-out (Professional Board)
- HSDI port B: dual 8-bit or single 16-bit interfaces with Samtec QTE/QSE connectors and HyperTransport Consortium DUT connector pin-out (Professional Board)
- Expansion Prototype Card (PROTO1)
- 10/100 Ethernet (RJ-45 connector)
- Serial RS-232 (DB-9 connector)
- Optrex LCD connector
- Switches and indicators
  - Four user-definable pushbutton switches
  - Eight-position user-definable dip switch bank
  - Eight user-definable LEDs
- Flexible power options
  - PCI connector
  - External power supply via adaptor cable
  - HSDI port A connector (Professional Board)
  - HSDI port B connector (Professional Board)

Debugging Interfaces

- Joint Test Action Group (JTAG) interface connector
- 8-bit Agilent/Samtec ASP differential probe connector
- 32-bit Mictor probe connector

Handling the Board

Observe the following precautions when handling the board.

Static Discharge Precaution—The board can be damaged without proper anti-static handling; therefore, take anti-static precautions while handling it.

Power Supply Precaution—The board has special power supply circuitry that can be damaged if more than one power source is applied to the board at the same time.

Environmental Requirements—The board should be stored between -40° and 100° C. The recommended operating temperature is between 0° and 55° C.

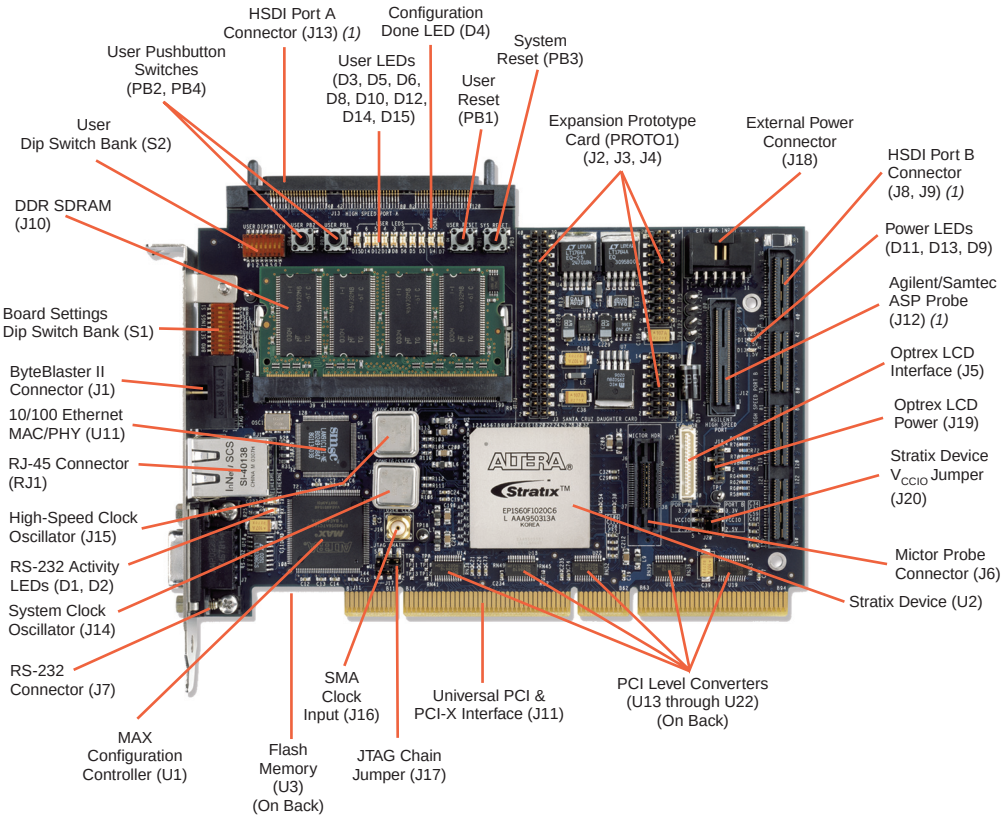
General Description

The Stratix PCI development board allows designers to evaluate, demonstrate, and develop system-level designs with PCI, PCI-X, DDR SDRAM, and 10/100 Ethernet. Additionally, the Professional Board allows for the development of HyperTransport, RapidIO and SPI-4.2 interfaces. Combined with intellectual property (IP) from Altera and Altera® Megafunction Partners Program (AMPP℠) partners, users can solve design problems that typically require custom solutions.

Components & Interfaces

Figure 1 shows a top view of the Stratix PCI development board.

Figure 1. Stratix PCI Development Board Components & Interfaces



Note to Figure 1:

(1) These features are only available on the Professional Board.

Table 1 describes the major components on the board and the interfaces it supports.

Table 1. Stratix PCI Development Board Components & Interfaces (Part 1 of 3)

Type	Component/ Interface	Board Reference	Description
FPGA	Stratix device	U2	Configurable Stratix device. See Table 2 on page 8. The EP1S25F1020C5 device is installed on the Starter Board. The EP1S60F1020C6 device is installed on the Professional Board.
PCI	PCI connector	J11	Universal PCI and PCI-X interface. See Table 3 on page 8.
	PCI level converters	U13 through U22	Level converters for 5.0-V PCI compatibility.
Memory	DDR connector and DDR SDRAM	J10	DDR SDRAM connector (SODIMM) including pre-installed 256-MByte PC333 DDR SDRAM memory module.
	Flash	U3	64-Mbit AMD DL-family boot-block flash.
Configuration	MAX® configuration controller	U1	Factory-programmed EPM3256ATC144-7 for Stratix device configuration.
	JTAG	J1, J17	JTAG test and control as well as ByteBlaster II configuration interface. JTAG chain jumper.
	Configuration done LED (D4)	D4	Indicates Stratix configuration is complete.
Clock	System clock oscillator	Installed at J14	33.333-MHz system clock.
	High-speed clock oscillator	Installed at J15	100-MHz high-speed reference clock.
	SMA clock	J16	Clock input.
Control	System reset pushbutton switch	PB3	Reset hardware and reconfigure Stratix device.
	User reset pushbutton switch	PB1	User-defined hardware reset.
	Board settings dip switch bank	S1	System settings and configuration selection. See Table 4 on page 9, Table 5 on page 9, Table 6 on page 9, Table 8 on page 12, and Table 11 on page 16.
User Settings	User pushbutton switches	PB2, PB4	User configurable.
	User dip switch bank	S2	User configurable.

Table 1. Stratix PCI Development Board Components & Interfaces (Part 2 of 3)

Type	Component/ Interface	Board Reference	Description
User Indicator	User LEDs	D3, D5, D6, D8, D10, D12, D14, D15	User configurable.
Power	Power connector	J18	External power supply adaptor.
Power Indicators	+2.5-V power OK LED	D11	2.5-V power supply indicator.
	+1.5-V power OK LED	D13	1.5-V power supply indicator.
	+1.25-V power OK LED	D9	1.25-V power supply indicator.
Test point	+3.3 V	TP4	3.3-V power testpoint.
	+5.0 V	TP2	5.0-V power testpoint.
	+12.0 V	TP7	12.0-V power testpoint.
	-12.0 V	TP5	-12.0-V power testpoint.
	Ground	TP6	Ground test point near DDR SDRAM.
		TP18	Ground test point near SMA clock input.
		TP1	Ground test point near LCD connector.

Table 1. Stratix PCI Development Board Components & Interfaces (Part 3 of 3)

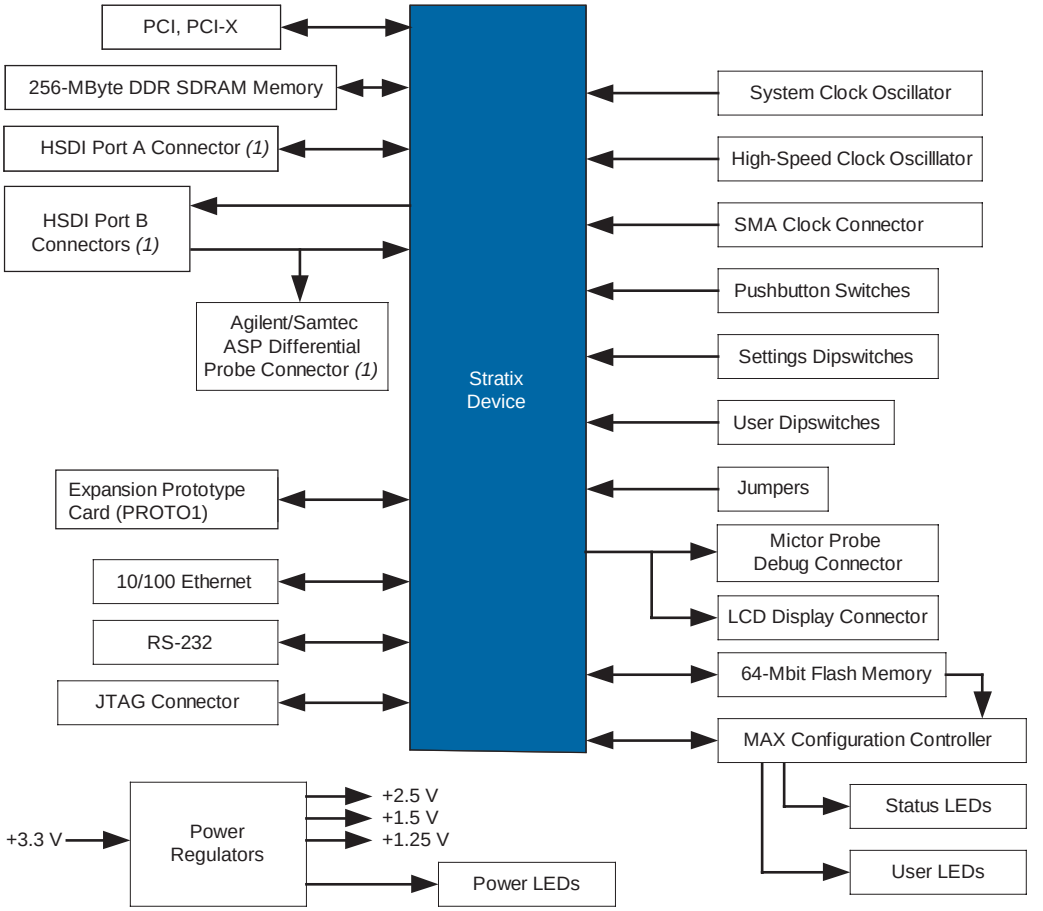
Type	Component/ Interface	Board Reference	Description
High-Speed Interface Connector *(1)*	HSDI port A, 8-bit high-speed interface connector	J13	This connector supports a bidirectional 8-bit differential interface running at a maximum of 840-Mbits/second. This port can be configured at 2.5 V to support the HyperTransport interface or at 3.3 V to support SPI-4.2, RapidIO, and LVDS-based interfaces. This connector was designed to meet the specifications required to plug directly into the Broadcom evaluation boards designed for the BCM1250 and BCM112x microprocessors, including BCM91250 and BCM91250E evaluation boards.
	HSDI port B, 16-bit high-speed interface connector	J8, J9 (bottom)	These connectors support either two eight-bit bidirectional differential interfaces or one 16-bit bidirectional differential interface running at up to 840 Mbits/second. This port can be operated at 2.5 V to support the HyperTransport interface or at 3.3 V to support SPI-4.2, RapidIO, and other LVDS-based interfaces. This connector is designed according to the DUT connector specifications from the HyperTransport Consortium. See Table 21 on page 23 for a description of this connector and its capabilities.
	Agilent/Samtec ASP Probe	J12	Agilent/Samtec ASP differential probe interface for Agilent logic analyzers.
Nios peripheral	Expansion Prototype Card (PROTO1)	J2, J3, J4	Interface to Expansion Prototype Card (PROTO1).
Display	LCD	J5, J19	Optrex LCD interface. +12.0-V output for LCD backlight inverter.
I/O	10/100 Ethernet	U11, RJ1, OSC1	10/100 Ethernet MAC/PHY. RJ-45 connector, 25-MHz oscillator.
Serial I/O	RS-232	U10, J7	RS-232 serial interface level shifter. DB9 connector.
	RS-232 Tx LED	D1	RS-232 transmitter active indicator.
	RS-232 Rx LED	D2	RS-232 receiver active indicator.
Debug	Mictor Probe	J6	Mictor probe interface for Agilent logic analyzers.

Note to Table 1:
(1) These features are only available on the Professional Board.

Functional Description

This section describes the operation of the Stratix PCI development board. Figure 2 show the block diagrams.

Figure 2. Stratix PCI Development Board Block Diagram



Note to Figure 2:

(1) These features are only available on the Professional Board.

Stratix Device

The Stratix device (U2), is connected to all of the components on the board through appropriate on-chip interfaces and board circuitry. The device supports PCI, DDR SDRAM memory, and high-speed differential interfaces such as the HyperTransport and RapidIO interfaces, SPI-4.2, and other LVDS-based interfaces. Users can program the Stratix device to implement their system logic. Table 2 shows the Stratix device that is installed on the board.

Table 2. Stratix Device

Board	Kit	Device
Professional Board	PCI High-Speed Development Kit, Stratix Professional Edition (Ordering code: PCI-BOARD/S60)	EP1S60F1020C6
Starter Board	PCI Development Kit, Stratix Edition (Ordering code: PCI-BOARD/S25)	EP1S25F1020C5

For more information on Stratix devices, refer to the Data Sheet section of the *Stratix Device Handbook*.

PCI

The Stratix PCI development board is compatible with the Altera `pci_mt64`, `pci_mt32`, `pci_t64`, and `pci_t32` MegaCore® functions. It can also be used with PCI and PCI-X IP cores from AMPP partners and other third-party vendors. The Stratix device and PCI connector (J11) support PCI revision 2.3 and PCI-X revision 2.0 mode 1 local bus standards. See Table 3 for details.

Table 3. PCI Support

Application	Width (Bits)	Voltage (V)	Speed (MHz)
PCI	32 and 64	3.3 and 5.0	33 and 66
PCI-X revision 2.0 mode 1	32 and 64	3.3	66, 100, and 133 *(1)*

Note to Table 3:

(1) PCI-X at 133 MHz is only available on the Starter Board. The Professional Board runs at a maximum of 100 MHz in PCI-X applications.

PCI Level Converters

U13 through U22 are IDT IDTQS3861Q level converters that convert between 5.0-V PCI backplane signals and Stratix 3.3-V signals.

PCI Operating Mode

The board settings dip switch bank (S1) sets the PCI operating mode and speed as shown in Tables 4, 5, and 6.

Table 4. PCI Operating Mode Selection

Board Settings Dip Switch Bank (S1) Position 3 (PSEL) Setting	PCI Operating Mode
Off	PCI-X at the speed shown in Table 6.
On	PCI at the speed shown in Table 5.

Table 5. PCI Operating Speed Selection

Board Settings Dip Switch Switch Bank (S1) Position 5 (PCIS) Setting	PCI Operating Speed (MHz)
Off	66
On	33

Table 6. PCI-X Operating Speed Selection

Board Settings Dip Switch Bank (S1) Position 4 (PCIXS) setting	PCI-X Operating Speed (MHz)
Off	133 and 100 *(1)*
On	66

Note to Table 6:

(1) You must ensure that your system does not attempt to operate the Professional Board above 100 MHz. Although the PCI-X maximum operating frequency for the Professional Board is 100 MHz, this setting indicates 133 MHz operation, which is not supported by the Professional Board.

DDR SDRAM Memory

The Stratix PCI development board was tested with the DDR SDRAM Memory Controller MegaCore function version 1.2.0. A 256-MByte DDR SDRAM memory module is installed in the 200-pin SODIMM connector (J10) and connects to banks 3 and 4 of the I/O Stratix device.

Designers can use other memory modules provided they meet the following requirements:

- 200-pin SODIMM DDR SDRAM
- 64 bits (non-ECC) or 72 bits (ECC)

Flash Memory

The flash memory (U3) on the board connects to the Stratix device and the MAX configuration controller. The flash memory is an Advanced Micro Devices AM29DL640D 64-Mbit DL-family boot-block device that connects to the Stratix device and the MAX configuration controller using LVTTL signals.

The flash memory capacity is 8 MBytes (67,108,864 bits). The flash memory contains one factory-programmed Stratix configuration image and the remaining space can be used to store user-defined Stratix configuration images and general-purpose user data such as Nios boot code. The MAX controller design controls the partitioning and function of the flash memory device. Table 7 on page 11 shows the actual portioning of the flash memory device as shipped from the factory.

The flash memory can operate in either 8- or 16-bit modes. A signal that is driven by the MAX configuration controller selects the mode in which the flash memory device runs. The default MAX configuration controller shipped with the board sets the flash memory device to operate in 8-bit mode.

When the MAX configuration controller is not configuring the Stratix device, it releases control of the flash memory to the Stratix device, which can then perform write and read operations on the flash memory. Reading, erasing, and writing to the flash memory requires strict adherence to the required timing of the flash memory device. For example, the flash memory has a read access time of 90 ns and flash write operations (erase or program) take microseconds or longer to complete. Therefore, the designer must monitor the flash memory status register for proper operation. You can review the MAX configuration controller and PCI-to-DDR SDRAM reference designs for sample Register Transfer Language (RTL) source code that demonstrates typical flash memory control operations.

MAX Configuration Controller

The MAX configuration controller (U1) is an Altera EPM3256ATC144 device. This device is factory-programmed to control Stratix device configuration, enable read / write access to the flash memory, and select the image used to configure the Stratix device. The MAX configuration controller also partitions the flash memory device into functional areas, as shown in Table 7. Due to the larger size of the configuration data for the EP1S60F1020 device, the number of user configuration images available for the Professional Board is less than the number available for the Starter Board.

Table 7. Flash Memory Device Partitions

Address Range	Starter Board	Professional Board
0x000000 - 0x1FFFFF	User program area	User program area
0x200000 - 0x2FFFFF	Stratix factory default configuration image	Stratix factory default configuration image
0x300000 - 0x3FFFFF	Stratix user configuration image 1	
0x400000 - 0x4FFFFF	Stratix user configuration image 2	
0x500000 - 0x5FFFFF	Stratix user configuration image 3	Stratix user configuration image 1
0x600000 - 0x6FFFFF	User program area	
0x700000 - 0x7FFFFF	User program area	

You can select which configuration image the MAX cofiguration controller device uses to configure the Stratix device at power up by setting positions 9 and 10 of the board settings dip switch bank (S1). See Table 8 on page 12 for details on the selection.

The MAX configuration controller configures the Stratix device when it is triggered by one of the following events:

- The board powers up
- The system reset pushbutton (PB3) is pressed
- The Stratix device pulses the CPLD_USER0 signal low

If the load is successful, the configuration done LED (D4) illuminates.

When the MAX configuration controller is not configuring the Stratix device, it releases control of the flash memory to the Stratix device. At that point, the Stratix device can perform read or write operations on the flash memory. Reading, erasing, and writing to the flash memory requires a flash memory controller designed into the Stratix device that meets the strict interface and timing requirements of the flash memory device. Refer to the MAX configuration controller and PCI-to-DDR SDRAM memory reference designs for sample designs that illustrate the required circuitry for the flash memory interface.

The size of the flash memory device used on the board and the factory programmed MAX configuration controller are designed to partition the flash memory into several sectors that contain different Stratix device configuration images. The board settings dip switch bank (S1) has two postions (9 and 10) used to select the configuration image for configuring the Stratix device. See Table 8 for more details.

Refer to the *PCI High-Speed Development Kit, Stratix Professional Edition Getting Started User Guide* for more details on the flash memory map for configuration images and general-purpose user data.

Table 8. Configuration Image Selection

Board Settings Dip Switch Bank		Configuration Image	
Switch S1 Position 9 (MPGM1) Setting	Switch S1 Position 10 (MPGM0) Setting	Starter Board	Professional Board
Off	Off	Factory-programmed image	Factory-programmed image
Off	On	User image 1	User image 1
On	Off	User image 2	Factory-programmed image
On	On	User image 3	User image 1

Clocks & Clock Distribution

The Stratix PCI development board has multiple clock sources, with most of the clocks driven directly to the Stratix device. Using the fast and enhanced PLLs integrated within the Stratix device, the designer has significant flexibility to achieve the appropriate clock configuration for prototyping.

Clock Sources

The Stratix PCI development board has three on-board oscillators, an SMA connector, and several application-specific clock sources located at the various expansion connectors. Table 9 shows the clock sources on the board.

Refer to the *Using General-Purpose PLLs in Stratix Devices* chapter of the *Stratix Device Handbook* for more information.

Table 9. Stratix Input Clocks (Part 1 of 2)

Signal Name	Source	Destination	Primary PLL Used *Notes (1), (2)*
PCI_CLK	PCI Connector (J11.B16) through level shifter (U14.13 and U14.11)	Stratix device (U2.AM15)	PLL12
CLK_OSC_A	Socketed 33.333-MHz oscillator (J14.5)	Stratix device (U2.A19), MAX configuration controller (U1.128), and Altera expansion prototype connector (PROTO1) (J4.9) *(3)*	PLL5
CLK_OSC_B	Socketed 100-MHz oscillator (J15.5)	Stratix device (U2.C19) *(4)*	PLL5
CLK_SMA	SMA Clock Input Connector (J16.1)	Stratix device (U2.T29 and U2.AK15)	PLL1, PLL7, PLL12
CLK_FROM_SCRUZ	Expansion Prototype Card (PROTO1) (J4.13)	Stratix device (U2.D15)	PLL11
B6_REF60_CLK	HSDI port A Connector (J13.10)	Stratix device (U2.AB4)	PLL9
B6_REF25_CLK	HSDI port A Connector (J13.10)	Stratix device (U2.T6)	PLL4, PLL10
B1_REF_CLK_IN	HSDI port B Connectors (J9.8, J8.153)	Stratix device (U2.T27)	PLL1
B6_RX_CLKn	HSDI port A Connector (J13.63)	Stratix device (U2.U3)	PLL3, PLL9
B6_RX_CLKp	HSDI port A Connector (J13.65)	Stratix device (U2.U4)	
B1A_RX_CLKn	HSDI port B Connectors (J9.46, J8.115)	Stratix device (U2.U32)	PLL2, PLL7
B1A_RX_CLKp	HSDI port B Connectors (J9.44, J8.117)	Stratix device (U2.U31)	

Table 9. Stratix Input Clocks (Part 2 of 2)			
Signal Name	**Source**	**Destination**	**Primary PLL Used** *Notes (1), (2)*
B1B_RX_CLKn	HSDI port B Connectors (J9.49, J8.112)	Stratix device (U2.AB29)	PLL8
B1B_RX_CLKp	HSDI port B Connectors (J9.47, J8.114)	Stratix device (U2.AB28)	
DDR_CLK_FBIN	Stratix device (D18)	Stratix device (U2.D17)	PLL5 FB
CLK_25MHZ	On-Board 25-MHz 10/100 Ethernet Oscillator (OSC1.4))	Ethernet MAC/PHY device (U11.127)	N/A

Note:

(1) A global clock input can feed Stratix high-speed PLLs directly. This table shows the direct connections and does not show the connection via global clock networks.

(2) PLL7 through PLL12 are not available in the EP1S25 device. Therefore, they are only available in the Professional Board.

(3) To use different PLLs within the Stratix device, the designer can drive the CLK_OSC_A signal to different input clock pins on the Stratix device by installing different resistors. The value shown in this table is the factory default setting. See page 15 of the board schematics for complete details on the various options available for the board.

(4) To use different PLLs within the Stratix device, the designer can drive the CLK_OSC_B signal to different input clock pins on the Stratix device by installing different resistors. The value shown in this table is the factory default setting. See page 15 of the board schematics for complete details on the various options available for the board.

SMA Clock Input Requirements

The SMA clock input CLK_SMA can be provided by an external signal source through the connector J16. Use a 50-Ω signal source and cable with an LVTTL-type signal (square-wave, with a voltage swing from 0.0 to +3.3 V). The maximum frequency of this input is 422 MHz.

Stratix Output Clocks

Table 10 lists the Stratix output clocks and their distribution on the board.

Table 10. Stratix Output Clocks (Part 1 of 2)			
Signal Name	**Stratix Source Pin**	**Stratix PLL**	**Destination**
DDR_CLK0n	U2.A16	PLL5	DDR SDRAM Memory Connector (J10.37)
DDR_CLK0p	U2.B16	PLL5	DDR SDRAM Memory Connector (J10.35)
DDR_CLK1n	U2.A17	PLL5	DDR SDRAM Memory Connector (J10.158)
DDR_CLK1p	U2.B17	PLL5	DDR SDRAM Memory Connector (J10.160)
DDR_CLK2n	U2.A18	PLL5	DDR SDRAM Memory Connector (J10.91)
DDR_CLK2p	U2.B18	PLL5	DDR SDRAM Memory Connector (J10.89)
DDR_CLK_FBOUT	U2.D18	PLL5	Stratix device (U2.D17)
CLK_TO_SCRUZ	U2.AL16	PLL6	Expansion Prototype Card (PROTO1) (J4.11)

Table 10. Stratix Output Clocks (Part 2 of 2)

CLK_TO_MAX_A	U2.AJ17	PLL6	MAX Configuration Controller (U1.125)
B1_REF_CLK_OUT	U2.AJ16	PLL6	HSDI port B Connector (J9.153, J8.8)
B1A_TX_CLKn	U2.V23	–	HSDI port B Connector (J9.115, J8.46)
B1A_TX_CLKp	U2.V24	–	HSDI port B Connector (J9.117, J8.44)
B1B_TX_CLKn	U2.AA26	–	HSDI port B Connector (J9.112, J8.49)
B1B_TX_CLKp	U2.AA27	–	HSDI port B Connector (J9.114, J8.47)
B6_TX_CLKn	U2.Y5	–	HSDI port A Connector (J13.58)
B6_TX_CLKp	U2.Y6	–	HSDI port A Connector (J13.56)

Power

CAUTION

The board has special power supply circuitry that can be damaged if more than one power source is applied to the board at the same time.

The Stratix PCI development board can be powered up from one of the following sources:

- PCI connector J11 supplies +3.3, +5.0, +12.0, and -12.0 V.
- Power connector J18 supplies +3.3, +5.0, +12.0, and -12.0 V from the external power adaptor cable plugged into an optional PC ATX power supply.
- HSDI port A connector J13 supplies +3.3 V.
- HSDI port B connector J8 or J9 supplies +3.3 V.

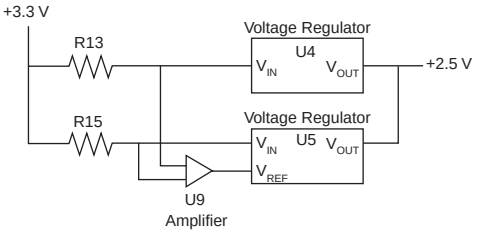
The +2.5-, +1.5-, and +1.25-V power OK LEDs require the -12.0-V supply to illuminate. These LEDs only illuminate when the PCI connector J11 or power connector J18 supplies power to the board.

An LCD display installed at J5 and J19 requires +5.0 and +12.0 V to operate. The LCD display only operates when the PCI connector J11 or the power connector J18 supplies power to the board.

+2.5-V Regulators

The board contains two voltage regulators that generate +2.5 V from the +3.3 V power for DDR SDRAM memory and the HSDI interfaces. The two voltage regulators U4 and U5 operate in parallel to supply the current required by the +2.5 V supply. Amplifier U9 equalizes the current flowing through U4 and U5 by monitoring and matching the current flowing through the resistors R13 and R15. See Figure 3 for more details.

Figure 3. 2.5-V Regulator



+1.5-V Regulator

Linear regulator U7 generates +1.5 V for the Stratix device from +3.3 V.

+1.25-V Regulator

Linear regulator U12 generates +1.25 V for DDR SDRAM memory termination and reference voltage.

External Power Adaptor Receptacle

J18 is a receptacle for power from a standard PC ATX power supply via the external power adapter cable. The board settings dip switch bank (S1) enables the external power supply, as shown in Table 11.

Table 11. External Power Supply Enable

Board Settings Dip Switch Bank (S1) Position 1 (PWR)	Description
Off	Disable external power supply.
On	Enable external power supply.

Stratix Device V_{CCIO} Jumper

J20 selects V_{CCIO} power for banks 6 and 1 of the Stratix device on the board, which in turn sets the operating voltage for HSDI port A and HSDI port B, respectively. Because the Starter Board does not come with HSDI port A or HSDI port B, jumper J20 does not serve any actual function. However, the shunts must be connected so that Bank 6 and 1 of the Stratix device are powered up to ensure proper operation of the Stratix device. Set the jumpers as shown in Table 12.

Table 12. Stratix Device V_{CCIO} Jumper Setting

Shunt Connects	I/O Bank	I/O Voltage (V)	Description
J20 pins 3 and 5	6	2.5	HSDI port A is set for the HyperTransport interface. Factory-default setting.
J20 pins 1 and 3	6	3.3	HSDI port A is set for the SPI-4.2 and RapidIO interfaces.
J20 pins 4 and 6	1	2.5	HSDI port B is set for the HyperTransport interface. Factory-default setting.
J20 pins 2 and 4	1	3.3	HSDI port B is set for the SPI-4.2 and RapidIO interfaces.

Test Points

Table 13 shows the power test points.

Table 13. Power Supply Test Points

Signal Name	Board Reference	Reference Designator	Description
3.3V	3.3V	TP4	3.3-V power.
5.0V	5.0V	TP2	5.0-V power.
+12V	+12V	TP7	+12.0-V power.
-12V	-12V	TP5	-12.0-V power.
GND		TP1	Ground, near the LCD connector.
		TP18	Ground, near the DDR SDRAM memory.
		TP6	Ground, near the SMA clock input.

Expansion Interface Power Sourcing Capabilities

Table 23 on page 25 shows the power sourcing capability to the HSDI port B interface when the development board is used as a host board.

Table 28 on page 35 shows the power sourcing capability to the Expansion Prototype Card (PROTO1) interface.

LEDs

The board has 3 power indication LEDs, 3 status LEDs, and 8 user LEDs.

Power LEDs

Table 14 shows the power indication LEDs.

The power indication LEDs require the -12.0-V supply to illuminate. These LEDs only illuminate when the PCI connector J11 or power connector J18 supplies power to the board.

Table 14. Power LEDs

Board Reference	Reference Designator	Color	Description
2.5V	D11	Blue	2.5-V power is on.
1.5V	D13	Blue	1.5-V power is on.
1.25V	D9	Blue	1.25-V power is on.

Status LEDs

Table 15 shows the status LEDs.

Table 15. Status LEDs

Board Reference	Reference Designator	Color	Description
CONF DONE	D4	Green	The Stratix device has been configured successfully.
TX	D1	Red	RS-232 transmission active.
RX	D2	Red	RS-232 receive active.

User LEDs

D3, D5, D6, D8, D10, D12, D14, and D15 are the user LEDs, as shown in Table 16. See "User LEDs" on page 44 for instructions on using the LEDs.

Table 16. User LEDs

User LEDs	Reference Designator	Color	Description
0	D3	Red	User defined.
1	D5	Red	User defined.
2	D6	Red	User defined.
3	D8	Red	User defined.
4	D10	Red	User defined.
5	D12	Red	User defined.
6	D14	Red	User defined.
7	D15	Red	User defined.

Board Settings Dip Switch Bank

Table 17 describes the board settings dip switch bank (S1).

Table 17. Board Settings Dip Switch Bank

Board Reference	Board Settings Dip switch	Factory Default Setting	Description
PWR	Switch S1 Position 1	On	External power supply enable. See Table 11 on page 16.
CLR	Switch S1 Position 2	Off	Reserved.
PSEL	Switch S1 Position 3	On	Select PCI speed and mode. See Table 4 on page 9, Table 5 on page 9, and Table 6 on page 9.
PCIXS	Switch S1 Position 4	Off	
PCIS	Switch S1 Position 5	Off	
RUnLU	Switch S1 Position 6	Off	Reserved.
MSEL2	Switch S1 Position 7	On	
USE M	Switch S1 Position 8	Off	
MPGM1	Switch S1 Position 9	Off	Stratix configuration image selection. Select the flash memory block used to configure the Stratix device. See Table 8 on page 12.
MPGM0	Switch S1 Position 10	Off	

Pushbutton Switches

Table 18 describes the pushbutton switches on the board.

Table 18. Pushbutton Switches

Board Reference	Reference Designator	Description
SYS RESET	PB3	Resets the MAX configuration controller and configures the Stratix device. Resets the Expansion Prototype Card (PROTO1), if installed.
USER RESET	PB1	User defined.
USER_PB1	PB2	User defined.
USER_PB2	PB4	User defined.

User Dip Switch Bank

Table 19 describes the user dip switch bank (S2). See "User Dip Switch Bank" on page 45 for signal connections.

Table 19. User Dip Switch Bank

User Dip Switch (S2)	Description
Positions 1 through 8	User defined. These dip switches are directly connected to the Stratix device.

Expansion Interfaces

The Stratix PCI development board includes the following interfaces:

- HSDI port A
- HSDI port B
- Expansion Prototype Card (PROTO1) Interface
- RS-232 Serial Interface
- 10/100 Ethernet
- LCD Display Interface

The HSDI port A and HSDI port B interfaces are only available on the Professional Board.

HSDI Port A Interface

The HSDI port A interface is only available on the Professional Board.

Bank 6 of the Stratix device contains an 8-bit HyperTransport-capable port wired to a connector that mates with several Broadcom reference boards. The connector at J13 allows the Stratix PCI development board to connect to other boards with a Broadcom-type HyperTransport connector. Compatible boards include:

- Broadcom BCM91250A evaluation board for BCM1250
- Broadcom BCM91250E PCI evaluation board for BCM1250
- Broadcom BCM91125E PCI evaluation board for BCM1125/BCM1125H
- A second Stratix PCI development board via an optional, custom interface cable

I/O Standard

Jumper J20 allows HSDI port A to operate at 2.5 V for the HyperTransport interface or 3.3 V for signaling standards such as the SPI-4.2 and RapidIO interfaces. Table 20 shows the jumper settings for the port A I/O standard.

Table 20. HSDI Port A I/O Standard Jumper (J20)

Standard	I/O Voltage (V)	Shunt Connects
HyperTransport interface	2.5	J20.3 to J20.5
SPI-4.2 and RapidIO interfaces	3.3	J20.1 to J20.3

HSDI port A uses discrete differential receive termination resistors as required by the HyperTransport, SPI-4.2, and RapidIO interfaces.

Reference Clock

Stratix device pin U2.AB4 receives B6_REF_CLK from HSDI port A connector J13. This clock connects to PLL9.

Optional HSDI Port A Interface Cable

An optional HSDI port A interface cable is available from Precision Interconnect (www.precisionint.com). Use the configuration code 023850120015NR20.

HSDI Port B Interface

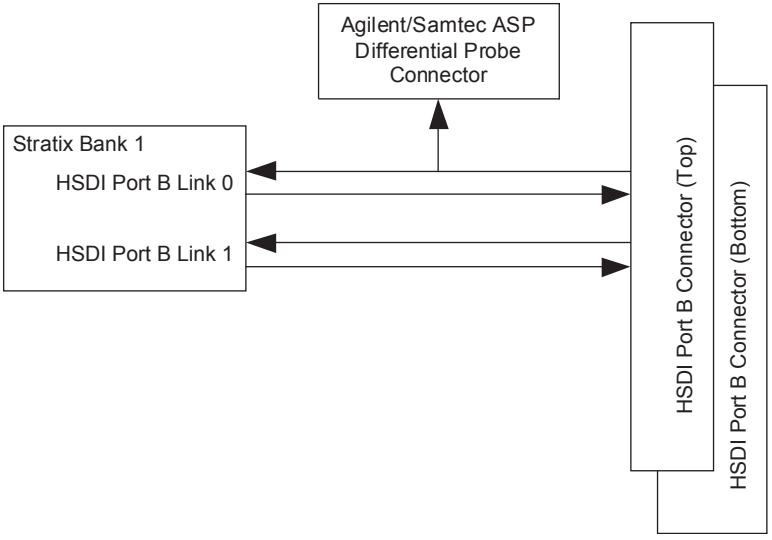
The HSDI port B interface is only available on the Professional Board.

Bank 1 of the Stratix device is connected to HyperTransport DUT connectors specified by the HyperTransport Consortium. This bank supports two independent bidirectional 8-bit differential interfaces or one bidirectional 16-bit differential interface. It can be used at 2.5 V for HyperTransport or at 3.3 V for SPI-4.2, RapidIO, and other LVDS-based interfaces.

J8 and J9 allow the Stratix PCI development board to connect to another board with a HyperTransport DUT connector. This interface operates at up to 840 Mbits/second double data rate (DDR) with a 420 MHz clock. Compatible HyperTransport DUT boards include a second Stratix PCI development board.

Figure 4 shows the HSDI port B interface.

Figure 4. HSDI Port B Interface



8- & 16-Bit Operation

The HSDI port B interface contains two 8-bit links, which can be operated as a 16-bit port. Although the Stratix device can be used in either host or slave applications, the choice of pins and layout used on the board limits the options on this port to a subset of the applications supported by the Stratix device. When using HSDI port B to connect to another board, consider the following items:

- A link with common transmit and receive clocks must connect to a link with separate transmit and receive clocks.
- A host application must allow the generation of a transmit clock using a separate PLL than the one used for the receive clock.
- A slave application can either use a common PLL for the Rx and Tx or a separate PLL.
- HSDI port B link 0 can operate with common transmit and receive clocks or independent common and receive clocks.
- HSDI port B link 1 must operate with common transmit and receive clocks; therefore, it cannot be used on a host board.

Table 21 shows the supported interfaces with Stratix PCI development boards operated as host or slave boards.

Table 21. HSDI Port B Supported Interfaces

Interface	Host	Slave
16-bit	Not supported	Supported
8-bit (link 0)	Supported	Supported
8-bit (link 1)	Not supported	Supported

HyperTransport DUT Chains

The HyperTransport DUT specification defines 3 board types:

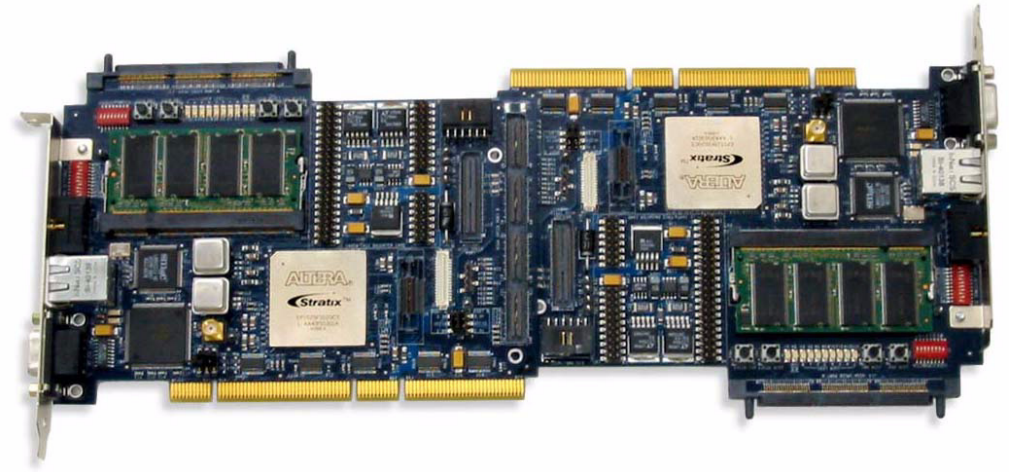
- Host
- Tunnel
- End-chain (cave)

The Stratix PCI development board operates as a host or cave board as determined by the application. Tunnel boards have at least two independent HyperTransport DUT interfaces and act as conduits between hosts, caves, and additional tunnels.

Operation with Two Stratix PCI Development Boards

Figure 5 shows two Stratix PCI development boards connected in the HyperTransport DUT host/cave configuration. The cave board's bottom-side connector at location J9 is inserted into the host board's top-side connector at J8. The cave board is rotated 180° with respect to the host board.

Figure 5. HyperTransport DUT Host/Cave Configuration



Power

Table 22 shows the power sourcing capability of the HSDI port B interface to a tunnel or cave board when the Stratix PCI development board is used as a host board.

☞ Do not apply power to a cave board from the PCI connector or the external power connector or both boards will be damaged.

Table 22. HSDI Port B Host Board Power Sourcing Capability

Voltage (V)	Maximum Source Current (A)
3.3	4

JTAG Chain

The JTAG chain can be made to pass through the HSDI port B connector. Refer to Table 26 on page 27 for instructions on setting the JTAG chain bypass jumper.

I/O Standard

Jumper plug J20 allows the HSDI port B interface to operate at either 2.5 V for HyperTransport applications or 3.3 V for signaling standards such as the SPI-4.2 and RapidIO interfaces. Table 23 shows the jumper settings.

Table 23. HSDI Port B Interface Signal Standard Jumper (J20)

Standard	I/O Voltage (V)	Shunt Connects
HyperTransport	2.5	J20.4 to J20.6
SPI-4.2, RapidIO	3.3	J20.2 to J20.4

The HSDI port B interface uses discrete differential receive termination resistors as required by the HyperTransport interface.

Agilent/Samtec ASP Differential Probe Interface

The Agilent / Samtec ASP differential probe interface at J12 allows the user to monitor the port B link 0 receive signals with high-speed test equipment.

Expansion Prototype Card (PROTO1) Interface

J2 through J4 allow the Stratix PCI development board to accept optional boards with a Expansion Prototype Card (PROTO1) interface. Compatible boards include the Altera Nios Ethernet Development Kit (EDK) daughter card. Additionally, these connectors can be used as a general purpose debugging or expansion interface with 40 pins of LVTTL signals.

Table 24 shows the maximum current available to the Expansion Prototype Card (PROTO1) interface.

Table 24. Maximum Allowed Current Draw for the Expansion Prototype Card (PROTO1)

Voltage (V)	Maximum Current (A)
3.3	4
12.0	1

Refer to the *Nios Development Board, Stratix Edition Data Sheet* for details about the Expansion Prototype Card (PROTO1) interface.

10/100 Ethernet

U11 is an SMSC LAN91C111 10/100 Ethernet MAC/Phy. RJ1 is an RJ-45 connector with integrated magnetics and activity LEDs.

RS-232 Serial Interface

J7 is a DB-9 connector wired as an RS-232 serial DTE device. U10 shifts the RS-232 signals to LVTTL levels for connection to the Stratix device.

LCD Display Interface

J5 and J19 allow the Stratix PCI development board to accept an optional LCD display. Compatible displays include the Optrex T-51382D064J-FW-P-AA 6.4 display (not included with the kit).

The LCD Interface shares Stratix signals with the Mictor probe debug interface. Only one of the interfaces can be used at a time.

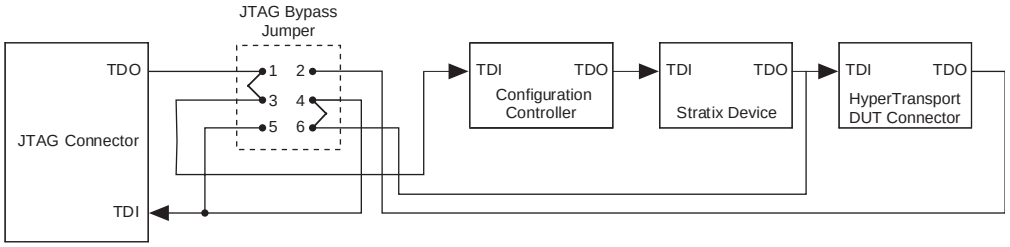
Debugging Interfaces

The Stratix PCI development board has the debugging interfaces described in the following sections.

JTAG

J1 provides access to the JTAG chain of the Stratix PCI development board. Figure 6 shows the JTAG chain. The factory-default setting for the JTAG bypass jumper sets the chain to loop through the MAX configuration controller and the Stratix device.

Figure 6. JTAG Chain



JTAG Chain Jumper

Table 25 shows the JTAG chain jumper.

Table 25. JTAG Chain Jumper	
Shunt Connects	**Description**
J17 pins 1 and 3	Factory-default setting.
J17 pins 4 and 6	

Changing the JTAG Chain

J17 is the JTAG chain bypass jumper. The JTAG chain changes when two Stratix PCI development boards are connected via the HSDI port B connector. Insert two shunts according to the configuration as shown in Table 26.

Table 26. JTAG Chain Bypass Jumper			
Number of Boards in Chain	**Board Position**	**Shunt 1 Connects**	**Shunt 2 Connects**
1 (Standalone)	–	J17.1 to J17.3	J17.4 to J17.6
2 (HyperTransport DUT host/cave)	Host	J17.1 to J17.3	J17.2 to J17.4
	Cave	J17.3 to J17.5	J17.2 to J17.4

SignalTap II Logic Analyzer

The JTAG debug interface can also be used for Altera's SignalTap II logic analyzer.

Refer to *AN 280: Design Verification Using the SignalTap II Embedded Logic Analyzer* for a description of the SignalTap II logic analyzer.

Agilent/Samtec ASP Differential Probe

J12 is an Agilent / Samtec ASP differential probe header that monitors port B link 0's receive signals. Compatible adaptors include the Agilent Technologies E5379A differential probe adaptor.

Mictor Probe

J6 is a Mictor header that provides probing capability for internal Stratix device signals. The Mictor probe is compatible with Agilent Technologies E5346A Probe Adapter for use with Agilent Technologies Logic Analyzers.

The Mictor Probe Debug Interface shares Stratix signals with the LCD Interface. Only one of the interfaces can be used at a time.

The SignalProbe™ feature can be used to route internal Stratix signals to J6. You do not need to recompile the Stratix design to use the SignalProbe feature.

Refer to *Technical Brief 82: SignalProbe Compilation Enables Fast System Debugging with the Quartus II Software* for a description of the SignalProbe feature.

Using the Board

When power is applied to the board, the user LEDs flash. At this time, the Stratix device is automatically configured and, upon successful configuration, the configuration done LED (D4) illuminates. To configure the board with a new design, the designer should perform the following steps, which are explained later in this section.

1. Apply power to the board.
2. Configure the Stratix device.

Apply Power

Power can be introduced by one of the following means:

- Installing the board into a universal PCI slot
- Attaching the board to an ATX power supply with the external power adaptor cable
- Attaching the board to an independently powered board via HSDI port A
- Attaching the board to an independently powered board via HSDI port B

CAUTION

The board has special power supply circuitry that can be damaged if more than one power source is applied to the board at the same time.

Operating the Board with an External Power Supply

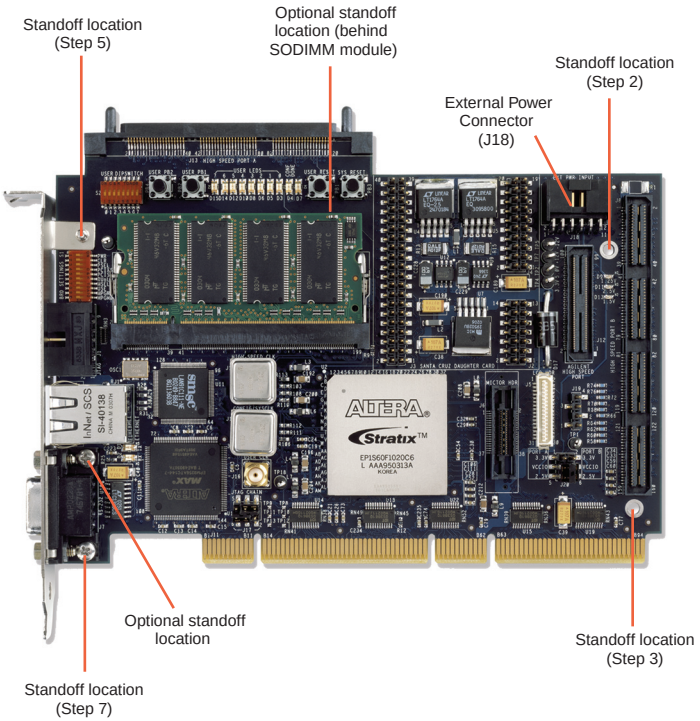
To operate the board with an external power supply, perform the following steps:

1. Insert the small 12-pin connector of the external power supply adapter cable into J18.
2. Insert the 20-pin connector into a standard ATX PC power supply.
3. On the board settings dip switch bank (S1), set the switch at position 1 (PWR), to the on position. See Table 11 on page 16.

Installing Standoffs for Bench-top Operation

The Stratix PCI development board is initially configured for installation in a conventional PCI slot. Six standoffs and four screws are included to install on the board for bench-top operation (Figure 7).

Figure 7. Configuring the Board for Bench-top Operation



1. Position the board face up with the PCI bracket on the left.
2. Insert a screw in the hole next to pin 99 of the Agilent/Samtec ASP Probe connector (J12) and fasten a standoff to the screw.
3. Insert a screw through the hole next to pin 160 of the HSDI port B connector (J8) and fasten a standoff to the screw.
4. Gently place the board face down with the PCI bracket on the right.
5. Remove the screw adjacent to RN4. Turn the board face up, insert the screw through the same hole, and fasten a standoff to the screw.
6. Gently place the board face down with the PCI bracket on the right
7. Remove the lower screw/nut combination of the RS-232 connector (J7). Turn the board face-up, place the screw through the same hole, and fasten a standoff to the screw.

For optional increased stability, perform the following steps:

1. Remove the upper screw/nut combination of the RS-232 connector. (J7). Turn the board face-up, place the screw through the same hole, and fasten a standoff to the screw.
2. Carefully remove the SDRAM SODIMM module in the SODIMM socket.
3. Add a final standoff in the hole provided next to the release on the right side of the SODIMM socket.

Configuration via the JTAG Interface

After power is applied to the Stratix PCI development board, the Stratix device can be configured. The JTAG interface permits the Quartus® II software to load the Stratix device with a user design through the ByteBlaster II cable. The user design remains in the Stratix device until power is removed from the board.

To configure the Stratix device using the Quartus II software and the ByteBlaster II cable, perform the following steps:

1. Connect the ByteBlaster II cable to J1.
2. Open the Quartus II SRAM Object File (**.sof**) that you want to load into the device, which launches the Quartus II Programmer.

3. Select ByteBlaster II as the hardware. Search for “Changing the Hardware Setup” in Quartus II Help for instructions.

4. Set the mode to JTAG.

5. Click **Start**.

☞ If the board is installed into a computer’s PCI slot when it is configured by the ByteBlaster II cable, the computer system could lock up. If this happens, reset the computer. Do not shutdown or the configuration will be lost. Restart the computer to re-enumerate the PCI bus.

Upon successful configuration, the configuration done LED (D4) illuminates.

Refer to Quartus II Help for instructions on how to use the ByteBlaster II cable.

Configuration from the Flash Memory

The Stratix device is volatile; therefore, it must be configured each time power is applied to the board. The Stratix PCI development board has a non-volatile configuration scheme that automatically configures the Stratix device with a factory default design, or, if selected, a user design, after power is applied.

Upon power-up, the configuration circuit, comprised of the EPM3256ATC144 device and flash memory, configures the Stratix device. If the board settings dip switch bank is set for user configuration, the circuit attempts to load the specified user design. If the load is unsuccessful, the configuration done LED (D4) does not illuminate and the Stratix device is not configured.

☞ The configuration circuit uses a factory-programmed default design in the EPM3256ATC144 device. Using the JTAG interface to program the EPM3256ATC144 device can disable the configuration circuit, requiring subsequent Stratix configurations to be performed with the JTAG interface.

☞ The factory-programmed default Stratix configuration image resides at a fixed location of flash memory. Altering this image can result in unpredictable board operation upon power-up and can prevent the configuration circuit from operating, thereby requiring subsequent Stratix configurations to be performed with the JTAG interface.

Factory Configuration

The user LEDs blink and the CONF DONE LED illuminates when the factory-programmed design is loaded into the Stratix device.

Refer to the *PCI Development Kit, Stratix Edition Getting Started User Guide* or *PCI High-Speed Development Kit, Stratix Professional Edition Getting Started User Guide* for details on the factory-programmed design.

Configuration Data

To configure the board, perform the following steps:

1. Create a HEX (**.hex**) file for your design.

   Refer to Quartus II Help for instructions on creating a HEX file.

2. Write the contents of the HEX file into flash memory. See the *PCI Development Kit, Stratix Edition Getting Started User Guide* or *PCI High-Speed Development Kit, Stratix Professional Edition Getting Started User Guide* for instructions.

3. Select the user configuration using the board settings dip switch bank.

4. Force the device to configure by pressing the system reset pushbutton (PB3).

Pin-Outs & Signal Specifications

This section provides the board's pin-out and signal specifications.

PCI & PCI-X

J11 is a 3.3/5.0-V universal PCI connector. U13 through U22 are level converters that reduce 5.0-V PCI backplane signals to allowable 3.3-V ranges. Figure 8 shows the flow of PCI signals between the PCI connector and the Stratix device.

Figure 8. PCI Level Converters

Table 27 shows the connection of the PCI connector to the Stratix device. The level converters are not shown.

Table 27. PCI Signals (Part 1 of 3)

PCI Signal	PCI Connector (J11)	Stratix Pin (U2)	Local Signal
PCI_CLK	B16	AM15 (PLL12)	LPCI_CLK
PCI_RSTn	A15	AL19	LPCI_RSTn
PCI_LOCKn	B39	AJ9	LPCI_LOCKn
PCI_INTAn	A6	AM4	LPCI_INTAn
PCI_IDSEL	A26	AK6	LPCI_IDSEL
PCI_REQn	B18	AK3	LPCI_REQn
PCI_GNTn	A17	AL3	LPCI_GNTn
PCI_REQ64n	A60	AC12	LPCI_REQ64n
PCI_ACK64n	B60	AD12	LPCI_ACK64n
PCI_FRAMEn	A34	AM9	LPCI_FRAMEn
PCI_DEVSELn	B37	AL9	LPCI_DEVSELn
PCI_IRDYn	B35	AC18	LPCI_IRDYn
PCI_TRDYn	A36	AL15	LPCI_TRDYn
PCI_STOPn	A38	AL10	LPCI_STOPn
PCI_PAR	A43	AE9	LPCI_PAR
PCI_PAR64	A67	AH13	LPCI_PAR64
PCI_PERRn	B40	AH9	LPCI_PERRn
PCI_SERRn	B42	AF9	LPCI_SERRn
PCI_CBEn0	A52	AF10	LPCI_CBEn0
PCI_CBEn1	B44	AD9	LPCI_CBEn1
PCI_CBEn2	B33	AH7	LPCI_CBEn2
PCI_CBEn3	B26	AJ6	LPCI_CBEn3
PCI_CBEn4	B66	AJ13	LPCI_CBEn4
PCI_CBEn5	A65	AK13	LPCI_CBEn5
PCI_CBEn6	B65	AL13	LPCI_CBEn6
PCI_CBEn7	A64	AM13	LPCI_CBEn7
PCI_AD0	A58	AE12	LPCI_AD0
PCI_AD1	B58	AJ12	LPCI_AD1
PCI_AD2	A57	AK12	LPCI_AD2
PCI_AD3	B56	AL12	LPCI_AD3
PCI_AD4	A55	AB11	LPCI_AD4
PCI_AD5	B55	AE11	LPCI_AD5
PCI_AD6	A54	AG11	LPCI_AD6
PCI_AD7	B53	AH11	LPCI_AD7
PCI_AD8	B52	AK11	LPCI_AD8
PCI_AD9	A49	AL11	LPCI_AD9

Table 27. PCI Signals (Part 2 of 3)

PCI Signal	PCI Connector (J11)	Stratix Pin (U2)	Local Signal
PCI_AD10	B48	AM11	LPCI_AD10
PCI_AD11	A47	AG10	LPCI_AD11
PCI_AD12	B47	AJ10	LPCI_AD12
PCI_AD13	A46	AK10	LPCI_AD13
PCI_AD14	B45	AK9	LPCI_AD14
PCI_AD15	A44	AC9	LPCI_AD15
PCI_AD16	A32	AK8	LPCI_AD16
PCI_AD17	B32	AL8	LPCI_AD17
PCI_AD18	A31	AM8	LPCI_AD18
PCI_AD19	B30	AJ8	LPCI_AD19
PCI_AD20	A29	AJ7	LPCI_AD20
PCI_AD21	B29	AK7	LPCI_AD21
PCI_AD22	A28	AL7	LPCI_AD22
PCI_AD23	B27	AM7	LPCI_AD23
PCI_AD24	A25	AL6	LPCI_AD24
PCI_AD25	B24	AM6	LPCI_AD25
PCI_AD26	A23	AH5	LPCI_AD26
PCI_AD27	B23	AJ5	LPCI_AD27
PCI_AD28	A22	AK5	LPCI_AD28
PCI_AD29	B21	AL5	LPCI_AD29
PCI_AD30	A20	AJ4	LPCI_AD30
PCI_AD31	B20	AK4	LPCI_AD31
PCI_AD32	A91	AK22	LPCI_AD32
PCI_AD33	B90	AL22	LPCI_AD33
PCI_AD34	A89	AM22	LPCI_AD34
PCI_AD35	B89	AJ21	LPCI_AD35
PCI_AD36	A88	AK21	LPCI_AD36
PCI_AD37	B87	AL21	LPCI_AD37
PCI_AD38	A86	AH20	LPCI_AD38
PCI_AD39	B86	AJ20	LPCI_AD39
PCI_AD40	A85	AK20	LPCI_AD40
PCI_AD41	B84	AL20	LPCI_AD41
PCI_AD42	A83	AM20	LPCI_AD42
PCI_AD43	B83	AB19	LPCI_AD43
PCI_AD44	A82	AD19	LPCI_AD44
PCI_AD45	B81	AA18	LPCI_AD45
PCI_AD46	A80	AH18	LPCI_AD46

Table 27. PCI Signals (Part 3 of 3)

PCI Signal	PCI Connector (J11)	Stratix Pin (U2)	Local Signal
PCI_AD47	B80	AJ18	LPCI_AD47
PCI_AD48	A79	AK18	LPCI_AD48
PCI_AD49	B78	AA15	LPCI_AD49
PCI_AD50	A77	AB15	LPCI_AD50
PCI_AD51	B77	AC15	LPCI_AD51
PCI_AD52	A76	AD15	LPCI_AD52
PCI_AD53	B75	AA14	LPCI_AD53
PCI_AD54	A74	AB14	LPCI_AD54
PCI_AD55	B74	AD14	LPCI_AD55
PCI_AD56	A73	AE14	LPCI_AD56
PCI_AD57	B72	AK14	LPCI_AD57
PCI_AD58	A71	AL14	LPCI_AD58
PCI_AD59	B71	AB13	LPCI_AD59
PCI_AD60	A70	AC13	LPCI_AD60
PCI_AD61	B69	AD13	LPCI_AD61
PCI_AD62	A68	AE13	LPCI_AD62
PCI_AD63	B68	AA12	LPCI_AD63

System Configuration

Table 28 shows the PCI system configuration signals.

Table 28. PCI System Configuration Signals

Board Reference	Board Settings Dip Switch Bank Positions (S1)	PCI Signal	PCI Connector (J11)	Attribute
PCIS	Switch S1 Position 5	PCI_M66EN	B49	Ground
PSEL	Switch S1 Position 3	PCI_XCAP	B38	Ground
PCIXS	Switch S1 Position 4			10-KΩ resistor to ground

DDR SDRAM Memory

The DDR SDRAM memory module installed at J10 uses SSTL-2 signaling and termination. A reference voltage of 1.25 V is supplied to banks 3 and 4 for SSTL-2 receiver biasing. On-board resistors provide fly-by termination at the DDR SDRAM memory connector pins. J10 is the SODIMM connector for the DDR SDRAM memory. Figure 9 shows the DDR SDRAM memory termination connections.

Figure 9. DDR SDRAM Memory Termination Connections

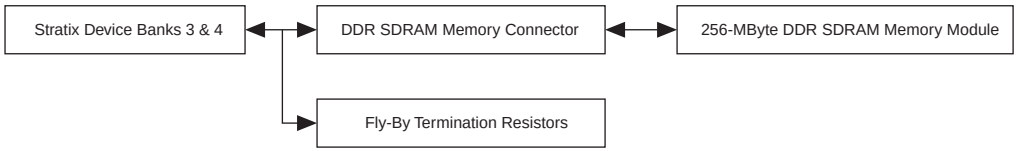


Table 29 shows the DDR SDRAM memory and fly-by termination connections.

Table 29. DDR SDRAM Memory & Fly-By Terminators (Part 1 of 4)

DDR SDRAM Signal	DDR SDRAM Connector (J10)	Fly-By Terminator	Stratix Pin (U2)
DDR_CLKEN0	96	RN29.13	C14
DDR_CLKEN1	95	RN29.14	B14
DDR_CS0n	121	RN12.16	F24
DDR_CS1n	122	RN12.15	G24
DDR_RASn	118	RN33.11	H22
DDR_CASn	120	RN33.9	H23
DDR_WEn	119	RN33.10	J24
DDR_A0	112	RN33.15	H20
DDR_A1	111	RN33.16	H19
DDR_A2	110	RN31.9	G23
DDR_A3	109	RN31.10	G21
DDR_A4	108	RN31.11	G20
DDR_A5	107	RN31.12	F23
DDR_A6	106	RN31.13	F20
DDR_A7	105	RN31.14	F19
DDR_A8	102	RN31.15	H11
DDR_A9	101	RN31.16	H12
DDR_A10	115	RN33.14	H13

Table 29. DDR SDRAM Memory & Fly-By Terminators (Part 2 of 4)

DDR SDRAM Signal	DDR SDRAM Connector (J10)	Fly-By Terminator	Stratix Pin (U2)
DDR_A11	100	RN29.9	H14
DDR_A12	99	RN29.10	F13
DDR_A13	97	RN29.12	F12
DDR_BA0	117	RN33.12	L21
DDR_BA1	116	RN33.13	J22
DDR_BA2	98	RN29.11	J23
DDR_DQS0	11	RN11.12	C5
DDR_DQS1	25	RN14.10	E7
DDR_DQS2	47	RN20.16	A7
DDR_DQS3	61	RN23.14	D11
DDR_DQS4	133	RN12.10	D20
DDR_DQS5	147	RN18.16	D22
DDR_DQS6	169	RN21.14	B26
DDR_DQS7	183	RN24.12	B27
DDR_DQS8	77	RN26.12	D12
DDR_DM0	12	RN11.11	F7
DDR_DM1	26	RN14.9	F8
DDR_DM2	48	RN20.15	F9
DDR_DM3	62	RN23.13	F10
DDR_DM4	134	RN12.9	D29
DDR_DM5	148	RN18.15	D28
DDR_DM6	170	RN21.13	C30
DDR_DM7	184	RN24.11	E28
DDR_DM8	78	RN26.11	G12
DDR_DP0	71	RN26.16	A11
DDR_DP1	73	RN26.14	B12
DDR_DP2	79	RN26.10	C12
DDR_DP3	83	RN29.16	C13
DDR_DP4	72	RN26.15	D13
DDR_DP5	74	RN26.13	E13
DDR_DP6	80	RN26.9	A13
DDR_DP7	84	RN29.15	B13
DDR_DQ0	5	RN11.16	D5
DDR_DQ1	7	RN11.14	C3
DDR_DQ2	13	RN11.10	E5
DDR_DQ3	17	RN14.16	C4

Table 29. DDR SDRAM Memory & Fly-By Terminators (Part 3 of 4)

DDR SDRAM Signal	DDR SDRAM Connector (J10)	Fly-By Terminator	Stratix Pin (U2)
DDR_DQ4	6	RN11.15	D4
DDR_DQ5	8	RN11.13	A4
DDR_DQ6	14	RN11.9	B4
DDR_DQ7	18	RN14.15	B3
DDR_DQ8	19	RN14.14	D6
DDR_DQ9	23	RN14.12	C6
DDR_DQ10	29	RN17.16	B5
DDR_DQ11	31	RN17.14	C7
DDR_DQ12	20	RN14.13	A5
DDR_DQ13	24	RN14.11	D7
DDR_DQ14	30	RN17.15	A6
DDR_DQ15	32	RN17.13	B6
DDR_DQ16	41	RN17.12	B7
DDR_DQ17	43	RN17.10	D8
DDR_DQ18	49	RN20.14	B8
DDR_DQ19	53	RN20.12	E9
DDR_DQ20	42	RN17.11	A8
DDR_DQ21	44	RN17.9	C9
DDR_DQ22	50	RN20.13	C8
DDR_DQ23	54	RN20.11	D9
DDR_DQ24	55	RN20.10	E11
DDR_DQ25	59	RN23.16	B9
DDR_DQ26	65	RN23.12	D10
DDR_DQ27	67	RN23.10	C10
DDR_DQ28	56	RN20.9	A9
DDR_DQ29	60	RN23.15	B11
DDR_DQ30	66	RN23.11	C11
DDR_DQ31	68	RN23.9	B10
DDR_DQ32	127	RN12.14	A20
DDR_DQ33	129	RN12.12	B20
DDR_DQ34	135	RN15.16	C20
DDR_DQ35	139	RN15.14	E20
DDR_DQ36	128	RN12.13	B21
DDR_DQ37	130	RN12.11	C21
DDR_DQ38	136	RN15.15	D21
DDR_DQ39	140	RN15.13	A22

Table 29. DDR SDRAM Memory & Fly-By Terminators (Part 4 of 4)

DDR SDRAM Signal	DDR SDRAM Connector (J10)	Fly-By Terminator	Stratix Pin (U2)
DDR_DQ40	141	RN15.12	B22
DDR_DQ41	145	RN15.10	C22
DDR_DQ42	151	RN18.14	B23
DDR_DQ43	153	RN18.12	C23
DDR_DQ44	142	RN15.11	A24
DDR_DQ45	146	RN15.9	E22
DDR_DQ46	152	RN18.13	B24
DDR_DQ47	154	RN18.11	D23
DDR_DQ48	163	RN18.10	D24
DDR_DQ49	165	RN21.16	A25
DDR_DQ50	171	RN21.12	C24
DDR_DQ51	175	RN21.10	B25
DDR_DQ52	164	RN18.9	C25
DDR_DQ53	166	RN21.15	D25
DDR_DQ54	172	RN21.11	A26
DDR_DQ55	176	RN21.9	E24
DDR_DQ56	177	RN24.16	C26
DDR_DQ57	181	RN24.14	A28
DDR_DQ58	187	RN24.10	A27
DDR_DQ59	189	RN27.16	D26
DDR_DQ60	178	RN24.15	C27
DDR_DQ61	182	RN24.13	B28
DDR_DQ62	188	RN24.9	D27
DDR_DQ63	190	RN27.15	E26

Clocks

Table 30 shows the DDR SDRAM memory clocks.

Table 30. DDR SDRAM Memory Clocks

Clock Signal	DDR SDRAM Memory (J10)	Stratix Pin (U2)
DDR_CLK0N	37	A16
DDR_CLK0P	35	B16
DDR_CLK1N	158	A17

Table 30. DDR SDRAM Memory Clocks		
DDR_CLK1P	160	B17
DDR_CLK2N	91	A18
DDR_CLK2P	89	B18
DDR_CLK_FBIN	-	B15, D17
DDR_CLK_FBOUT	-	D18

Flash Memory

Table 31 shows the connections from the flash memory to the Stratix device and the MAX configuration controller.

Table 31. Flash Memory (Part 1 of 2)			
Flash Memory Signal	**Flash Memory (U3)**	**Stratix Pin (U2)**	**MAX Configuration Controller (U1)**
FLASH_RESETn	12	-	122
FLASH_CEn	26	AM27	60
FLASH_WEn	11	AM28	62
FLASH_WPn	14	-	-
FLASH_OEn	28	AK26	61
FLASH_RDY_BSYn	15	-	63
FLASH_BYTEn	47	-	65
FLASH_A0	25	AJ26	56
FLASH_A1	24	AK27	55
FLASH_A2	23	AL28	113
FLASH_A3	22	AJ27	112
FLASH_A4	21	AH26	111
FLASH_A5	20	AL27	110
FLASH_A6	19	AC20	109
FLASH_A7	18	AH19	108
FLASH_A8	8	AL26	107
FLASH_A9	7	AH24	106
FLASH_A10	6	AJ24	103
FLASH_A11	5	AJ25	102
FLASH_A12	4	AK25	101
FLASH_A13	3	AL25	100
FLASH_A14	2	AK24	99
FLASH_A15	1	AM25	98

Table 31. Flash Memory (Part 2 of 2)

Flash Memory Signal	Flash Memory (U3)	Stratix Pin (U2)	MAX Configuration Controller (U1)
FLASH_A16	48	AM26	81
FLASH_A17	17	AJ22	80
FLASH_A18	16	AJ23	79
FLASH_A19	9	AL24	78
FLASH_A20	10	AH22	75
FLASH_A21	13	AM24	74
FLASH_D0	29	E14	121
FLASH_D1	31	F14	120
FLASH_D2	33	F15	119
FLASH_D3	35	C16	118
FLASH_D4	38	G19	117
FLASH_D5	40	J19	116
FLASH_D6	42	K19	97
FLASH_D7	44	J20	96
FLASH_D8	30	AB20	93
FLASH_D9	32	AF22	92
FLASH_D10	34	AD21	91
FLASH_D11	36	AG23	90
FLASH_D12	39	AC21	88
FLASH_D13	41	AD22	87
FLASH_D14	43	AB21	86
FLASH_D15	45	AA21	84

MAX Configuration Controller

U1 is a factory programmed EPM3256ATC144 device. Table 32 shows the connections between the MAX configuration controller, Stratix device, and flash memory, which configure the Stratix device.

Table 32. MAX Configuration Controller Connections (Part 1 of 3)

Configuration Signal	MAX Configuration Controller (U1)	Stratix Pin (U2)	Flash Memory (U3)
DCLK	23	E19	-
EP1S_CONF_DONE	7	G18	-
EP1S_INIT_DONE	141	AE15	-

Table 32. MAX Configuration Controller Connections (Part 2 of 3)

Configuration Signal	MAX Configuration Controller (U1)	Stratix Pin (U2)	Flash Memory (U3)
EP1S_nCONFIG	9	J18	-
EP1S_nSTATUS	8	G16	-
FLASH_RESETn	122	-	12
FLASH_CEn	60	AM27	26
FLASH_WEn	62	AM28	11
FLASH_OEn	61	AK26	28
FLASH_RDY_BSYn	63	-	15
FLASH_BYTEn	65	-	47
FLASH_A0	56	AJ26	25
FLASH_A1	55	AK27	24
FLASH_A2	113	AL28	23
FLASH_A3	112	AJ27	22
FLASH_A4	111	AH26	21
FLASH_A5	110	AL27	20
FLASH_A6	109	AC20	19
FLASH_A7	108	AH19	18
FLASH_A8	107	AL26	8
FLASH_A9	106	AH24	7
FLASH_A10	103	AJ24	6
FLASH_A11	102	AJ25	5
FLASH_A12	101	AK25	4
FLASH_A13	100	AL25	3
FLASH_A14	99	AK24	2
FLASH_A15	98	AM25	1
FLASH_A16	81	AM26	48
FLASH_A17	80	AJ22	17
FLASH_A18	79	AJ23	16
FLASH_A19	78	AL24	9
FLASH_A20	75	AH22	10
FLASH_A21	74	AM24	13
FLASH_D0	121	E14	29
FLASH_D1	120	F14	31
FLASH_D2	119	F15	33
FLASH_D3	118	C16	35
FLASH_D4	117	G19	38
FLASH_D5	116	J19	40

Table 32. MAX Configuration Controller Connections (Part 3 of 3)

Configuration Signal	MAX Configuration Controller (U1)	Stratix Pin (U2)	Flash Memory (U3)
FLASH_D6	97	K19	42
FLASH_D7	96	J20	44
FLASH_D8	93	AB20	30
FLASH_D9	92	AF22	32
FLASH_D10	91	AD21	34
FLASH_D11	90	AG23	36
FLASH_D12	88	AC21	39
FLASH_D13	87	AD22	41
FLASH_D14	86	AB21	43
FLASH_D15	84	AA21	45

Table 33 shows the settings connections between the MAX configuration controller and board settings dip switch bank.

Table 33. Board Settings Dip Switch Bank (S1) Connections

Board Reference	Board Settings Dip Switch Bank Position	Signal	MAX Configuration Controller (U1)
USE M	Switch S1 Position 8	USE_MPGM	36
MPGM1	Switch S1 Position 9	MPGM1	34
MPGM0	Switch S1 Position 10	MPGM0	35

Table 34 shows the user connections between the MAX configuration controller and the Stratix device.

Table 34. User Connections

User Signal	MAX Configuration Controller (U1)	Stratix Pin (U2)
CPLD_USER0	67	AL4
CPLD_USER1	68	AG12

User LEDs

Signals USER_LED0 through USER_LED7 are driven by the Stratix device through the MAX configuration controller to the user LEDs as shown in Figure 10 and Table 35. Set the control signal to a logic '1' to illuminate the LED.

Figure 10. User LED Drive & Control Signals

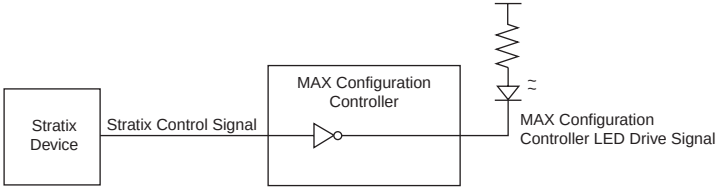


Table 35. User LEDs

Label	Reference Designator	Stratix Device Control Signal	Stratix Pin (U2)	MAX Configuration Controller Input (U1)	MAX Configuration Controller Output (U1)	MAX Configuration Controller LED Drive Signal
0	D3	USER_LED0	AK28	37	38	USER_LED_DRV0
1	D5	USER_LED1	AH28	137	138	USER_LED_DRV1
2	D6	USER_LED2	AK30	134	136	USER_LED_DRV2
3	D8	USER_LED3	AJ28	132	133	USER_LED_DRV3
4	D10	USER_LED4	AJ29	19	131	USER_LED_DRV4
5	D12	USER_LED5	AK29	16	18	USER_LED_DRV5
6	D14	USER_LED6	AL30	14	15	USER_LED_DRV6
7	D15	USER_LED7	AL29	11	12	USER_LED_DRV7

Board Settings Dip Switch Bank

Table 36 describes the signal names and pin connections for the board settings dip switch bank (S1).

Table 36. Board Settings Dip Switch Bank

Board Reference	Board Settings Dip Switch Bank Position	Signal	Destination Pin
PWR	Switch S1 Position 1	MAIN_SW	External power connector J18.6
CLR	Switch S1 Position 2	DEV_CLRn	Stratix pin (U2) AH14
PSEL	Switch S1 Position 3	PCI_XCAP	PCI connector J11.B38
PCIXS	Switch S1 Position 4		
PCIS	Switch S1 Position 5	PCI_M66EN	PCI connector J11.B49
RUnLU	Switch S1 Position 6	RUnLU	Stratix pin (U2) AF14
MSEL2	Switch S1 Position 7	SMSEL2	Stratix pin (U2) AE19
USE MPGM	Switch S1 Position 8	USE_MPGM	MAX configuration controller U1.36
MPGM1	Switch S1 Position 9	MPGM1	MAX configuration controller U1.34
MPGM0	Switch S1 Position 10	MPGM0	MAX configuration controller U1.35

User Dip Switch Bank

Table 37 shows the signal names and pin connections for the user dip switch bank (S2).

Table 37. User Dip Swich Bank (S2)

Board Reference	User Dip Switch	Signal	Stratix Pin (U2)
USER DIPSWITCH 0	Switch 2 Position 1	USER_DIPSW0	AD23
USER DIPSWITCH 1	Switch 2 Position 2	USER_DIPSW1	AE24
USER DIPSWITCH 2	Switch 2 Position 3	USER_DIPSW2	AE23
USER DIPSWITCH 3	Switch 2 Position 4	USER_DIPSW3	AF24
USER DIPSWITCH 4	Switch 2 Position 5	USER_DIPSW4	AC22
USER DIPSWITCH 5	Switch 2 Position 6	USER_DIPSW5	AG24
USER DIPSWITCH 6	Switch 2 Position 7	USER_DIPSW6	AB22
USER DIPSWITCH 7	Switch 2 Position 8	USER_DIPSW7	AF23

Pushbutton Switches

Table 38 shows the signal names and pin connections for the pushbutton switches.

Table 38. Pushbuttons

Board Reference	Pin	Signal	Stratix Pin (U2)
SYS RESET	PB3.2	SYS_RESETn	AG13
USER RESET	PB1.2	USER_RESETn	AG22
USER_PB1	PB2.2	USER_PB1	AG9
USER_PB2	PB4.2	USER_PB2	AM5

External Power Header

Table 39 shows the connections for J18, the external power header.

Table 39. External Power Header

Supply Voltage	External Power Header (J18)
3.3 V	1, 2, 11, 12
5.0 V	5
+12.0 V	7
-12.0 V	8
GND	3, 4, 9, 10
MAIN_SW	6

HSDI Port A Interface

HSDI port A is only available in the Professional Board. Table 40 shows the HSDI port A Tx interface.

Table 40. HSDI Port A Tx Interface (Part 1 of 2)

Signal	Connector (J13)	Stratix Pin (U2)
B6_TX_CLKn	58	Y5
B6_TX_CLKp	56	Y6
B6_TX_CTLn	92	V5
B6_TX_CTLp	90	V6
B6_TX_CADn0	32	AA9
B6_TX_CADp0	30	AA8

Table 40. HSDI Port A Tx Interface (Part 2 of 2)

Signal	Connector (J13)	Stratix Pin (U2)
B6_TX_CADn1	38	W5
B6_TX_CADp1	36	W6
B6_TX_CADn2	46	W8
B6_TX_CADp2	44	W7
B6_TX_CADn3	52	W10
B6_TX_CADp3	50	W9
B6_TX_CADn4	66	Y7
B6_TX_CADp4	64	Y8
B6_TX_CADn5	72	Y10
B6_TX_CADp5	70	Y9
B6_TX_CADn6	78	V9
B6_TX_CADp6	76	V10
B6_TX_CADn7	86	V8
B6_TX_CADp7	84	V7

Table 41 shows the HSDI port A Rx interface.

Table 41. HSDI Port A Rx Interface (Part 1 of 2)

Signal	Connector (J13)	Stratix Pin (U2)	Termination Resistor
B6_RX_CLKn	63	U3	R99.2
B6_RX_CLKp	65	U4	R99.1
B6_RX_CTLn	29	AG1	R141.1
B6_RX_CTLp	31	AG2	R141.2
B6_RX_CADn0	89	AD3	R133.1
B6_RX_CADp0	91	AD4	R133.2
B6_RX_CADn1	83	AE4	R134.1
B6_RX_CADp1	85	AE3	R134.2
B6_RX_CADn2	75	AF4	R135.1
B6_RX_CADp2	77	AF3	R135.2
B6_RX_CADn3	69	AG4	R136.1
B6_RX_CADp3	71	AG3	R136.2
B6_RX_CADn4	55	AC3	R137.1
B6_RX_CADp4	57	AC4	R137.2
B6_RX_CADn5	49	AD2	R138.1
B6_RX_CADp5	51	AD1	R138.2

Table 41. HSDI Port A Rx Interface (Part 2 of 2)			
Signal	**Connector (J13)**	**Stratix Pin (U2)**	**Termination Resistor**
B6_RX_CADn6	43	AE2	R139.1
B6_RX_CADp6	45	AE1	R139.2
B6_RX_CADn7	35	AF2	R140.1
B6_RX_CADp7	37	AF1	R140.2

Table 42 shows the HSDI port A control interface.

Table 42. HSDI Port A Control Interface		
Signal	**Connector (J13)**	**Stratix Pin (U2)**
B6_RESETn	23	F22
B6_REF_CLK	10	T6 through resistor R254 AB4 through resistor R255
B6_PWROK	25	G22
B6_IO_RESETn	26	K24
B6_IO_CSn	20	K23
B6_IO_WRn	18	L24
B6_IO_OEn	16	K22
B6_IO_RDYn	14	L23
B6_IO_AD24	98	K14
B6_IO_AD25	100	L14
B6_IO_AD26	102	L22
B6_IO_AD27	104	C28
B6_IO_AD28	106	C29
B6_IO_AD29	108	B30
B6_IO_AD30	110	B29
B6_IO_AD31	112	A29

HSDI Port B Interface

HSDI port B is only available in the Professional Board. J8 and J9 are the HSDI port B connectors. Table 43 shows the HSDI port B link 0 Tx connections.

Table 43. HSDI Port B Link 0 TX Interface

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
B1A_TX_CLKn	115	46	V23
B1A_TX_CLKp	117	44	V24
B1A_TX_CTLn	83	78	Y24
B1A_TX_CTLp	85	76	Y23
B1A_TX_CADn0	139	22	W24
B1A_TX_CADp0	141	20	W23
B1A_TX_CADn1	133	28	W26
B1A_TX_CADp1	135	26	W25
B1A_TX_CADn2	127	34	W28
B1A_TX_CADp2	129	32	W27
B1A_TX_CADn3	121	40	AA24
B1A_TX_CADp3	123	38	AA25
B1A_TX_CADn4	107	54	V25
B1A_TX_CADp4	109	52	V26
B1A_TX_CADn5	101	60	V27
B1A_TX_CADp5	103	58	V28
B1A_TX_CADn6	95	66	Y27
B1A_TX_CADp6	97	64	Y28
B1A_TX_CADn7	89	72	Y25
B1A_TX_CADp7	91	70	Y26

Table 44 shows the HSDI port B link 0 Rx connections.

Table 44. HSDI Port B Link 0 Rx Interface (Part 1 of 2)

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)	Termination Resistor
B1A_RX_CLKn	46	115	U32	R97.2
B1A_RX_CLKp	44	117	U31	R97.1
B1A_RX_CTLn	78	83	V31	R132.1
B1A_RX_CTLp	76	85	V32	R132.2

Table 44. HSDI Port B Link 0 Rx Interface (Part 2 of 2)

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)	Termination Resistor
B1A_RX_CADn0	22	139	AA29	R116.1
B1A_RX_CADp0	20	141	AA28	R116.2
B1A_RX_CADn1	28	133	Y29	R118.1
B1A_RX_CADp1	26	135	Y30	R118.2
B1A_RX_CADn2	34	127	W29	R120.1
B1A_RX_CADp2	32	129	W30	R120.2
B1A_RX_CADn3	40	121	V29	R122.1
B1A_RX_CADp3	38	123	V30	R122.2
B1A_RX_CADn4	54	107	AB30	R124.1
B1A_RX_CADp4	52	109	AB31	R124.2
B1A_RX_CADn5	60	101	AA30	R126.1
B1A_RX_CADp5	58	103	AA31	R126.2
B1A_RX_CADn6	66	95	Y31	R128.1
B1A_RX_CADp6	64	97	Y32	R128.2
B1A_RX_CADn7	72	89	W31	R130.1
B1A_RX_CADp7	70	91	W32	R130.2

Table 45 shows the HSDI port B link 1 Tx connections.

Table 45. HSDI Port B Link 1 Tx Interface (Part 1 of 2)

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
B1B_TX_CLKn	112	49	AA26
B1B_TX_CLKp	114	47	AA27
B1B_TX_CTLn	82	79	AF28
B1B_TX_CTLp	84	77	AF27
B1B_TX_CADn0	136	25	AC26
B1B_TX_CADp0	138	23	AC25
B1B_TX_CADn1	130	31	AD25
B1B_TX_CADp1	132	29	AD26
B1B_TX_CADn2	124	37	AE26
B1B_TX_CADp2	126	35	AE25
B1B_TX_CADn3	118	43	AF25
B1B_TX_CADp3	120	41	AF26
B1B_TX_CADn4	106	55	AB26

Table 45. HSDI Port B Link 1 Tx Interface (Part 2 of 2)

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
B1B_TX_CADp4	108	53	AB27
B1B_TX_CADn5	100	61	AC28
B1B_TX_CADp5	102	59	AC27
B1B_TX_CADn6	94	67	AD27
B1B_TX_CADp6	96	65	AD28
B1B_TX_CADn7	88	73	AE27
B1B_TX_CADp7	90	71	AE28

Table 46 shows the HSDI port B link 1 Rx connections.

Table 46. HSDI Port B Link 1 Rx Interface

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)	Termination Resistor
B1B_RX_CLKn	49	112	AB29	R98.2
B1B_RX_CLKp	47	114	AB28	R98.1
B1B_RX_CTLn	79	82	AC31	R131.1
B1B_RX_CTLp	77	84	AB32	R131.2
B1B_RX_CADn0	25	136	AG32	R115.1
B1B_RX_CADp0	23	138	AG31	R115.2
B1B_RX_CADn1	31	130	AF31	R117.1
B1B_RX_CADp1	29	132	AF32	R117.2
B1B_RX_CADn2	37	124	AE31	R119.1
B1B_RX_CADp2	35	126	AE32	R119.2
B1B_RX_CADn3	43	118	AD31	R121.1
B1B_RX_CADp3	41	120	AD32	R121.2
B1B_RX_CADn4	55	106	AF29	R123.1
B1B_RX_CADp4	53	108	AF30	R123.2
B1B_RX_CADn5	61	100	AE29	R125.1
B1B_RX_CADp5	59	102	AE30	R125.2
B1B_RX_CADn6	67	94	AD29	R127.1
B1B_RX_CADp6	65	96	AD30	R127.2
B1B_RX_CADn7	73	88	AC30	R129.1
B1B_RX_CADp7	71	90	AC29	R129.2

Table 47 shows the HSDI port B control connections.

Table 47. HSDI Port B Control Interface

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
B1_SYS_RESETn	151	151	R5
B1_RESETn	147	147	R9
B1_REF_CLK_IN	8	153	T27
B1_REF_CLK_OUT	153	8	-
B1_PWROK	144	144	R6
B1_REQn	145	145	R10
B1_STOPn	142	142	P7
B1_SMBCLK	14	14	R7
B1_SMBDAT	16	16	P8

Table 48 shows the HSDI port B user signals.

Table 48. HSDI Port B User Signals

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
B1_USER_A0	152	9	P3
B1_USER_A1	9	152	P4
B1_USER_B0	150	11	P1
B1_USER_B1	11	150	P2
B1_USER_C0	149	12	R3
B1_USER_C1	12	149	R4
B1_USER_D0	148	13	R1
B1_USER_D1	13	148	R2
B1_USER_E0	146	15	T2
B1_USER_E1	15	146	T1

Table 49 shows the HSDI port B miscellaneous signals.

Table 49. HSDI Port B Miscellaneous Signals (Part 1 of 2)

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
JTAG_SAMTEC_TDO	154	7	-

Table 49. HSDI Port B Miscellaneous Signals (Part 2 of 2)

Signal	QTE (Bottom) Connector (J9)	QSE (Top) Connector (J8)	Stratix Pin (U2)
JTAG_STRATIX_TDO	7	154	F16 through resistor R9
JTAG_TCK	19	19	G14
JTAG_TMS	10	10	E15
JTAG_TRST	17	17	-

Expansion Prototype Card (PROTO1)

Table 50 shows the Expansion Prototype Card (PROTO1) interface.

Table 50. Expansion Prototype Card (PROTO1) Connectors (Part 1 of 2)

Signal	Connector	Stratix Pin (U2)
SYS_RESETN	J3.1	AG13
CLK_TO_SCRUZ	J4.11	AL16 (through resistor R101)
CLK_OSC_A	J4.9	T4 (through resistor R111) A19 (through resistor R112) AM19 (through resistor R106) *(1)*
CLK_FROM_SCRUZ	J4.13	D15
SCRUZ_CARDSELN	J3.38	G28
SCRUZ_IO0	J3.3	T31
SCRUZ_IO1	J3.4	T32
SCRUZ_IO2	J3.5	R29
SCRUZ_IO3	J3.6	R26
SCRUZ_IO4	J3.7	R25
SCRUZ_IO5	J3.8	R24
SCRUZ_IO6	J3.9	R23
SCRUZ_IO7	J3.1	P260
SCRUZ_IO8	J3.1	P251
SCRUZ_IO9	J3.1	R272
SCRUZ_IO10	J3.13	R28
SCRUZ_IO11	J3.14	P27
SCRUZ_IO12	J3.15	P28
SCRUZ_IO13	J3.16	N26
SCRUZ_IO14	J3.17	N25
SCRUZ_IO15	J3.18	P24
SCRUZ_IO16	J3.21	P23

Table 50. Expansion Prototype Card (PROTO1) Connectors (Part 2 of 2)		
Signal	**Connector**	**Stratix Pin (U2)**
SCRUZ_IO17	J3.23	N28
SCRUZ_IO18	J3.25	N27
SCRUZ_IO19	J3.27	N23
SCRUZ_IO20	J3.28	N24
SCRUZ_IO21	J3.29	M25
SCRUZ_IO22	J3.31	M24
SCRUZ_IO23	J3.32	M27
SCRUZ_IO24	J3.33	M26
SCRUZ_IO25	J3.35	L26
SCRUZ_IO26	J3.36	L27
SCRUZ_IO27	J3.37	K25
SCRUZ_IO28	J3.39	K26
SCRUZ_IO29	J2.4	K27
SCRUZ_IO30	J2.5	K28
SCRUZ_IO31	J2.6	J26
SCRUZ_IO32	J2.7	J25
SCRUZ_IO33	J2.8	H26
SCRUZ_IO34	J2.9	H25
SCRUZ_IO35	J2.10	J28
SCRUZ_IO36	J2.11	J27
SCRUZ_IO37	J2.12	H27
SCRUZ_IO38	J2.13	H28
SCRUZ_IO39	J2.14	G27

Note to Table 50:
(1) Only one of these resistors can be installed. R112 is the factory default.

RS-232

Table 51 shows the RS-232 Serial interface.

Table 51. RS-232 Serial Interface					
Connector Signal	**Connector Pin**	**Level Shifter A**	**Level Shifter B**	**Stratix Pin (U2)**	**Stratix Signal**
DB9_TXD	J7.2	U10.14	U10.11	AC14	RS232_TXD
DB9_RXD	J7.3	U10.13	U10.12	AF12	RS232_RXD
DB9_RTS	J7.7	U10.8	U10.9	AF13	RS232_RTS

Table 51. RS-232 Serial Interface

Connector Signal	Connector Pin	Level Shifter A	Level Shifter B	Stratix Pin (U2)	Stratix Signal
DB9_CTS	J7.8	U10.7	U10.10	AM14	RS232_CTS

LCD Header

Table 52 shows the LCD header connections.

Table 52. LCD Header

Signal	Connector Pin (J5)	Stratix Pin (U2)
MICTOR_CLKE	2	F32
MICTOR_DE0	6	G30
MICTOR_DE1	7	H30
MICTOR_DE2	8	H29
MICTOR_DE3	9	G31
MICTOR_DE4	10	G32
MICTOR_DE5	11	H31
MICTOR_DE6	13	H32
MICTOR_DE7	14	J29
MICTOR_DE8	15	J30
MICTOR_DE9	16	K30
MICTOR_DE10	17	K29
MICTOR_DE11	18	J32
MICTOR_DE12	3	J31
MICTOR_DE13	27	K31
MICTOR_DE14	31	L32
MICTOR_DE15	30	M28
MICTOR_DO0	20	M29
MICTOR_DO1	21	L30
MICTOR_DO2	22	L31
MICTOR_DO3	23	M31
MICTOR_DO4	24	M30
MICTOR_DO5	25	N29
MICTOR_DO6	4	N30

JTAG

Table 53 shows the connections to the JTAG header.

Table 53. JTAG

JTAG Signal	JTAG Connector (J1)
JTAG_TCK	1
JTAG_CONN_TDO	9
JTAG_CONN_TDI	3
JTAG_TMS	5
GND	2, 10
3.3V	4, 6

Agilent/Samtec ASP Differential Probe

Table 54 shows the connections from the HSDI port B link 0 receive signals to the Agilent / Samtec ASP differential probe.

Table 54. Agilent/Samtec ASP Differential Probe (Part 1 of 2)

Probe Signal	ASP Pin (J12)	Termination Resistor	Isolation Resistor	Stratix Pin (U2)	Signal
SAMTEC_RX_CLKn	79	R95.1	R75.1	U32	B1A_RX_CLKn
SAMTEC_RX_CLKp	80	R96.1	R76.1	U31	B1A_RX_CLKp
SAMTEC_RX_CTLn	67	R93.1	R73.1	V31	B1A_RX_CTLn
SAMTEC_RX_CTLp	68	R94.1	R74.1	V32	B1A_RX_CTLp
SAMTEC_RX_CADn0	7	R77.1	R57.1	AA29	B1A_RX_CADn0
SAMTEC_RX_CADp0	8	R78.1	R58.1	AA28	B1A_RX_CADp0
SAMTEC_RX_CADn1	11	R79.1	R59.1	Y29	B1A_RX_CADn1
SAMTEC_RX_CADp1	12	R80.1	R60.1	Y30	B1A_RX_CADp1
SAMTEC_RX_CADn2	15	R81.1	R61.1	W29	B1A_RX_CADn2
SAMTEC_RX_CADp2	16	R82.1	R62.1	W30	B1A_RX_CADp2
SAMTEC_RX_CADn3	19	R83.1	R63.1	V29	B1A_RX_CADn3
SAMTEC_RX_CADp3	20	R84.1	R64.1	V30	B1A_RX_CADp3
SAMTEC_RX_CADn4	23	R85.1	R65.1	AB30	B1A_RX_CADn4
SAMTEC_RX_CADp4	24	R86.1	R66.1	AB31	B1A_RX_CADp4
SAMTEC_RX_CADn5	27	R87.1	R67.1	AA30	B1A_RX_CADn5
SAMTEC_RX_CADp5	28	R88.1	R68.1	AA31	B1A_RX_CADp5
SAMTEC_RX_CADn6	31	R89.1	R69.1	Y31	B1A_RX_CADn6
SAMTEC_RX_CADp6	32	R90.1	R70.1	Y32	B1A_RX_CADp6

Table 54. Agilent/Samtec ASP Differential Probe (Part 2 of 2)

Probe Signal	ASP Pin (J12)	Termination Resistor	Isolation Resistor	Stratix Pin (U2)	Signal
SAMTEC_RX_CADn7	35	R91.1	R71.1	W31	B1A_RX_CADn7
SAMTEC_RX_CADp7	36	R92.1	R72.1	W32	B1A_RX_CADp7

Mictor Header

Table 55 shows the connections to the Mictor header.

Table 55. Mictor Header (Part 1 of 2)

Signal	Mictor Header Pin (J6)	Stratix Pin (U2)
MICTOR_CLKO	6	G29
MICTOR_CLKE	5	F32
MICTOR_DE0	37	G30
MICTOR_DE1	35	H30
MICTOR_DE2	33	H29
MICTOR_DE3	31	G31
MICTOR_DE4	29	G32
MICTOR_DE5	27	H31
MICTOR_DE6	25	H32
MICTOR_DE7	23	J29
MICTOR_DE8	21	J30
MICTOR_DE9	19	K30
MICTOR_DE10	17	K29
MICTOR_DE11	15	J32
MICTOR_DE12	13	J31
MICTOR_DE13	11	K31
MICTOR_DE14	9	L32
MICTOR_DE15	7	M28
MICTOR_DO0	38	M29
MICTOR_DO1	36	L30
MICTOR_DO2	34	L31
MICTOR_DO3	32	M31
MICTOR_DO4	30	M30
MICTOR_DO5	28	N29
MICTOR_DO6	26	N30
MICTOR_DO7	24	N31

Table 55. Mictor Header (Part 2 of 2)

Signal	Mictor Header Pin (J6)	Stratix Pin (U2)
MICTOR_D08	22	N32
MICTOR_D09	20	P29
MICTOR_D010	18	P30
MICTOR_D011	16	P31
MICTOR_D012	14	P32
MICTOR_D013	12	R32
MICTOR_D014	10	R31
MICTOR_D015	8	R30

Schematics

The subsequent pages provide the schematics for the Stratix PCI development board.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com

NOTES:

1. Altera Stratix Schematic Symbol Breakdown:
   - (a) Bank1 - HSDI
   - (b) Bank2 - HSDI
   - (c) Bank3 - GPIO/DDR/PCI
   - (d) Bank4 - GPIO/DDR/PCI
   - (e) Bank5 - HSDI
   - (f) Bank6 - HSDI
   - (g) Bank7 - GPIO/DDR/PCI
   - (h) Bank8 - GPIO/DDR/PCI
   - (i) Configuration/GPIO
   - (j) Clocks/GPIO
   - (k) VCCINT/GND
   - (l) VCCIO/GND
2. Board is to be powered from any ONE of the following interfaces at any one time:
   - (a) PCI Edge Connector
   - (b) ATX Power Connector
3. Related Documents
   - (a) 100-0216200-01 Raw PCB
   - (b) 110-0216200-01 Gerber Files
   - (c) 120-0216200-01 PCB Design Files
   - (d) 130-0216200-01 Assembly Drawing
   - (e) 140-0216200-01 Fab Drawing
   - (f) 150-0216200-01 Schematic
   - (g) 160-0216200-01 Film
   - (h) 170-0216200-01 BOM

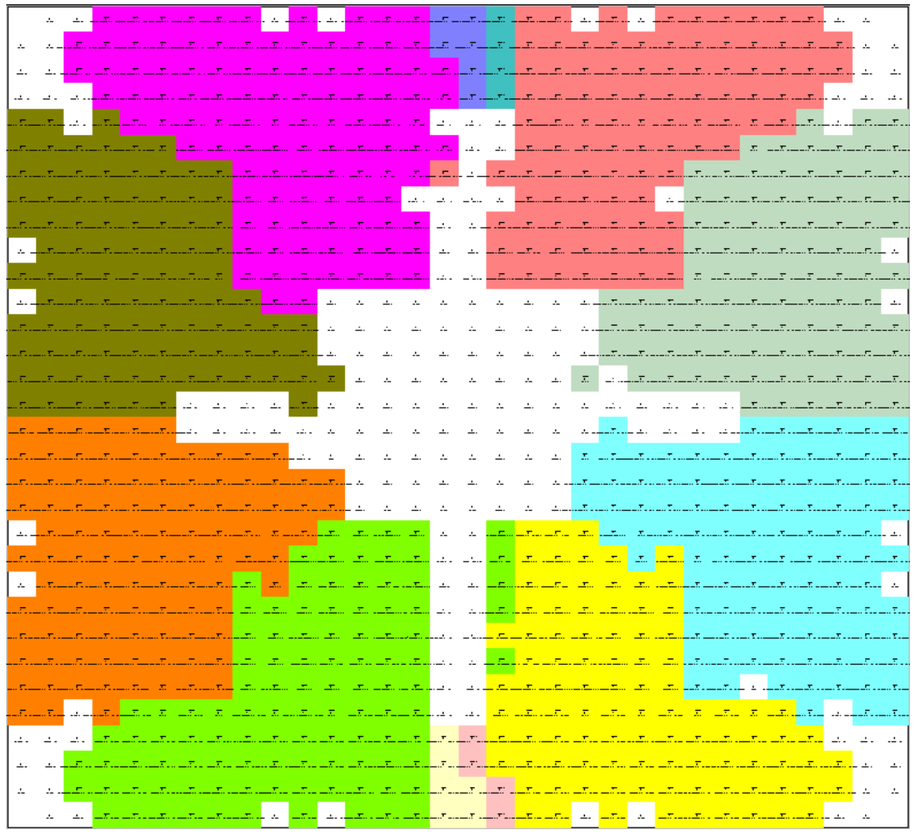
506 Parts, 50 Library Parts, 846 Nets, 3967 Pins

REV	DATE	PAGES	DESCRIPTION
A	12/02/2002	All	Changed to Rev A, first fabricated PCB revision.
B	02/12/2003	10, 13-14, 16-18	Modified J8/J9 symbols to add chamfer, Changed J13 symbol TX/RX naming, Pulled down LAN_ADSn & LAN_LCLK, Labelled RS-232 RX/TX LEDs, Modified 2.5V Regulator Circuit, Changed B1/B6 VCCIO select fuses to jumpers, Separated CONF_DONEn LED signal from CONF_DONE config signal, Changed C1/C2 to 47uF.

Stratix Package Top View

BANK 4
VCCIO = 2.5V
DDR SDRAM DATA LANES 0, 1, 2, 3
DDR SDRAM ADDRESS, PARITY BITS

BANK 3
VCCIO = 2.5V
DDR SDRAM DATA LANES 4, 5, 6, 7
DDR SDRAM ADDRESS, MASK BITS



BANK 5
VCCIO = 3.3V
10/100 MAC/PHY
RS-232 SIGNALS

BANK 2
VCCIO = 3.3V
MICTOR, LCD HEADER
PUSHBUTTONS
SANTA CRUZ DAUGHTERCARD

BANK 6
VCCIO = 2.5V -or- 3.3V
SAMTEC QTE-060
EDGE CONNECTOR
1x 8-BIT HIGH-SPEED PORT

BANK 1
VCCIO = 2.5V -or- 3.3V
SAMTEC QTE-080
TOP/BOT CONNECTORS
2x 8-BIT HIGH-SPEED PORTS

BANK 7
VCCIO = 3.3V
PCI SIGNALS
USER DIPSWITCH

BANK 8
VCCIO = 3.3V
PCI SIGNALS
FLASH ADDRESS, DATA
USER LEDS

PAGE	DESCRIPTION
1	Title, Notes, Revision History
2	Primary PCI
3	PCI Voltage Limit Switches
4	PCI Voltage Switch Bypass Resistors
5	Stratix Bank 7, 8, LEDs
6	DDR SDRAM SO-DIMM
7	DDR-SDRAM Terminations
8	Stratix Bank 2, 5
9	Stratix Bank 3, 4
10	Bank 1 HSDI Top/Bottom Connectors
11	Bank 1 Debug, Bank 6 HSDI Connector
12	Stratix Bank 1, 6
13	10/100 Ethernet Interface
14	Santa Cruz Card, RS-232, LCD Header
15	Clocking, JTAG Bypass Jumper
16	Power
17	CPLD, Flash, Board-Specific DIP Switches
18	Decoupling
19	-
20	-
21	-
22	-
23	-
24	-
25	-

Analog Ground

Ground

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix PCI Development Board**

Size	Document Number	Rev
B	150-0216200-01	B

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Primary PCI

Notes:

(1) Pin B38 = GND in PCI 2.2 and PCI-XCAP in PCI-X. It can be grounded or 10K pullup here.
(2) Pin A14 = 3.3Vauxin PCI2.2 but is unused for our board and PCI core.
(3) Pins B9 & B11 are power requirement strapping pins. We are strapped for maximum 25W power.
(4) Pin B49 is M66EN and is selectable 33 or 66MHz for PCI via DIPswitch
(5) PMEn pin A19 not connected. Board does not support Power Management features.

32-Bit Standard PCI Connector

J11A

3.3V	5.0V	-12V		+12V	5.0V	3.3V
B1	-12V		TRSTn	A1	
B2	TCK		+12V	A2	
B3	GND1		TMS	A3	
B4	TDO		TDI	A4	
B5	+5V1		+5V5	A5	
B6	+5V2		INTAn	A6	3,4 PCI_INTAn
B7	INTBn		INTCn	A7	
B8	INTDn		+5V6	A8	
B9	PRSNT1n		RESERVED3	A9	
B10	RESERVED1		VCCIO3	A10	
B11	PRSNT2n		RESERVED4	A11	
	3.3V Keyway				
B14	RESERVED2		RESERVED5	A14	
B15	GND2		RSTn	A15	3,4 PCI_RSTn
B16	CLK		VCCIO4	A16	
B17	GND3		GNTn	A17	3,4 PCI_GNTn
B18	REQn		GND11	A18	
B19	VCCIO1		PMEn	A19	
B20	AD(31)		AD(30)	A20	PCI_AD30
B21	AD(29)		+3.3V7	A21	
B22	GND4		AD(28)	A22	PCI_AD28
B23	AD(27)		AD(26)	A23	PCI_AD26
B24	AD(25)		GND12	A24	
B25	+3.3V1		AD(24)	A25	PCI_AD24
B26	CBEn(3)		IDSEL	A26	3,4 PCI_IDSEL
B27	AD(23)		+3.3V8	A27	
B28	GND5		AD(22)	A28	PCI_AD22
B29	AD(21)		AD(20)	A29	PCI_AD20
B30	AD(19)		GND13	A30	
B31	+3.3V2		AD(18)	A31	PCI_AD18
B32	AD(17)		AD(16)	A32	PCI_AD16
B33	CBEn(2)		+3.3V9	A33	
B34	GND6		FRAMEn	A34	3,4 PCI_FRAMEn
B35	IRDYn		GND14	A35	
B36	+3.3V3		TRDYn	A36	3,4 PCI_TRDYn
B37	DEVSELn		GND15	A37	
B38	PCIXCAP		STOPn	A38	3,4 PCI_STOPn
B39	LOCKn		+3.3V10	A39	
B40	PERRn		RESERVED6	A40	
B41	+3.3V4		RESERVED7	A41	
B42	SERRn		GND16	A42	
B43	+3.3V5		PAR	A43	3,4 PCI_PAR
B44	CBEn(1)		AD(15)	A44	3,4 PCI_AD15
B45	AD(14)		+3.3V11	A45	
B46	GND7		AD(13)	A46	PCI_AD13
B47	AD(12)		AD(11)	A47	PCI_AD11
B48	AD(10)		GND17	A48	
B49	M66EN		AD(9)	A49	PCI_AD9
	5V Keyway				
B52	AD(8)		CBEn(0)	A52	PCI_CBEn0
B53	AD(7)		+3.3V12	A53	
B54	+3.3V6		AD(6)	A54	PCI_AD6
B55	AD(5)		AD(4)	A55	PCI_AD4
B56	AD(3)		GND20	A56	
B57	GND10		AD(2)	A57	PCI_AD2
B58	AD(1)		AD(0)	A58	PCI_AD0
B59	VCCIO2		VCCIO5	A59	
B60	ACK64n		REQ64n	A60	3,4 PCI_REQ64n
B61	+5V3		+5V7	A61	
B62	+5V4		+5V8	A62	

PCI64_CONN

PCI_CLK 3,4
PCI_REQn 3,4
PCI_IRDYn 3,4
PCI_DEVSELn 3,4
PCI_XCAP 17
PCI_LOCKn 3,4
PCI_PERRn 3,4
PCI_SERRn 3,4
PCI_M66EN 17
PCI_ACK64n 3,4

3,4 PCI_AD[63..0]
3,4 PCI_CBEn[7..0]

64-bit Extensions

J11B

	B63	RESERVED8	GND29	A63	
	B64	GND21	CBEn(7)	A64	PCI_CBEn7
PCI_CBEn6	B65	CBEn(6)	CBEn(5)	A65	PCI_CBEn5
PCI_CBEn4	B66	CBEn(4)	VCCIO9	A66	
	B67	GND22	PAR64	A67	3,4 PCI_PAR64
PCI_AD63	B68	AD(63)	AD(62)	A68	PCI_AD62
PCI_AD61	B69	AD(61)	GND30	A69	
	B70	VCCIO6	AD(60)	A70	PCI_AD60
PCI_AD59	B71	AD(59)	AD(58)	A71	PCI_AD58
PCI_AD57	B72	AD(57)	GND31	A72	
	B73	GND23	AD(56)	A73	PCI_AD56
PCI_AD55	B74	AD(55)	AD(54)	A74	PCI_AD54
PCI_AD53	B75	AD(53)	VCCIO10	A75	
	B76	GND24	AD(52)	A76	PCI_AD52
PCI_AD51	B77	AD(51)	AD(50)	A77	PCI_AD50
PCI_AD49	B78	AD(49)	GND32	A78	
	B79	VCCIO7	AD(48)	A79	PCI_AD48
PCI_AD47	B80	AD(47)	AD(46)	A80	PCI_AD46
PCI_AD45	B81	AD(45)	GND33	A81	
	B82	GND25	AD(44)	A82	PCI_AD44
PCI_AD43	B83	AD(43)	AD(42)	A83	PCI_AD42
PCI_AD41	B84	AD(41)	VCCIO11	A84	
	B85	GND26	AD(40)	A85	PCI_AD40
PCI_AD39	B86	AD(39)	AD(38)	A86	PCI_AD38
PCI_AD37	B87	AD(37)	GND34	A87	
	B88	VCCIO8	AD(36)	A88	PCI_AD36
PCI_AD35	B89	AD(35)	AD(34)	A89	PCI_AD34
PCI_AD33	B90	AD(33)	GND35	A90	
	B91	GND27	AD(32)	A91	PCI_AD32
	B92	RESERVED9	RESERVED11	A92	
	B93	RESERVED10	GND36	A93	
	B94	GND28	RESERVED12	A94	

PCI64_CONN

PCI_M66EN
PCI_XCAP
C234 0.1uF X7R
C235 0.1uF X7R

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Title: **Stratix PCI Development Board**

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B	150-0216200-01	B

Date: Wednesday, February 12, 2003 Sheet 2 of 18

PCI Voltage Limit Switches

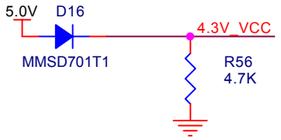
NOTE: Systems without a 5V power source must either:

(a) Remove these switches and populate the bypass resistor packs on the next page. (3.3V PCI signalling only)
(b) Connect the 4.3V VCC net to an acceptable voltage per the desired application (see manufacturer's datasheet for specs).

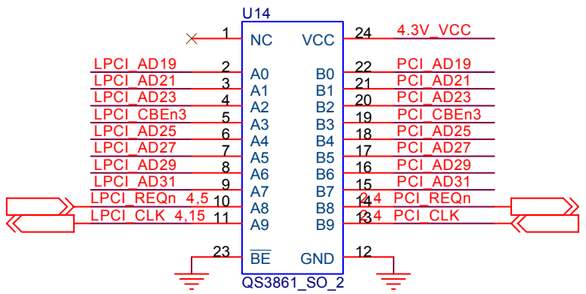
2,4 PCI_AD[63..0]
4,5 LPCI_AD[63..0]

2,4 PCI_CBEn[7..0]
4,5 LPCI_CBEn[7..0]

PCI Voltage Translation Switch Threshold (gate) Voltage



TOP #1



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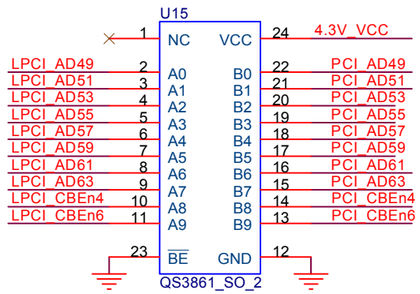
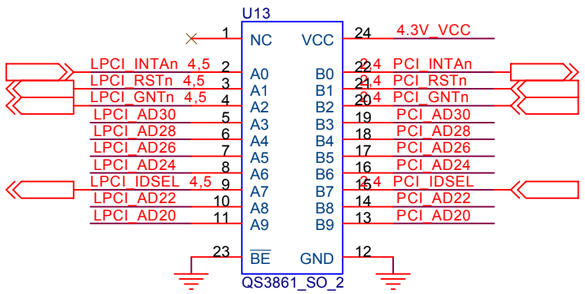
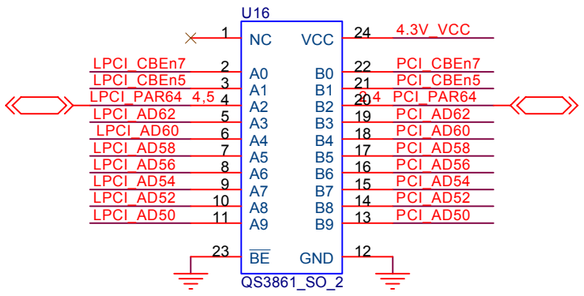


BOTTOM #1



BOTTOM #4

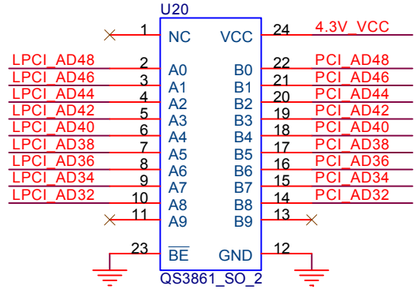


TOP #2

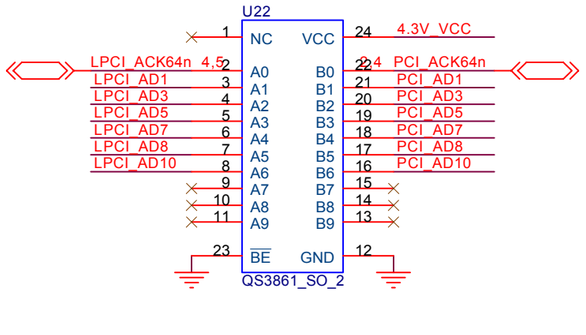
TOP #5

BOTTOM #2

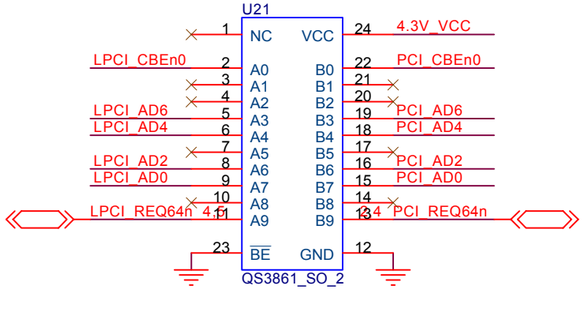
BOTTOM #5



TOP #3



BOTTOM #3



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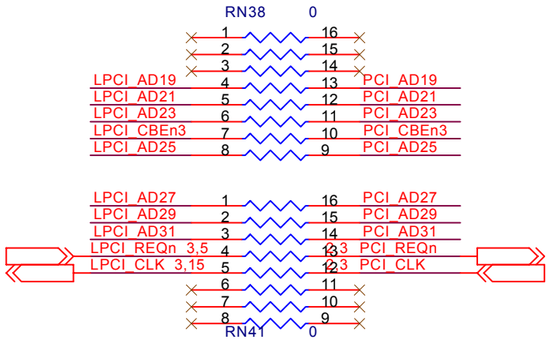
PCI Voltage Switch Bypass Resistors

NOTE: These resistor packs are not installed by default. They are ONLY installed when the proceeding page's FET switches are not installed (mutually exclusive).

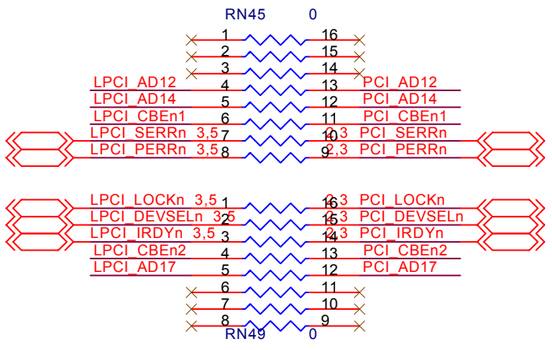
2,3 PCI_AD[63..0]
3,5 LPCI_AD[63..0]

2,3 PCI_CBEn[7..0]
3,5 LPCI_CBEn[7..0]

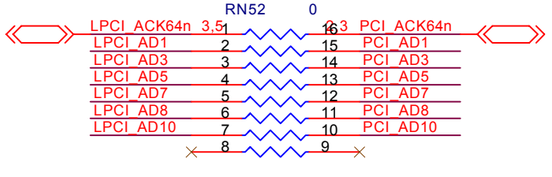
TOP #1



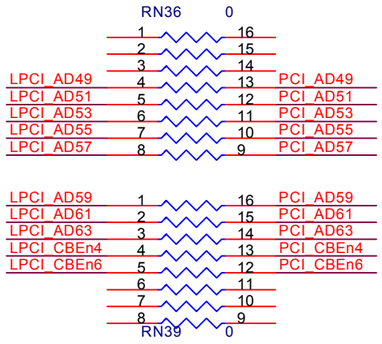
TOP #2



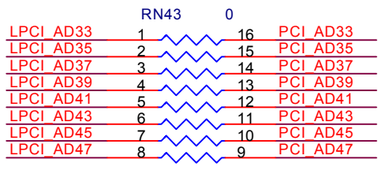
TOP #3



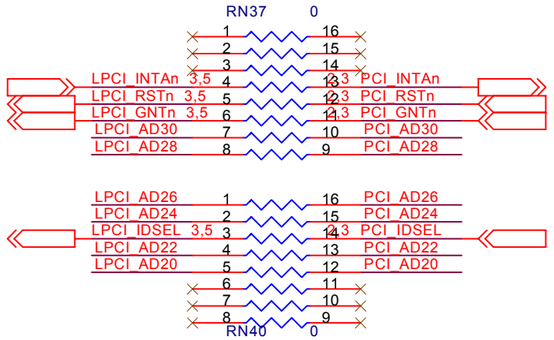
TOP #4



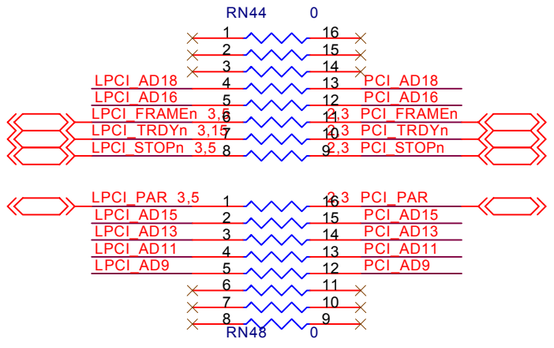
TOP #5



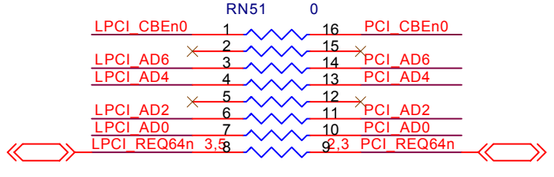
BOTTOM #1



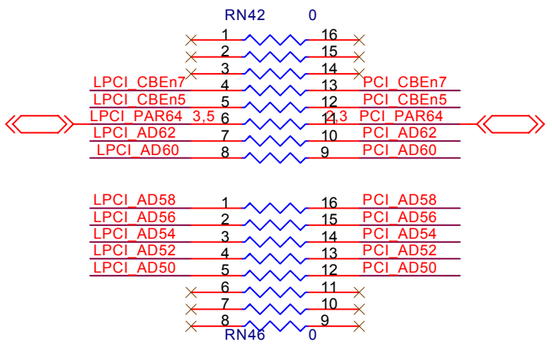
BOTTOM #2



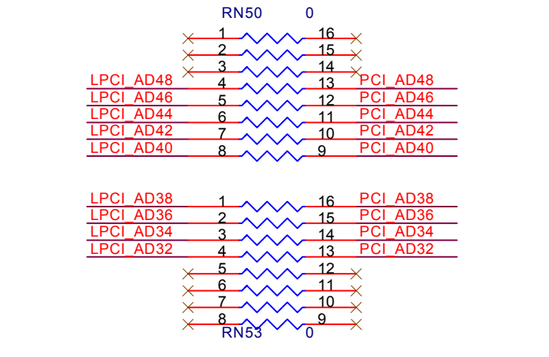
BOTTOM #3



BOTTOM #4



BOTTOM #5



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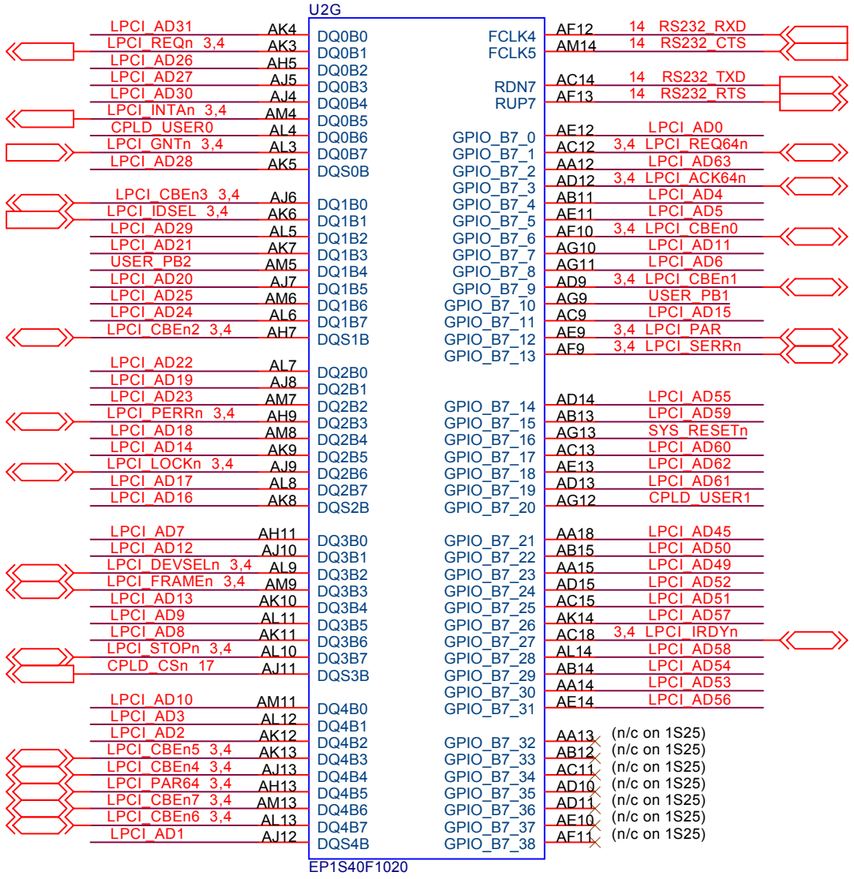
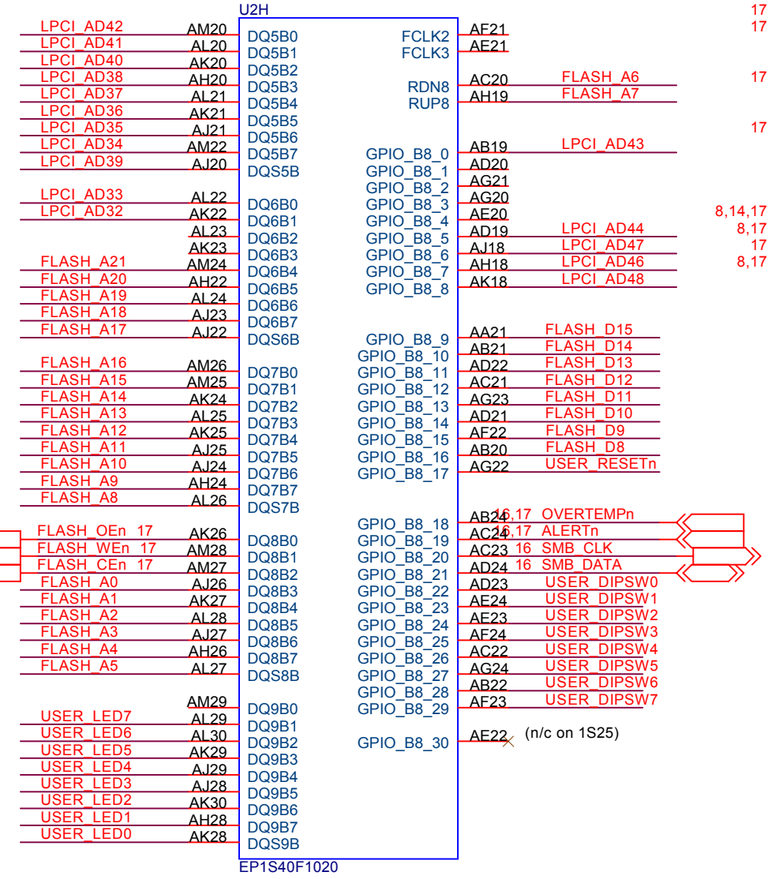
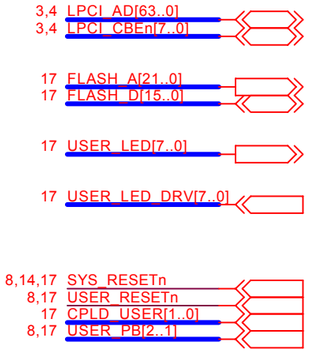
Stratix Bank 7, Bank 8, LEDs

BANK 7
(3.3V PCI & 3.3V LVTTL)

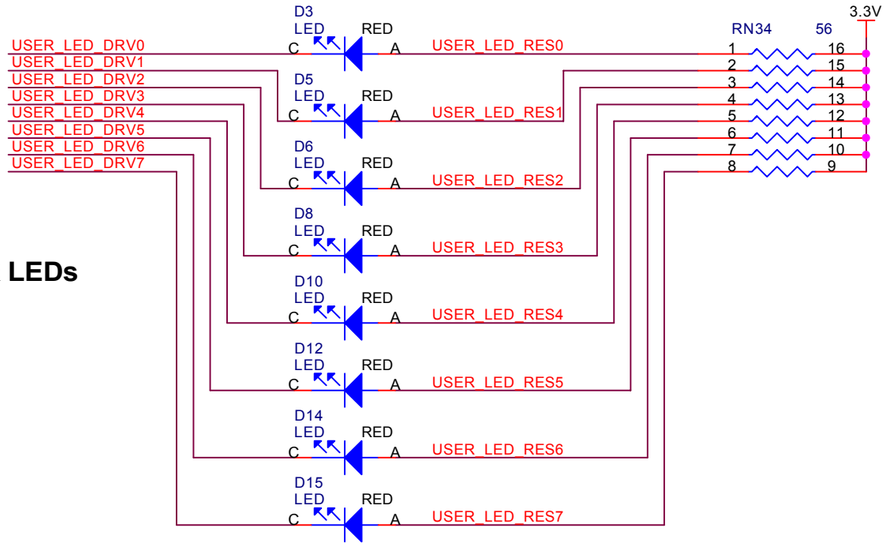


BANK 8
(3.3V PCI & 3.3V LVTTL)

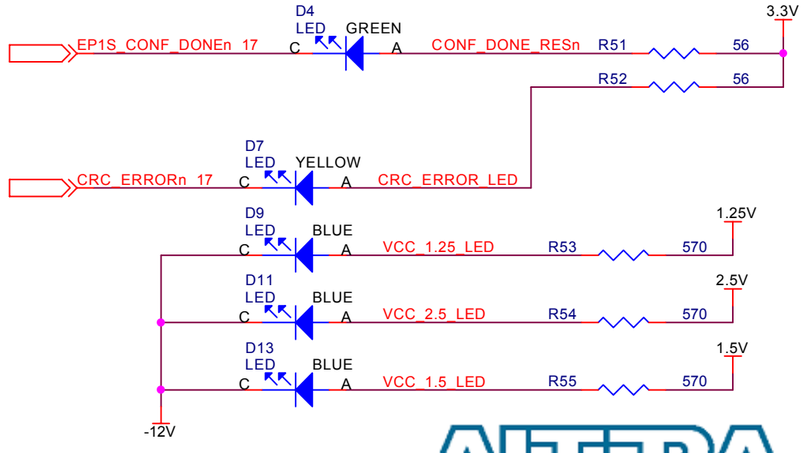




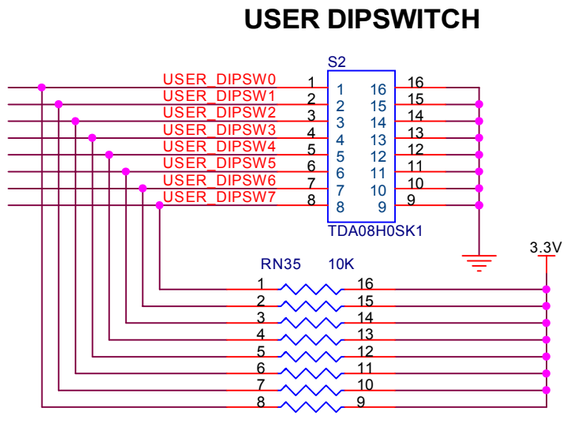
USER LEDs



POWER & CONFIG LEDs



USER DIPSWITCH



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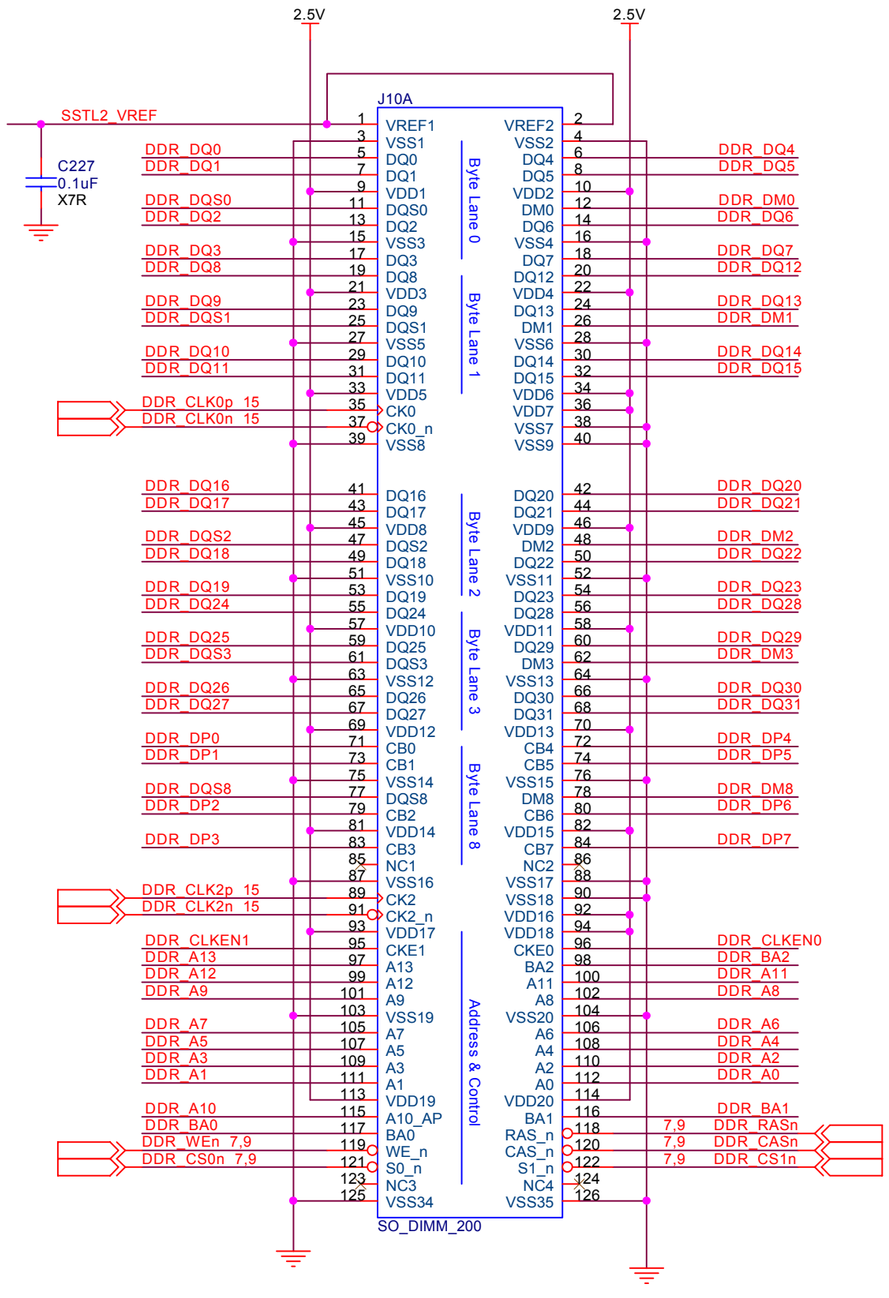
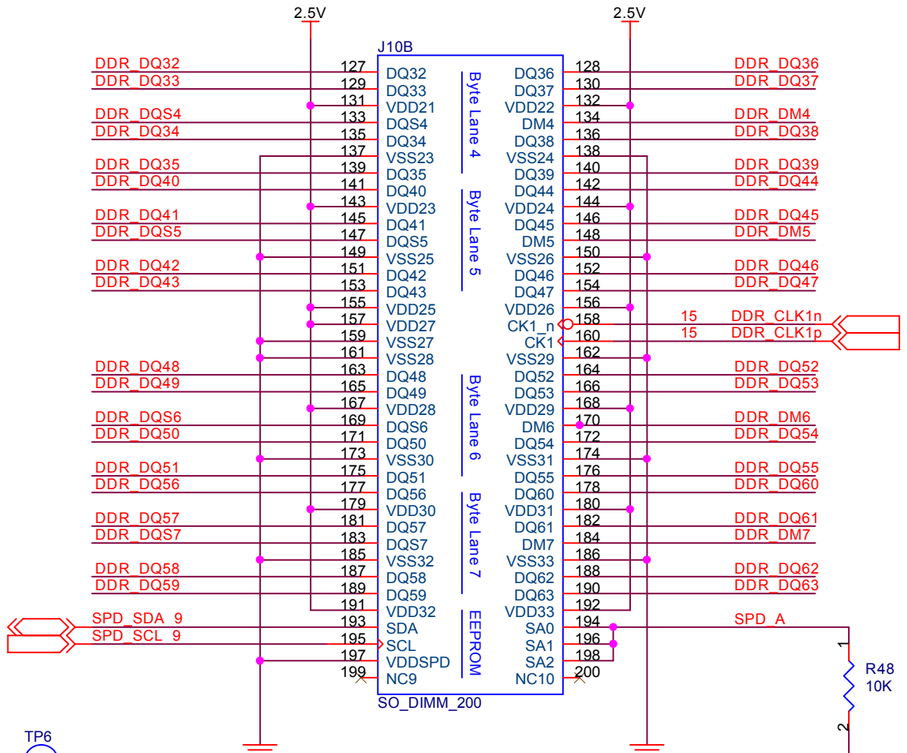
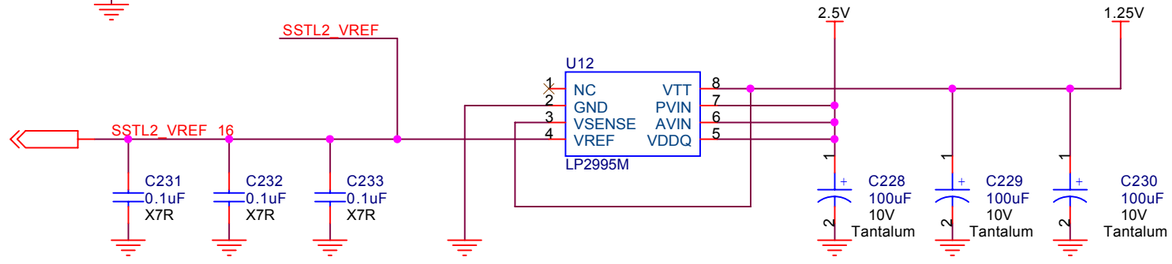
DDR SDRAM SO-DIMM







SSTL2 TERMINATION VOLTAGE REGULATOR

(1.5A / 3.0A Peak)

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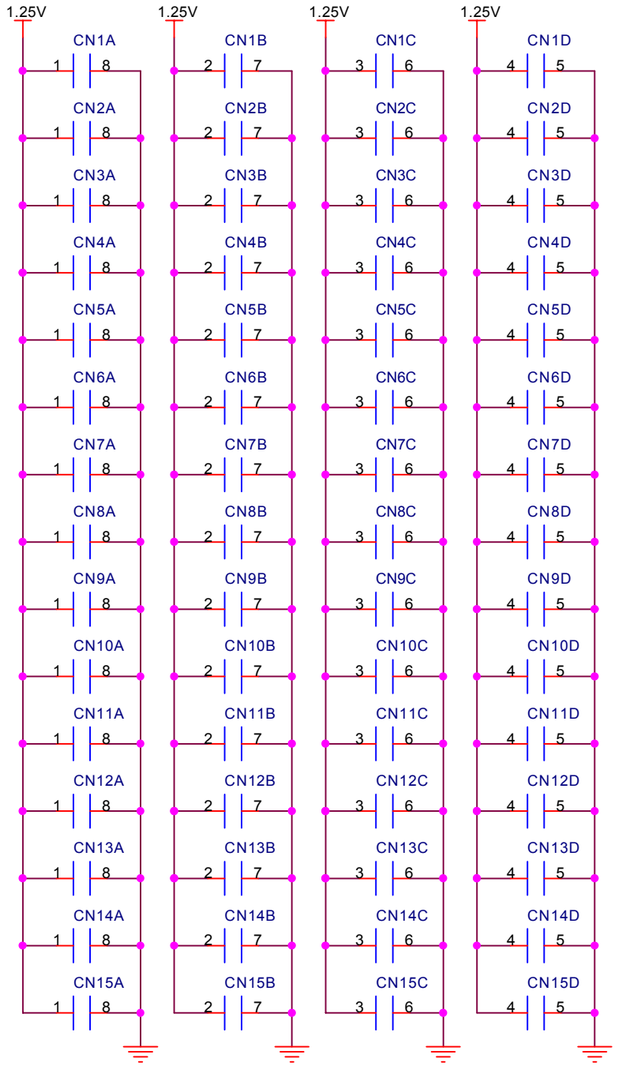
DDR SDRAM TERMINATIONS

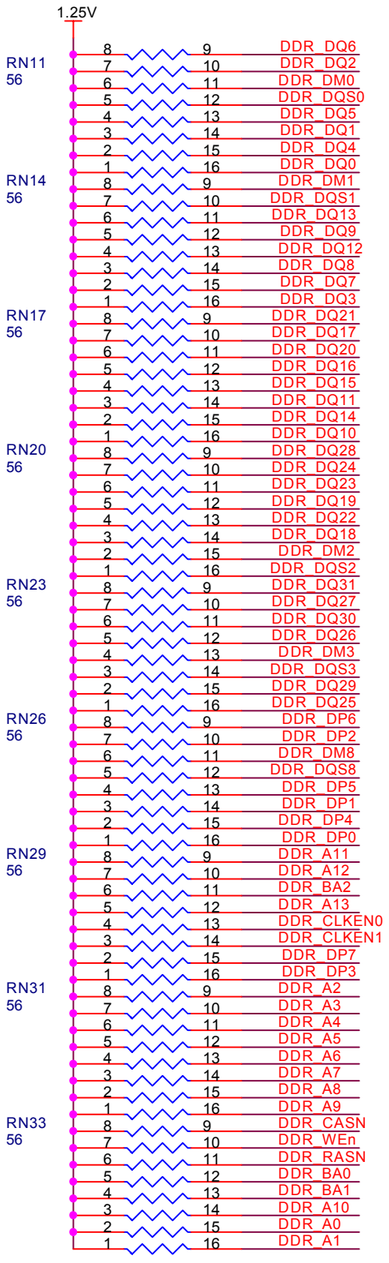
FLY-BY TERMINATION BYPASSING CAPS



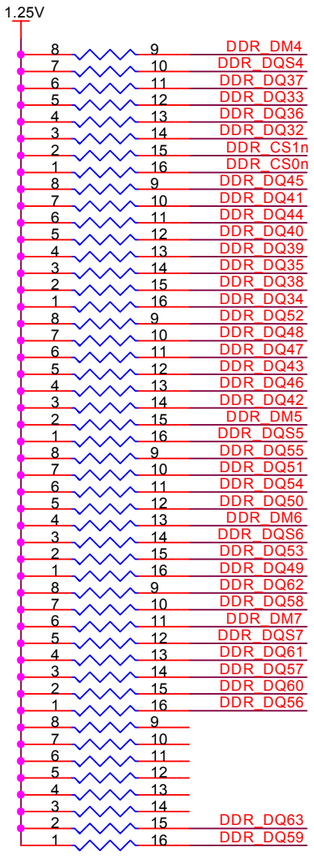
NOTE: THE FOLLOWING 0.1uF BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 56 OHM PULL UP RESISTOR.

NOTE: PLACE ONE QUAD CAPACITOR NETWORK AS CLOSE AS POSSIBLE TO ONE ROCTAL RESISTOR PACK.

FLY-BY TERMINATION RESISTORS



FLY-BY TERMINATION RESISTORS



NOTE: ALL OF THE 56 OHM PULL UP RESISTORS MUST BE PLACED AFTER THE SODIMM (i.e. AFTER THE CONNECTOR) AND AS CLOSE AS POSSIBLE TO THE SODIMM.

6,9 DDR_CS0n
6,9 DDR_CS1n
6,9 DDR_WEn
6,9 DDR_CLKEN0
6,9 DDR_CLKEN1
6,9 DDR_RASn
6,9 DDR_CASn
6,9 DDR_BA[2..0]
6,9 DDR_DM[8..0]
6,9 DDR_A[13..0]
6,9 DDR_DQS[8..0]
6,9 DDR_DP[7..0]
6,9 DDR_DQ[63..0]

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Stratix Bank 2, Bank 5, Buttons

BANK 5
(3.3V LVTTL)

U2E

(n/c on 1S25)	F5	DIFFIO_RX45n	DIFFIO_TX45n	G7	(n/c on 1S25)
(n/c on 1S25)	E4	DIFFIO_RX45p	DIFFIO_TX45p	G8	(n/c on 1S25)
(n/c on 1S25)	E2	DIFFIO_RX46n	DIFFIO_TX46n	G6	LAN_D2
(n/c on 1S25)	E1	DIFFIO_RX46p	DIFFIO_TX46p	G5	LAN_D3
(n/c on 1S25)	F3	DIFFIO_RX47n	DIFFIO_TX47n	H8	LAN_D4
(n/c on 1S25)	F4	DIFFIO_RX47p	DIFFIO_TX47p	H7	LAN_D5
LAN_D0	G3	DIFFIO_RX48n	DIFFIO_TX48n	H5	LAN_D6
LAN_BEn3	G4	DIFFIO_RX48p	DIFFIO_TX48p	H6	LAN_D7
LAN_BEn2	F1	DIFFIO_RX49n	DIFFIO_TX49n	J7	LAN_D8
LAN_BEn1	F2	DIFFIO_RX49p	DIFFIO_TX49p	J8	LAN_D9
LAN_BEn0	H3	DIFFIO_RX50n	DIFFIO_TX50n	J5	LAN_D10
LAN_A0	H4	DIFFIO_RX50p	DIFFIO_TX50p	J6	LAN_D11
LAN_A1	G1	DIFFIO_RX51n	DIFFIO_TX51n	K8	LAN_D12
LAN_A2	G2	DIFFIO_RX51p	DIFFIO_TX51p	K7	LAN_D13
LAN_A3	H1	DIFFIO_RX52n	DIFFIO_TX52n	K5	LAN_D14
LAN_A4	H2	DIFFIO_RX52p	DIFFIO_TX52p	K6	LAN_D15
LAN_A5	J3	DIFFIO_RX53n	DIFFIO_TX53n	L6	LAN_D16
LAN_A6	J4	DIFFIO_RX53p	DIFFIO_TX53p	L7	LAN_D17
LAN_A7	K4	DIFFIO_RX54n	DIFFIO_TX54n	M6	LAN_D18
LAN_A8	K3	DIFFIO_RX54p	DIFFIO_TX54p	M7	LAN_D19
LAN_A9	J2	DIFFIO_RX55n	DIFFIO_TX55n	M8	LAN_D20
LAN_A10	J1	DIFFIO_RX55p	DIFFIO_TX55p	M9	LAN_D21
LAN_A11	L1	DIFFIO_RX56n	DIFFIO_TX56n	N10	LAN_D22
LAN_A12	K2	DIFFIO_RX56p	DIFFIO_TX56p	N9	LAN_D23
LAN_A13	M4	DIFFIO_RX57n/RDN5	DIFFIO_TX57n	N5	LAN_D24
LAN_A14	M5	DIFFIO_RX57p/RUP5	DIFFIO_TX57p	N6	LAN_D25
LAN_RESET	L2	DIFFIO_RX58n	DIFFIO_TX58n	P9	LAN_D26
LAN_AEN	L3	DIFFIO_RX58p	DIFFIO_TX58p	P10	LAN_D27
LAN_IOCHRDY	M2	DIFFIO_RX59n	DIFFIO_TX59n	N7	LAN_D28
LAN_INTRQ0	M3	DIFFIO_RX59p	DIFFIO_TX59p	N8	LAN_D29
LAN_LDEVn	N3	DIFFIO_RX60n	DIFFIO_TX60n	P6	LAN_D30
LAN_IORn	N4	DIFFIO_RX60p	DIFFIO_TX60p	P5	LAN_D31
LAN_IOWn	N1	DIFFIO_RX61n	DIFFIO_TX61n	R10	B1_REQn
LAN_LOOPBACK	N2	DIFFIO_RX61p	DIFFIO_TX61p	R9	B1_RESETn
B1_USER_A0	P3	DIFFIO_RX62n	DIFFIO_TX62n	R5	B1_SYS_RESETn
B1_USER_A1	P4	DIFFIO_RX62p	DIFFIO_TX62p	R6	B1_PWROK
B1_USER_B0	P1	DIFFIO_RX63n	DIFFIO_TX63n	P7	B1_STOPn
B1_USER_B1	P2	DIFFIO_RX63p	DIFFIO_TX63p	P8	B1_SMBDAT
B1_USER_C0	R3	DIFFIO_RX64n	DIFFIO_TX64n	R7	B1_SMBCLK
B1_USER_C1	R4	DIFFIO_RX64p	DIFFIO_TX64p	R8	LAN_D1
B1_USER_D0	R1	DIFFIO_RX65n	DIFFIO_TX65n	P11	(n/c on 1S25)
B1_USER_D1	R2	DIFFIO_RX65p	DIFFIO_TX65p	N11	(n/c on 1S25)
B1_USER_E0	T2	DIFFIO_RX66n	DIFFIO_TX66n	T11	(n/c on 1S25)
B1_USER_E1	T1	DIFFIO_RX66p	DIFFIO_TX66p	R11	(n/c on 1S25)

EP1S40F1020

BANK 2
(3.3V LVTTL)

U2B

SCRUZ_IO0	T31	DIFFIO_RX23n	DIFFIO_TX23n	P22	(n/c on 1S25)
SCRUZ_IO1	T32	DIFFIO_RX23p	DIFFIO_TX23p	N22	(n/c on 1S25)
SCRUZ_IO2	R29	DIFFIO_RX24n	DIFFIO_TX24n	M22	(n/c on 1S25)
MICTOR_DO15	R30	DIFFIO_RX24p	DIFFIO_TX24p	M23	(n/c on 1S25)
MICTOR_DO14	R31	DIFFIO_RX25n	DIFFIO_TX25n	R26	SCRUZ_IO3
MICTOR_DO13	R32	DIFFIO_RX25p	DIFFIO_TX25p	R25	SCRUZ_IO4
MICTOR_DO12	P32	DIFFIO_RX26n	DIFFIO_TX26n	R24	SCRUZ_IO5
MICTOR_DO11	P31	DIFFIO_RX26p	DIFFIO_TX26p	R23	SCRUZ_IO6
MICTOR_DO10	P30	DIFFIO_RX27n	DIFFIO_TX27n	P26	SCRUZ_IO7
MICTOR_DO9	P29	DIFFIO_RX27p	DIFFIO_TX27p	P25	SCRUZ_IO8
MICTOR_DO8	N32	DIFFIO_RX28n	DIFFIO_TX28n	R27	SCRUZ_IO9
MICTOR_DO7	N31	DIFFIO_RX28p	DIFFIO_TX28p	R28	SCRUZ_IO10
MICTOR_DO6	N30	DIFFIO_RX29n	DIFFIO_TX29n	P27	SCRUZ_IO11
MICTOR_DO5	N29	DIFFIO_RX29p	DIFFIO_TX29p	P28	SCRUZ_IO12
MICTOR_DO4	M30	DIFFIO_RX30n	DIFFIO_TX30n	N26	SCRUZ_IO13
MICTOR_DO3	M31	DIFFIO_RX30p	DIFFIO_TX30p	N25	SCRUZ_IO14
MICTOR_DO2	L31	DIFFIO_RX31n	DIFFIO_TX31n	P24	SCRUZ_IO15
MICTOR_DO1	L30	DIFFIO_RX31p	DIFFIO_TX31p	P23	SCRUZ_IO16
MICTOR_DO0	M29	DIFFIO_RX32n/RDN2	DIFFIO_TX32n	N28	SCRUZ_IO17
MICTOR_DE15	M28	DIFFIO_RX32p/RUP2	DIFFIO_TX32p	N27	SCRUZ_IO18
MICTOR_DE14	L32	DIFFIO_RX33n	DIFFIO_TX33n	N23	SCRUZ_IO19
MICTOR_DE13	K31	DIFFIO_RX33p	DIFFIO_TX33p	N24	SCRUZ_IO20
MICTOR_DE12	J31	DIFFIO_RX34n	DIFFIO_TX34n	M25	SCRUZ_IO21
MICTOR_DE11	J32	DIFFIO_RX34p	DIFFIO_TX34p	M24	SCRUZ_IO22
MICTOR_DE10	K29	DIFFIO_RX35n	DIFFIO_TX35n	M27	SCRUZ_IO23
MICTOR_DE9	K30	DIFFIO_RX35p	DIFFIO_TX35p	M26	SCRUZ_IO24
MICTOR_DE8	J30	DIFFIO_RX36n	DIFFIO_TX36n	L26	SCRUZ_IO25
MICTOR_DE7	J29	DIFFIO_RX36p	DIFFIO_TX36p	L27	SCRUZ_IO26
MICTOR_DE6	H32	DIFFIO_RX37n	DIFFIO_TX37n	K25	SCRUZ_IO27
MICTOR_DE5	H31	DIFFIO_RX37p	DIFFIO_TX37p	K26	SCRUZ_IO28
MICTOR_DE4	G32	DIFFIO_RX38n	DIFFIO_TX38n	K27	SCRUZ_IO29
MICTOR_DE3	G31	DIFFIO_RX38p	DIFFIO_TX38p	K28	SCRUZ_IO30
MICTOR_DE2	H29	DIFFIO_RX39n	DIFFIO_TX39n	J26	SCRUZ_IO31
MICTOR_DE1	H30	DIFFIO_RX39p	DIFFIO_TX39p	J25	SCRUZ_IO32
MICTOR_DE0	G30	DIFFIO_RX40n	DIFFIO_TX40n	H26	SCRUZ_IO33
MICTOR_CLKO	G29	DIFFIO_RX40p	DIFFIO_TX40p	H25	SCRUZ_IO34
MICTOR_CLKE	F32	DIFFIO_RX41n	DIFFIO_TX41n	J28	SCRUZ_IO35
(n/c on 1S25)	F31	DIFFIO_RX41p	DIFFIO_TX41p	J27	SCRUZ_IO36
(n/c on 1S25)	F30	DIFFIO_RX42n	DIFFIO_TX42n	H27	SCRUZ_IO37
(n/c on 1S25)	F29	DIFFIO_RX42p	DIFFIO_TX42p	H28	SCRUZ_IO38
(n/c on 1S25)	E31	DIFFIO_RX43n	DIFFIO_TX43n	G27	SCRUZ_IO39
(n/c on 1S25)	E32	DIFFIO_RX43p	DIFFIO_TX43p	G28	14 SCRUZ_CARDSELn
(n/c on 1S25)	F28	DIFFIO_RX44n	DIFFIO_TX44n	G26	(n/c on 1S25)
(n/c on 1S25)	E29	DIFFIO_RX44p	DIFFIO_TX44p	G25	(n/c on 1S25)

EP1S40F1020

14 SCRUZ_IO[39..0]
13 LAN_D[31..0]
13 LAN_A[14..0]
13 LAN_BEn[3..0]
13 LAN_RESET
13 LAN_INTRQ0
13 LAN_AEN
13 LAN_IORn
13 LAN_IOWn
13 LAN_IOCHRDY
13 LAN_LDEVn
13 LAN_LOOPBACK

HSDI CONTROL SIGNALS (TTL)

10 B1_STOPn
10 B1_REQn
10,17 B1_RESETn
10,17 B1_PWROK
10 B1_SYS_RESETn
10 B1_SMBCLK
10 B1_SMBDAT

HSDI USER DEFINED SIGNALS

10 B1_USER_A[1..0]
10 B1_USER_B[1..0]
10 B1_USER_C[1..0]
10 B1_USER_D[1..0]
10 B1_USER_E[1..0]

14 MICTOR_DE[15..0]
14 MICTOR_DO[15..0]
14 MICTOR_CLKO
14 MICTOR_CLKE

5,17 USER_PB[2..1]
5,14,17 SYS_RESETn
5,17 USER_RESETn
5,17 CPLD_USER[1..0]

3.3V
2.5V
RN9 10K

1	16	SYS_RESETn	
2	15	USER_RESETn	
3	14	USER_PB2	
4	13	USER_PB1	
5	12		
6	11	B1_REQn	
7	10	B1_RESETn	
8	9	B1_SYS_RESETn	

PB1 PB2 PB3 PB4

USER_RESETn — PB1 — PB2 — USER_PB1

Button is intended to reset internal Stratix logic (analagous to a soft reset)

Two user-defined pushbuttons for any use.

SYS_RESETn — PB3 — PB4 — USER_PB2

Button resets board and re-loads Stratix device from flash memory.

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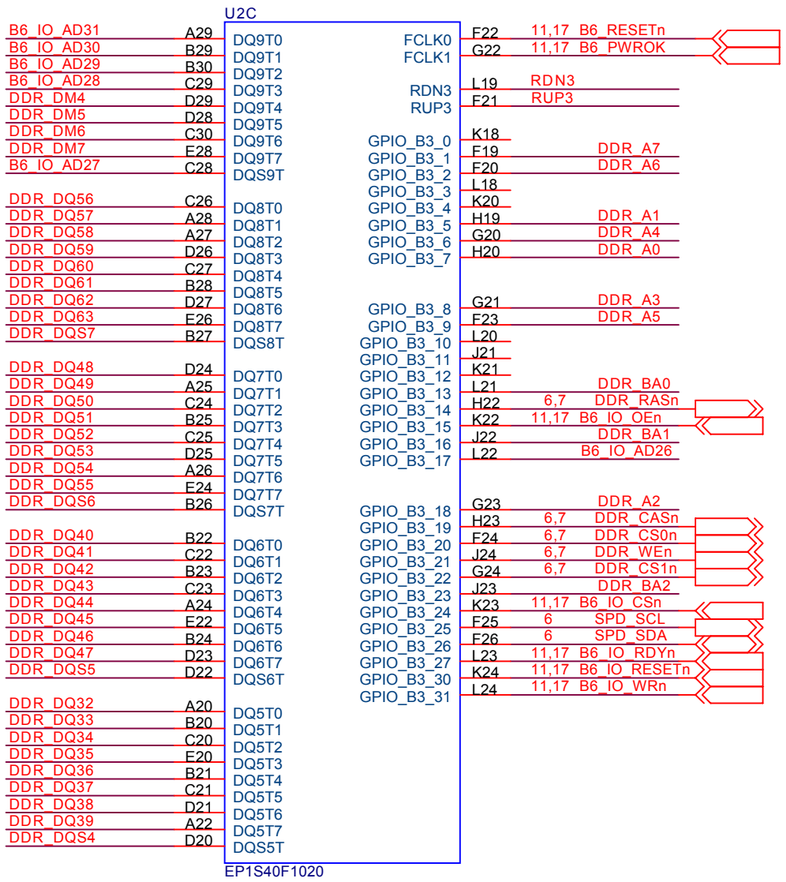
Stratix Bank 3, Bank 4

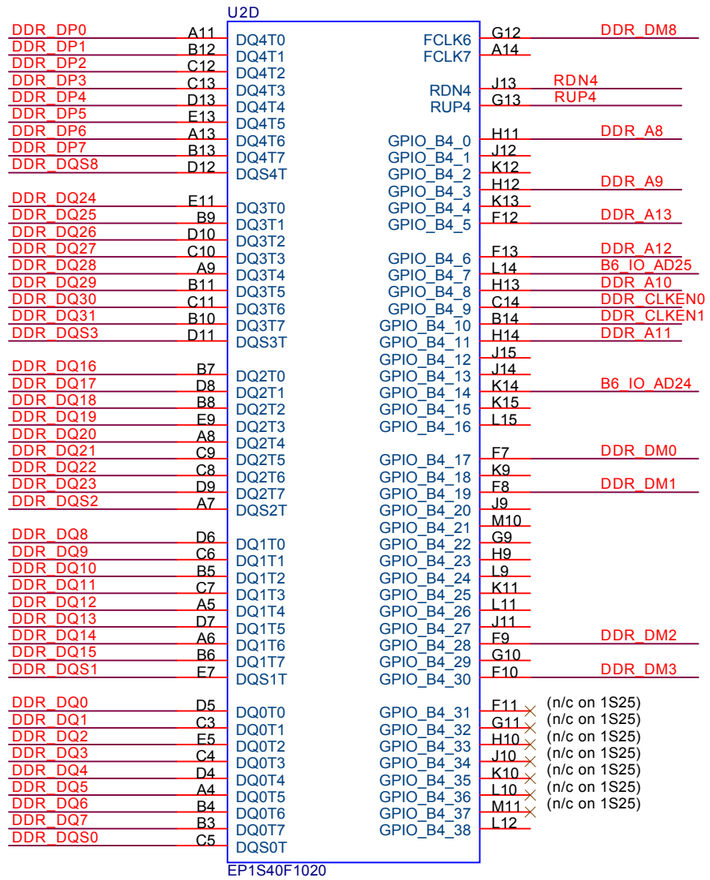
Bank 3

(2.5V SSTL-2 / 2.5V LVTTL)



Bank 4

(2.5V SSTL-2 / 2.5V LVTTL)



6,7 DDR_DQ[63..0]

6,7 DDR_DP[7..0]

6,7 DDR_A[13..0]

6,7 DDR_BA[2..0]

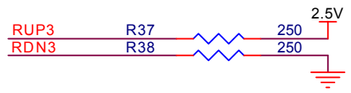
6,7 DDR_DM[8..0]

6,7 DDR_DQS[8..0]

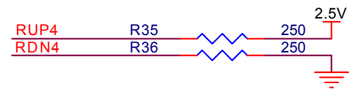
6,7 DDR_CLKEN[1..0]

12 B6_IO_AD[31..24]

On-chip termination biasing resistors



On-chip termination biasing resistors



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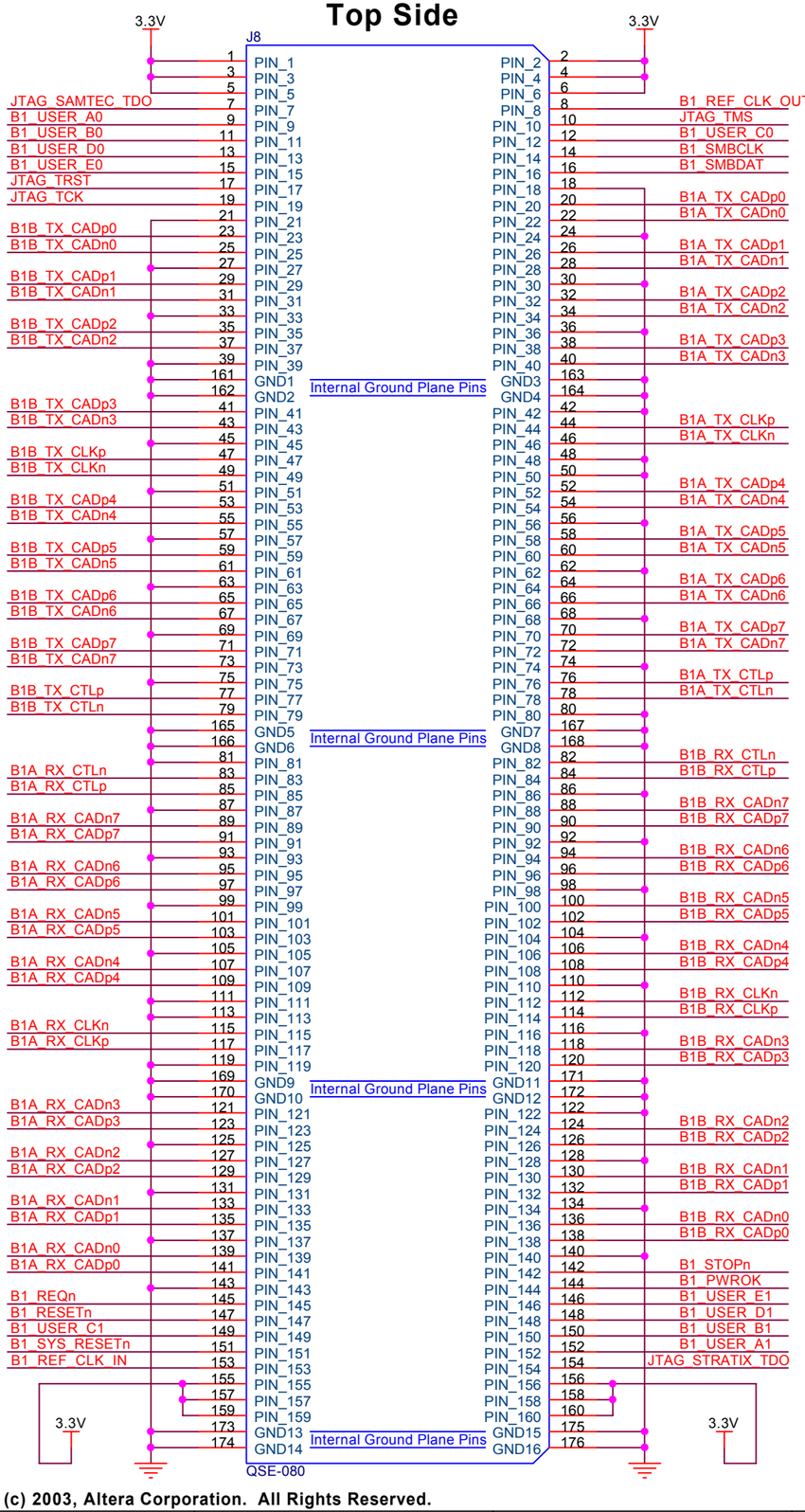
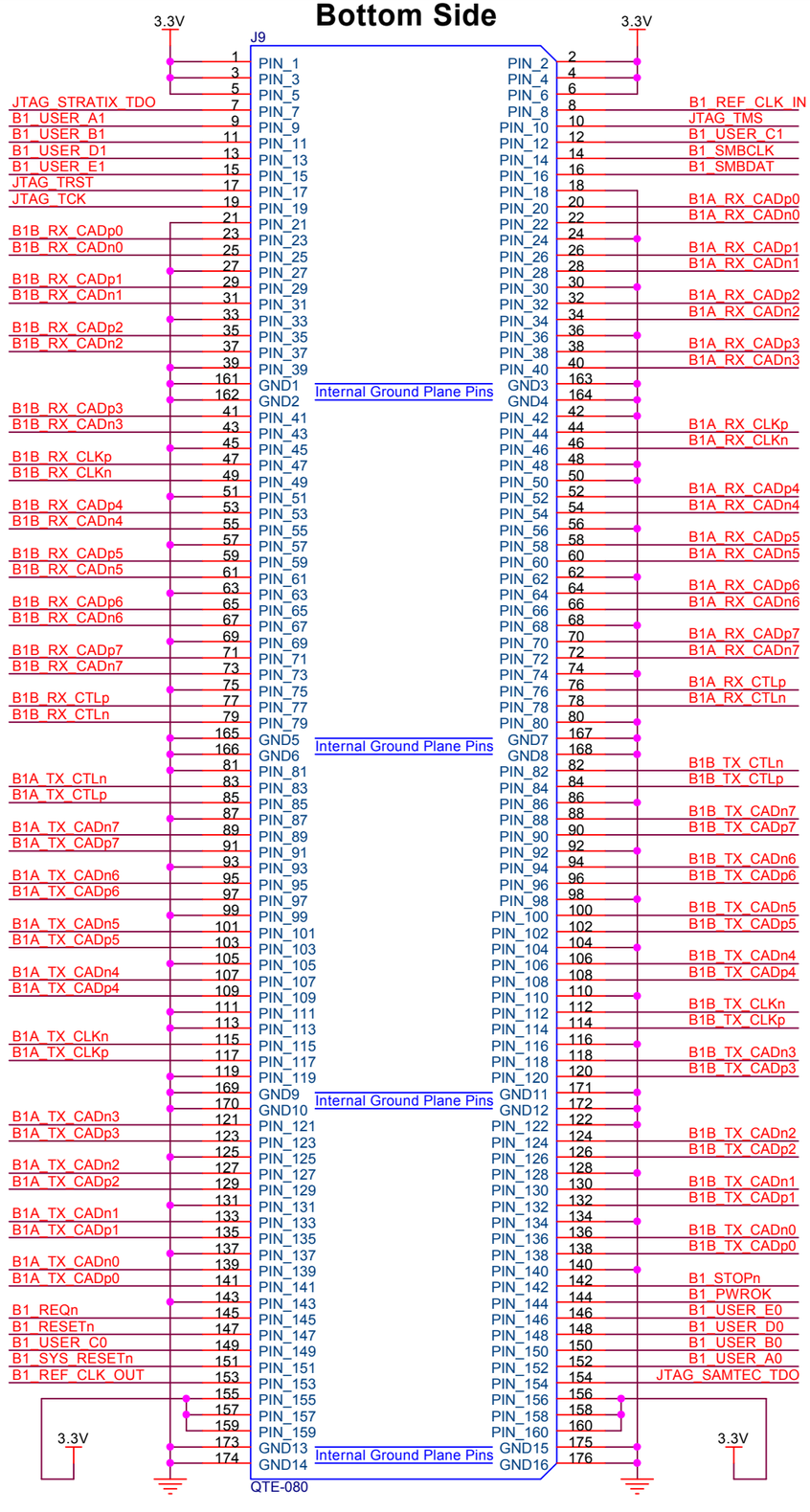
Top Side



Bottom Side



Bank 1 HSDI Connectors

HSDI BANK 1A TX INTERFACE

12 B1A_TX_CLKp
12 B1A_TX_CLKn
12 B1A_TX_CTLp
12 B1A_TX_CTLn

12 B1A_TX_CADp[7..0]
12 B1A_TX_CADn[7..0]

HSDI BANK 1A RX INTERFACE

11,15 B1A_RX_CLKp
11,15 B1A_RX_CLKn
11,12 B1A_RX_CTLp
11,12 B1A_RX_CTLn

11,12 B1A_RX_CADp[7..0]
11,12 B1A_RX_CADn[7..0]

HSDI BANK 1B TX INTERFACE

12 B1B_TX_CLKp
12 B1B_TX_CLKn
12 B1B_TX_CTLp
12 B1B_TX_CTLn

12 B1B_TX_CADp[7..0]
12 B1B_TX_CADn[7..0]

HSDI BANK 1B RX INTERFACE

15 B1B_RX_CLKp
15 B1B_RX_CLKn
12 B1B_RX_CTLp
12 B1B_RX_CTLn

12 B1B_RX_CADp[7..0]
12 B1B_RX_CADn[7..0]

OTHER HSDI CONTROL SIGNALS

15 B1_REF_CLK_IN
15 B1_REF_CLK_OUT
8 B1_STOPn
8 B1_REQn
8 B1_SYS_RESETn
8,17 B1_RESETn
8,17 B1_PWROK
8 B1_SMBCLK
8 B1_SMBDAT

HSDI JTAG INTERFACE

17 JTAG_TMS
15 JTAG_SAMTEC_TDO
17 JTAG_TRSTn
17 JTAG_TCK
15,17 JTAG_STRATIX_TDO

HSDI USER SIGNALS

8 B1_USER_A[1..0]
8 B1_USER_B[1..0]
8 B1_USER_C[1..0]
8 B1_USER_D[1..0]
8 B1_USER_E[1..0]

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Bank 1 Debug, Bank 6 HSDI Connector

PLACE 226 OHM RESISTORS AS CLOSE TO THE DATAPATH TAP AS POSSIBLE (MINIMIZE THE STUB LENGTH)

B1A_RX_CADn0	R57	226	SAMTEC_RX_CADn0	7	D0N	GND1	1
B1A_RX_CADp0	R58	226	SAMTEC_RX_CADp0	8	D0P	GND2	2
B1A_RX_CADn1	R59	226	SAMTEC_RX_CADn1	11	D1N	GND3	5
B1A_RX_CADp1	R60	226	SAMTEC_RX_CADp1	12	D1P	GND4	6
B1A_RX_CADn2	R61	226	SAMTEC_RX_CADn2	15	D2N	GND5	9
B1A_RX_CADp2	R62	226	SAMTEC_RX_CADp2	16	D2P	GND6	10
B1A_RX_CADn3	R63	226	SAMTEC_RX_CADn3	19	D3N	GND7	13
B1A_RX_CADp3	R64	226	SAMTEC_RX_CADp3	20	D3P	GND8	14
B1A_RX_CADn4	R65	226	SAMTEC_RX_CADn4	23	D4N	GND9	17
B1A_RX_CADp4	R66	226	SAMTEC_RX_CADp4	24	D4P	GND10	18
B1A_RX_CADn5	R67	226	SAMTEC_RX_CADn5	27	D5N	GND11	21
B1A_RX_CADp5	R68	226	SAMTEC_RX_CADp5	28	D5P	GND12	22
B1A_RX_CADn6	R69	226	SAMTEC_RX_CADn6	31	D6N	GND13	25
B1A_RX_CADp6	R70	226	SAMTEC_RX_CADp6	32	D6P	GND14	26
B1A_RX_CADn7	R71	226	SAMTEC_RX_CADn7	35	D7N	GND15	29
B1A_RX_CADp7	R72	226	SAMTEC_RX_CADp7	36	D7P	GND16	30
				39	D8N	GND17	33
				40	D8P	GND18	34
				43	D9N	GND19	37
				44	D9P	GND20	38
				47	D10N	GND21	41
				48	D10P	GND22	42
				51	D11N	GND23	45
				52	D11P	GND24	46
				55	D12N	GND25	49
				56	D12P	GND26	50
				59	D13N	GND27	53
				60	D13P	GND28	54
				63	D14N	GND29	57
				64	D14P	GND30	58
B1A_RX_CTLn	R73	226	SAMTEC_RX_CTLn	67	D15N	GND31	61
B1A_RX_CTLp	R74	226	SAMTEC_RX_CTLp	68	D15P	GND32	62
B1A_RX_CLKn	R75	226	SAMTEC_RX_CLKn	79	CLKN	GND33	65
B1A_RX_CLKp	R76	226	SAMTEC_RX_CLKp	80	CLKP	GND34	66
				3	NC1	GND35	69
				4	NC2	GND36	70
				71	NC3	GND37	73
				72	NC4	GND38	74
				75	NC5	GND39	77
				76	NC6	GND40	78
				83	NC7	GND41	81
				84	NC8	GND42	82
				87	NC9	GND43	85
				88	NC10	GND44	86
				91	NC11	GND45	89
				92	NC12	GND46	90
				97	NC13	GND47	93
				98	NC14	GND48	94
				99	NC15	GND49	95
				100	NC16	GND50	96

J12

ASP-65067-01

PLACE THE 75 OHM RESISTORS AS CLOSE TO THE SAMTEC CONNECTOR TERMINATION PIN AS POSSIBLE.

SAMTEC_RX_CADn0	R77	75
SAMTEC_RX_CADp0	R78	75
SAMTEC_RX_CADn1	R79	75
SAMTEC_RX_CADp1	R80	75
SAMTEC_RX_CADn2	R81	75
SAMTEC_RX_CADp2	R82	75
SAMTEC_RX_CADn3	R83	75
SAMTEC_RX_CADp3	R84	75
SAMTEC_RX_CADn4	R85	75
SAMTEC_RX_CADp4	R86	75
SAMTEC_RX_CADn5	R87	75
SAMTEC_RX_CADp5	R88	75
SAMTEC_RX_CADn6	R89	75
SAMTEC_RX_CADp6	R90	75
SAMTEC_RX_CADn7	R91	75
SAMTEC_RX_CADp7	R92	75
SAMTEC_RX_CTLn	R93	75
SAMTEC_RX_CTLp	R94	75
SAMTEC_RX_CLKn	R95	75
SAMTEC_RX_CLKp	R96	75

Edge-Mount

J13

		1	VDD33_1
		3	VDD33_3
		5	VDDLDT_1
		7	GND1
		9	TCK
		11	TMS
		13	TDI
		15	TDO
		17	TRST_L
		19	SCL
		21	SDA
B6_RESETn 9,17		23	LDT_RESET_L
B6_PWROK 9,17		25	LDT_PWROK
		27	GND4
B6_RX_CTLn 12		29	LDT_TX_CTLn
B6_RX_CTLp 12		31	LDT_TX_CTLp
		33	GND6
B6_RX_CADn7		35	LDT_TX_CADn7
B6_RX_CADp7		37	LDT_TX_CADp7
		39	GND8
		41	GND10
B6_RX_CADn6		43	LDT_TX_CADn6
B6_RX_CADp6		45	LDT_TX_CADp6
		47	GND12
B6_RX_CADn5		49	LDT_TX_CADn5
B6_RX_CADp5		51	LDT_TX_CADp5
		53	GND14
B6_RX_CADn4		55	LDT_TX_CADn4
B6_RX_CADp4		57	LDT_TX_CADp4
		59	GND16
		61	GND18
B6_RX_CLKn 15		63	LDT_TX_CLKn
B6_RX_CLKp 15		65	LDT_TX_CLKp
		67	GND20
B6_RX_CADn3		69	LDT_TX_CADn3
B6_RX_CADp3		71	LDT_TX_CADp3
		73	GND22
B6_RX_CADn2		75	LDT_TX_CADn2
B6_RX_CADp2		77	LDT_TX_CADp2
		79	GND24
		81	GND26
B6_RX_CADn1		83	LDT_TX_CADn1
B6_RX_CADp1		85	LDT_TX_CADp1
		87	GND28
B6_RX_CADn0		89	LDT_TX_CADn0
B6_RX_CADp0		91	LDT_TX_CADp0
		93	GND30
		95	AD0
		97	AD1
		99	AD2
		101	AD3
		103	AD4
		105	AD5
		107	AD6
		109	AD7
		111	AD8
		113	GND32
		115	VDDLDT_3
		117	VDD33_5
		119	VDD33_7
		121	GND34
		123	GND36
		125	GND38
		127	GND40
		129	GND42
		131	GND44

		2	VDD33_2
		4	VDD33_4
		6	VDDLDT_2
		8	GND2
		10	CLK100
		12	GND3
		14	RDY
		16	OE_L
		18	WR_L
		20	CS_L0
		22	CS_L1
		24	INT
		26	RESET_L
		28	GND5
LDT_RX_CADp0		30	LDT_RX_CADp0
LDT_RX_CADn0		32	LDT_RX_CADn0
		34	GND7
LDT_RX_CADp1		36	LDT_RX_CADp1
LDT_RX_CADn1		38	LDT_RX_CADn1
		40	GND9
		42	GND11
LDT_RX_CADp2		44	LDT_RX_CADp2
LDT_RX_CADn2		46	LDT_RX_CADn2
		48	GND13
LDT_RX_CADp3		50	LDT_RX_CADp3
LDT_RX_CADn3		52	LDT_RX_CADn3
		54	GND15
LDT_RX_CLKp		56	LDT_RX_CLKp
LDT_RX_CLKn		58	LDT_RX_CLKn
		60	GND17
		62	GND19
LDT_RX_CADp4		64	LDT_RX_CADp4
LDT_RX_CADn4		66	LDT_RX_CADn4
		68	GND21
LDT_RX_CADp5		70	LDT_RX_CADp5
LDT_RX_CADn5		72	LDT_RX_CADn5
		74	GND23
LDT_RX_CADp6		76	LDT_RX_CADp6
LDT_RX_CADn6		78	LDT_RX_CADn6
		80	GND25
		82	GND27
LDT_RX_CADp7		84	LDT_RX_CADp7
LDT_RX_CADn7		86	LDT_RX_CADn7
		88	GND29
LDT_RX_CTLp		90	LDT_RX_CTLp
LDT_RX_CTLn		92	LDT_RX_CTLn
		94	GND31
		96	AD9
		98	AD24
		100	AD25
		102	AD26
		104	AD27
		106	AD28
		108	AD29
		110	AD30
		112	AD31
		114	GND33
		116	VDDLDT_4
		118	VDD33_6
		120	VDD33_8
		122	GND35
		124	GND37
		126	GND39
		128	GND41
		130	GND43
		132	GND45

3.3V

3.3V

3.3V

3.3V

B6_REF_CLK

B6_IO_RDYn
B6_IO_OEn
B6_IO_WRn
B6_IO_CSn

B6_IO_RESETn

B6_TX_CADp0
B6_TX_CADn0
B6_TX_CADp1
B6_TX_CADn1
B6_TX_CADp2
B6_TX_CADn2
B6_TX_CADp3
B6_TX_CADn3
B6_TX_CLKp
B6_TX_CLKn
B6_TX_CADp4
B6_TX_CADn4
B6_TX_CADp5
B6_TX_CADn5
B6_TX_CADp6
B6_TX_CADn6
B6_TX_CADp7
B6_TX_CADn7
B6_TX_CTLp
B6_TX_CTLn

B6_IO_AD24
B6_IO_AD25
B6_IO_AD26
B6_IO_AD27
B6_IO_AD28
B6_IO_AD29
B6_IO_AD30
B6_IO_AD31

12
12
12
12

QTE-060-EM

Internal Ground Plane Pins

PCB Solder-Side (Bottom)

Bank 6 Receive (Inputs to this board)

PCB Component-Side (Top)

Bank 6 Transmit (Outputs from this board)

BANK 1A HDSI DEBUG

10,12 B1A_RX_CADp[7..0]
10,12 B1A_RX_CADn[7..0]
10,15 B1A_RX_CLKp
10,15 B1A_RX_CLKn
10,12 B1A_RX_CTLp
10,12 B1A_RX_CTLn

BANK 6 HSDI

12 B6_RX_CADp[7..0]
12 B6_RX_CADn[7..0]
12 B6_TX_CADp[7..0]
12 B6_TX_CADn[7..0]

BANK 6 USER BUS

12 B6_IO_AD[31..24]

12 B6_REF25_CLK

R254
0

B6_REF_CLK

R255
0

12 B6_REF60_CLK

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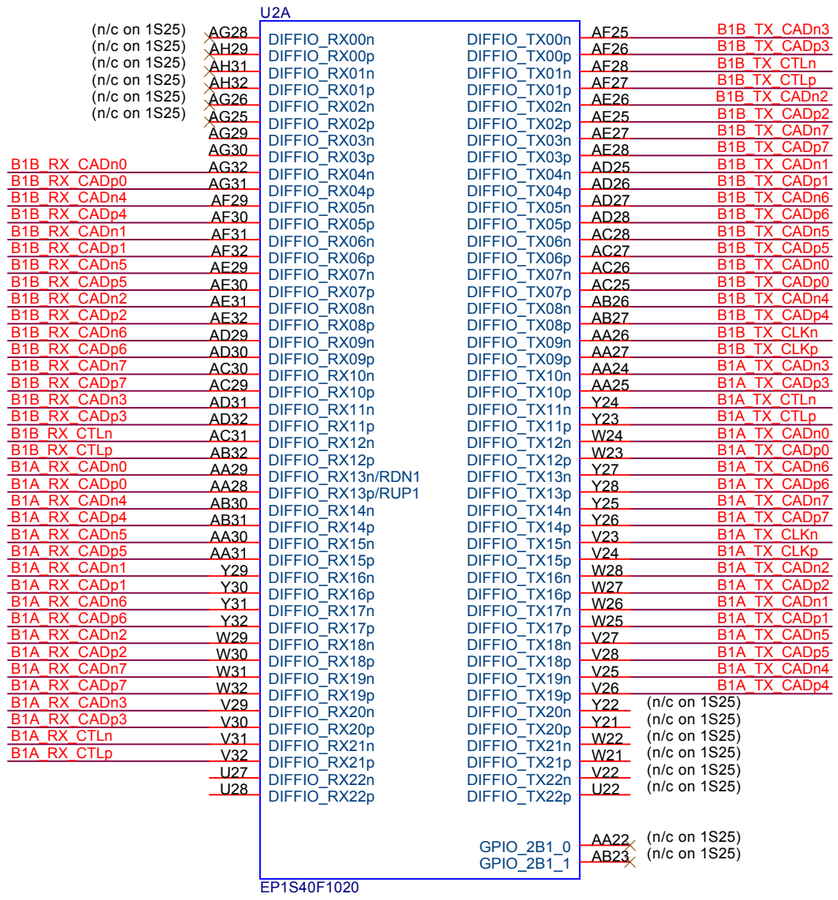
Stratix Bank 1, Bank 6

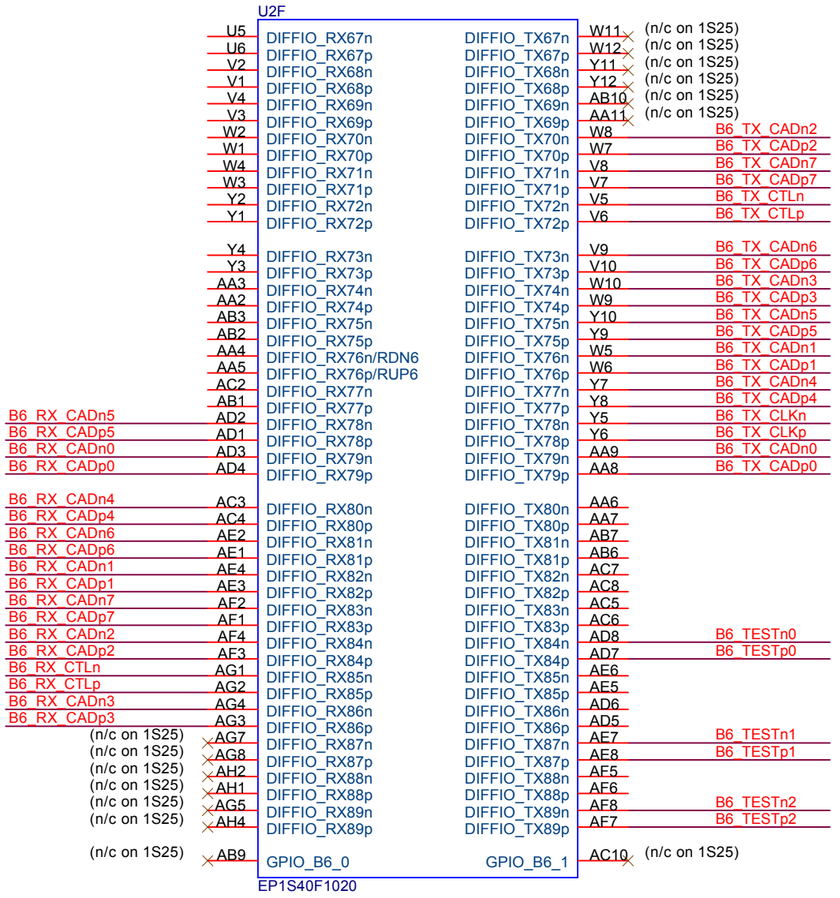
Bank 1

(Switchable 2.5V HyperTransport / 3.3V LVDS)

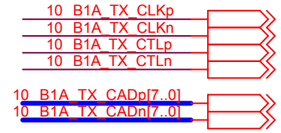


Bank 6

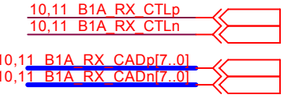
(Switchable 2.5V HyperTransport / 3.3V LVDS)



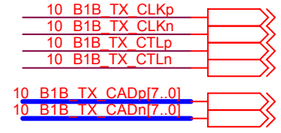
HSDI BANK 1A TX INTERFACE



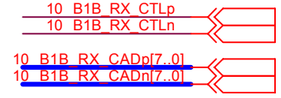
HSDI BANK 1A RX INTERFACE



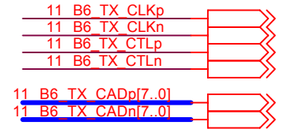
HSDI BANK 1B TX INTERFACE



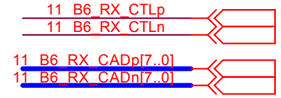
HSDI BANK 1B RX INTERFACE



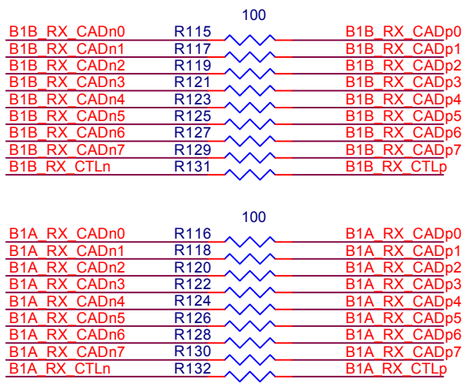
HSDI BANK 6 TX INTERFACE



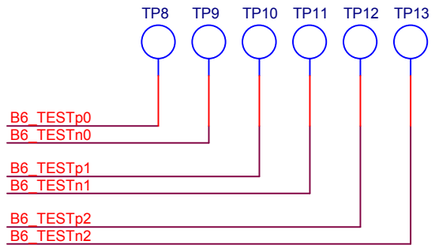
HSDI BANK 6 RX INTERFACE



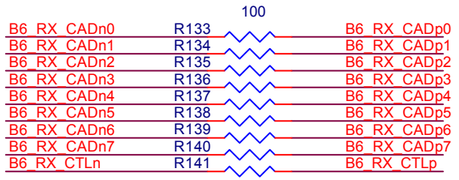
Differential RX Termination Resistors



Differential I/O Test Points



Differential RX Termination Resistors



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10/100 Ethernet Interface

MAC/PHY

LAN91C111

LOCAL BUS INTERFACE PINS

PHY

MII INTERFACE

EEPROM

Integrated RJ45
(includes LEDs and magnetics)

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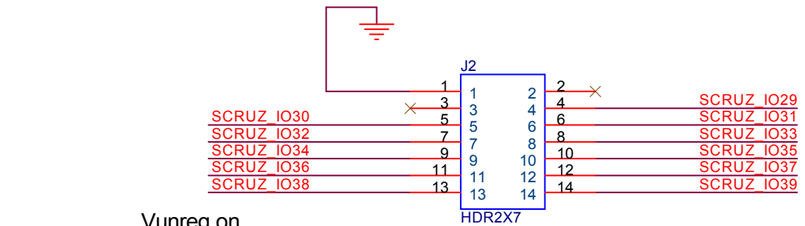
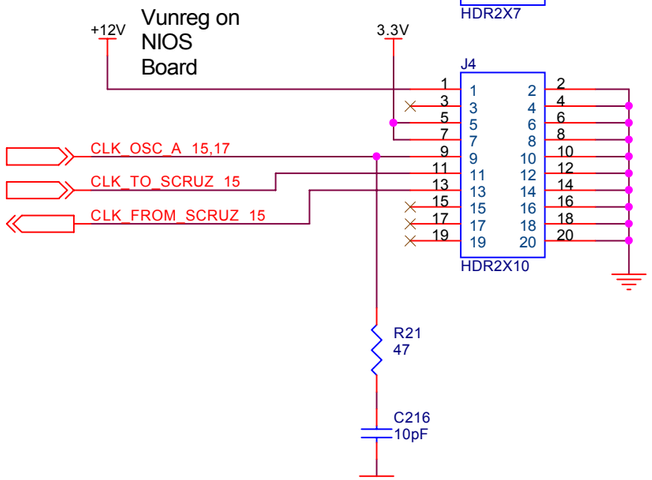
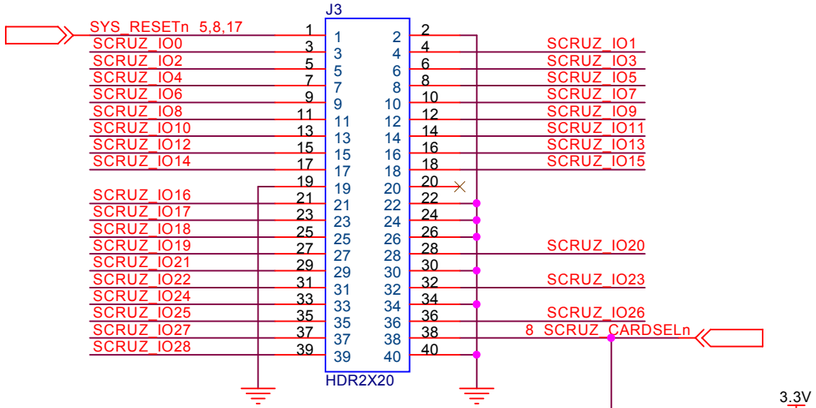
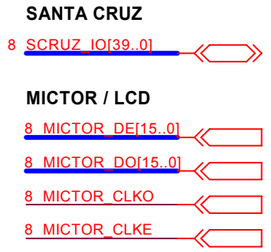
Expansion Prototype Card (PROTO1), RS-232, LCD, Mictor

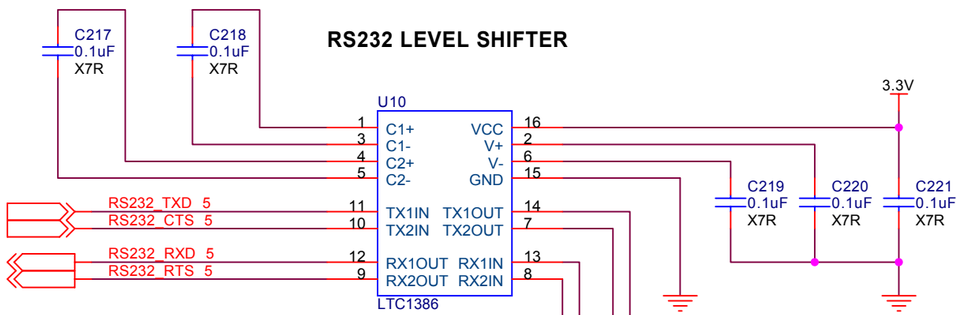




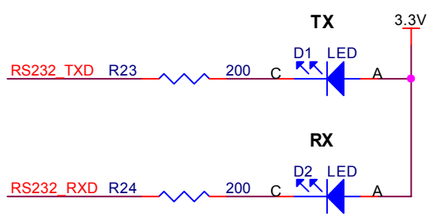




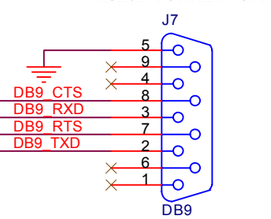
RS232 LEVEL SHIFTER



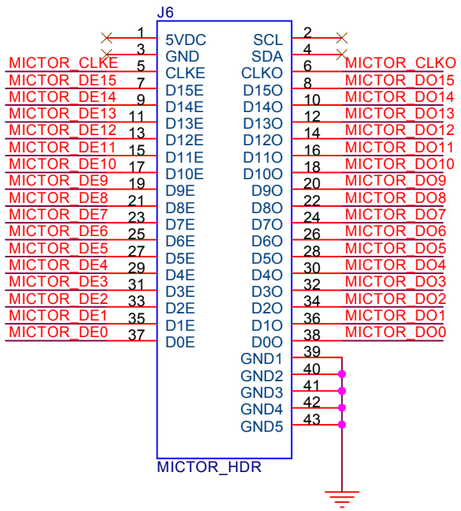
RS232 ACTIVITY INDICATORS



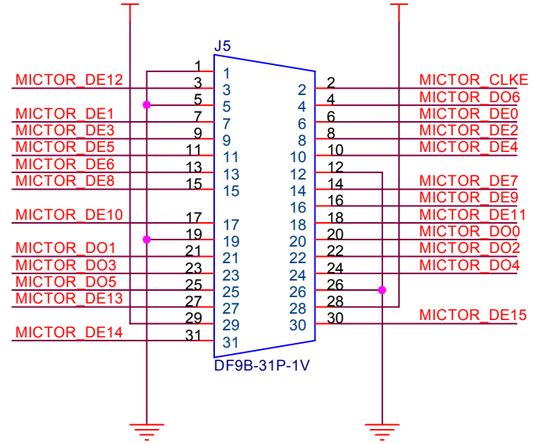
FEMALE RS232 CONNECTOR



MICTOR CONNECTOR



LCD HEADER



MICTOR TO LCD SIGNAL MAP

```
MICTOR_CLKE =>  LCD_CLK

MICTOR_DE0  =>  LCD_RED0
MICTOR_DE1  =>  LCD_RED1
MICTOR_DE2  =>  LCD_RED2
MICTOR_DE3  =>  LCD_RED3
MICTOR_DE4  =>  LCD_RED4
MICTOR_DE5  =>  LCD_RED5

MICTOR_DE6  =>  LCD_GREEN0
MICTOR_DE7  =>  LCD_GREEN1
MICTOR_DE8  =>  LCD_GREEN2
MICTOR_DE9  =>  LCD_GREEN3
MICTOR_DE10 => LCD_GREEN4
MICTOR_DE11 => LCD_GREEN5

MICTOR_DO0  =>  LCD_BLUE0
MICTOR_DO1  =>  LCD_BLUE1
MICTOR_DO2  =>  LCD_BLUE2
MICTOR_DO3  =>  LCD_BLUE3
MICTOR_DO4  =>  LCD_BLUE4
MICTOR_DO5  =>  LCD_BLUE5

MICTOR_DE12 =>  LCD_HSYNC
MICTOR_DE13 =>  LCD_DISABLE
MICTOR_DE14 =>  LCD_UP_N_DOWN
MICTOR_DE15 =>  LCD_RIGHT_N_LEFT
MICTOR_DO6   =>  LCD_VSYNC
```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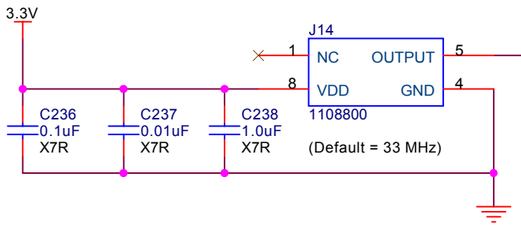
Clocking, JTAG Bypass Jumper

Configuration / System Clock

(socketed half-can oscillator)

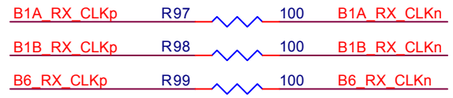


CLK_OSC_A

14,17 CLK_OSC_A

Also drives MAX3256A for configuration and Santa Cruz Daughtercard for potential use on a daughtercard. AC termination on sheet 14.

Differential input termination resistors for High-Speed Bank 1 and Bank 6 clock inputs.



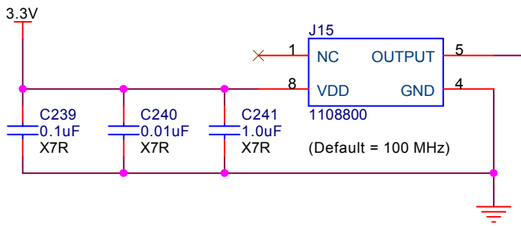
PLL5 Output Vcc = 2.5V

PLL6 Output Vcc = 3.3V

(place near socketed oscillators)

High-Speed Clock

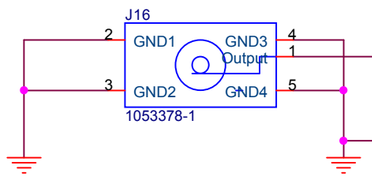
(socketed half-can oscillator)

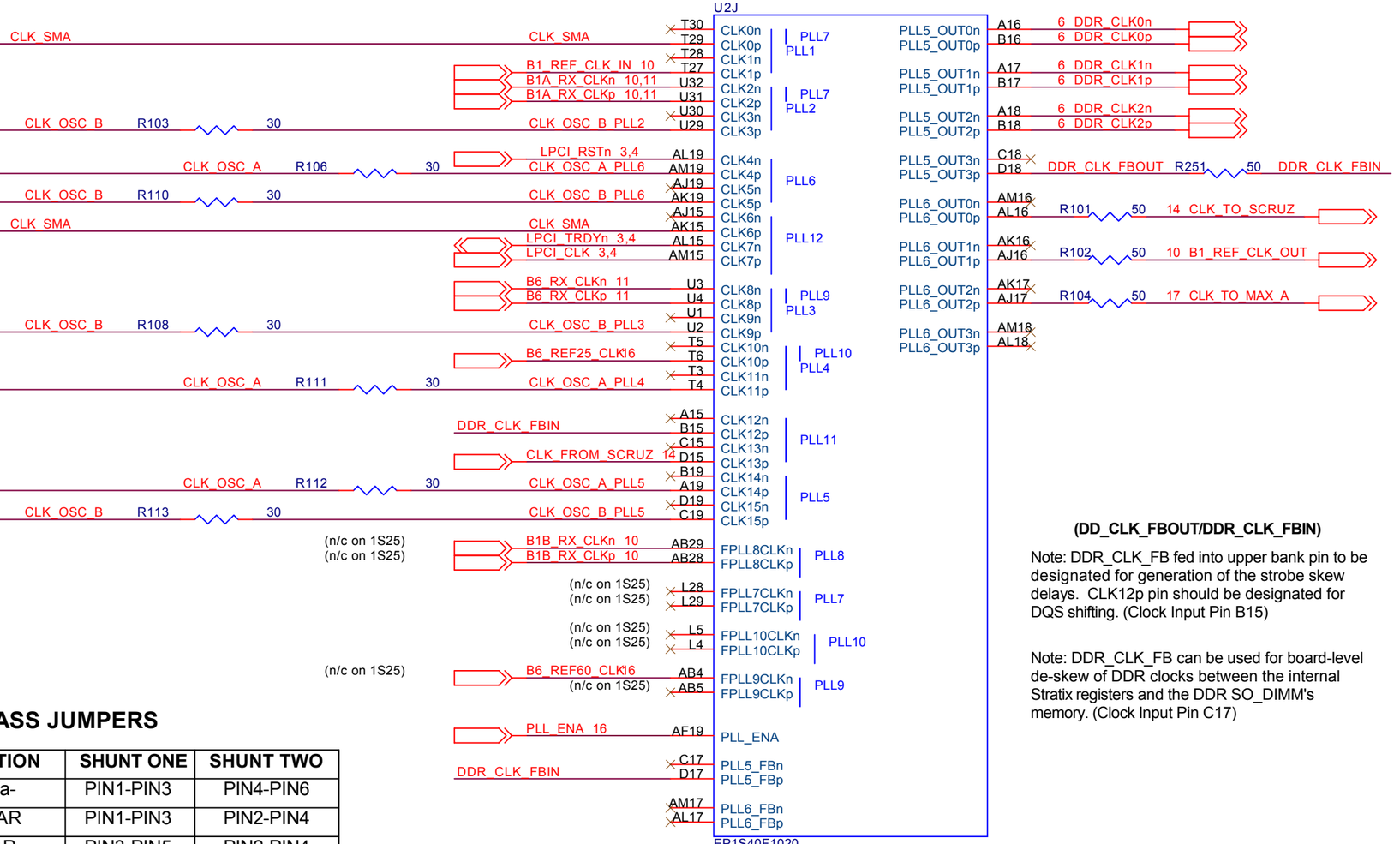


CLK_OSC_B

SMA Connector

(external clock source)





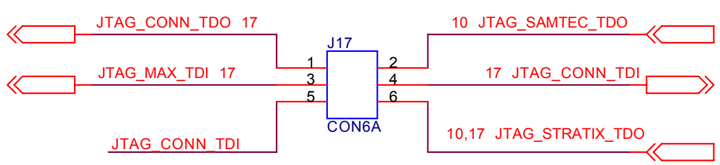
(DD_CLK_FBOUT/DDR_CLK_FBIN)

Note: DDR_CLK_FB fed into upper bank pin to be designated for generation of the strobe skew delays. CLK12p pin should be designated for DQS shifting. (Clock Input Pin B15)

Note: DDR_CLK_FB can be used for board-level de-skew of DDR clocks between the internal Stratix registers and the DDR SO_DIMM's memory. (Clock Input Pin C17)

JTAG BYPASS JUMPERS

BOARDS IN CHAIN	POSITION	SHUNT ONE	SHUNT TWO
SINGLE (default)	-n/a-	PIN1-PIN3	PIN4-PIN6
DOUBLE (w/bank 1)	NEAR	PIN1-PIN3	PIN2-PIN4
DOUBLE (w/bank 1)	FAR	PIN3-PIN5	PIN2-PIN4



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Power, Temperature Sense

+2.5V @ 6A (3A each)

3.3V
R13 0.01
3.3V_INPUT1
2.5V_SHDNn
U4 LT1764AEQ-2.5 (IN, SHDN, GND, OUT, GNDPAD, SENSE/ADJ)
2.5V_RAW
L1 60R100M6A 2.5V
C242 47uF 10V TAN
R15 0.01
3.3V_INPUT2
U5 LT1764AEQ
R16 2.2K
R17 2.2K
R14 4.42K
2.5V_SENSE
R18 4.12K
R19 1K
2.5V_SENSE_AMPOUT
Keep 2.5V_SENSE node at 1.21V DC
C243 0.01uF X7R
C188 0.01uF X7R
U9 LT1366 (OUTA, INA-, INA+, V-, V+, OUTB, INB-, INB+)
3.3V_SENSE2
3.3V_SENSE1
AUX_IN
J19 CON4PIN
+12V
LCD BACKLIGHT INVERTER POWER CONNECTOR
D17 SB5100
U7 MIC29502BU (EN, VI, VO, GND, TAB, ADJ)
VCC2.6
1.5V_RAW
L2 60R100M6A 1.5V
C189 100uF 10V Tantalum
+1.5V @ 5A
R252 64.9
R253 310
C190 100uF 10V Tantalum
ADJ
EXTERNAL POWER INPUT
+12V 5.0V 3.3V 3.3V -12V
J18 CON12A
17 MAIN_SW

TEMPERATURE SENSE
U8 MAX1619 (ADD1, ADD0, DXP, DXN, STBY, VCC, OVERT, ALERT, SMBCLK, SMBDATA, GND1, GND2, GND3)
TEMPDIODEp
TEMPDIODEn
5,17 OVERTEMPn
5,17 ALERTn
5 SMB_CLK
5 SMB_DATA
R20 200
C191 0.1uF X7R

L11 600R100M1A
L12 600R100M1A
L13 600R100M1A
L14 600R100M1A
L5 600R100M1A

L4 600R100M1A — VCCA_PLL3_PLL9 — C196 2.2uF X7R, C197 0.1uF X7R, C198 0.01uF X7R, C199 0.001uF X7R
L3 600R100M1A — VCCA_PLL5_PLL11 — C192 2.2uF X7R, C193 0.1uF X7R, C194 0.01uF X7R, C195 0.001uF X7R
L6 600R100M1A — VCCA_PLL4_PLL10 — C200 2.2uF X7R, C201 0.1uF X7R, C202 0.01uF X7R, C203 0.001uF X7R
L7 600R100M1A — VCCA_PLL6_PLL12 — C204 2.2uF X7R, C205 0.1uF X7R, C206 0.01uF X7R, C207 0.001uF X7R
L8 600R100M1A — VCCA_PLL1_PLL7 — C208 2.2uF X7R, C209 0.1uF X7R, C210 0.01uF X7R, C211 0.001uF X7R
L9 600R100M1A — VCCA_PLL2_PLL8 — C212 2.2uF X7R, C213 0.1uF X7R, C214 0.01uF X7R, C215 0.001uF X7R

U2K EP1S40F1020

M12	VCCINT1	GND1	H24
M14	VCCINT2	GND2	AA16
M19	VCCINT3	GND3	AA17
M21	VCCINT4	GND4	AC1
N13	VCCINT5	GND5	AC32
N15	VCCINT6	GND6	AL1
N18	VCCINT7	GND7	AL2
N20	VCCINT8	GND8	AL31
P12	VCCINT9	GND9	AL32
P14	VCCINT10	GND10	AM10
P16	VCCINT11	GND11	AM2
P17	VCCINT12	GND12	AM23
P19	VCCINT13	GND13	AM31
P21	VCCINT14	GND14	B1
R13	VCCINT15	GND15	B2
R15	VCCINT16	GND16	B31
R18	VCCINT17	GND17	B32
R20	VCCINT18	GND18	K1
T14	VCCINT19	GND19	K32
T16	VCCINT20	GND20	M13
T17	VCCINT21	GND21	M15
T19	VCCINT22	GND22	M16
U14	VCCINT23	GND23	M17
U16	VCCINT24	GND24	AD17
U17	VCCINT25	GND25	AF17
U19	VCCINT26	GND26	J17
V13	VCCINT27	GND27	H18
V15	VCCINT28	GND28	M18
V18	VCCINT29	GND29	M20
V20	VCCINT30	GND30	N12
W14	VCCINT31	GND31	N14
W16	VCCINT32	GND32	N16
W17	VCCINT33	GND33	N17
W19	VCCINT34	GND34	N19
Y13	VCCINT35	GND35	N21
Y15	VCCINT36	GND36	P13
Y18	VCCINT37	GND37	P15
Y20	VCCINT38	GND38	P18
F18	TEMPDIODEn		
E18	TEMPDIODEp		
T25	VCCA_PLL1	GNDA_PLL1	T26
U25	VCCA_PLL2	GNDA_PLL2	U26
U8	VCCA_PLL3	GNDA_PLL3	U7
T8	VCCA_PLL4	GNDA_PLL4	T7
G17	VCCA_PLL5	GNDA_PLL5	F17
AG17	VCCA_PLL6	GNDA_PLL6	AH17
D31	VCCA_PLL07	GNDA_PLL07	D32
AJ31	VCCA_PLL08	GNDA_PLL08	AJ32
AJ2	VCCA_PLL09	GNDA_PLL09	AJ1
D2	VCCA_PLL10	GNDA_PLL10	D1
E16	VCCA_PLL11	GNDA_PLL11	E17
AG16	VCCA_PLL12	GNDA_PLL12	AH16
R22	VCCG_PLL1	GNDG_PLL1	T22
U24	VCCG_PLL2	GNDG_PLL2	T24
V11	VCCG_PLL3	GNDG_PLL3	U11
T9	VCCG_PLL4	GNDG_PLL4	U9
J16	VCCG_PLL5	GNDG_PLL5	L16
AD16	VCCG_PLL6	GNDG_PLL6	AB16
D30	VCCG_PLL07	GNDG_PLL07	E30
AJ30	VCCG_PLL08	GNDG_PLL08	AH30
AJ3	VCCG_PLL09	GNDG_PLL09	AH3
D3	VCCG_PLL10	GNDG_PLL10	E3
H16	VCCG_PLL11	GNDG_PLL11	H15
AF16	VCCG_PLL12	GNDG_PLL12	AE16

TEMPDIODEn
TEMPDIODEp
VCCA_PLL1_PLL7
VCCA_PLL2_PLL8
VCCA_PLL3_PLL9
VCCA_PLL4_PLL10
VCCA_PLL5_PLL11
VCCA_PLL6_PLL12
VCCA_PLL1_PLL7
VCCA_PLL2_PLL8
VCCA_PLL3_PLL9
VCCA_PLL4_PLL10
VCCA_PLL5_PLL11
VCCA_PLL6_PLL12

RN5 10K
OVERTEMPn
ALERTn
SMB_CLK
SMB_DATA
PLL_ENA 15
AUX_IN
2.5V_SHDNn

BANK 1 / BANK 6 VCCIO SELECT

VCCIO_B1 18
VCCIO_B1
U20 CON6A
SSTL2_VREF 6
VCCIO_B6
VCCIO_B6 18

U2L EP1S40F1020

AA32	VCCIO1_1	GND39	P20
AK31	VCCIO1_2	GND40	R14
AK32	VCCIO1_3	GND41	R16
U23	VCCIO1_4	GND42	R17
AB25	VREF2B1	GND43	R19
AA23	VREF3B1	GND44	T12
V21	VREF4B1	GND45	T13
C31	VCCIO2_1	GND46	T15
C32	VCCIO2_2	GND47	T18
M32	VCCIO2_3	GND48	T20
T23	VCCIO2_4	GND49	T21
R21	VREF2B2	GND50	U12
L25	VREF3B2	GND51	U13
F27	VREF4B2	GND52	U15
A21	VCCIO3_1	GND53	U18
A30	VCCIO3_2	GND54	U20
K17	VCCIO3_3	GND55	U21
E27	VREF2B3	GND56	V14
E25	VREF3B3	GND57	V16
E23	VREF4B3	GND58	V17
E21	VREF5B3	GND59	V19
A12	VCCIO4_1	GND60	W13
A3	VCCIO4_2	GND61	W15
K16	VCCIO4_3	GND62	W18
E12	VREF2B4	GND63	W20
E10	VREF3B4	GND64	Y14
E8	VREF4B4	GND65	Y16
E6	VREF5B4	GND66	Y17
C1	VCCIO5_1	GND67	Y19
C2	VCCIO5_2	GND68	A10
M1	VCCIO5_3	GND69	A2
T10	VCCIO5_4	GND70	A23
F6	VREF2B5	GND71	A31
L8	VREF3B5		
R12	VREF4B5		
AA1	VCCIO6_1		
AK1	VCCIO6_2		
AK2	VCCIO6_3		
U10	VCCIO6_4		
AA10	VREF2B6		
AB8	VREF3B6		
AG6	VREF4B6		
AC16	VCCIO7_1		
AM12	VCCIO7_2		
AM3	VCCIO7_3		
AH6	VREF2B7		
AH8	VREF3B7		
AH10	VREF4B7		
AH12	VREF5B7		
AC17	VCCIO8_1		
AM21	VCCIO8_2		
AM30	VCCIO8_3		
AH21	VREF2B8		
AH23	VREF3B8		
AH25	VREF4B8		
AH27	VREF5B8		

VCC_PLL5_OUTA H17
VCC_PLL5_OUTB L17
VCC_PLL6_OUTA AE17
VCC_PLL6_OUTB AB17

TP4 3.3V
TP2 5.0V
TP7 +12V
TP5 -12V

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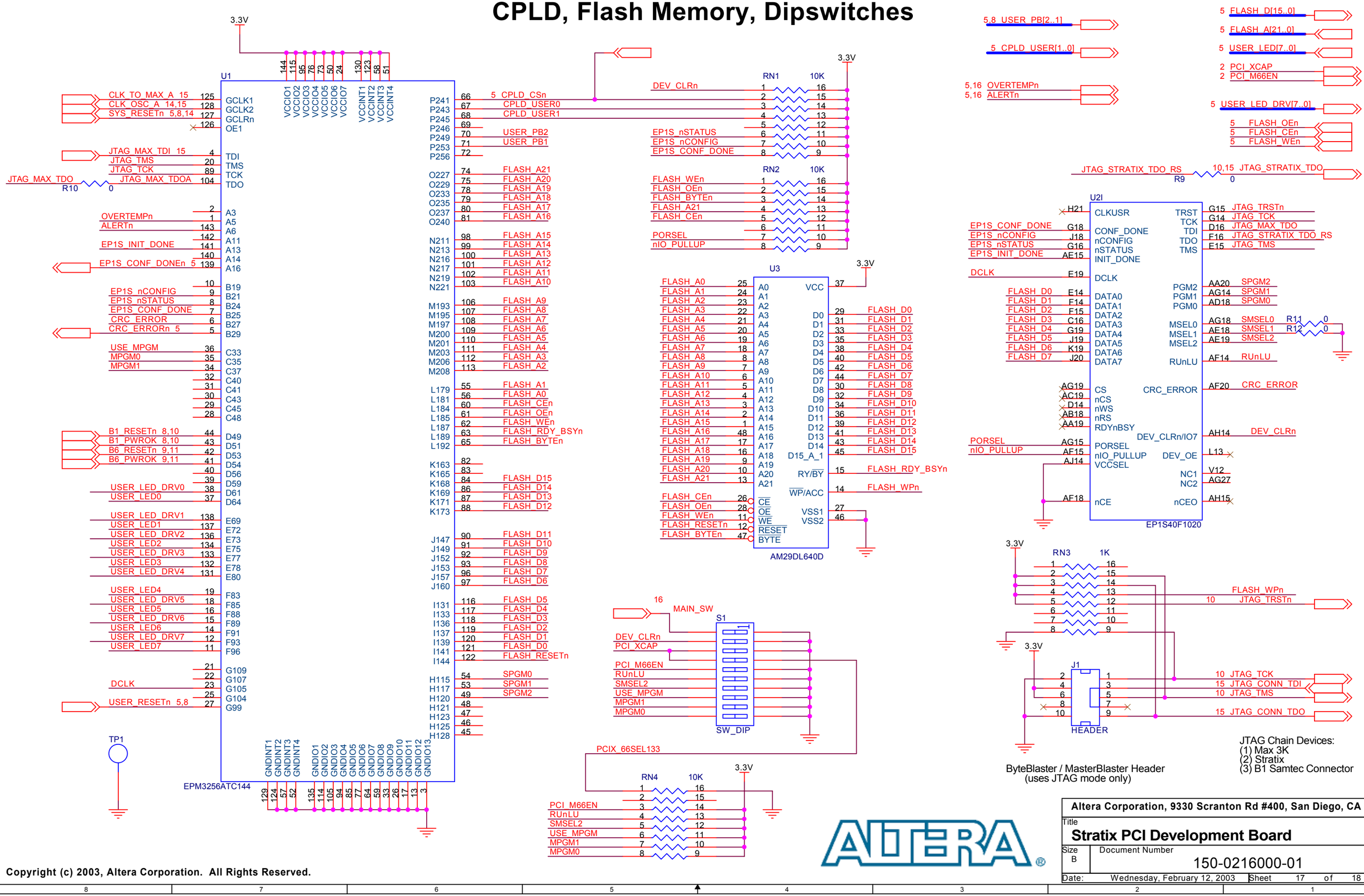
CPLD, Flash Memory, Dipswitches



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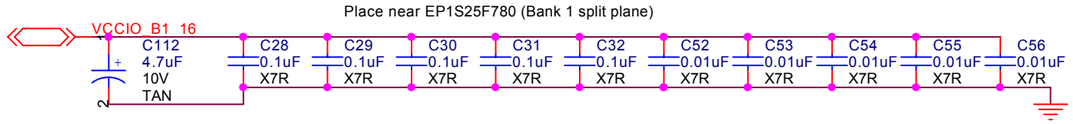
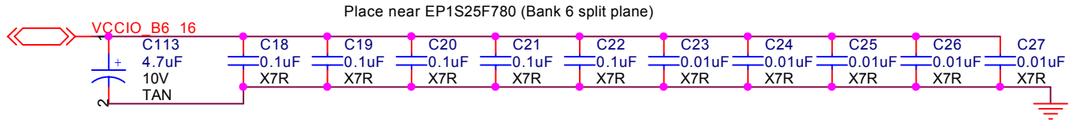
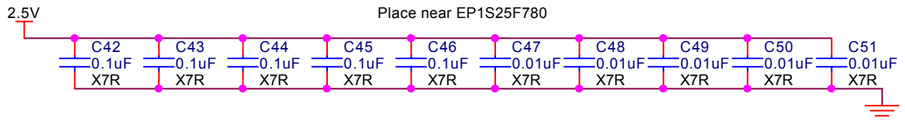
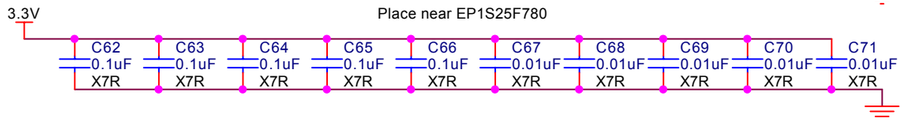
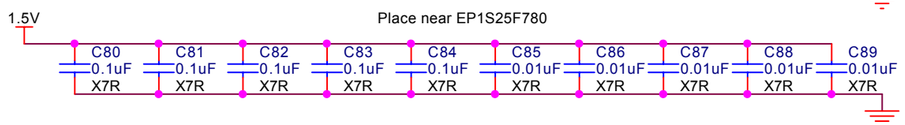
Decoupling

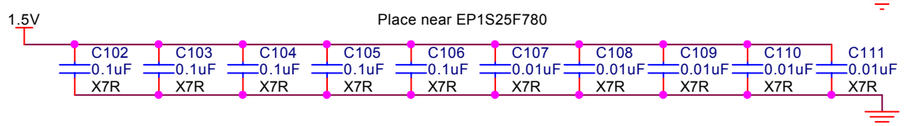


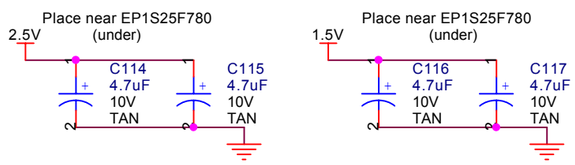


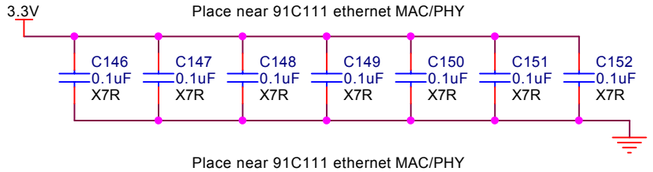


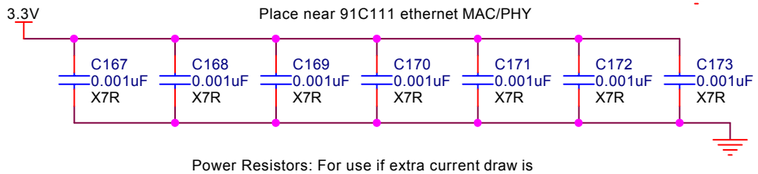


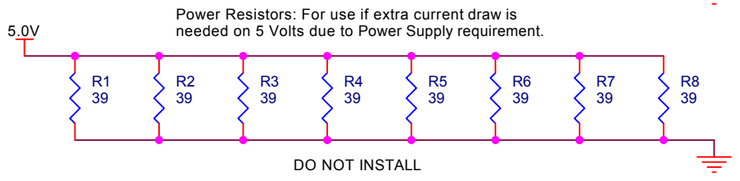


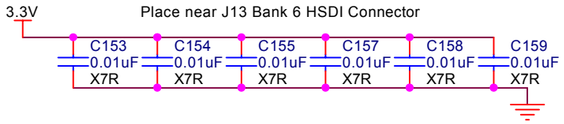


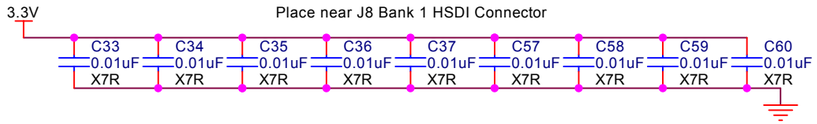


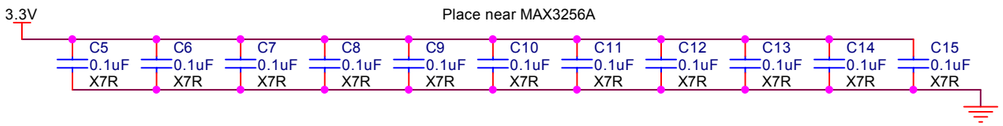


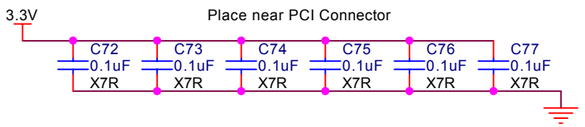


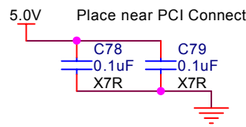


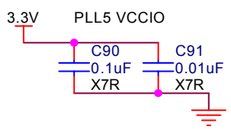


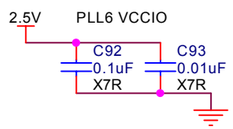


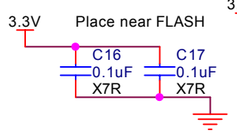


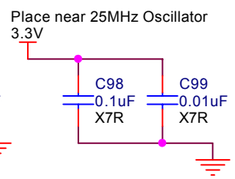


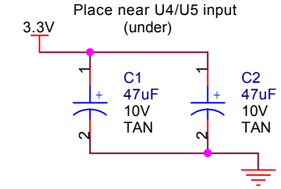


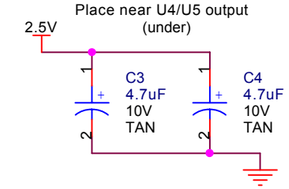


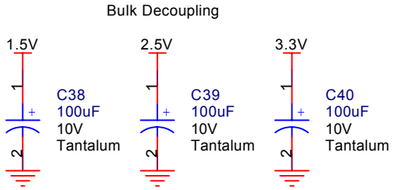


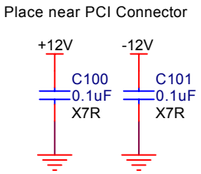


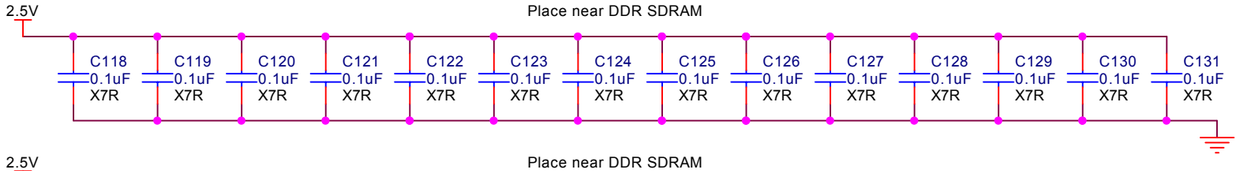


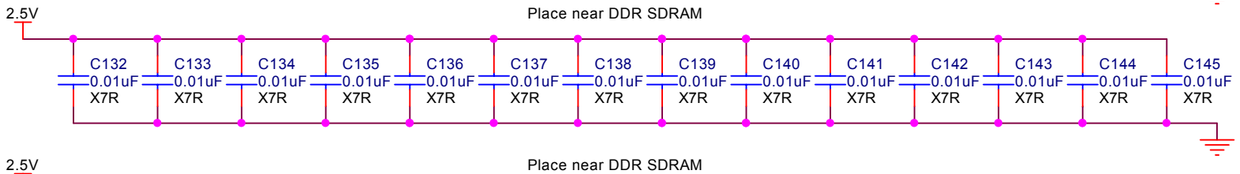


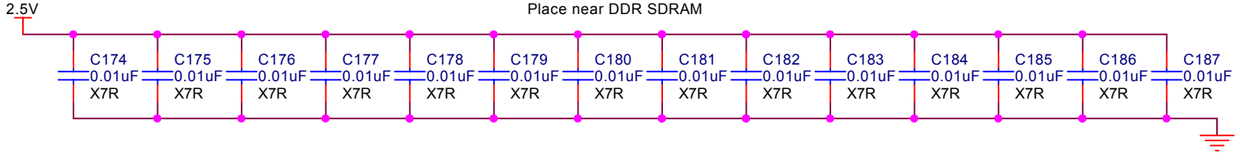












Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix PCI Development Board**		
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