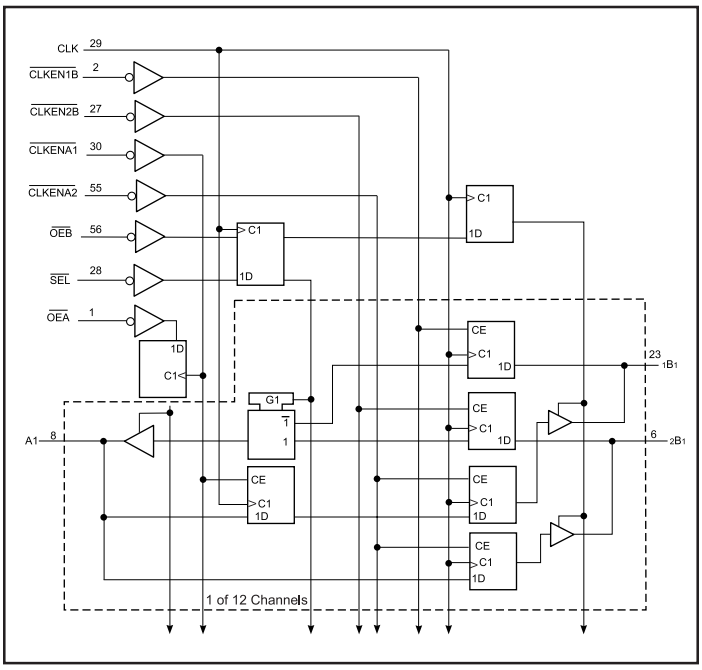
PI74ALVCH162268

12-Bit To 24-Bit Registered Bus Exchanger with 3-State Outputs

Product Features

- PI74ALVCH162268 is designed for low voltage operation V_{CC} = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- B-port outputs have equivalent 26Ω series resistors, no external resistors are required.
- Bus Hold retains last active bus state during 3-state eliminates the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A56)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

This 12-bit to 24-bit registered bus exchanger is designed for 2.3V to 3.6V V_{cc} operation.

The PI74ALVCH162268 is used for applications in which data must be transferred from a narrow high-speed bus to a wide, lower frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB}$). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12mA, include equivalent 26Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver. Because $\overline{OE}$ is being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock
$\overline{SEL}$	Select (Active Low)
$\overline{CLKEN}$	Clock Enable (Active Low)
A,1B,2B	3-State Outputs
GND	Ground
VCC	Power

Truth Tables(1)

Output Enable

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A to B STORAGE ($\overline{OEB}$ = L)

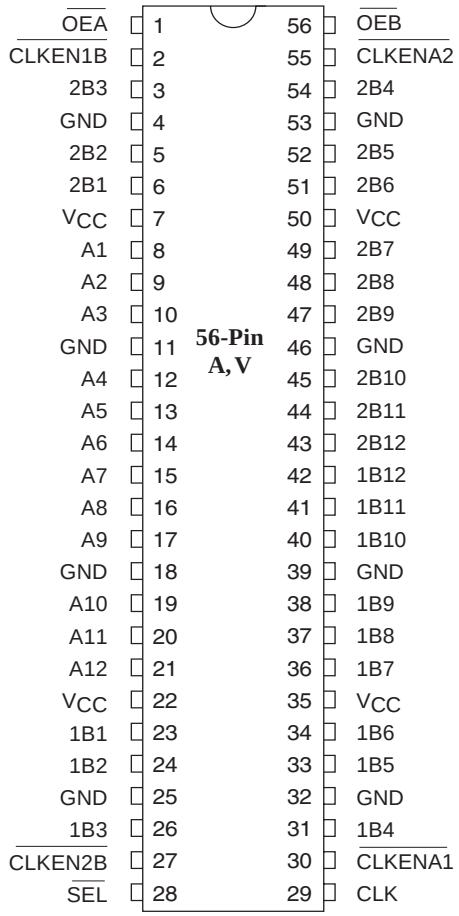
INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B0(3)	2B0(3)
L	L	↑	L	L(2)	X
L	L	↑	H	H(2)	X
X	L	↑	L	X	L
X	L	↑	H	X	H

B to A STORAGE ($\overline{OEA}$ = L)

INPUTS						Outputs
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	A
H	X	X	H	X	X	A0(3)
X	H	X	L	X	X	A0(3)
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

Notes:
1. H = High Signal Level, L = Low Signal Level
   X = Irrelevant, Z = High Impedance
   ↑ = Transition, Low to High
2. Two CLK edges are needed to propagate data
3. Output level before the indicated steady state input conditions were established.

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage Range, V_{CC} ..... –0.5V to 4.6V
Input Voltage Range, V_I :
Except I/O ports (See Note 1): ..... –0.5V to 4.6V
I/O ports (See Notes 1 and 2) ..... –0.5V to V_{CC} + 0.5V
Output Voltage Range, V_O (See Notes 1and 2) .. –0.5V to V_{CC} + 0.5V
Input Clamp current, I_{IK} (V_I < 0) ..... –50mA
Output Clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50mA
Continous Output Current, I_O (V_O = 0 to V_{CC}) ..... ±50mA
Continous Current through each V_{CC} or GND ..... ±100mA
Maximum Power Dissipation:
A package 1W
V package 1.4W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 10%)

Parameters	Description	Test Conditions[3]	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	HIGH-level Output Current (A Port)	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}	LOW-level Output Current (A Port)	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	
I_{OH}	HIGH-level Output Current (B Port)	V_{CC} = 2.3V			-6	
		V_{CC} = 2.7V			-8	
		V_{CC} = 3.0V			-12	
I_{OL}	LOW-level Output Current (B Port)	V_{CC} = 2.3V			6	
		V_{CC} = 2.7V			8	
		V_{CC} = 3.0V			12	

Notes:
1. The input and output negative-voltage ratings maybe exceeded if the input and outputclamp-current ratings are observed.
2. This value is limited to 4.6V maximum.
3. Unused control inputs must be held HIGH or LOW to prevent them from floating.

DC Electrical Characteristics-Continued (Over the Operating Range, T_A = -40ºC to +85ºC, V_{CC} = 3.3V ± 10%

Parameters	Test Conditions		V_{CC}(1)	Min.	Typ.(2)	Max.	Units
V_{OH} (A Port)	I_{OH} = -100µA		Min. toMax.	V_{CC} -0.2			V
	I_{OH} = -6mA	V_{IH} = 1.7V	2.3V	2.0			
	I_{OH} = -12mA	V_{IH} = 1.7V	2.3V	1.7			
		V_{IH} = 2.0V	2.7V	2.2			
		V_{IH} = 2.0V	3.0V	2.4			
	I_{OH} = -24mA	V_{IH} = 2.0V	3.0V	2.0			
V_{OH} (B Port)	I_{OH} = -100µA		Min. to Max.	V_{CC} -0.2			
	I_{OH} = -4mA	V_{IH} = 1.7V	2.3V	1.9			
	I_{OH} = -6mA	V_{IH} = 1.7V	2.3V	1.7			
		V_{IH} = 2.0V	3.0V	2.4			
	I_{OH} = -8mA	V_{IH} = 2.0V	2.7V	2.0			
	I_{OH} = -12mA	V_{IH} = 2.0V	3.0V	2.0			
V_{OL}(A Port)	I_{OL} = 100µA		Min. to Max.			0.2	
	I_{OL} = 6mA	V_{IL} = 0.7V	2.3V			0.4	
	I_{OL} = 12mA	V_{IL} = 0.7V	2.3V			0.7	
		V_{IL} = 0.8V	2.7V			0.4	
	I_{OL} = 24mA	V_{IL} = 0.8V	3.0V			0.55	
V_{OL}(B Port)	I_{OL}= 100µA		Min. to Max.			0.2	
	I_{OL} = 4mA	V_{IL} = 0.7V	2.3V			0.4	
	I_{OL} = 6mA	V_{IL} = 0.7V	2.3V			0.55	
		V_{IL} = 0.8V	3.0V			0.55	
	I_{OL} = 8mA	V_{IL} = 0.8V	2.7V			0.6	
	I_{OL} = 12mA	V_{IL} = 0.8V	3.0V			0.8	
I_I	V_I = V_{CC} or GND		3.6V			±5	µA
I_I (Hold)	V_I = 0.7V		2.3V	45			
	V_I = 1.7V			-45			
	V_I = 0.8V		3.0V	75			
	V_I = 2.0V			-75			
	V_I = 0 to 3.6V(3)		3.6V			±500	
I_{OZ}(4)	V_O = V_{CC} or GND		3.6V			±10	
I_{CC}	V_I = V_{CC} or GND, I_O = 0		3.6V			40	
ΔI_{CC}	One input at V_{CC} - 0.6V, Other inputs at V_{CC} or GND		3V to 3.6V			750	
C_I Control Inputs	V_I = V_{CC} or GND		3.3V		3.5		pF
C_{IO} A or B Ports	V_O = V_{CC} or GND		3.3V		9		

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25ºC ambient and maximum loading.
3. Bus hold maximum dynamic current required to switch the input from one state to another
4. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency		0	120	0	125	0	150	Mhz
t_W	Pulse duration, CLK high or Low		3.3		3.3		3.3		ns
t_{SU}	Setup time	A data before CLK↑	4.5		4		3.4		ns
		B data before CLK↑	0.8		1.2		1		
		$\overline{SEL}$ before CLK↑	1.4		1.6		1.3		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	3.6		3.4		2.8		
		$\overline{CLKENB1}$ or $\overline{CLKENB2}$ before CLK↑	3.2		3		2.5		
		$\overline{OE}$ before CLK↑	4.2		3.9		3.2		ns
t_H	Hold time	A data after CLK↑	0		0		0.2		
		B data after CLK↑	1.3		1.2		1.3		
		$\overline{SEL}$ after CLK↑	1		1		1		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	0.1		0.1		0.4		
		$\overline{CLKENB1}$ or $\overline{CLKENB2}$ after CLK↑	0.1		0		0.5		
		$\overline{OE}$ after CLK↑	0		0		0.2		
$\Delta t/\Delta v$[1]	Input Transition Rise or Fall		0	10	0	10	0	10	ns/V

Notes:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics over Operating Range[1]

Parameters	From (INPUT)	To (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.[2]	
f_{MAX}			120		125		150		MHz
t_{PD}	CLK	B	1.6	6.1		5.9	1.8	5.4	ns
t_{PD}		A (1B)	1.6	5.8		5.4	1.7	4.8	
t_{PD}		B (2B)	1.6	5.8		5.3	1.8	4.8	
t_{PD}		A (SEL)	2.5	7.3		6.5	2.4	5.8	
t_{EN}		B	2.7	7.2		6.8	2.6	6.1	
t_{DIS}		B	2.8	7.2		6.1	2.5	5.9	
t_{EN}		A	2	6.2		5.6	1.8	5.1	
t_{DIS}		A	2	6.5		5.4	2.1	5	

Notes:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, $T_A = 25°C$

Parameter		Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Units
			Typical	Typical	
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L= 50pF, F = 10 MHz	87	120	pF
	Outputs Disabled		80.5	118	