FAIRCHILD SEMICONDUCTOR™

October 1987
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MM88C29 • MM88C30
Quad Single-Ended Line Driver • Dual Differential Line Driver

General Description

The MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM88C30 line driver. The differential output of the MM88C30 eliminates ground-loop errors.

The MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low output ON resistance: 20Ω (typ.)

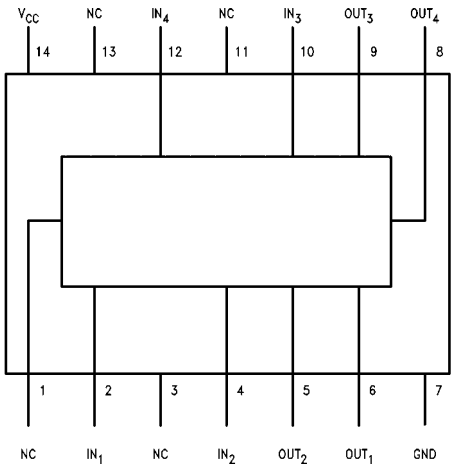
Ordering Code:

Order Number	Package Number	Package Description
MM88C29N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM88C30M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM88C30N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

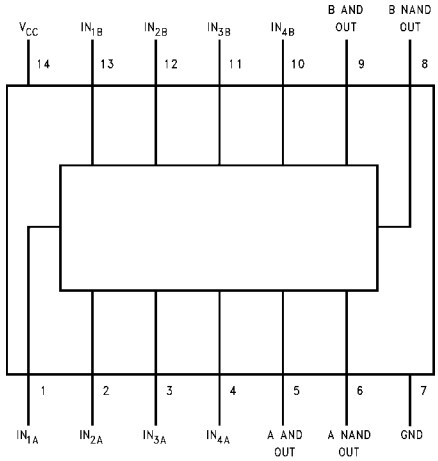
Connection Diagrams

Pin Assignments for DIP
MM88C29



Top View

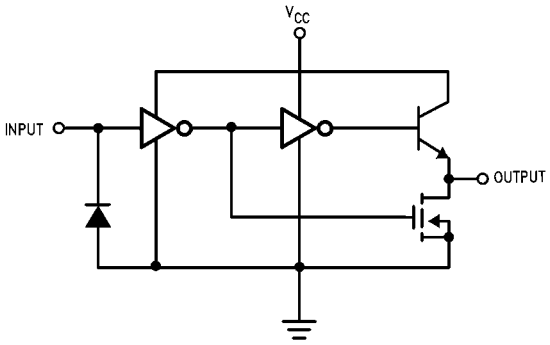
Pin Assignments for DIP and SOIC
MM88C30



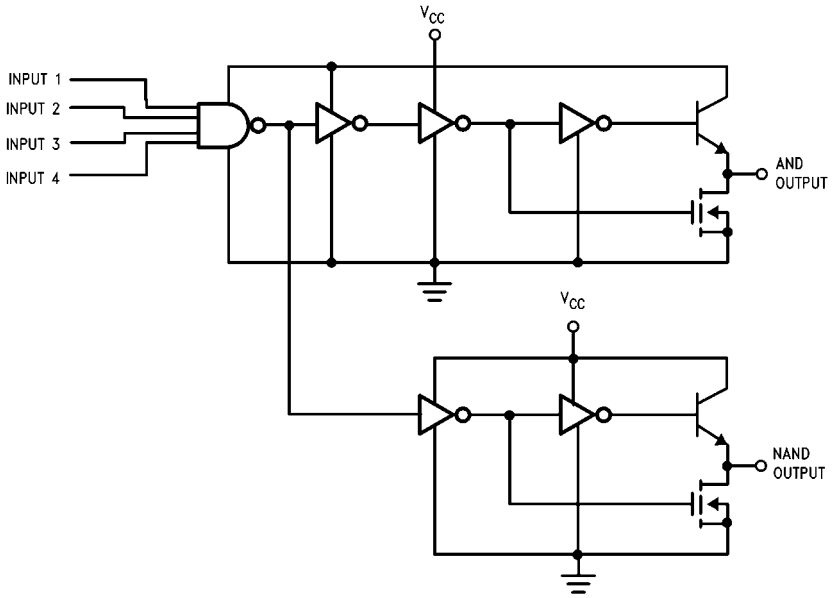
Top View

Logic Diagrams

1/4 MM88C29



1/2 MM88C30



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin (Note 2)	−0.3V to V_{CC} +16V
Operating Temperature Range	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Average Current at Output	
MM88C30	50 mA
MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

Note 2: AC Parameters are guaranteed by DC correlated testing.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	100	mA
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current	$V_{OUT} = V_{CC} - 1.6V$,				
		$V_{CC} \geq 4.75V$, T_j = 25°C	−47	−80		mA
		T_j = 85°C	−32	−60		mA
	MM88C29	$V_{OUT} = V_{CC} - 0.8V$	−2	−20		mA
	MM88C30	$V_{CC} \geq 4.5V$				
I_{SINK}	Output Sink Current	V_{OUT} = 0.4V, V_{CC} = 4.75V,				
		T_j = 25°C	9.5	22		mA
		T_j = 85°C	8	18		mA
		V_{OUT} = 0.4V, V_{CC} = 10V,				
		T_j = 25°C	19	40		mA
		T_j = 125°C	15.5	33		mA
I_{SOURCE}	Output Source Resistance	$V_{OUT} = V_{CC} - 1.6V$,				
		$V_{CC} \geq 4.75V$, T_j = 25°C		20	34	Ω
		T_j = 85°C		27	50	Ω
I_{SINK}	Output Sink Resistance	V_{OUT} = 0.4V, V_{CC} = 4.75V,				
		T_j = 25°C		18	41	Ω
		T_j = 85°C		22	50	Ω
		V_{OUT} = 0.4V, V_{CC} = 10V,				
		T_j = 25°C		10	21	Ω
		T_j = 85°C		12	26	Ω
	Output Resistance Temperature Coefficient					
	Source			0.55		%/°C
	Sink			0.40		%/°C
θ_{JA}	Thermal Resistance (N-Package)			150		°C/W

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to					
	Logical "1" or "0"	(See Figure 1)				
	MM88C29	$V_{CC} = 5V$		80	200	ns
		$V_{CC} = 10V$		35	100	ns
	MM88C30	$V_{CC} = 5V$		110	350	ns
		$V_{CC} = 10V$		50	150	ns
t_{pd}	Differential Propagation Delay	$R_L = 100\Omega$, $C_L = 5000$ pF				
	Time to Logical "1" or "0"	(See Figure 2)				
	MM88C30	$V_{CC} = 5V$			400	ns
		$V_{CC} = 10V$			150	ns
C_{IN}	Input Capacitance					
	MM88C29	(Note 3)		5.0		pF
	MM88C30	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance					
	MM88C29	(Note 3)		150		pF
	MM88C30	(Note 3)		200		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90 (CMOS Logic Databook).

AC Test Circuits

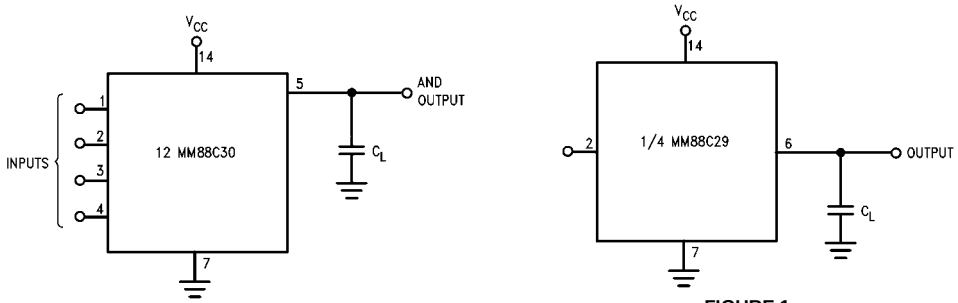


FIGURE 1.

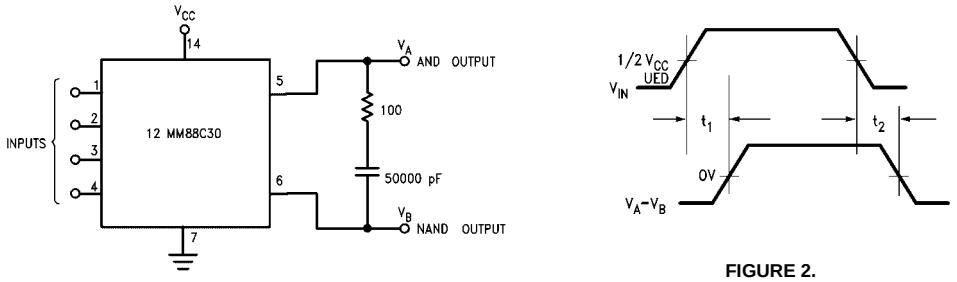
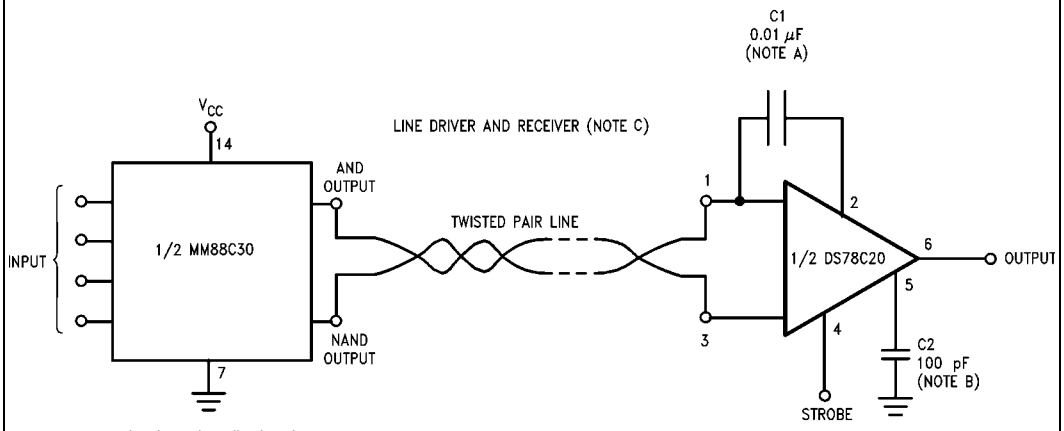


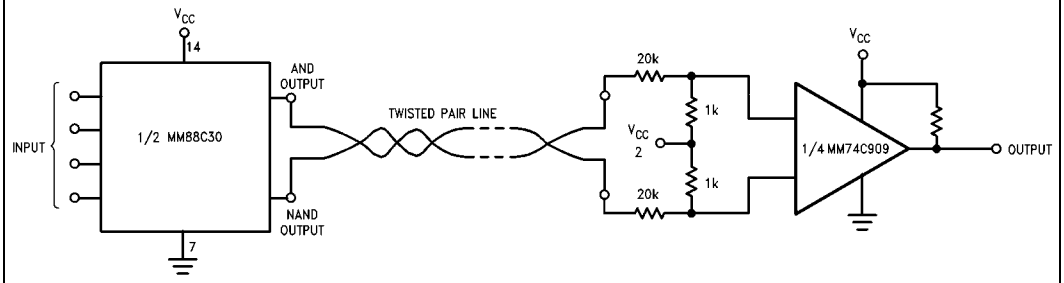
FIGURE 2.

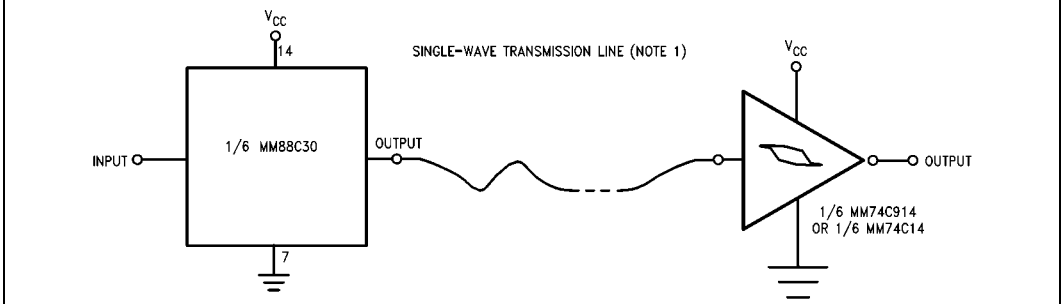
Typical Applications

Digital Data Transmission



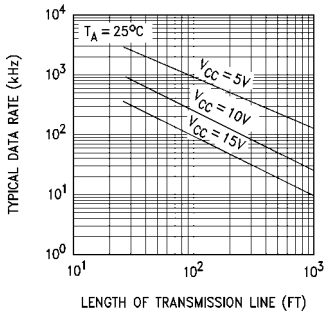
Note A: Exact value depends on line length.
Note B: Optional to control response time.
Note C: V_{CC}= 4.5V to 5.5V for the DS7820, V_{CC}=4.5V to 15V for the DS78C20.





V_{CC} is 3V to 15V.

Typical Data Rate vs Transmission Line Length

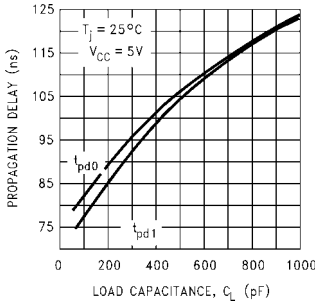


Note: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

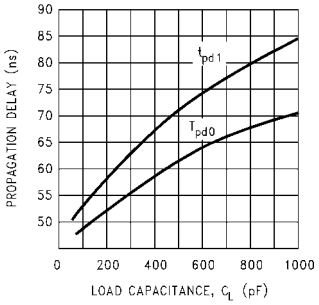
Note: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

Typical Performance Characteristics

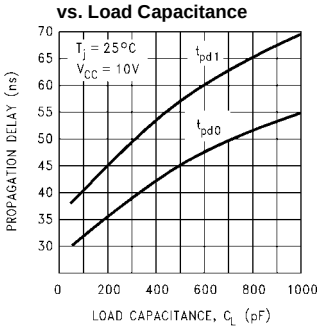
MM88C29
Typical Propagation Delay
vs. Load Capacitance



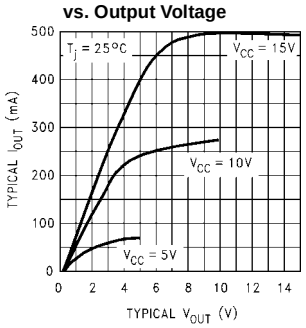
MM88C30
Typical Propagation Delay
vs. Load Capacitance



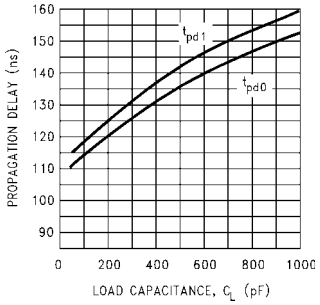
MM88C29
Typical Propagation Delay
vs. Load Capacitance



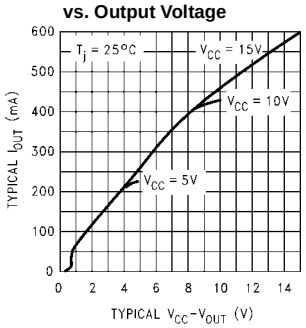
Typical Sink Current
vs. Output Voltage



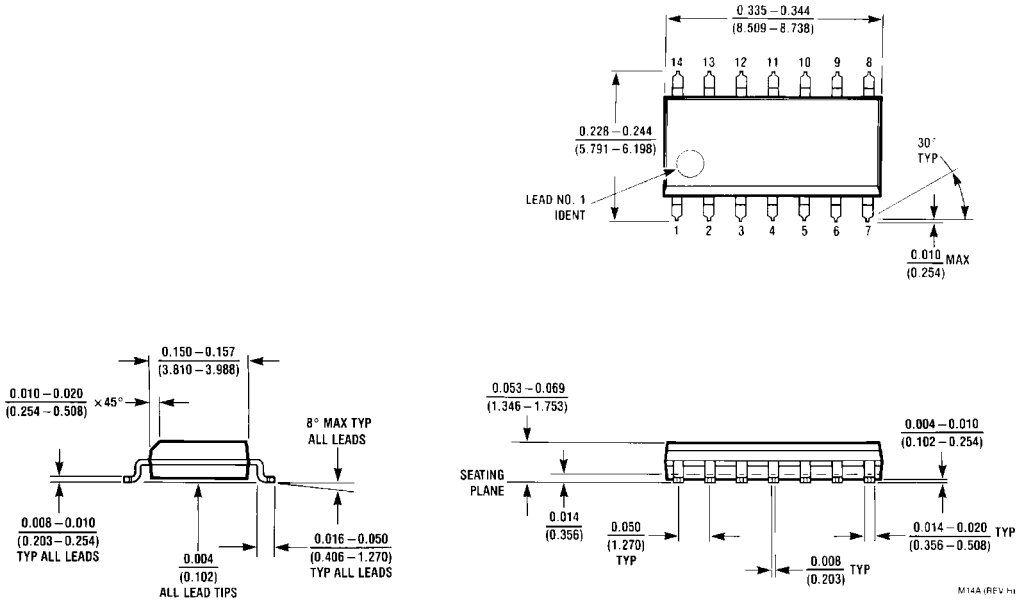
MM88C30
Typical Propagation Delay
vs. Load Capacitance



Typical Source Current
vs. Output Voltage

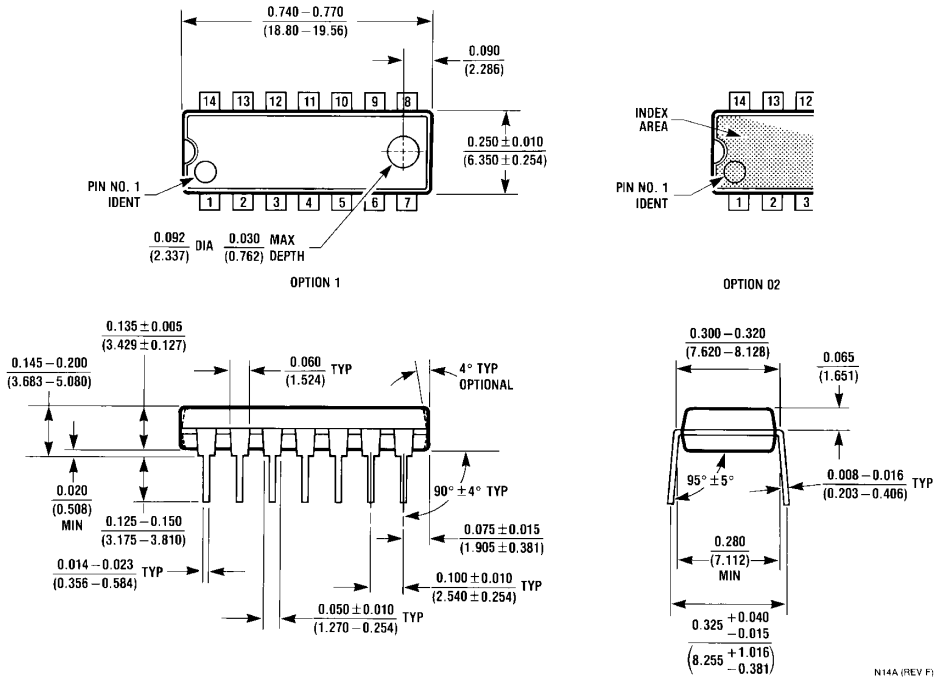


Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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