Data Sheet, Rev. 1.1, Jan. 2009

TLE 7241E

Dual Channel Constant Current Control Solenoid Driver

Automotive Power

Never stop thinking

Table of Contents

AEC Qualified RoHS

1 Overview

PG-DSO-20-27

1.1 Features

- Two Fully Independent Channels
- Integrated N-channel DMOS transistors
- Programmable Average Current with 10-bit resolution via SPI
  - I_{avg} range = 0 to 1000 mA (typical)
- Programmable Superimposed Dither
  - Programmable Frequency (41 Hz to 1 kHz typ)
  - Programmable Amplitude (12.5 to 390 mVpp typ)
  - Programmable Hysteresis (40 to 110 mVpp typ)
- Interface and Control
  - 16-bit SPI (Serial Peripheral Interface) daisy chainable
  - A single “Default” pin to disable both channels and reset the programmable registers of both channels
  - 5.0 V and 3.3 V logic compatible I/O
  - The contents of all registers can be verified via SPI
  - Operation with or without external reference possible
- Protection
  - Overcurrent
  - Overvoltage
  - Overtemperature
- Diagnostics
  - Overcurrent / shorted solenoid
  - Overtemperature
  - Open load
  - Short to GND
- Green Product (RoHS compliant)
- AEC Qualified

Type	Ordering Code	Package
TLE 7241E	on request	PG-DSO-20-27

1.2 Applications

- Variable force solenoids (e.g. automatic transmission solenoids)
- Constant current controlled solenoids like
  - Idle Speed Control
  - Exhaust Gas Recirculation
  - Valve control
  - Suspension Control

1.3 General Description

The TLE 7241E is a dual channel constant current control solenoid driver with integrated DMOS power transistors. The average load current can be programmed to a value in the range of 0 mA to 1000 mA (with a 1 Ω external sense resistor) with 10 bits of resolution. Load current is controlled using a hysteretic control scheme with a programmable hysteresis value. A triangular “dither” waveform can be superimposed on the switching current waveform in order to improve the transfer function of the solenoid. The amplitude and frequency of the dither waveform are programmable by the SPI interface. The device is protected from damage due to overcurrent, overvoltage and overtemperature conditions, and is able to diagnose and report open loads, shorted loads, and loads shorted to ground.

Note: An external free-wheeling diode must be provided when using the TLE 7241E in constant current control mode, otherwise the IC will be damaged.

For best accuracy, an external 2.5 V reference voltage should be supplied at the REF pin. The TLE 7241E also includes an internal 2.5 V reference voltage, which can be selected by connecting the REF pin to ground. The reference voltage selection (internal or external) can be verified via the SPI interface.

Application Block Diagram

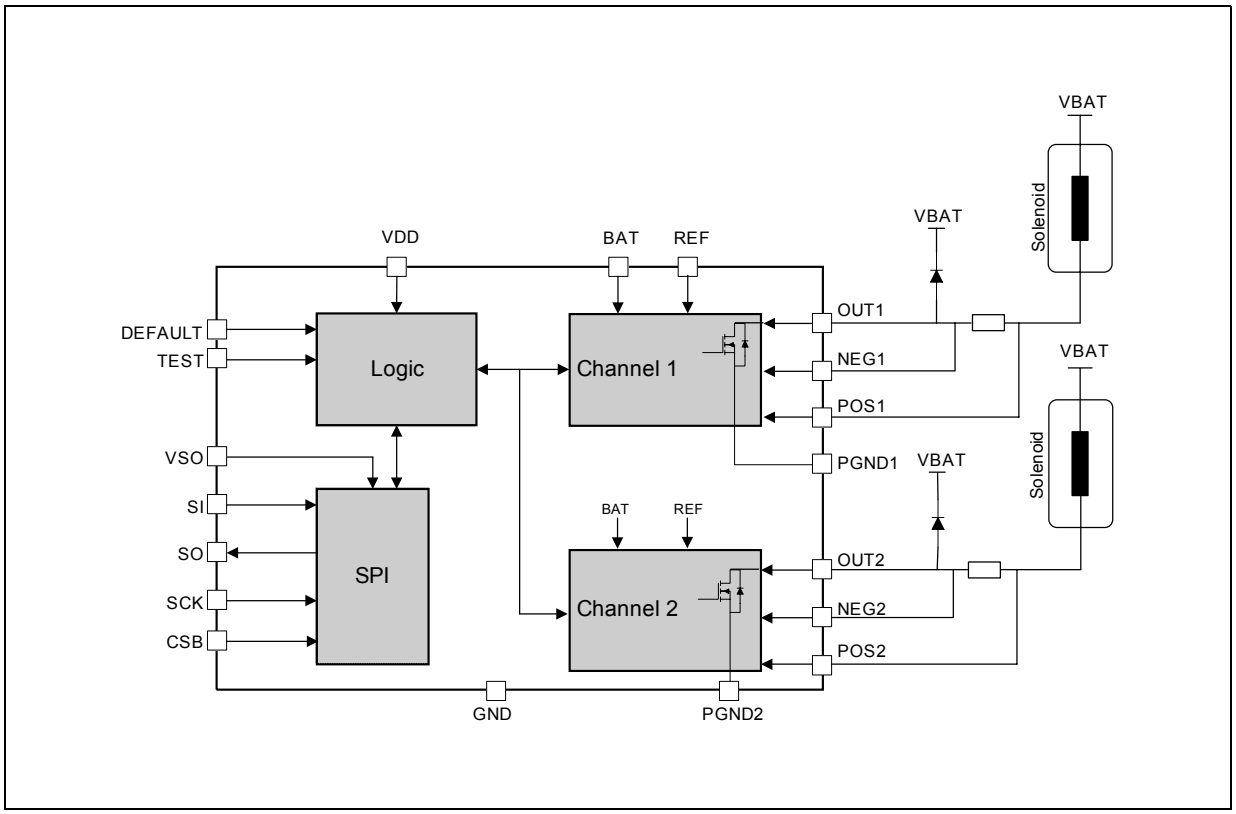

Figure 1 Basic Application Diagram

Detailed Block Diagram

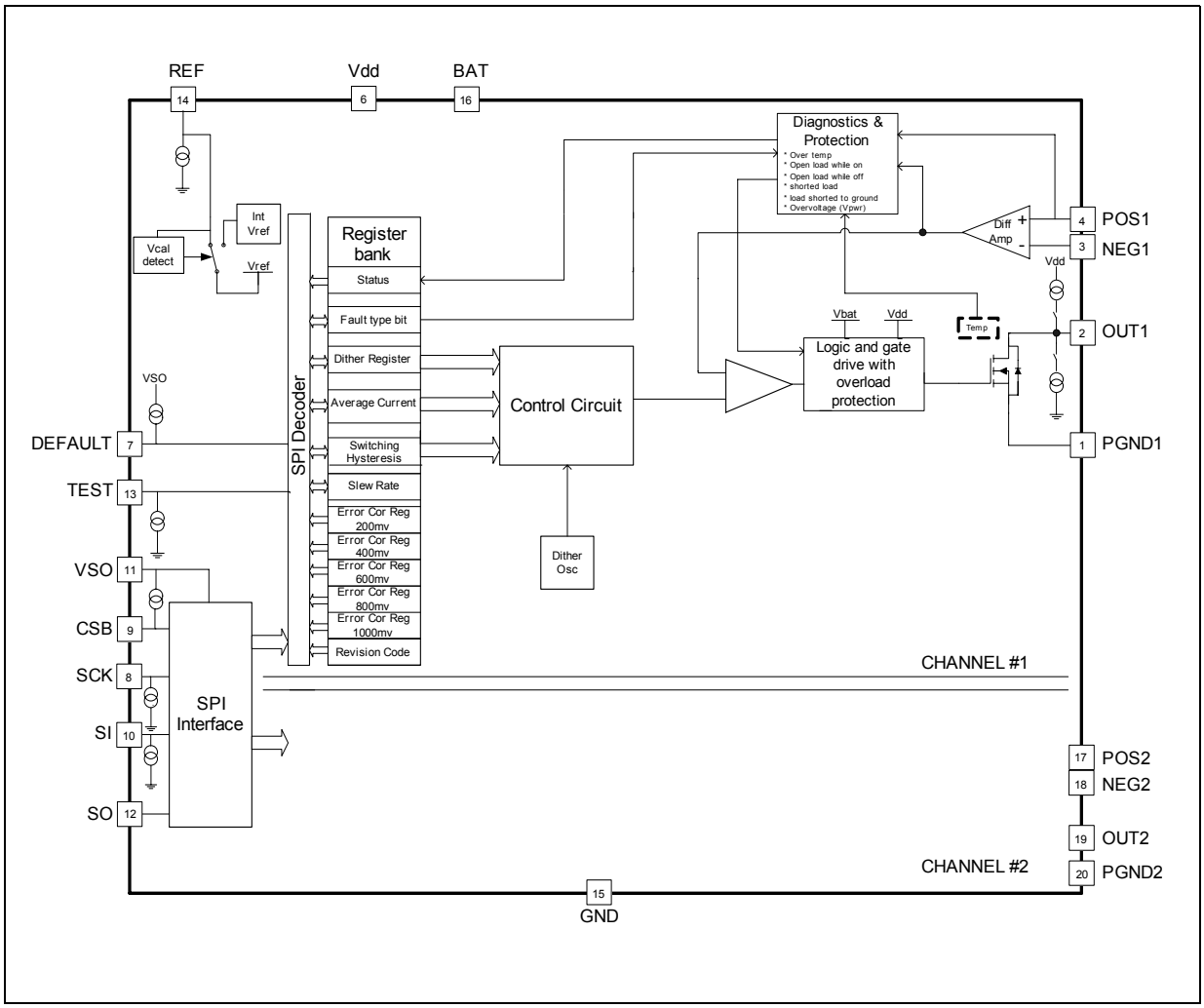

Figure 2 Detailed Block Diagram

2 Pin Configuration

Pin Assignment

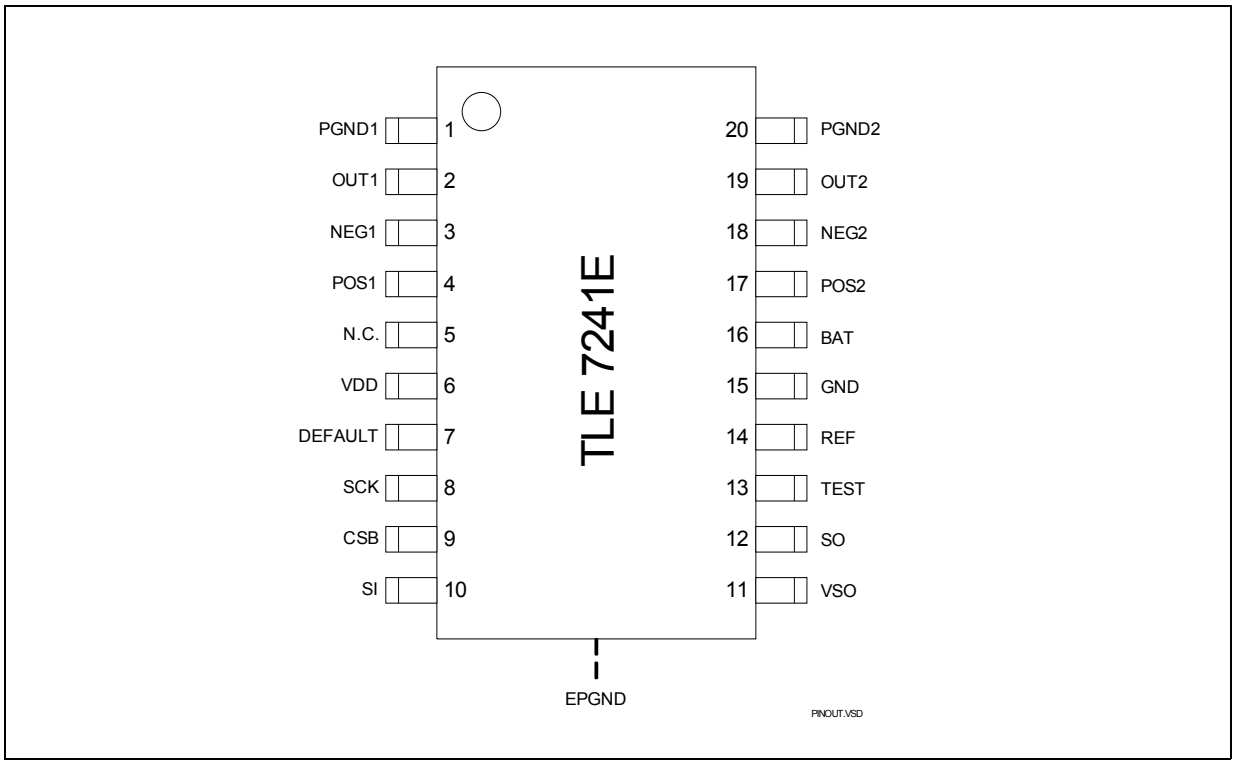

Figure 3 Pin-Out

Pin Definitions and Functions

Pin	Pin Name	Pin Description
1	PGND1	**Power Ground Channel 1;** internally connected to PGND2
2	OUT1	**Output Channel 1**; Drain of Output DMOS; connect to negative terminal of external sense resistor
3	NEG1	**Negative Sense Pin Channel 1**; connect to negative terminal of external sense resistor with dedicated trace
4	POS1	**Positive Sense Pin Channel 1**; connect to positive terminal of external sense resistor with dedicated trace
5	NC	**Not Connected;** not bonded internally
6	V_{DD}	**Logic Supply Voltage;** connect a ceramic capacitor to GND near the device
7	DEFAULT	**Control Input;** Active high digital input. 3.3V and 5.0V logic compatible. In case of not used, connect to ground

Pin Definitions and Functions (cont'd)

Pin	Pin Name	Pin Description
8	SCK	**SPI Clock**; Digital input pin. 3.3V and 5.0V logic compatible
9	CSB	**Chip Select Bar**; Active low digital input pin. 3.3V and 5.0V logic compatible
10	SI	**Serial Data Input;** 3.3V and 5.0V logic compatible
11	V_{SO}	**SPI Supply Voltage;** connect a ceramic capacitor to GND near the device
12	SO	**Serial Data Output**; Supplied by Vso pin
13	TEST	**Test Pin;** connect to GND
14	REF	**Voltage Reference;** connect to external 2.5 V reference, or connect to GND to enable internal reference.
15	GND	**Ground**; signal ground
16	BAT	**BAT Input;** connect to the solenoid supply voltage through a series resistor. Connect a ceramic capacitor to GND near the device
17	POS2	**Positive Sense Pin Channel 2**; connect to positive terminal of external sense resistor with dedicated trace
18	NEG2	**Negative Sense Pin Channel 2**; connect to negative terminal of external sense resistor with dedicated trace
19	OUT2	**Output Channel 2**; Drain of Output DMOS; connect to negative terminal of external sense resistor
20	PGND2	**Power Ground Channel 2;** internally connected to PGND1
Exposed Lead Frame	EPGND	**GND;** Should be connected to GND, PGND1 and PGND2 and to the ground plane of the ECU

Note: If a channel is unused, the OUTx, NEGx, and POSx pins should be connected together.

3 Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 to 150 °C

Pos.	Parameter	Symbol	Limit Values		Unit	Notes
			Min.	Max.		
Voltages						
M.1	Supply Voltage	BAT V_{DD} V_{SO}	-0.3 -0.3 -0.3	50 6.0 6.0	Vdc Vdc Vdc	–
M.2	Analog Input Voltage	POSx NEGx POSx-NEGx	-0.3 -0.3 -0.3	50 50 20	Vdc Vdc Vdc	–
M.3	Output Voltage	OUTx	-0.3	50	Vdc	–
M.4	Digital Input Voltage	REF TEST SI SCK CSB DEFAULT	-0.3 -0.3 -0.3 -0.3 -0.3 -0.3	min. (6.0, V_{DD} + 0.3) 6.0 6.0 6.0 min. (6.0, V_{SO} + 0.3) min. (6.0, V_{SO} + 0.3)	Vdc Vdc Vdc Vdc Vdc Vdc	–
M.5	Digital Output Pin Voltage	SO	-0.3	min. (6.0, V_{SO} + 0.3)	Vdc	–
M.6	Dynamic Clamp Voltage T_{clamp} < 2.0 ms	BAT POSx NEGx OUTx	-1.5 -1.5 -1.5 -1.5	– – – –	V V V V	–
M.7	Ground Pin Voltage (GND)	GND	-0.3	0.3	Vdc	–
M.8	Difference between PGND1 and PGND2	PGNDx	-0.3	0.3	Vdc	–
Others						
M.9	Biased Junction Temperature	T_j	-40	150	°C	–
M.10	Storage Temperature	T_{st}	-55	150	°C	–
M.11	Single Clamp Energy (OUTx) I=1.0A Tj=150 °C	E_{max}	–	30	mJ	–

Absolute Maximum Ratings[1] (cont'd)

T_j = -40 to 150 °C

Pos.	Parameter	Symbol	Limit Values		Unit	Notes
			Min.	Max.		
M.12	ESD HBM all pins EIA/JESD22-A 114B (1.5 K Ω, 100 pF)	–	-2	+2	kV	–
M.13	ESD MM all pins EIA/JESD22-A115A (0 Ω, 200 pF)	–	-200	200	V	–

1) Not subject to production test, specified by design

All voltages are with respect to PGND1 & 2. Positive current flows into the pin unless otherwise specified.

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4 Functional Range

Functional Range

T_j = -40 to 150 °C; V_{REF} = 2.5V

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
F.1	Voltage at BAT	V_{BAT}	9	18	V	–
F.2	Voltage at V_{DD}	V_{DD}	4.75	5.25	V	–
F.3	Voltage at VSO	V_{VSO}	3.1	V_{DD} + 0.3 or 5.25V	V	–
F.4	Voltage at SI, SCK	V_{IN1}	-0.3	V_{DD} + 0.3	V	–
F.5	Voltage at CSB, DEFAULT, SO	V_{IN2}	-0.3	V_{SO} + 0.3	V	–
F.6	Voltage at POS1, POS2, NEG1, NEG2, OUT1, OUT2	V_{OUT}, V_{POS}, V_{NEG}	-0.3	50	V	–
F.7	Voltage Difference POS1-NEG1, POS2-NEG2	V_{POS} - V_{NEG}	0	1.23	V	–
F.8	Voltage at PGND1, PGND2, GND	V_{GND}	-0.3	0.3	V	–
F.9	SPI Clock Frequency	f_{clk}		3.2	MHz	C_{SO} = 200 pF max; V_{VSO} = 5 V
F.10	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.1 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
G.1	Junction to Case[1)]	R_{thjC}			5.2	K/W	[2)]
G.2	Junction to Ambient[1)]	R_{thjA}		26		K/W	[2) 3)]

1) Not subject to production test, specified by design.
2) Both channels on with 1W power dissipation per channel
3) Specified RthJA value is according to Jedec JESD51-2, -5, -7 at natural convection on FR4 2s2p board. The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70mm Cu, 2 x 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner layer.

5 Functional Description and Electrical Characteristics

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

5.1 Supply and Reference

The device has incorporated a power-on reset circuit. This feature will reset the commanded average current to 0 mA (device off), and will reset the programmable registers to their default values. The fault register bits are reset during power on reset. The device will remain off until a valid command is received. The device will also be reset in the case of an undervoltage condition on the pin V_{DD}. Note that if the voltage on the pin *REF* pin is greater than the voltage on the pin $V_{DD,}$ a current will flow from the *REF* pin to the V_{DD} pin.

Electrical Characteristics [1]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2]	Max.		
5.1.1	REF Bias Current	I_{REF}	-20	–	20	µA	V_{REF} = 2.5 V (includes leakage current and a small current sink)
5.1.2	V_{DD} 5 V Supply Current	I_{DD}	–	–	15	mA	V_{DD} = 5.25 V; CSB = 5.0 V; DAC = 3FF
5.1.3	V_{SO} I/O Supply Current	I_{SO}	–	–	1	mA	V_{SO} = 5.25 V; CSB = 5.0 V
5.1.4	BAT Supply Current	I_{BAT}	–	–	1	mA	V_{DD} = 5.25 V; CSB = 5.0 V
5.1.5	V_{DD} Power-On Reset Threshold	V_{POR}	2.5	–	3.5	V	Power-On Reset Threshold
5.1.6	Internal Reference Voltage	V_{IREF}	2.45	2.5	2.55	V	Tested at wafer test.

1) Positive current flow is into the device.

2) Target @T_J = 25 °C

5.2 Input/Output

The DEFAULT pin is an active high input. A weak pull-up current (typical 15 µA) on this pin ensures a defined level when this pin is not connected (e.g. open pin). An active high signal on the DEFAULT pin sets the commanded current for both channels to 0 mA, and resets all programmable registers to their default values. Any SPI commands that are received while the DEFAULT pin is high will be ignored, and the SO pin will remain in a high impedance state.

The fault register bits are not cleared when the Default pin is asserted.

Upon coming out of default mode, the commanded current will remain at 0 mA, device off, and the programmable registers will remain at their default values.

The DEFAULT pin must be asserted high whenever the voltage on the pin V_{DD} is less than the minimum V_{DD} operating voltage (4.75 V), otherwise the electrical characteristic specifications (see table below) may not be met. The diagnostic functions are not operational when the V_{DD} voltage is less than 4.75V.

The TEST pin is an active high pin. This pin must be connected directly to ground in the application, as it is only used for IC test purposes. A passive pull-down resistor in the device ensures a logic low value when the pin is not connected.

Electrical Characteristics [1]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2]	Max.		
5.2.1	DEFAULT Input Bias Current	$I_{DEFAULT}$	-25	-10	-5	µA	$V_{DEFAULT}$ = 0 V; Pull-up source is pin V_{SO}
5.2.2	TEST Pull-down Resistor	R_{TEST}	–	20	–	kΩ	–
5.2.3	SI, SCK, CSB, DEFAULT Input Threshold	V_{IH}	2.0	–	–	V	SCK is specified by design, not subject to production test.
5.2.4	SI, SCK, CSB, DEFAULT Input Threshold	V_{IL}	–	–	0.8	V	SCK is specified by design, not subject to production test.
5.2.5	SO Output High Voltage	V_{OH}	0.8 V_{SO}	–	–	V	SO I_o = -1 mA
5.2.6	SO Output Low Voltage	V_{OL}	–	–	0.4	V	SO I_o = 1 mA

1) Positive current flow is into the device.

2) Target @T_J = 25 °C

5.3 Power Output

The slew rate of the voltage on the pins OUT1 and OUT2 are programmable via the SPI interface. The fast settings are intended for fast switching solenoids (low inductance) to minimize power dissipation within the TLE 7241E, and to minimize DC current error due to overshooting the switch points. The slower slew rates can be used with slower switching solenoids (high inductance) to improve radiated emissions from the wiring harness.

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.3.1	OUTx rise and fall times Slew Rate reg = 0	OUTx t_R and t_F	0.25	0.5	1	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.2	OUTx rise and fall times Slew Rate reg = 1	OUTx t_R and t_F	0.5	1	2	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.3	OUTx rise and fall times Slew Rate reg = 2	OUTx t_R and t_F	1	2	4	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.4	OUTx rise and fall times Slew Rate reg = 3	OUTx t_R and t_F	2.5	5	10	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.5	OUTx Output Off Leakage (00_H)	I_{DSS}	–	–	10	µA	V_{DS} = 24 V
5.3.6	OUTx Output Off Leakage (00_H)	I_{DSS}	–	–	3	mA	V_{DS} = V_{CLAMP} - 1V V_{CLAMP} is the measured clamp voltage (**Item 5.4.1.3**)
5.3.7	OUTx[3)] Driver on Resistance	$R_{DS(ON)}$	–	240	450	mΩ	Driver on Resistance @T_J = 150 °C

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Electrical Distributions must be performed on this parameter as defined in the AEC-Q100 Specification Table 2 test 27.

5.4 Protection and Control

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.1	POS/NEG IBIAS	POS/NEG IBIAS	-500	–	500	µA	DAC command =3FF POS=NEG=0V & POS=NEG=17V
5.4.2	POS/NEG LEAKAGE	POS/NEG LEAKAGE	20	40	60	µA	Fault typing bit = 0, Zero Current, POS = NEG = 14 V
			-20	0	20	µA	Fault typing bit = 1, Zero Current, POS = NEG = 14 V

1) Positive current flow is into the device.

2) T_J = 25 °C

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.

5.4.1 Overvoltage Sensing and Protection

When the voltage on the BAT pin exceeds the Overvoltage Shutdown Threshold (see table below, **Item 5.4.1.1**), the output channel will shut off to protect the IC from excessive power dissipation. A short filter with a typical value of 6.5 µs is included to prevent undesired shutdown due to short transient voltage spikes. Although SPI communication will remain functional, the output will remain off. The device will resume normal operation when the BAT voltage has dropped below the overvoltage hysteresis level. Note that the programmable registers are not reset, and the dither counter continues to operate during an overvoltage event.

Both channels are disabled when an overvoltage condition is detected.

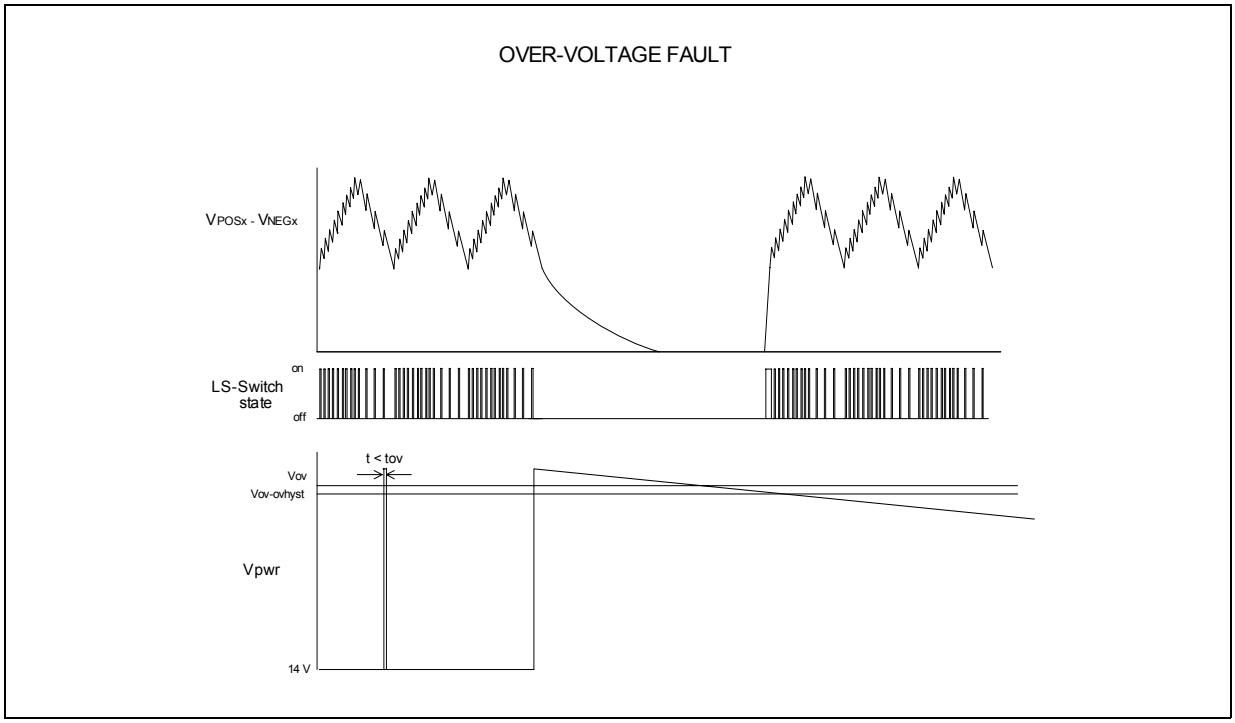

Figure 4 Overvoltage Shutdown

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.1.1	BAT Overvoltage Shutdown	OV	30	35	40	Vdc	Ramp up BAT until outputs Off
5.4.1.2	BAT Overvoltage hysteresis	OV_{HYST}	–	1.0	–	Vdc	Ramp BAT down until outputs On[3)]
5.4.1.3	OUTx Active Clamp Voltage	V_{clamp}	50	53	60	V	I_d = 20 mA, output off

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, specified by design.

5.4.2 Overcurrent / Short to V_{BAT} Sensing

An overcurrent fault is detected by sensing the voltage at the POS input pin. A comparator is used to detect the voltage while the gate drive is on. When the voltage at the POS input pin exceeds the short circuit / overcurrent threshold (see table below, **Item 5.4.2.3**) for a time greater than the short sense time (see table below, **Item 5.4.2.1**)

the driver will be turned off and the Overcurrent / Short to V_{BAT} (V_{SHT}) fault bit will be latched until the fault register is read via SPI. The driver will remain in the off condition for the short circuit refresh time (see table below, **Item 5.4.2.2**). After the refresh time, the driver will automatically turn on again. If the short condition is no longer present, the channel will operate normally. If the short circuit condition persists, the driver will be cycled off after the short sense time once again. The refresh time has been chosen for minimal increase in power dissipation during a continuous fault condition.

In order to prevent false detection of an overcurrent / short to V_{BAT} fault during an “off to on” transition of the low-side output transistor, the detection circuit is disabled for a blanking time (see **“Electrical Characteristics” on Page 31**, **Item 5.5.1.1** and **Item 5.5.1.2**) after the transistor is enabled (see **Figure 16** and **Figure 17**).

The output transistor control circuit includes a current limit feature that will limit the transistor current to a maximum value (see table below, **Item 5.4.2.4**) in order to protect the device from excessive current flow.

If a new average current command or configuration command is received for a shorted channel while that channel is within the short circuit refresh time, the new data will be stored but the channel will remain in the off state until the refresh time expires. The new data will become active when the short circuit condition is released.

The Overcurrent / Short to VBAT detection is channel specific.

Note: An Overcurrent / Short to VBAT fault is not detected if the average current command is <50 mA (with 1 W sense resistor).

Note: An overcurrent / short to V_{BAT} fault is latched until read via the MISO return word.

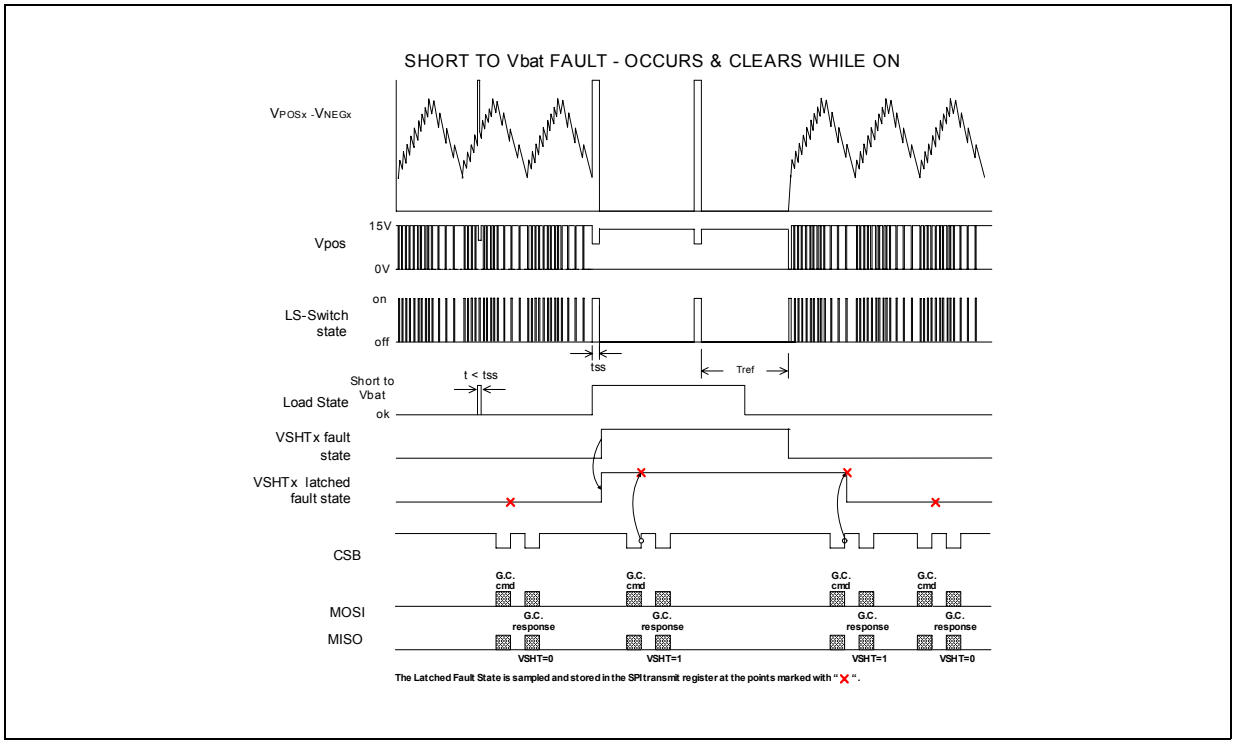

Figure 5 Short to V_{BAT} - Channel On

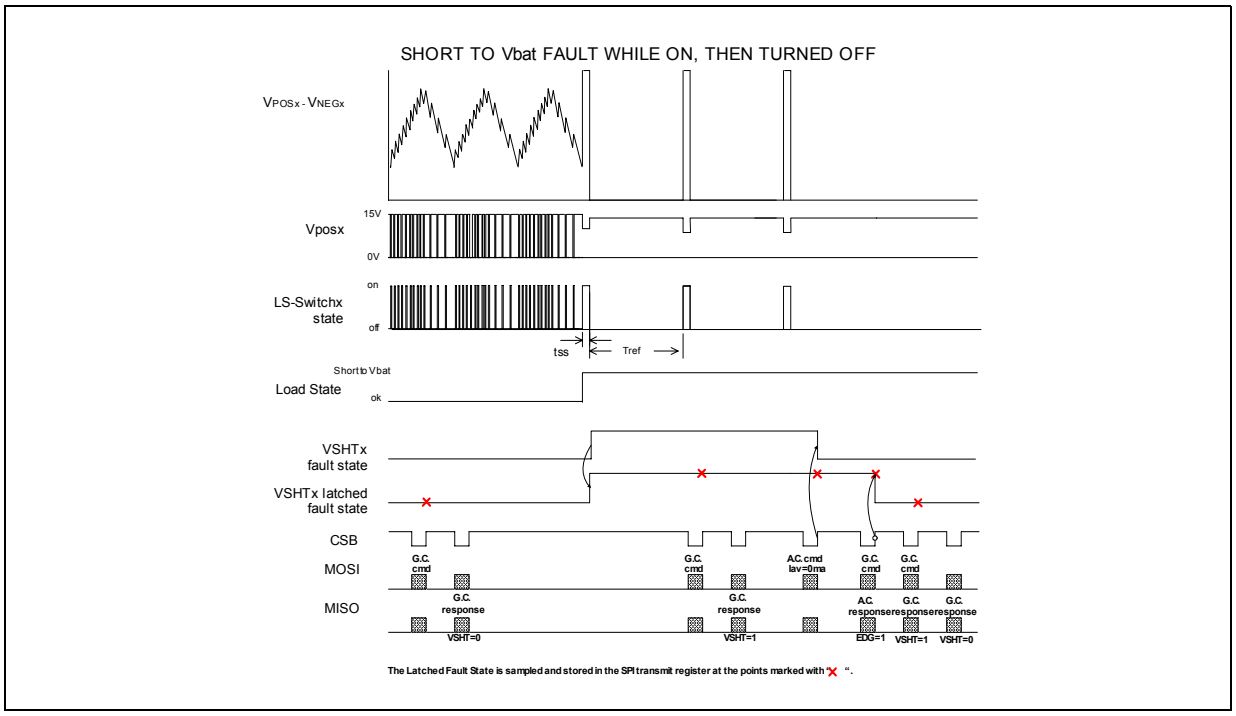

Figure 6 Short to V_{BAT} - Channel On Then Turned Off

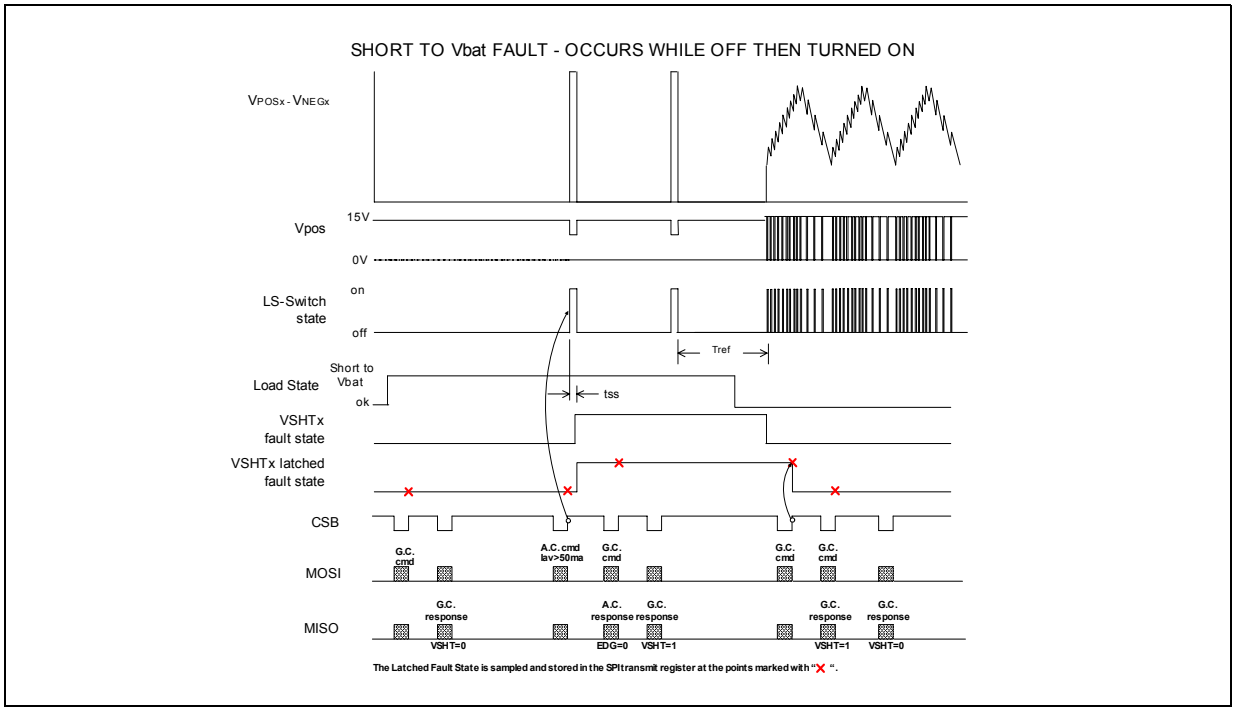

Figure 7 Short to V_{BAT} - Channel Off Then Turned On

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.2.1	OUTx Short Sense Time	t_{ss}	30	60	90	µs	50 - 50 Threshold
5.4.2.2	OUTx Short Refresh Time	t_{ref}	3	14	24	ms	50 - 50 Threshold
5.4.2.3	OUTx Short circuit/ Overcurrent Fault Threshold	$V_{VSHTOCT}$	2.0	2.5	3.0	Vdc	V_{REF} = 2.5 V
5.4.2.4	OUTx Current Limit	I_{dlim}	3.0	5.0	6.0	A	V_{BAT} = 14 V; V_{DD} = 5V; output on

1) Positive current flow is into the device.

2) T_J = 25 °C

5.4.3 Open Load / Short to Ground Detection

The OLSG fault bit is set under the following conditions.

Operating Condition #1

The average current command is > 50 mA (with 1 Ω sense resistor) and the low-side driver is ON (solenoid current is increasing).

The OLSG (open load/short to ground) fault bit will be set if the low-side transistor remains on for a time greater than the on state open sense time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.3**).

Operating Condition #2

The average current command is > 50 mA (with 1 Ω sense resistor) and the low-side driver is OFF.

The OLSG fault bit is set if the voltage on the NEGx pin is less than the NEG pin OLSG threshold voltage (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.6**) for a time greater than the NEG pin OLSG delay time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.5**).

Operating Condition #3

The average current command is < 50 mA (with a 1 Ω sense resistor) and the fault typing bit = 0.

The OLSG (open load/short to ground) fault bit will be set if the POS pin voltage is less than the off state open load threshold (**"Electrical Characteristics" on Page 20**, **Item 5.4.2.3**) for longer than the off state open load sense time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.4**) or the NEG pin is less than the NEG pin OLSG threshold voltage (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.6**) for a time greater than the NEG pin OLSG delay time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.5**). A pull-down current (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.1**) will be activated between the POS pin and ground when the Fault Typing bit = 0.

Operating Condition #4

The average current command is < 50 mA (with a 1 Ω sense resistor) and the fault typing bit = 1.

The OLSG fault bit will be set when the voltage on the pin POSx is below the off state open load threshold (**"Electrical Characteristics" on Page 20**, **Item 5.4.2.3**) for the a time greater than $t_{os(off)}$ (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.4**) or the NEG pin is less than the NEG pin OLSG threshold voltage (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.6**) for a time greater than the NEG pin OLSG delay time

(**“Electrical Characteristics” on Page 23**, **Item 5.4.3.5**). A pull-up current (**“Electrical Characteristics” on Page 23**, **Item 5.4.3.2**) will be activated between V_{DD} and the POS pin when the Fault Typing bit = 1.

Distinguishing between Open Load and Short to Ground Faults

When an Open Load/Short to Ground is flagged, to distinguish between Open Load and Short-To-Ground, a general configuration command word must be sent three times to the appropriate channel with the fault typing bit set, and the average current must be programmed to zero. Check the OL/SG fault bit from the third write. A ‘0’ signifies Open Load, ‘1’ signifies Short-To-Ground. A short to ground will still be flagged for 0 mA command current. Note that setting the fault typing bit under both normal & fault conditions does not change the status of the output or the current flowing.

The fault typing bit enables a 40 µA pull-up current on the POS pin when high, and enables a 40 µA pull-down current on the POS pin when low.

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.3.1	POS Open detect current	I_{OL}	20	40	60	µA	Fault typing bit = 0, Zero Current
5.4.3.2	POS Load short to ground detect	I_{SG}	-60	-40	-20	µA	Fault typing bit = 1, Zero Current, POS = NEG = 2 V
5.4.3.3	OUTx On-State open sense time – POS pin	$t_{os}(on)$	6	12	24	ms	50 - 50 Threshold[3)]
5.4.3.4	OUTx Off-State open sense time – POS pin	$t_{os}(off)$	30	60	90	µs	50 - 50 Threshold[3)]
5.4.3.5	NEGx Open load / short to ground filter time – NEG pin	T_{OLSG_N} (off)	30	60	90	µs	–
5.4.3.6	NEGx Open load / short to ground detection threshold – NEG pin	V_{OLSG_N}	2.0	2.8	3.6	V	–

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, tested by scanpath.

Diagnostics Timing Diagrams

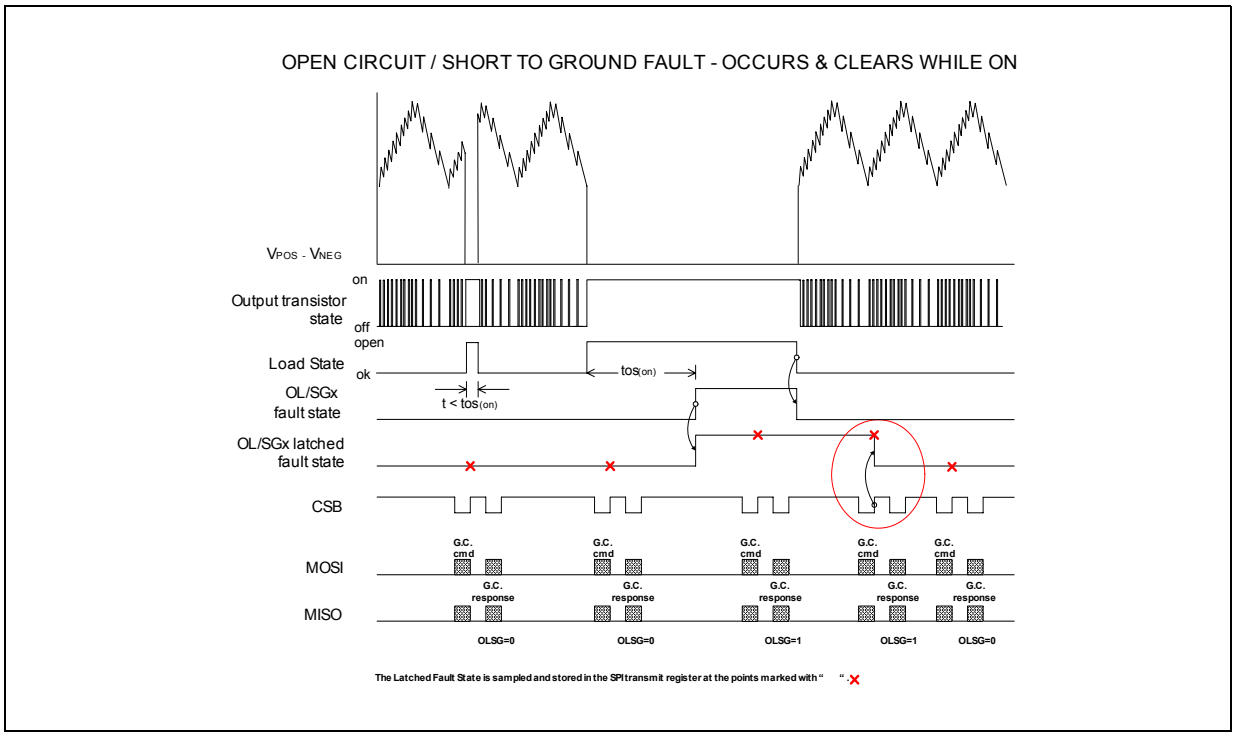

Figure 8 Open Load / Short to Ground Fault - Channel On

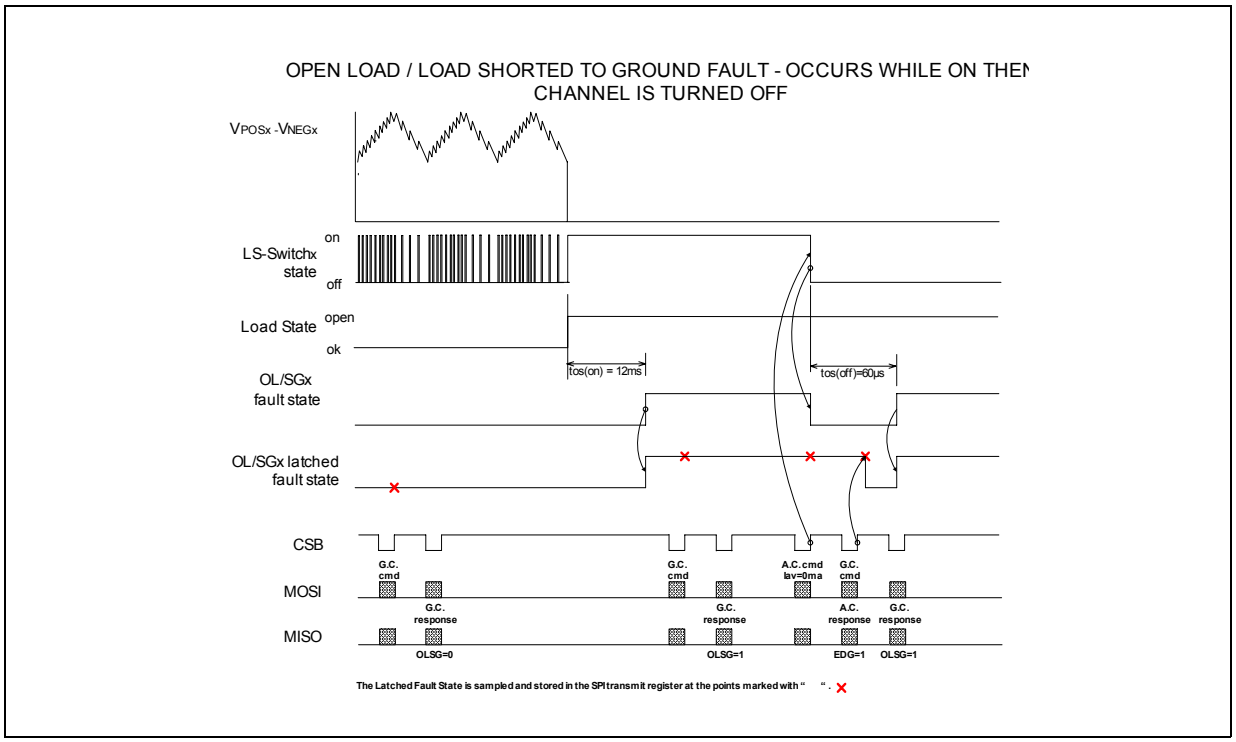

Figure 9 Open Load / Short to Ground - Channel On Then Turned Off

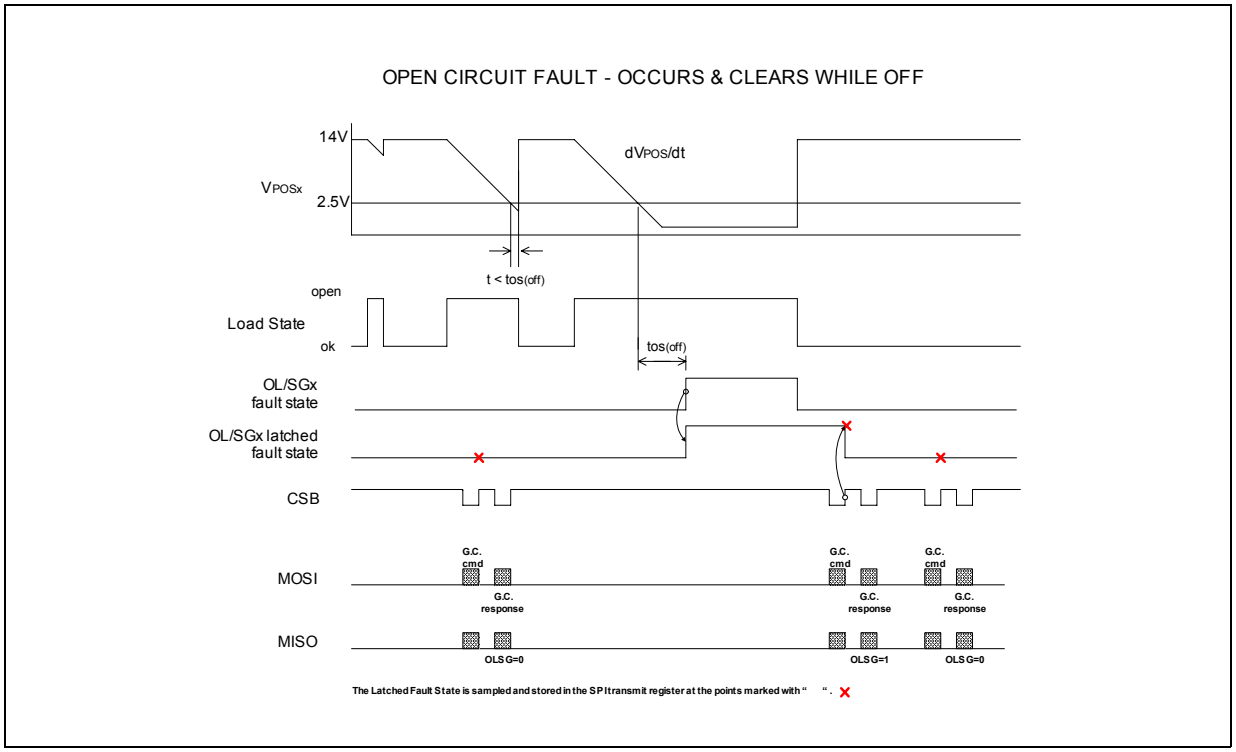

Figure 10 Open Load Short to Ground - Channel Off

$$\frac{\mathrm{d}V_{POS}}{\mathrm{d}t} = \frac{-(i_{OL} - i_{Rrecirc})}{(C_{POS} + C_{NEG} + C_{OUT})} \quad (1)$$

i_{OL} = open load detection pull down current (5.4.3.1)

$i_{Rrecirc}$ = reverse leakage current of recirculation diode

C_{POS} = external capacitance on the POS pin

C_{NEG} = external capacitance of the NEG pin

C_{OUT} = external capacitance on the OUT pin

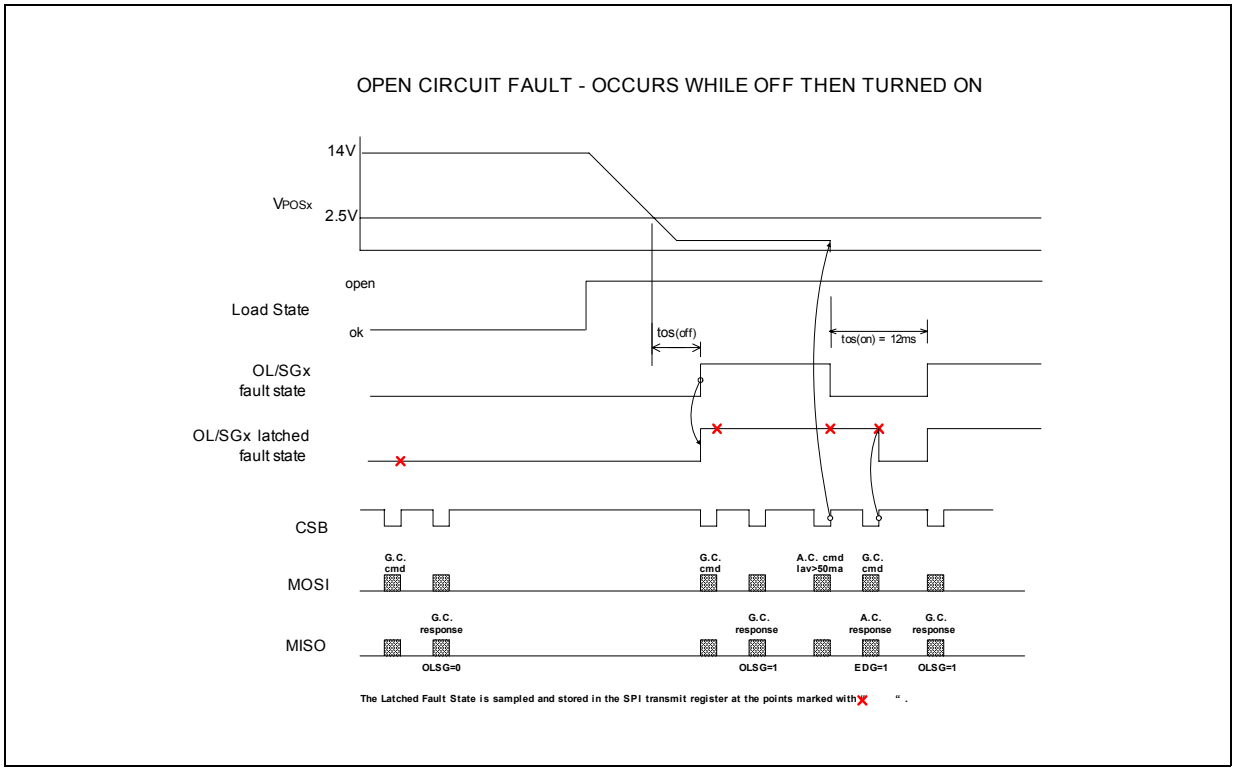

Figure 11 Open Load / Short to Ground - Channel Off Then Turned On

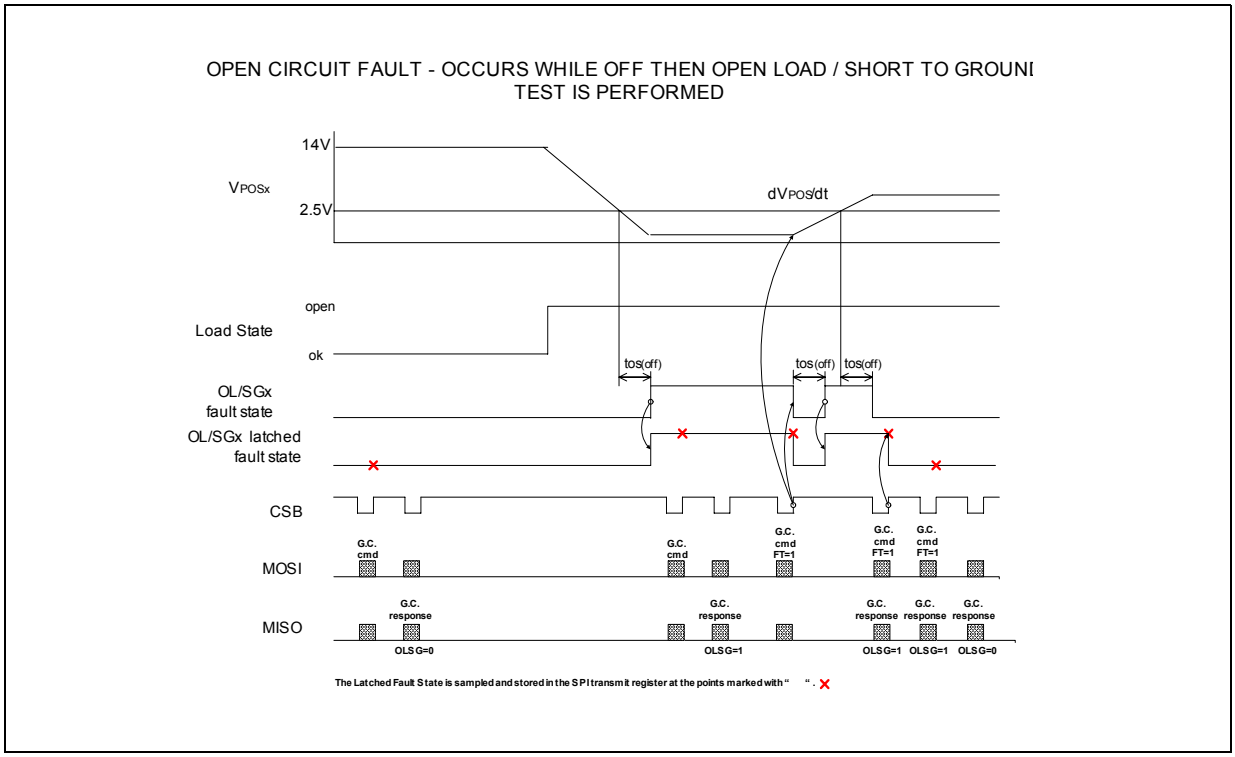

Figure 12 Open Load - Fault Type Bit = 1 Test

$$\frac{\mathrm{d}V_{POS}}{\mathrm{d}t} = \frac{-(i_{SG} - i_{Rrecirc})}{(C_{POS} + C_{NEG} + C_{OUT})} \quad (2)$$

i_{SG} = short to ground detection pull up current (5.4.3.2)

$i_{Rrecirc}$ = reverse leakage current of recirculation diode

C_{POS} = external capacitance on the POS pin

C_{NEG} = external capacitance of the NEG pin

C_{OUT} = external capacitance on the OUT pin

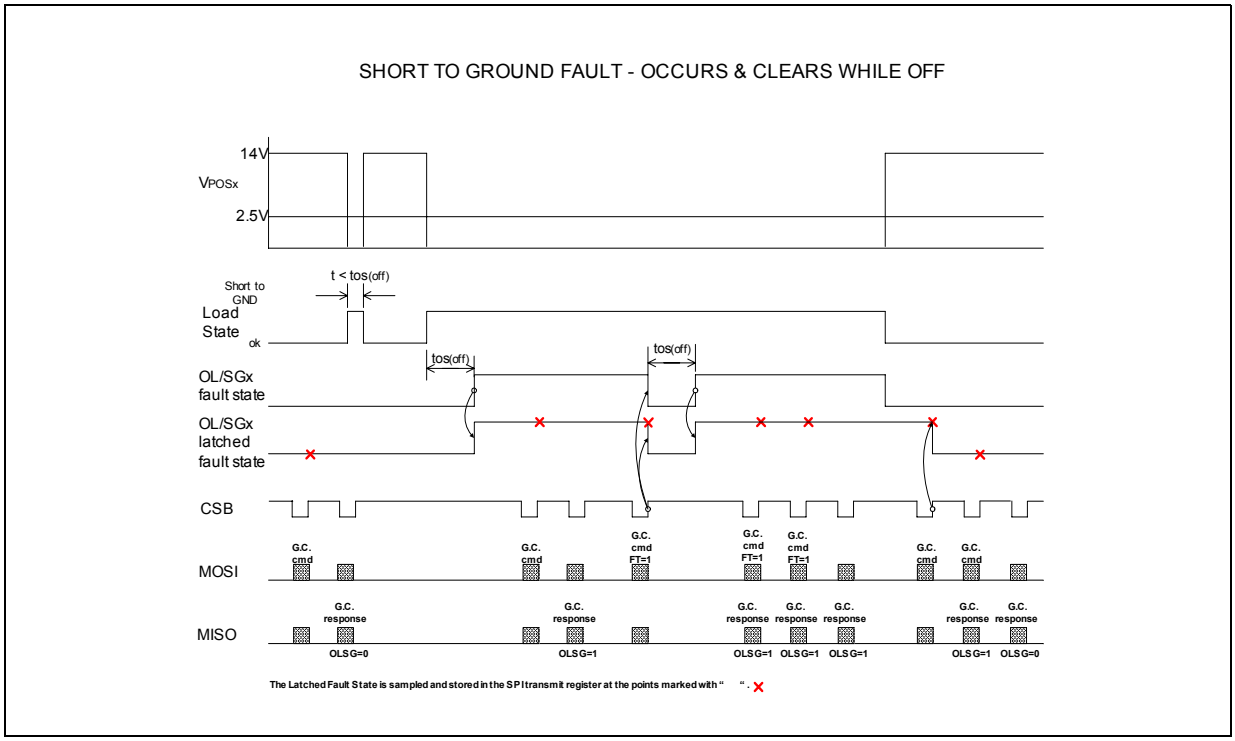

Figure 13 Short to Ground Fault Type Bit = 1 Test

5.4.4 Thermal Shutdown

Each output transistor includes an independent thermal shutdown circuit. When the temperature of the output transistor exceeds a threshold value (see table below, **Item 5.4.4.1**), the output transistor will be turned off and a fault bit will be set for the failed channel. The transistor will remain off until the local transistor temperature has decreased by the thermal hysteresis value (see table below, **Item 5.4.4.2**), the output transistor will then turn on again.

Thermal shutdown faults are channel specific.

Note: A thermal fault is latched until read via the MISO return word.

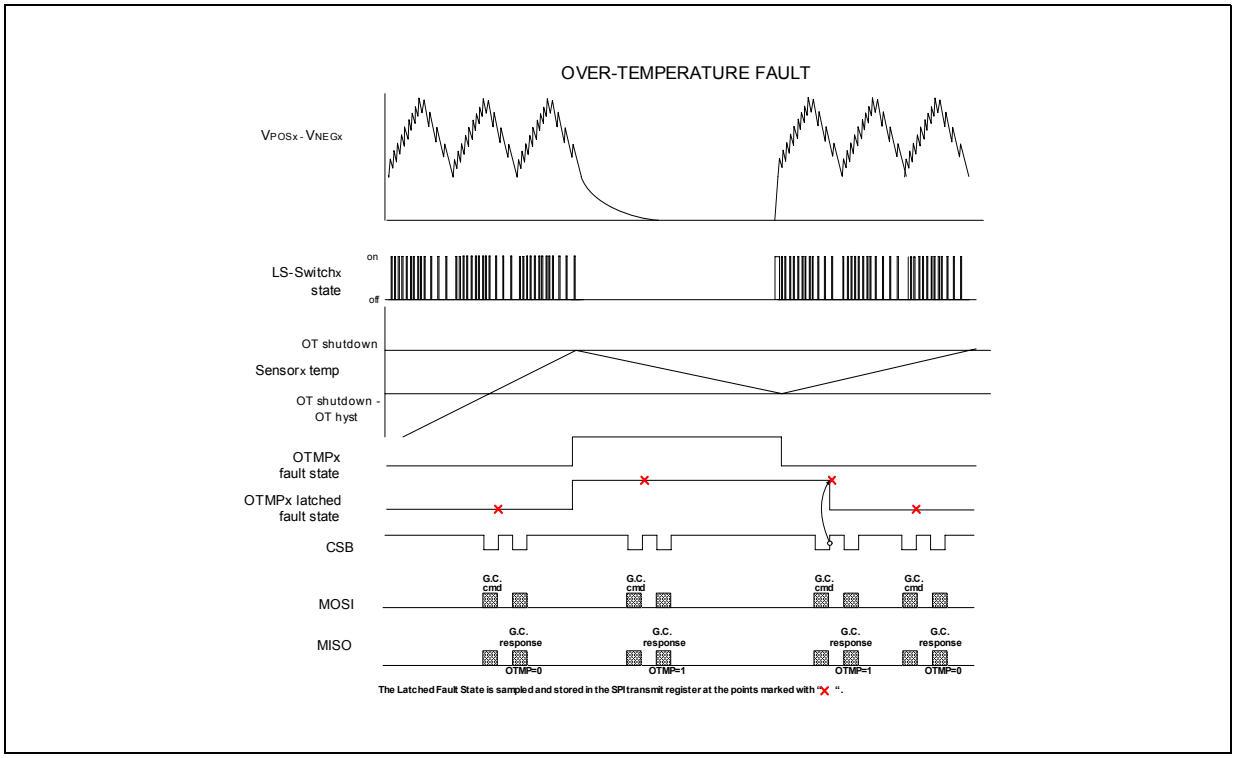

Figure 14 Overtemperature Shutdown with Restart

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.4.1	OUTx Overtemperature shutdown threshold	OTsd	160	–	190	°C	3)
5.4.4.2	OUTx Overtemperature hysteresis	OThys	–	10	–	°C	3)

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, specified by design.

5.5 Current Control

5.5.1 Hysteretic Current Control

The TLE 7241E device uses a hysteretic control method to regulate the solenoid current. The output transistor is toggled on and off based on the measured value of the solenoid current. The solenoid current is measured at the pins POSx and NEGx which are connected to an external current sense resistor. The device calculates an upper and lower switch point based on the input commands from the microprocessor. The output transistor is turned on until the upper threshold is reached, and then turned off until the lower threshold is reached. See **Figure 15** for an example of the solenoid current waveform. In this example, the dither is disabled.

The average switch point

$$SP_{AVG} = \frac{\text{Upper switch pt + Lower switch pt}}{2} \quad (3)$$

is determined by the contents of the average current command register.

The relationship is:

$$SP_{AVG} = \frac{\text{register value}}{2^{10}} \times 1230\ \text{mV} \quad (4)$$

The hysteresis value can be programmed to a value from 40 mVpp to 110 mVpp in steps of 10 mVpp.

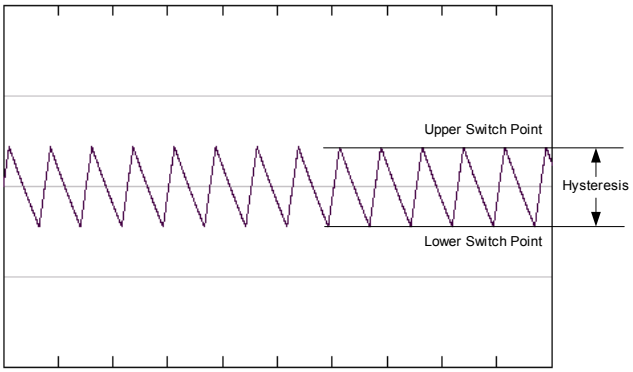

Figure 15 Output Current Waveform - No Dither

Note that the switching frequency and duty cycle of the output transistor are not directly controlled by the TLE 7241E device and are dependent on the characteristics of the solenoid (inductance, resistance, etc.) and the solenoid supply voltage.

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.5.1.1	OUTx[3)] Blanking time 1 (see **Figure 16**, **Figure 17**)	T_{blank1}	–	5	–	µs	Slew Rate Register = 0 or 1. From enable/disable of lowside output transistor to enabling of V_{pos} comparator.
5.5.1.2	OUTx[3)] Blanking time 2 (see **Figure 16**, **Figure 17**)	T_{blank2}	–	15	–	µs	Slew Rate Register = 2 or 3. From enable/disable of output transistor to enabling of V_{pos} comparator.
5.5.1.3	OUTx[4)5)] dV_{OUT} = 200 mV I_{avg} register = $0A6_H$	$dV_{OUT\ 200}$	-5%	200	+5%	mV	Output current I_{OUT} = 200 mA with R_{sense} = 1.0 Ω *REF* = 2.5V
5.5.1.4	OUTx[4)5)] dV_{OUT} = 400 mV I_{avg} register = $14D_H$	$dV_{OUT\ 400}$	-2.5 %	400	2.5%	mV	Output current I_{OUT} = 400 mA with R_{sense} = 1.0 Ω *REF* = 2.5V
5.5.1.5	OUTx[4)5)] dV_{OUT} = 600 mV I_{avg} register = $1F3_H$	$dV_{OUT\ 600}$	-2%	600	2%	mV	Output current I_{OUT} = 600 mA with R_{sense} = 1.0 Ω *REF* = 2.5V
5.5.1.6	OUTx[4)5)] dV_{OUT} = 800 mV I_{avg} register = $29A_H$	$dV_{OUT\ 800}$	-2%	800	2%	mV	Output current I_{OUT} = 800 mA with R_{sense} = 1.0 Ω *REF* = 2.5V

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.5.1.7	OUTx[4)5)] dV_{OUT} = 1000 mV I_{avg} register = 340_H	$dV_{OUT1000}$	-3%	1000	3%	mV	Output current I_{OUT} = 1000 mA with R_{sense} = 1.0 Ω *REF* = 2.5V
5.5.1.8	OUTx[3)5)] Switching hysteresis 40 Sw Hyst. register = 0 DAC counts = ±17	dV_{hyst40}	29.6	39.6	49.6	mVpp	40 mV programmed setting Input Command > 200 mV *REF* = 2.5V
5.5.1.9	OUTx[3)5)] Switching hysteresis 50 Sw Hyst. register = 1 DAC counts = ±21	dV_{hyst50}	40.4	50.4	60.4	mVpp	50 mV programmed setting Input Command > 200 mV *REF* = 2.5V
5.5.1.10	OUTx[3)5)] Switching hysteresis 60 Sw Hyst. register = 2 DAC counts = ±25	dV_{hyst60}	50.1	60.1	70.1	mVpp	60 mV programmed setting Input Command > 200 mV *REF* = 2.5V

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.5.1.11	OUTx[3)5)] Switching hysteresis 70 Sw Hyst. register = 3 DAC counts = ±29	dV_{hyst70}	59.7	69.7	79.7	mVpp	70 mV programmed setting Input Command > 200 mV *REF* = 2.5V
5.5.1.12	OUTx[3)5)] Switching hysteresis 80 Sw Hyst. register = 4 DAC counts = ±33	dV_{hyst80}	70.5	80.5	90.5	mVpp	80 mV programmed setting Input Command > 200 mV *REF* = 2.5V
5.5.1.13	OUTx[3)5)] Switching hysteresis 90 Sw Hyst. register = 5 DAC counts = ±37	dV_{hyst90}	80.1	90.1	101.1	mVpp	90 mV programmed setting Input Command > 200 mV *REF* = 2.5V

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.5.1.14	OUTx[3)5)] Switching hysteresis 100 Sw Hyst. register = 6 DAC counts = ±42	$dV_{hyst100}$	88.7	99.7	109.7	mVpp	100 mV programmed setting Input Command > 200 mV *REF* = 2.5V
5.5.1.15	OUTx[3)5)] Switching hysteresis 110 Sw Hyst. register = 7 DAC counts = ±46	$dV_{hyst110}$	100.5	110.5	120.5	mVpp	110 mV programmed setting Input Command > 200 mV *REF* = 2.5V

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, specified by design.

4) Electrical Distributions must be performed on this parameter as defined in the AEC-Q100 Specification Table 2 test 27.

5) When the internal reference is used (REF pin grounded), the minimum and maximum limits must be increased by +/- 2%

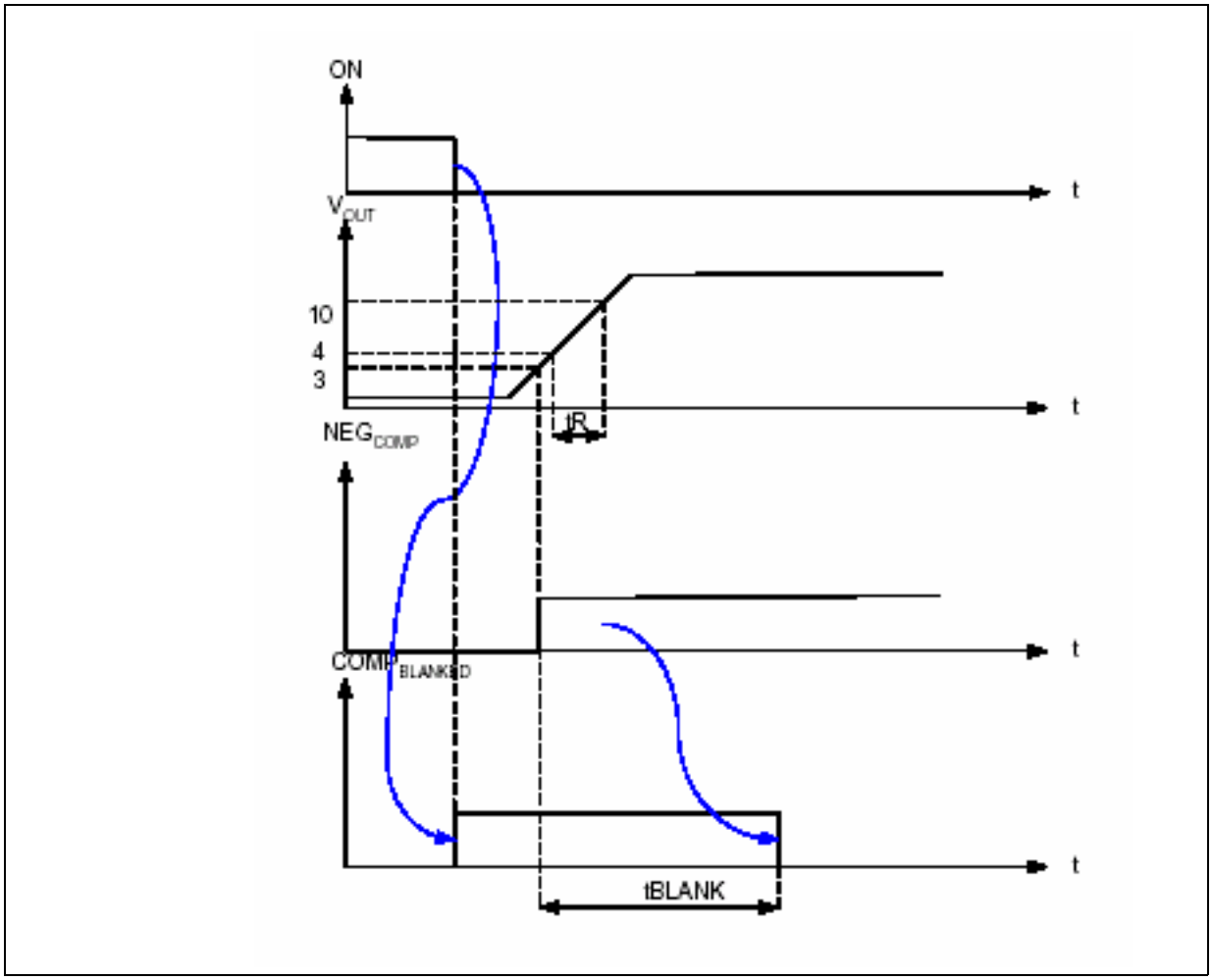

Figure 16 Blanking Time (output transistor turning off)

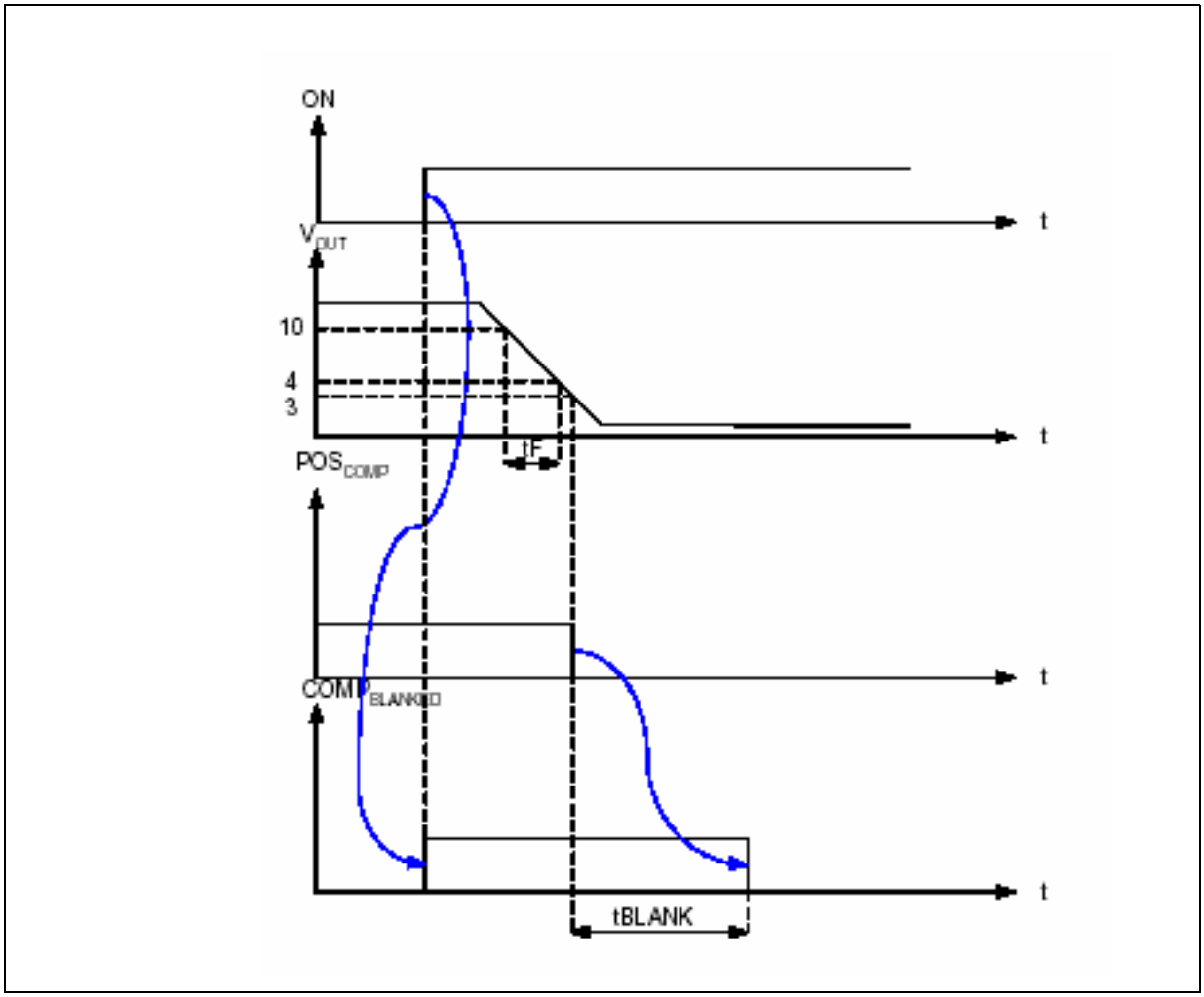

Figure 17 Blanking Time (output transistor turning on)

5.5.2 Dither Control and Operation

The dither waveform is generated digitally within the TLE 7241E by periodically adding or subtracting from the average current command register contents. **Figure 18** is an illustration of the Dither Waveform.

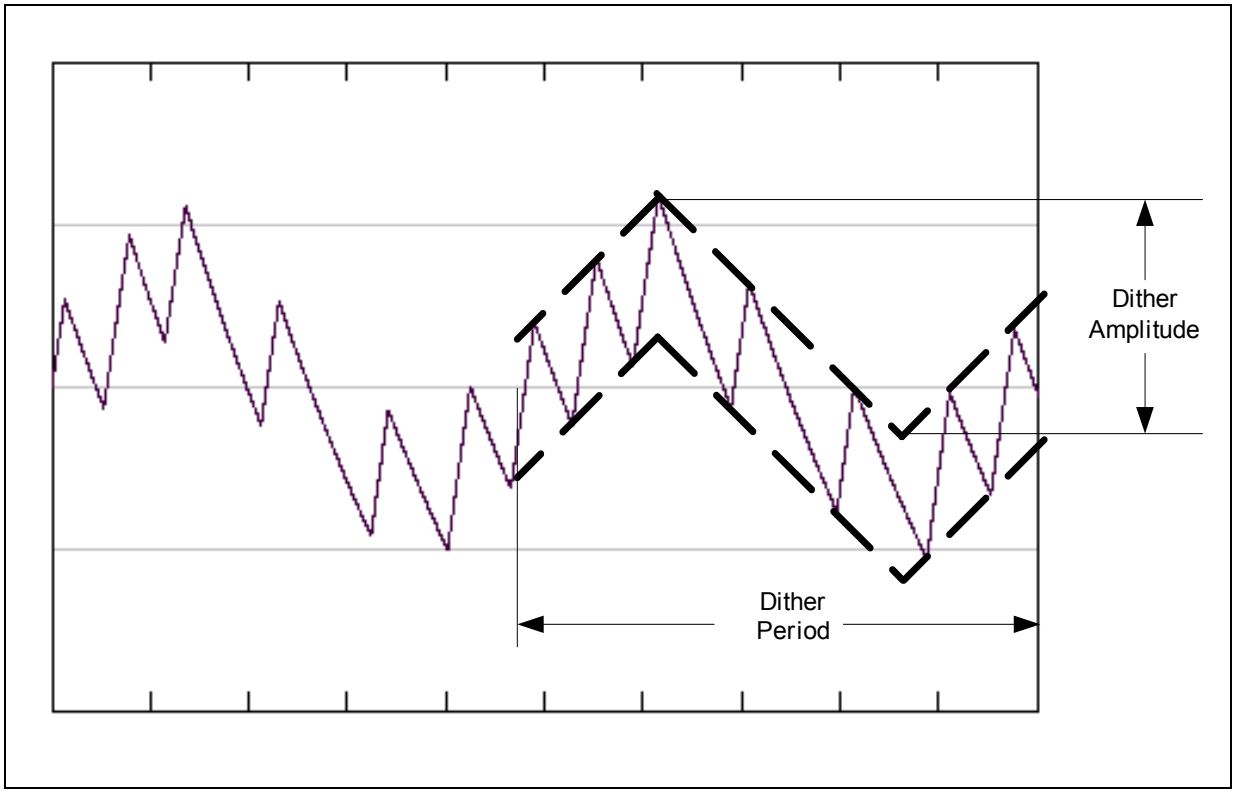

Figure 18 Dither Waveform

The Dither Frequency can be programmed over a range of 41 Hz to 1 kHz.

The Dither Amplitude can be programmed over a range from 12.5 mVpp to 390 mVpp.

The Dither waveform can be disabled by clearing both the dither amplitude and dither frequency fields in the Dither Configuration Register.

Note: Programming the Dither Frequency field to zero when the Dither Amplitude is programmed to a non-zero value will result in incorrect current regulation.

In some applications, an enhanced dither waveform is required. The enhanced dither waveform will hold the lower switch point at the minimum value (lowest lower switch point within the dither period) until the solenoid current crosses the lower switch point. This mode may be useful when the decay time of the solenoid current is slower than the slope of the dither waveform. See **Figure 19** for an illustration of the enhanced dither waveform. Enhanced Dither can be enabled by setting a bit in the SPI Dither Configuration word.

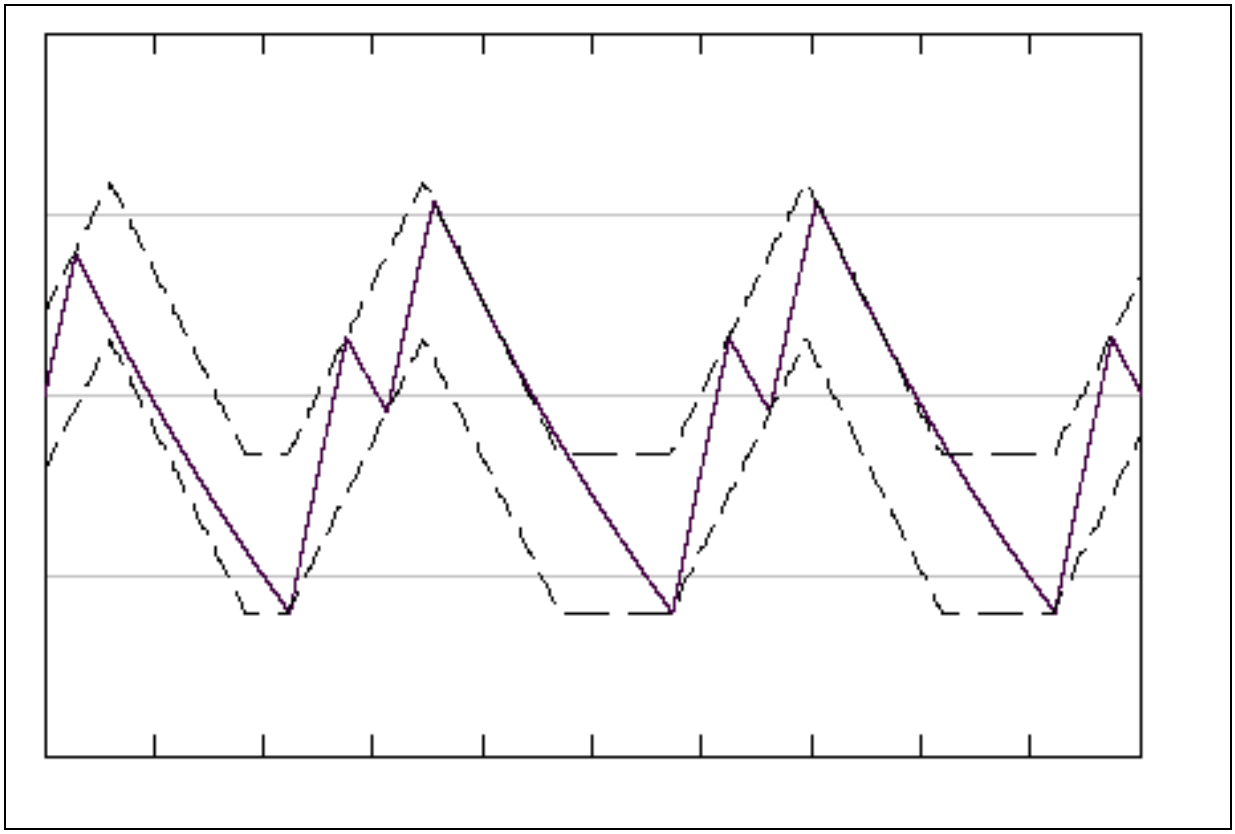

Figure 19 Enhanced Dither Waveform

When the enhanced dither bit is selected, the dither period will only be extended if the lower switch threshold is not crossed during the entire negative slope portion of the dither waveform.

Example see **Figure 20**.

The first dither period is not extended since the lower threshold was crossed during the negative slope portion of the dither waveform, the following two dither periods are extended since the low switch point was not crossed during the negative slope portion of the waveform.

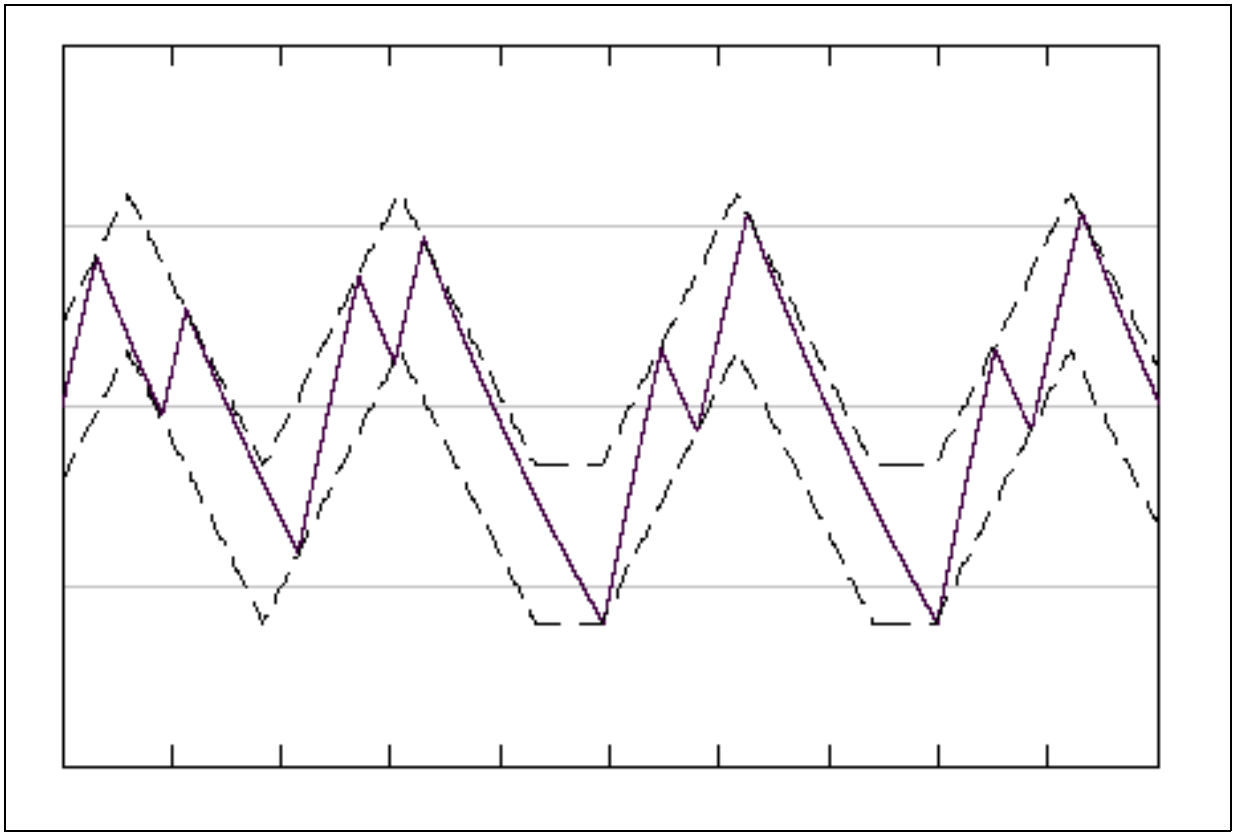

Figure 20 Enhanced Dither Waveform

The extension of the dither period will be terminated when the lower switch threshold is crossed or when the extension time has exceeded the enhanced dither time out period (minimum 15 ms) - see **Figure 21**.

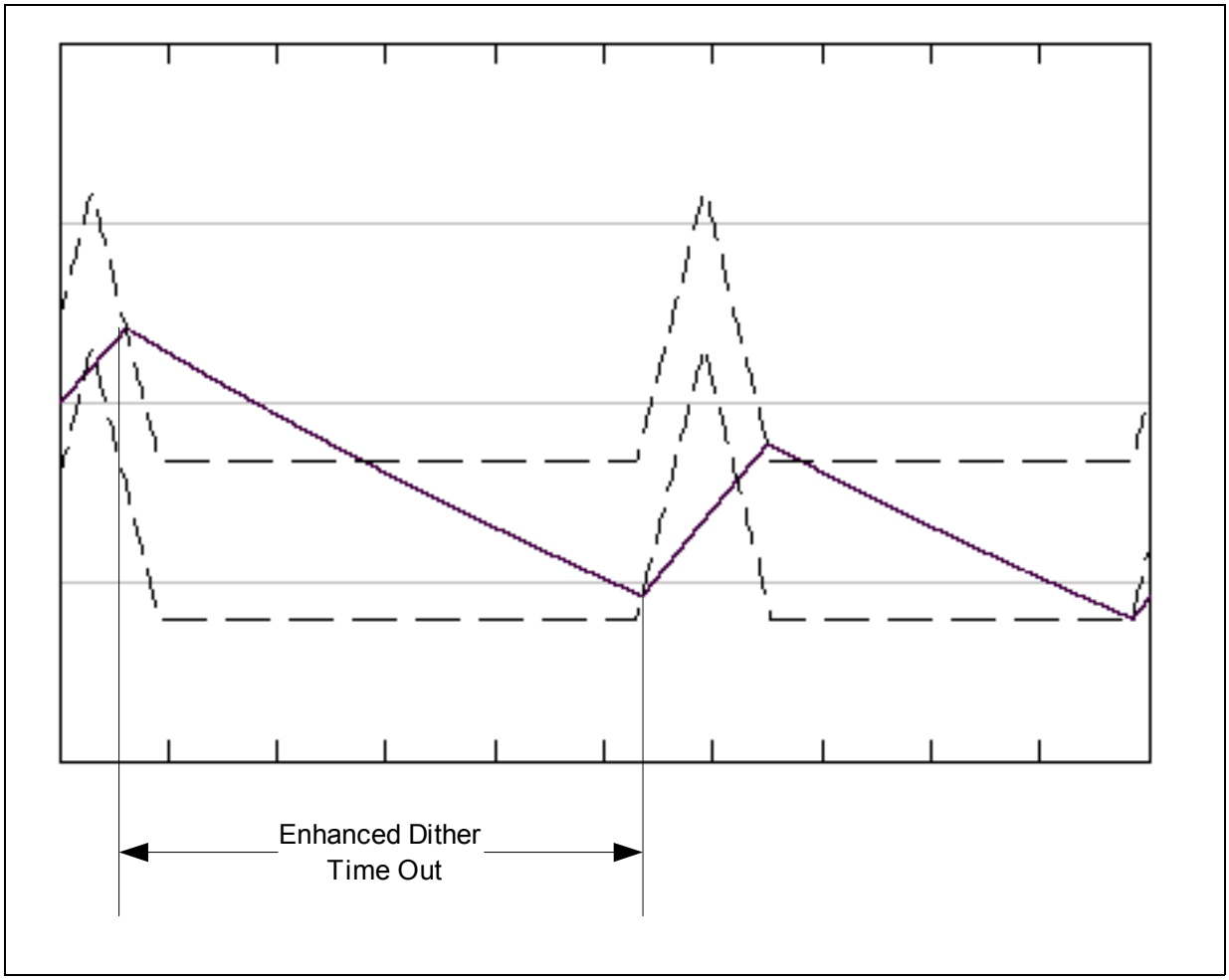

Figure 21 Enhanced Dither Time-out

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.5.2.1	OUTx[3)] Enhanced Dither time out	$T_{out(eD)}$	15	–	25	ms	–
5.5.2.2	OUTx Dither[3)4)] Amplitude Reg = 04_H	I_{DAP-P}	40.5	50	60.5	mVpp	50 mV setting programmed REF = 2.5V
5.5.2.3	OUTx Dither[3)4)] Amplitude Reg = 08_H	I_{DAP-P}	90.9	101	110.9	mVpp	100 mV setting programmed REF = 2.5V
5.5.2.4	OUTx Dither[3)4)] Amplitude Reg = $0C_H$	I_{DAP-P}	141.4	151	161.4	mVpp	150 mV setting programmed REF = 2.5V
5.5.2.5	OUTx Dither[3)4)] Amplitude Reg = 10_H	I_{DAP-P}	191.8	202	211.8	mVpp	200 mV setting programmed REF = 2.5V
5.5.2.6	OUTx Dither[3)4)] Amplitude Reg = 14_H	I_{DAP-P}	242.3	252	262.3	mVpp	250 mV setting programmed REF = 2.5V
5.5.2.7	OUTx Dither[3)4)] Amplitude Reg = 18_H	I_{DAP-P}	292.7	303	312.7	mVpp	300 mV setting programmed REF = 2.5V
5.5.2.8	OUTx Dither[3)4)] Amplitude Reg = $1C_H$	I_{DAP-P}	343.2	353	363.2	mVpp	350 mV setting programmed REF = 2.5V
5.5.2.9	OUTx Dither Frequency Reg = 34_H	f_{dither}	-15%	100	+15%	Hz	100 Hz setting programmed[3)]
5.5.2.10	OUTx Dither Frequency Reg = 23_H	f_{dither}	-15%	150	+15%	Hz	150 Hz setting programmed[3)]
5.5.2.11	OUTx Dither Frequency Reg = $1A_H$	f_{dither}	-15%	200	+15%	Hz	200 Hz setting programmed[3)]

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.5.2.12	OUTx Dither Frequency Reg = 15_H	f_{dither}	-15%	250	+15%	Hz	250 Hz setting programmed[3)]
5.5.2.13	OUTx Dither Frequency Reg = 11_H	f_{dither}	-15%	308	+15%	Hz	300 Hz setting programmed[3)]
5.5.2.14	OUTx Dither Frequency Reg = $0F_H$	f_{dither}	-15%	350	+15%	Hz	350 Hz setting programmed[3)]
5.5.2.15	OUTx Dither Frequency Reg = $0D_H$	f_{dither}	-15%	403	+15%	Hz	400 Hz setting programmed[3)]
5.5.2.16	OUTx Dither Frequency Reg = $0C_H$	f_{dither}	-15%	437	+15%	Hz	450 Hz setting programmed[3)]
5.5.2.17	OUTx Dither Frequency Reg = $0A_H$	f_{dither}	-15%	524	+15%	Hz	500 Hz setting programmed[3)]

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, specified by design

4) When the internal reference is used (REF pin grounded), the minimum and maximum limits must be increased by +/- 2%

5.5.3 Input Command Out of Range / Dither Clipping

If an average current command between 000_H and 029_H inclusive (0 mA and 50 mA with a 1 Ω sense resistor) is received, then the average current will be set to 000 (channel disabled) and the COR (command out of range) error bit will be set. The average current set point verification reported in the MISO word, however, will be the actual average current command, not 000_H.

If an average current command greater than $3D6_H$ (1.18 A with a 1 Ω sense resistor) is received, then the average current will be set to $3D6_H$, and the COR error bit will be set. The average current set point verification reported in the MISO word, however, will be the actual commanded current, not $3D6_H$.

The minimum limit for the lower switch point is 19_H (30 mA with a 1 Ω sense resistor) and the maximum limit for the upper switch point is $3FF_H$ (1.23 A with a 1 Ω sense resistor). If the microprocessor sets the average current command and the switching hysteresis setting to values that result in switch points beyond these limits, the TLE 7241E will clip the switch point to 19_H or $3FF_H$ and the COR error bit will be set.

If the average current set point and the switching hysteresis setting do not result in switch points outside the usable range (19_H to $3FF_H$), but dither is enabled and the dither amplitude setting results in an out of range switch point, then the DCLP fault bit will be set. The fault bit is set when the calculated switch point (average current + hysteresis + dither) exceeds the upper or lower limit, not when the registers are programmed.

When the DCLP fault bit is set, the TLE 7241E will enter “symmetrical dither clipping” mode within one dither cycle after the clipping occurs. During symmetrical dither clipping mode, the device maintains the average current set-point by reducing the amplitude of the dither waveform. Up to one full dither cycle may be required to exit the “symmetrical dither clipping mode” and resume normal operation when the registers are re-programmed. See **Figure 22** for an example of the dither clipping waveform.

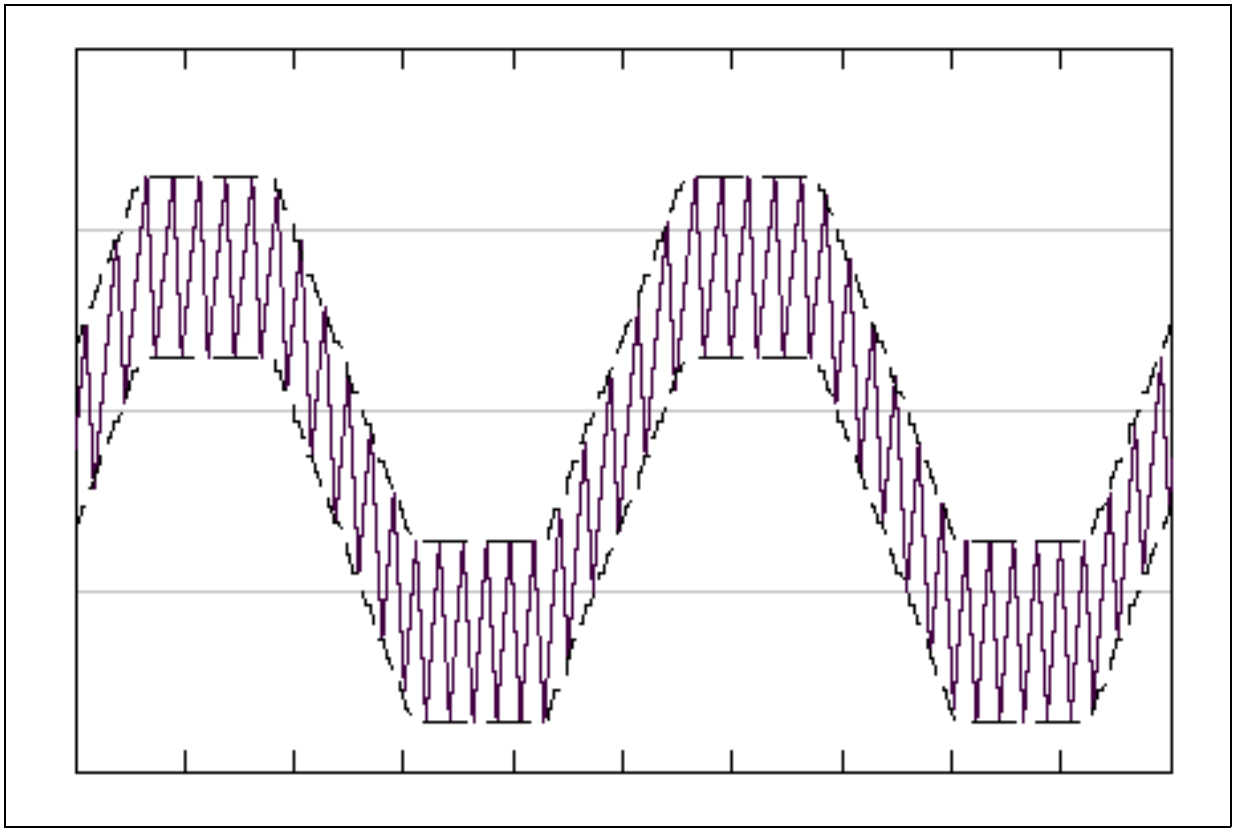

Figure 22 Symmetrical Dither Clipping

5.5.4 Error Correction Registers / Average Switch Threshold Trimming

The average switch threshold of each channel is trimmed at wafer test under the following operating conditions: T_{amb} = 25 °C, V_{BAT} = 14 V, V_{cc} = 5.0 V, V_{REF} = 2.5 V, average current command = 299_H (800 mA with 1 Ω sense resistor), dither = off, hysteresis = 80 mVpp.

The TLE 7241E includes 5 error correction registers for each channel. The registers are written during room temperature wafer testing. After the device has been trimmed, the average of the upper and lower switch thresholds is measured at 5 average current operating points. The difference in the measured value and the ideal value is permanently stored in the 5 error registers. The contents of the error correction register are an 8 bit signed value that must be added to the ideal current command to minimize the average current error.

Error Correction Register #	Corresponding Average Current Register Setting (Hex)	Corresponding Ideal Average Current with a 1 Ω ext. Sense Resistor
0	0A6	200 mA
1	14D	400 mA
2	1F3	600 mA
3	29A	800 mA
4	340	1000 mA

For example:

- Measured average switch threshold at $0A6_H$ during Infineon production test = 207 mV
- Ideal average switch threshold at $0A6_H$ = 199.6 mV
- Error Correction = -7.4 mV / (1.2 mV/count) = -6 counts
- The contents of the error correction register are -6 or FA_H

The contents of the error correction registers can be used by the application microcontroller to improve the accuracy of the average switch points. In the above example, when the microcontroller requests an average current of 200 mA (assuming a 1 Ω sense resistor), the command sent should be 0A6 (ideal) - 6 (error correction) = 0A0.

For current commands between the 5 measured operating points, the microprocessor can use linear (or more complex) interpolation to calculate the appropriate error correction values.

5.6 SPI Command and Diagnosis Structure

5.6.1 SPI Signal Description

The SPI serial interface has the following features:

- Full duplex, 4-wire synchronous communication
- Slave mode operation only
- Fixed SCK polarity and phase requirements
- Fixed 16-bit command word

SCK operation up to 5.0 MHz (the maximum clock frequency may be limited to a value less than 5.0 MHz by the minimum required SO setup time of the SPI master device and by the total capacitive load on the SO bus node. With a SO load capacitance of 200 pF the maximum SPI frequency is 3.2 MHz).

The TLE 7241E IC Serial Peripheral Interface (SPI) is used to transmit and receive data synchronously with the master SPI device. Communication occurs over a full-duplex, four wire SPI bus. The TLE 7241E IC will operate only as a slave device to the master, and requires four external pins; SI, SO, SCK, and CSB. All words are 16 bits long and sent MSB first. The device is selected when the CSB signal is asserted (low). The master will then send 16 (or a multiple of 16) clock pulses over the SCK pin. The TLE 7241E will simultaneously turn on the serial output SO and return the MISO return bits. When receiving, valid data is latched on the rising edge of each SCK pulse. The serial output data is available on the rising edge of SCK, and transitions on the falling edge of SCK. See **Figure 23** for SPI timing diagram.

The number of clock cycles occurring on the pin SCK while the CSB pin is asserted low must be 16 or an integer multiple of 16, otherwise the SPI MOSI data will be ignored.

The fault registers are double buffered. The first buffer layer will latch a fault at the time the fault is detected. This inner layer buffer is cleared when the fault condition is no longer present and the fault bit has been communicated to the microprocessor by a MISO response. The second layer buffer will latch the output of the inner layer buffer whenever the CSB pin transitions from low to high. The output of this buffer layer is transferred to the MISO shift register one SPI frame after the corresponding MOSI command has been received from the microcontroller.

The MISO data word value of $FFFF_H$ is never generated by the TLE 7241E, and will indicate a Hi-Z state on the SO pin when an external pull-up resistor to V_{DD} is used. This feature can be used to detect an open connection between the SO pin of the TLE 7241 E and the microcontroller.

All undefined MOSI command words will be ignored by the TLE 7241E, and the MISO response during the next SPI frame will be undefined (but not $FFFF_H$).

Note: The OL/SG fault bit is latched into the MISO register, and then updated within t_{dly} ($\leq$ 1.7 µs) after the rising edge of the CSB signal when the received MOSI word is an General Configuration command.

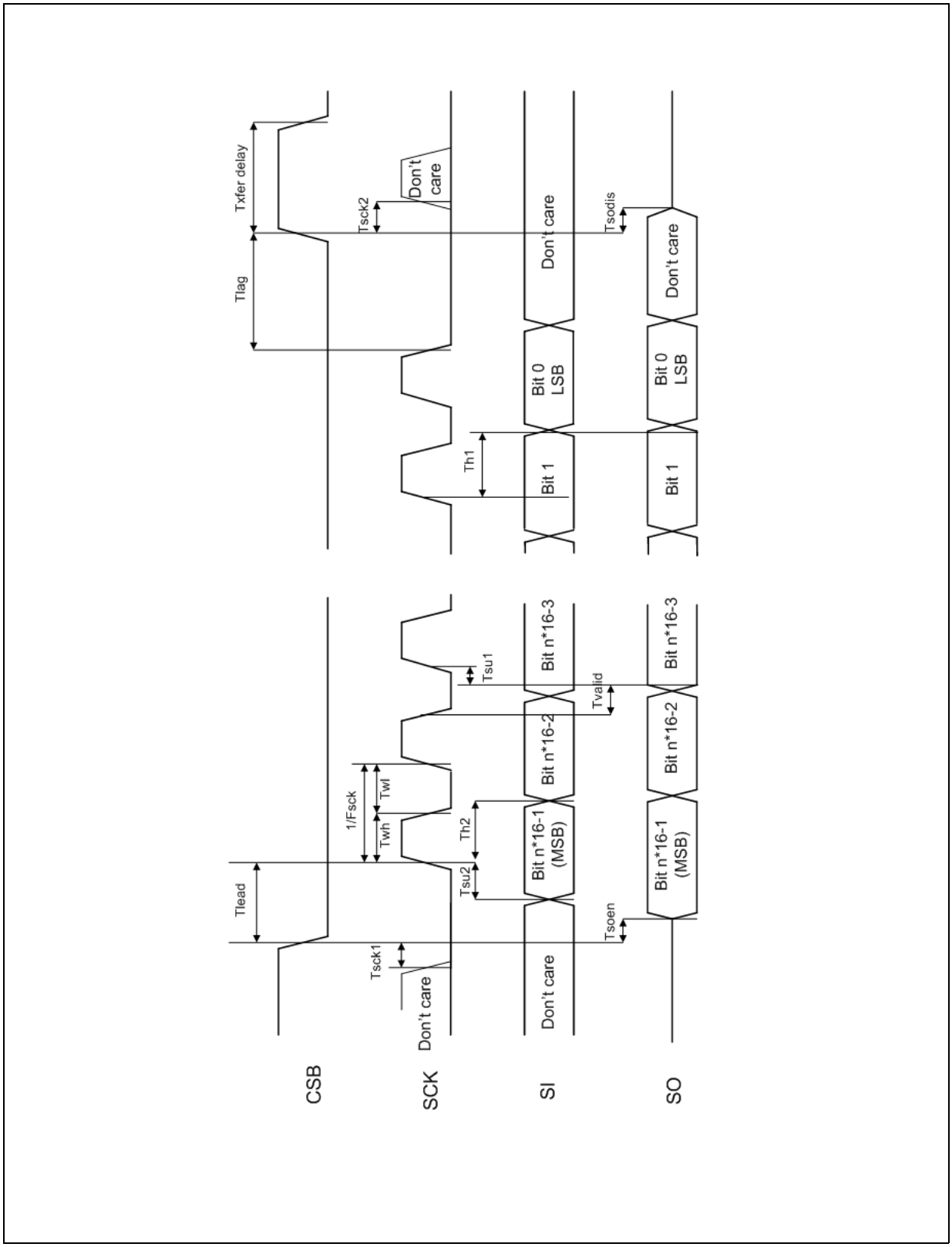

Figure 23 SPI Timing Diagram

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.6.1.1	CSB Input Bias Current	I_{CSB}	-25	-10	-5	µA	V_{CSB} = 0 V Pull-up source is from pin V_{SO}
5.6.1.2	SI Input Pull-down Current	I_{SI}	5	10	25	µA	V_{SI} = V_{VSO}
5.6.1.3	SCK Input Pull-down Current	I_{SCK}	5	10	25	µA	V_{SCK} = V_{VSO}
5.6.1.4	SO Tri-state Leakage Current	I_{SOT}	-10	0	10	µA	CSB = 0.7 V_{DD} 0 V < V_{SO} < V_{VSO}
5.6.1.5	SI, SCK, CSB, DEFAULT Input Capacitance	C_{IN}	–	–	20	pF	0 V < V_{SO} < 5.25 V [3)]
5.6.1.6	SO Tri-state Output Capacitance	C_{SOT}	–	–	20	pF	0 V < V_{SO} < 5.25 V [3)]
5.6.1.7	SCK Serial Clock Frequency	f_{SCK}	–	–	3.2	MHz	SPI clock SPI communications tested at C_L = 200 pF on the SO pin, T_{su1} = 40 ns
5.6.1.8	SCK Clock Pulse High Time	T_{wh}	85	–	–	ns	f_{SCK} = 3.2 MHz, SCK = 2 V to 2 V (see **Figure 23**)
5.6.1.9	SCK Clock Pulse Low Time	T_{wl}	85	–	–	ns	f_{SCK} = 3.2 MHz, SCK = 0.8 V to 0.8 V (see **Figure 23**)

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.6.1.10	SO, CSB SO Pin Enable/ Disable	Tsoen, Tsodis	–	–	80	ns	CSB = 2.0 V to SO = 0.8 V/2.0 V, 10K ext. SO pull-up (see **Figure 23**) - enable CSB = 0.8 V to SO hi-Z, 10K ext. SO pull-up (see **Figure 23**) - disable
5.6.1.11	SO, SCK[3)] Output Data Setup Time, SO to SCK Rising Edge	T_{su1}	80	–	–	ns	Required setup time by microprocessor equivalent to T_{wl} - T_{valid} SO = 0.8 V/2.0 V to SCK = 0.8 V (see **Figure 23**)
5.6.1.12	SO, SCK[3)] Output Data Hold Time, SO Hold After SCK Rising Edge	T_{h1}	150	–	–	ns	Required hold time by microprocessor equivalent to T_{wh} + T_{valid} - T_{rso}/T_{fso} SCK = 2.0 V to SO = 0.8 V/2.0 V (see **Figure 23**)
5.6.1.13	SI, SCK Input Data Setup Time, SI to SCK Rising Edge	T_{su2}	20	–	–	ns	SI = 0.8 V/2.0 V to SCK = 2.0 V at 3.2 MHz (see **Figure 23**)
5.6.1.14	SI, SCK Input Data Hold Time, SI Hold after SCK Rising Edge	T_{h2}	30	–	–	ns	SCK = 2.0 V to SI = 0.8 V/2.0 V at 3.2 MHz (see **Figure 23**)
5.6.1.15	SO Serial Output Rise/Fall Time	T_{rso}/T_{fso}	–	–	50	ns	C_{ld} = 200 pF (see **Figure 23**)

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.6.1.16	SI, CSB, SCK Serial Inputs Rise/Fall Time	T_{rsi}/T_{fsi}	–	–	25	ns	[3)]
5.6.1.17	CSB, SCK CSB Falling Edge to SCK Rising Edge	T_{lead}	100	–	–	ns	CSB = 0.8 V to SCK = 0.8 V (see **Figure 23**)
5.6.1.18	CSB, SCK SCK Falling Edge to CSB Rising Edge	T_{lag}	50	–	–	ns	SCK = 0.8 V to CSB = 0.8 V (see **Figure 23**)
5.6.1.19	SCK, SO Falling Edge SCK to SO Data Valid	Data Valid	–	–	80	ns	SCK = 0.8 V to SO Data Valid, C_{ld} = 200 pF at 3.2 MHz (see **Figure 23**)
5.6.1.20	CSB[3)] Sequential Transfers	Xfer Delay	1	–	–	µs	CSB = 2.0 V (increasing) to CSB = 2.0 V (decreasing). IC will not require more than maximum time stated between communications.
5.6.1.21	SCK, CSB Falling edge of SCK to falling edge of CSB	T_{sck1}	20	–	–	ns	SCK = 0.8 V to CSB = 2.0 V (see **Figure 23**)
5.6.1.22	SCK, CSB Rising edge of CSB to rising edge of SCK	T_{sck2}	10	–	–	ns	CSB = 2.0 V to SCK = 0.8 V (see **Figure 23**)

Electrical Characteristics (cont'd)[1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.6.1.23	SCK Number of SCK pulses while CSB low (n is a positive integer)	n_{SCK}	16	n × 16	–	Pul-ses	–
5.6.1.24	CSB[3)] MISO shift register load delay time	t_{dly}	–	1.7	–	µs	CSB = 2.0 V (increasing) to MISO data loaded into shift register (see **Figure 24**)

1) Positive current flow is into the device.

2) T_J = 25 °C.

3) Not subject to production test, specified by design.

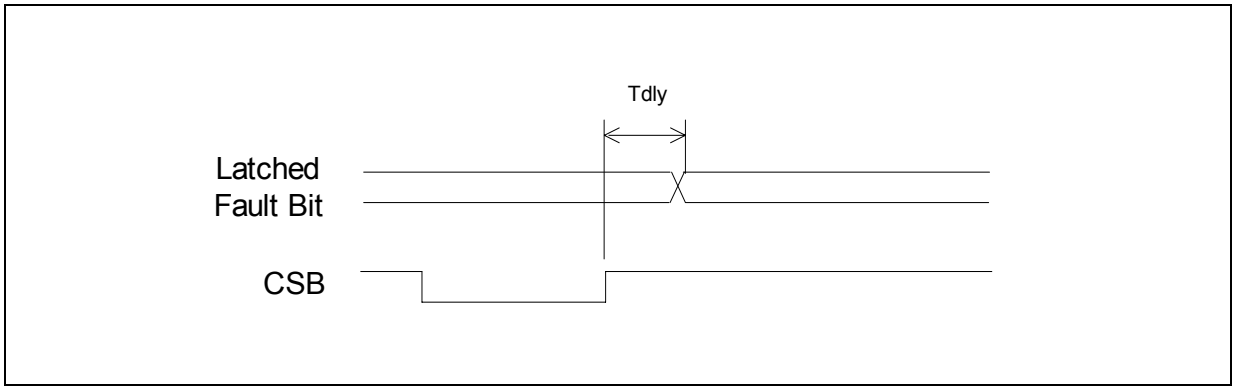

Figure 24 Fault Bit Refresh Delay Time (t_{dly})

5.6.2 SPI Command Structure

Table 1 SPI Command Summary

Channel	Instruction ID		Command Type	MISO Response - Next CSB Assertion
B15	B14	B13		
0	0	0	Average Current Set Point - CH#1	Average Current Verification and Status - CH#1
0	0	1	Dither Configuration - CH#1	Dither Config Verification CH#1
0	1	0	General Configuration - CH#1	General Config Verification CH#1
0	1	1	Read Register - CH#1	Register Contents - CH#1
1	0	0	Average Current Set Point - CH#2	Average Current Verification and Status - CH#2
1	0	1	Dither Configuration - CH#2	Dither Config Verification CH#2
1	1	0	General Configuration - CH#2	General Config Verification CH#2
1	1	1	Read Register - CH#2	Register Contents - CH#2

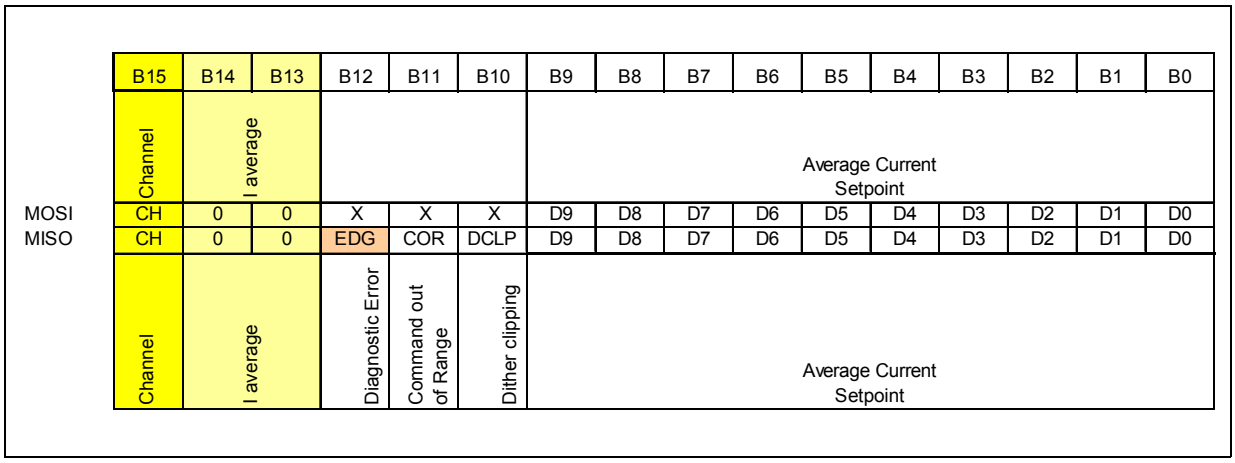

Figure 25 Average Current Set Point

MOSI

- B12 - B10 NU: Not used, Default = 0 (40 mVpp)
- B9 - B0: Average Current Set point, Average Current Set point setting (see **Table 2**), Default = 0 (0 mA)

MISO

- B12 Diagnostic Error: = 1 if OL/SG = 1 or VSHT = 1 or OTMP = 1 (channel specific)
- B11 Command out of Range: = 1 if the average current set point + the hysteresis setting result in a switch point > 1.23 V or < 0.03 V
- B10 Dither Clipping: = 1 if the dither setting, average current set point, and hysteresis setting result in a switch point > 1.23 V or < 0.03 V
- B9 - B0 Average Current Set point: Contents of the average current set point command (non-clipped)

Table 2 Average Output Current Key (typical) - Partial Table

COR	Hex	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	Average Switch Point [mV]	Load Current with 1 Ω Sense Resistor [mA]	Load Current with 0.68 Ω Sense Resistor [mA]
0	000	0	0	0	0	0	0	0	0	0	0	0.00	0.00	0.00
1	001	0	0	0	0	0	0	0	0	0	1	0.00	0.00	0.00
1	002	0	0	0	0	0	0	0	0	1	0	0.00	0.00	0.00
1	003	0	0	0	0	0	0	0	0	1	1	0.00	0.00	0.00
…														
1	028	0	0	0	0	1	0	1	0	0	0	0.00	0.00	0.00
1	029	0	0	0	0	1	0	1	0	0	1	0.00	0.00	0.00
[1)]	02A	0	0	0	0	1	0	1	0	1	0	50.45	50.45	74.19
[1)]	02B	0	0	0	0	1	0	1	0	1	1	51.65	51.65	75.96
[1)]	02C	0	0	0	0	1	0	1	1	0	0	52.85	52.85	77.72
…														
0	0A6	0	0	1	0	1	0	0	1	1	0	199.39	199.39	293.23
…														
0	14D	0	1	0	1	0	0	1	1	0	1	399.99	399.99	588.22
…														
0	1F3	0	1	1	1	1	1	0	0	1	1	599.38	599.38	881.45
…														
0	29A	1	0	1	0	0	1	1	0	1	0	799.98	799.98	1176.44
…														

Table 2 Average Output Current Key (typical) - Partial Table (cont'd)

COR	Hex	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	Average Switch Point [mV]	Load Current with 1 Ω Sense Resistor [mA]	Load Current with 0.68 Ω Sense Resistor [mA]
0	340	1	1	0	1	0	0	0	0	0	0	999.38	999.38	1469.67
…														
1)	3D3	1	1	1	1	0	1	0	0	1	1	1175.95	1175.95	1729.33
1)	3D4	1	1	1	1	0	1	0	1	0	0	1177.15	1177.15	1731.10
1)	3D5	1	1	1	1	0	1	0	1	0	1	1178.35	1178.35	1732.87
1)	3D6	1	1	1	1	0	1	0	1	1	0	1178.35	1178.35	1732.87
1	3D7	1	1	1	1	0	1	0	1	1	1	1178.35	1178.35	1732.87
…														
1	3FC	1	1	1	1	1	1	1	1	0	0	1178.35	1178.35	1732.87
1	3FD	1	1	1	1	1	1	1	1	0	1	1178.35	1178.35	1732.87
1	3FE	1	1	1	1	1	1	1	1	1	0	1178.35	1178.35	1732.87
1	3FF	1	1	1	1	1	1	1	1	1	1	1178.35	1178.35	1732.87

1) COR state dependent on the switching hysteresis value.

$$SP_{AVG} = \frac{\text{register value}}{2^{10}} \times 1230\ \text{mV} \quad (5)$$

$$I_{AVG} = \frac{\text{register value}}{2^{10}} \times \frac{1230}{R_{sense}}\ \text{mA} \quad (6)$$

Note: When a new average current command or hysteresis setting is received, the new data is loaded immediately with the rising edge of CSB (not synchronized with the dither waveform). The dither waveform is not reset when the new average current command or hysteresis setting is received.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	Channel	Dither Configuration		Enhanced Dither	Dither Amplitude					Dither Frequency						
MOSI	CH	0	1	ED	DA4	DA3	DA2	DA1	DA0	DF6	DF5	DF4	DF3	DF2	DF1	DF0
MISO	CH	0	1	ED	DA4	DA3	DA2	DA1	DA0	DF6	DF5	DF4	DF3	DF2	DF1	DF0
	Channel	Dither Configuration		Enhanced Dither	Dither Amplitude					Dither Frequency						

Figure 26 Dither Programming

MOSI

- B12 Enhanced Dither: Enables the enhanced dither feature when ED = 1, Default = 0 (disabled)
- B11 - B7 Dither Amplitude: Setting for the amplitude of the dither waveform (see **Table 3**), Default = 00_H (Dither Disabled)
- B6 - B0 Dither Frequency: Setting for the frequency of the dither waveform (see **Table 4**), Default = 00_H (Dither Disabled)

Note: To disable the dither waveform, both the amplitude and frequency fields must be set to zero. These fields must both be cleared in the same SPI communication frame. Programming the frequency to zero when the amplitude is set to a non-zero value will result in incorrect current regulation.

MISO

- B12 Enhanced Dither: Contents of the ED bit of the dither configuration register
- B11 - B7 Dither Amplitude: Contents of the dither amplitude register (shadow register)
- B6 - B0 Dither Frequency: Contents of the dither frequency register (shadow register)

Note: When a Dither Configuration command is received which changes either the dither frequency or the dither amplitude settings, the new dither waveform characteristics will take effect at the beginning of the next dither period.

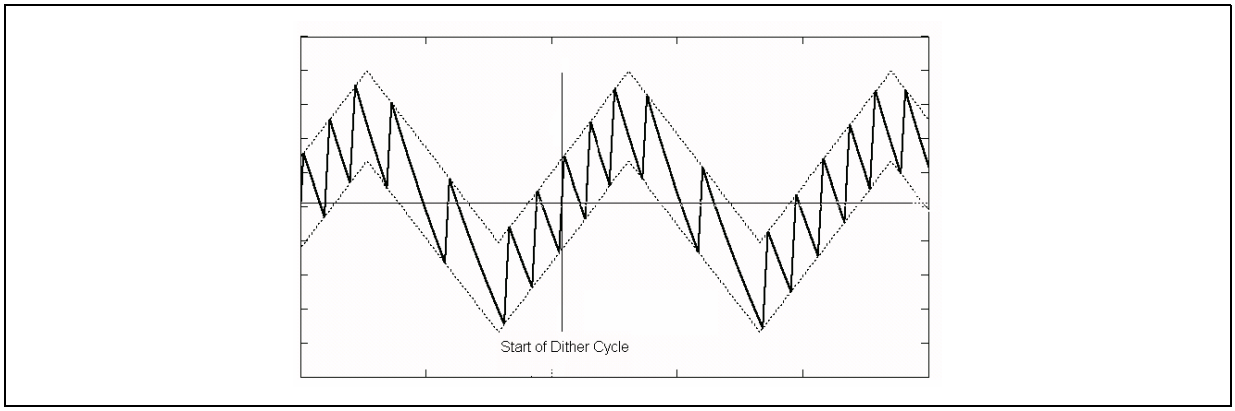

Figure 27 Start of Dither Cycle

Table 3 Ideal Dither Amplitude Key (typical)

Hex	DA4	DA3	DA2	DA1	DA0	Dither Amplitude [mVpp]	Dither Amplitude with 1 Ω sense resistor [mApp]	Dither Amplitude with 0.68 Ω sense resistor [mApp]
00	0	0	0	0	0	0.0	0.00	0.00
01	0	0	0	0	1	12.6	12.6	18.5
02	0	0	0	1	0	25.2	25.2	37.1
03	0	0	0	1	1	37.8	37.8	55.6
04	0	0	1	0	0	50.5	50.45	74.19
05	0	0	1	0	1	63.1	63.06	92.74
06	0	0	1	1	0	75.7	75.68	111.29
07	0	0	1	1	1	88.3	88.29	129.84
08	0	1	0	0	0	100.9	100.90	148.38
09	0	1	0	0	1	113.5	113.51	166.93
0A	0	1	0	1	0	126.1	126.13	185.48
0B	0	1	0	1	1	138.7	138.74	204.03
0C	0	1	1	0	0	151.4	151.35	222.58
0D	0	1	1	0	1	164.0	163.96	241.12
0E	0	1	1	1	0	176.6	176.58	259.67
0F	0	1	1	1	1	189.2	189.19	278.22
10	1	0	0	0	0	201.8	201.80	296.77
11	1	0	0	0	1	214.4	214.41	315.32
12	1	0	0	1	0	227.0	227.03	333.86
13	1	0	0	1	1	239.6	239.64	352.41
14	1	0	1	0	0	252.3	252.25	370.96
15	1	0	1	0	1	264.9	264.86	389.51
16	1	0	1	1	0	277.5	277.48	408.05
17	1	0	1	1	1	290.1	290.09	426.60
18	1	1	0	0	0	302.7	302.70	445.15
19	1	1	0	0	1	315.3	315.32	463.70
1A	1	1	0	1	0	327.9	327.93	482.25
1B	1	1	0	1	1	340.5	340.54	500.79

Table 3 Ideal Dither Amplitude Key (typical)

Hex	DA4	DA3	DA2	DA1	DA0	Dither Amplitude [mVpp]	Dither Amplitude with 1 Ω sense resistor [mApp]	Dither Amplitude with 0.68 Ω sense resistor [mApp]
1C	1	1	1	0	0	353.2	353.15	519.34
1D	1	1	1	0	1	365.8	365.77	537.89
1E	1	1	1	1	0	378.4	378.38	556.44
1F	1	1	1	1	1	391.0	390.99	574.99

$$V_{\text{dithamp}} = \frac{\text{register value} \times 10.5}{2^{10}} \times 1230 \text{ mVpp} \quad (7)$$

$$I_{\text{dithamp}} = \frac{\text{register value} \times 10.5}{2^{10}} \times \frac{1230}{R_{\text{sense}}} \text{ mApp} \quad (8)$$

Table 4 Ideal Dither Frequency Key (typical)- Partial Table

Hex	DF6	DF5	DF4	DF3	DF2	DF1	DF0	Dither Frequency
00	0	0	0	0	0	0	0	0.0 Hz
01	0	0	0	0	0	0	1	5238.1 Hz
02	0	0	0	0	0	1	0	2619.0 Hz
03	0	0	0	0	0	1	1	1746.0 Hz
04	0	0	0	0	1	0	0	1309.5 Hz
05	0	0	0	0	1	0	1	1047.6 Hz
06	0	0	0	0	1	1	0	873.0 Hz
07	0	0	0	0	1	1	1	748.3 Hz
08	0	0	0	1	0	0	0	654.8 Hz
09	0	0	0	1	0	0	1	582.0 Hz
0A	0	0	0	1	0	1	0	523.8 Hz
0B	0	0	0	1	0	1	1	476.2 Hz
0C	0	0	0	1	1	0	0	436.5 Hz
0D	0	0	0	1	1	0	1	402.9 Hz
0E	0	0	0	1	1	1	0	374.2 Hz
0F	0	0	0	1	1	1	1	349.2 Hz

Table 4 Ideal Dither Frequency Key (typical)- Partial Table (cont'd)

Hex	DF6	DF5	DF4	DF3	DF2	DF1	DF0	Dither Frequency
10	0	0	1	0	0	0	0	327.4 Hz
11	0	0	1	0	0	0	1	308.1 Hz
12	0	0	1	0	0	1	0	291.0 Hz
13	0	0	1	0	0	1	1	275.7 Hz
14	0	0	1	0	1	0	0	261.9 Hz
15	0	0	1	0	1	0	1	249.4 Hz
16	0	0	1	0	1	1	0	238.1 Hz
17	0	0	1	0	1	1	1	227.7 Hz
18	0	0	1	1	0	0	0	218.3 Hz
19	0	0	1	1	0	0	1	209.5 Hz
1A	0	0	1	1	0	1	0	201.5 Hz
1B	0	0	1	1	0	1	1	194.0 Hz
1C	0	0	1	1	1	0	0	187.1 Hz
1D	0	0	1	1	1	0	1	180.6 Hz
1E	0	0	1	1	1	1	0	174.6 Hz
1F	0	0	1	1	1	1	1	169.0 Hz
20	0	1	0	0	0	0	0	163.7 Hz
21	0	1	0	0	0	0	1	158.7 Hz
22	0	1	0	0	0	1	0	154.1 Hz
23	0	1	0	0	0	1	1	149.7 Hz
24	0	1	0	0	1	0	0	145.5 Hz
25	0	1	0	0	1	0	1	141.6 Hz
26	0	1	0	0	1	1	0	137.8 Hz
27	0	1	0	0	1	1	1	134.3 Hz
28	0	1	0	1	0	0	0	131.0 Hz
29	0	1	0	1	0	0	1	127.8 Hz
2A	0	1	0	1	0	1	0	124.7 Hz
2B	0	1	0	1	0	1	1	121.8 Hz
2C	0	1	0	1	1	0	0	119.0 Hz
2D	0	1	0	1	1	0	1	116.4 Hz

Table 4 Ideal Dither Frequency Key (typical)- Partial Table (cont'd)

Hex	DF6	DF5	DF4	DF3	DF2	DF1	DF0	Dither Frequency
2E	0	1	0	1	1	1	0	113.9 Hz
2F	0	1	0	1	1	1	1	111.4 Hz
30	0	1	1	0	0	0	0	109.1 Hz
31	0	1	1	0	0	0	1	106.9 Hz
32	0	1	1	0	0	1	0	104.8 Hz
33	0	1	1	0	0	1	1	102.7 Hz
34	0	1	1	0	1	0	0	100.7 Hz
35	0	1	1	0	1	0	1	98.8 Hz
36	0	1	1	0	1	1	0	97.0 Hz
37	0	1	1	0	1	1	1	95.2 Hz
38	0	1	1	1	0	0	0	93.5 Hz
39	0	1	1	1	0	0	1	91.9 Hz
3A	0	1	1	1	0	1	0	90.3 Hz
3B	0	1	1	1	0	1	1	88.8 Hz
3C	0	1	1	1	1	0	0	87.3 Hz
3D	0	1	1	1	1	0	1	85.9 Hz
3E	0	1	1	1	1	1	0	84.5 Hz
3F	0	1	1	1	1	1	1	83.1 Hz
40	1	0	0	0	0	0	0	81.8 Hz
41	1	0	0	0	0	0	1	80.6 Hz
42	1	0	0	0	0	1	0	79.4 Hz
43	1	0	0	0	0	1	1	78.2 Hz
44	1	0	0	0	1	0	0	77.0 Hz
45	1	0	0	0	1	0	1	75.9 Hz
46	1	0	0	0	1	1	0	74.8 Hz
47	1	0	0	0	1	1	1	73.8 Hz
48	1	0	0	1	0	0	0	72.8 Hz
49	1	0	0	1	0	0	1	71.8 Hz
4A	1	0	0	1	0	1	0	70.8 Hz
4B	1	0	0	1	0	1	1	69.8 Hz

Table 4 Ideal Dither Frequency Key (typical)- Partial Table (cont'd)

Hex	DF6	DF5	DF4	DF3	DF2	DF1	DF0	Dither Frequency
4C	1	0	0	1	1	0	0	68.9 Hz
4D	1	0	0	1	1	0	1	68.0 Hz
4E	1	0	0	1	1	1	0	67.2 Hz
4F	1	0	0	1	1	1	1	66.3 Hz
50	1	0	1	0	0	0	0	65.5 Hz
51	1	0	1	0	0	0	1	64.7 Hz
52	1	0	1	0	0	1	0	63.9 Hz
53	1	0	1	0	0	1	1	63.1 Hz
54	1	0	1	0	1	0	0	62.4 Hz
55	1	0	1	0	1	0	1	61.6 Hz
56	1	0	1	0	1	1	0	60.9 Hz
57	1	0	1	0	1	1	1	60.2 Hz
58	1	0	1	1	0	0	0	59.5 Hz
59	1	0	1	1	0	0	1	58.9 Hz
5A	1	0	1	1	0	1	0	58.2 Hz
5B	1	0	1	1	0	1	1	57.6 Hz
5C	1	0	1	1	1	0	0	56.9 Hz
5D	1	0	1	1	1	0	1	56.3 Hz
5E	1	0	1	1	1	1	0	55.7 Hz
5F	1	0	1	1	1	1	1	55.1 Hz
60	1	1	0	0	0	0	0	54.6 Hz
61	1	1	0	0	0	0	1	54.0 Hz
62	1	1	0	0	0	1	0	53.5 Hz
63	1	1	0	0	0	1	1	52.9 Hz
64	1	1	0	0	1	0	0	52.4 Hz
65	1	1	0	0	1	0	1	51.9 Hz
66	1	1	0	0	1	1	0	51.4 Hz
67	1	1	0	0	1	1	1	50.9 Hz
68	1	1	0	1	0	0	0	50.4 Hz
69	1	1	0	1	0	0	1	49.9 Hz

Table 4 Ideal Dither Frequency Key (typical)- Partial Table (cont'd)

Hex	DF6	DF5	DF4	DF3	DF2	DF1	DF0	Dither Frequency
6A	1	1	0	1	0	1	0	49.4 Hz
6B	1	1	0	1	0	1	1	49.0 Hz
6C	1	1	0	1	1	0	0	48.5 Hz
6D	1	1	0	1	1	0	1	48.1 Hz
6E	1	1	0	1	1	1	0	47.6 Hz
6F	1	1	0	1	1	1	1	47.2 Hz
70	1	1	1	0	0	0	0	46.8 Hz
71	1	1	1	0	0	0	1	46.4 Hz
72	1	1	1	0	0	1	0	45.9 Hz
73	1	1	1	0	0	1	1	45.5 Hz
74	1	1	1	0	1	0	0	45.2 Hz
75	1	1	1	0	1	0	1	44.8 Hz
76	1	1	1	0	1	1	0	44.4 Hz
77	1	1	1	0	1	1	1	44.0 Hz
78	1	1	1	1	0	0	0	43.7 Hz
79	1	1	1	1	0	0	1	43.3 Hz
7A	1	1	1	1	0	1	0	42.9 Hz
7B	1	1	1	1	0	1	1	42.6 Hz
7C	1	1	1	1	1	0	0	42.2 Hz
7D	1	1	1	1	1	0	1	41.9 Hz
7E	1	1	1	1	1	1	0	41.6 Hz
7F	1	1	1	1	1	1	1	41.2 Hz

$$f_{dith} = \frac{1.76 \times 10^6}{\text{register value} \times 336}\ \text{Hz} \quad (9)$$

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	Channel	General Configuration									Fault Typing Current Source	Slew Rate		Switching Hysteresis		
MOSI	CH	1	0	X	X	X	X	X	X	X	FT	SR1	SR0	SW2	SW1	SW0
MISO	CH	1	0	OL/SG	VSHT	OTMP	0	0	0	REF	FT	SR1	SR0	SW2	SW1	SW0
	Channel	General Configuration		Open Load or Short to GND	Short to Vpwr	Over Temperature				Ext./Int. Reference Volt.	Fault Typing Current Source	Slew Rate		Switching Hysteresis		

Figure 28 General Configuration Register

MOSI

- B12 - B6: Not used, Ignored - Don't Care
- B5 Fault Typing Bit: Activates a 40 µA pull-up current on POSx pin for SG/OL differentiation. Default = 0 (disabled)
- B4 - B3 Slew Rate: Setting for the slew rate (see **Table 5**). Default = 3 (1.2 V/µs)
- B2 - B0 Switching Hysteresis: Setting for the hysteresis value (see **Table 6**), Default = 0 (40 mVpp)

MISO

- B12 OL/SG: Open Load / Short to Ground fault flag
- B11 VSHT: Short to BAT (Shorted Load) fault flag
- B10 OTMP: Overtemperature fault flag
- B9 - B7: Not used, always 0
- B6 REF: = 0 when an external reference is detected on the REF pin,
  B6 REF: = 1 when the REF pin is grounded and the internal 2.5 V reference is active
- B5 FT: Contents of the FT-bit in the general configuration register
- B4 - B3 Slew Rate: Contents of the Slew Rate settings in the general configuration register
- B2 - B0 SW: Contents of the switching hysteresis setting in the general configuration register

Table 5 Slew Rate Control Key

SR1	SR0	T_f/T_r (4 V - 10 V)	Slew Rate
0	0	0.5 µs	12 V/µs
0	1	1 µs	6 V/µs
1	0	2 µs	3 V/µs
1	1	5 µs	1.2 V/µs

Table 6 Switching Hysteresis Key

SH2	SH1	SH0	Hysteresis
0	0	0	40 mVpp
0	0	1	50 mVpp
0	1	0	60 mVpp
0	1	1	70 mVpp
1	0	0	80 mVpp
1	0	1	90 mVpp
1	1	0	100 mVpp
1	1	1	110 mVpp

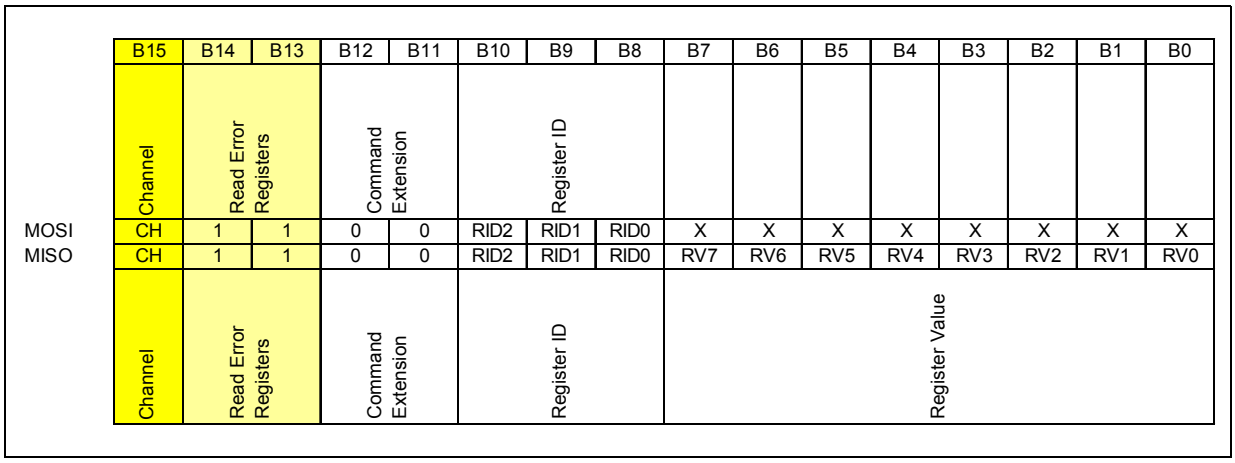

Figure 29 Read Error Register

MOSI

- B12 - B11 Command Extension: Always send as 00
- B10 - B8 Register ID: Selects Register to be transmitted to µP during next SPI frame (see **Table 7**)
- B7 - B0: Not used, Ignored / Don't Care

MISO

- B12 - 11 Command Extension: Always 00
- B10 - B8 RID0-2: Register ID of the register contents in B7 - B0
- B7 - B0 RV: Register contents

Table 7 Error Register Values per Channel

RID2	RID1	RID0	Register Name
0	0	0	Error Correction - 200 mV
0	0	1	Error Correction - 400 mV
0	1	0	Error Correction - 600 mV
0	1	1	Error Correction - 800 mV
1	0	0	Error Correction - 1000 mV
1	0	1	Chip Revision Code
1	1	0	00_H
1	1	1	00_H

The MOSI Commands “X1101XXX XXXXXXXX”, “X1110XXX XXXXXXXX”, and “X1111XXX XXXXXXXX” are not valid commands for the TLE7241 E. The MISO return words associated with these commands are undefined, but exclude the word “$FFFF_H$”.

6 Application

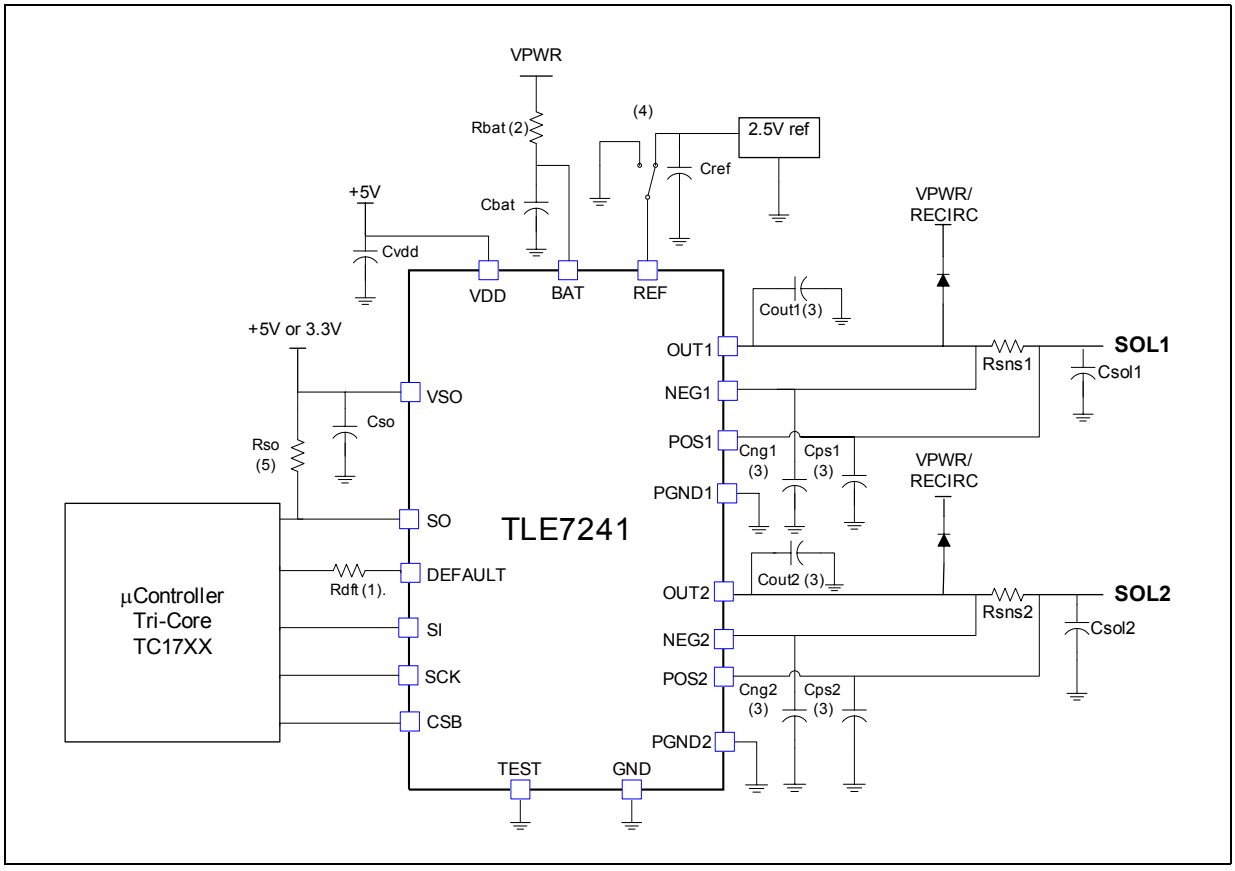

Figure 30 Application Circuit

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

1. Recommended for applications with microcontroller I/O voltage levels less than 5.0 V. The resistor will limit the microcontroller input current when the adjacent pins DEFAULT and V_{DD} are shorted together.
2. Required for applications that do not provide a reverse battery protected BAT supply. R_{BAT} may also be required to limit the BAT pin current during BAT voltage transient events (e. g. ISO pulses).
3. May be required for module level compliance with EMC specifications, but they are not required for TLE7241 functionality or stability.
4. Connect to the REF pin directly to GND to enable the internal 2.5 V voltage reference.
5. Optional. Defines SO signal voltage when the SO pin has failed as an open circuit.

Note: In case of an unused channel, the OUTx, NEGx, and POSx pins should be connected together.

6.1 Layout Notes

- The POS pin should be connected directly to the external sense resistor with a dedicated trace.
- The NEG pin should be connected directly to the external sense resistor with a dedicated trace.
- The POS pin trace should be routed near the NEG pin trace and both traces should not be routed near noise inducing signal lines and/or components (SPI clock signals, switching power supply inductors, etc.).
- For best accuracy, the external sense resistor should be placed near the IC.
- A capacitor should be connected between the V_{DD} pin and ground near the IC.
- A capacitor should be connected between the V_{SO} pin and ground near the IC.
- A capacitor should be connected between the BAT pin and ground near the IC.
- A capacitor should be connected between the REF pin and ground near the IC.
- The exposed lead frame should be connected to a large area ground plane and to the pins PGND1, PGND2.
- The GND pin should be connected directly to the ground plane.

7 Package Outlines

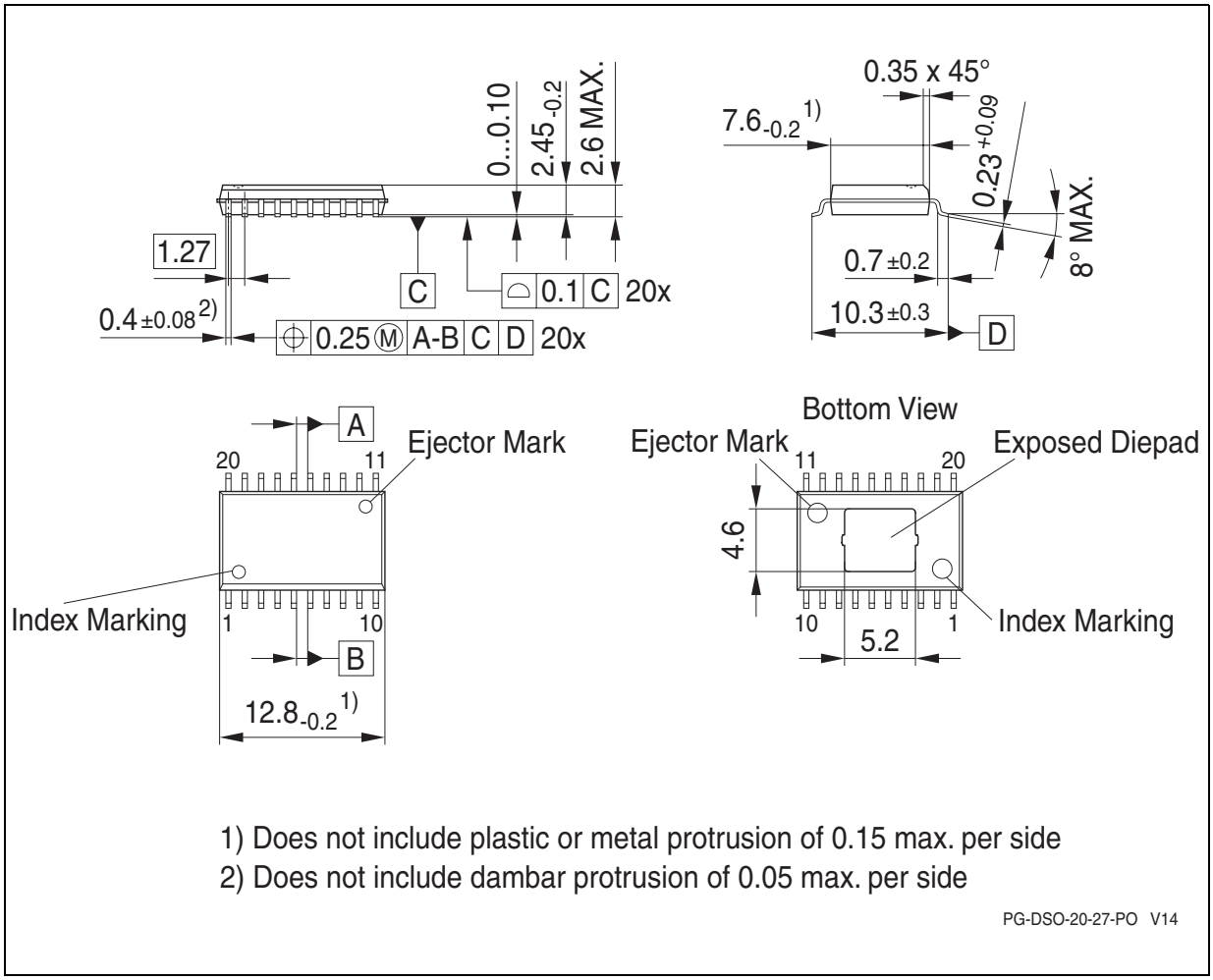

Figure 31 PG-DSO-20-27 EDP(Plastic Dual Small Outline Exposed Die Pad)

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mn

8 Revision History

Version	Date	Changes
Rev. 1.1	2009-01-19	Page 68: Updated Package drawing (Stand-off) Page 69-70: added Revision History, updated Legal Disclaimer

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