

# DDR3 SDRAM SODIMM

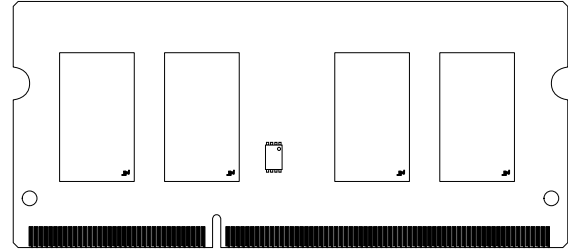
**MT4JSF6464HZ – 512MB**
**MT4JSF12864HZ – 1GB**

## Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 204-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 512MB (64 Meg x 64), 1GB (128 Meg x 64)
- $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = +3.0V$  to  $+3.6V$
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- On-board I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 204-Pin SODIMM (MO-268 R/C C)**

Module Height: 30mm (1.18 in)



## Options

- Operating temperature
  - Commercial ( $0^{\circ}C \leq T_A \leq +70^{\circ}C$ )
- Package
  - 204-pin DIMM (halogen-free)
- Frequency/CAS latency
  - 1.25ns @ CL = 11 (DDR3-1600)
  - 1.5ns @ CL = 9 (DDR3-1333)
  - 1.87ns @ CL = 7 (DDR3-1066)

## Marking

None  
Z  
-1G6  
-1G4  
-1G1

**Table 1: Key Timing Parameters**

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							t <sub>RCD</sub> (ns)	t <sub>RP</sub> (ns)	t <sub>RC</sub> (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

**Table 2: Addressing**

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	8K A[12:0]	16K A[13:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (64 Meg x 16)	2Gb (128 Meg x 16)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	1 S0#	1 S0#

**Table 3: Part Numbers and Timing Parameters – 512MB Modules**

 Base device: MT41J64M16,<sup>1</sup> 1Gb DDR3 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT4JSF6464HZ-1G6__	512MB	64 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT4JSF6464HZ-1G4__	512MB	64 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT4JSF6464HZ-1G1__	512MB	64 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

**Table 4: Part Numbers and Timing Parameters – 1GB Modules**

 Base device: MT41J128M16,<sup>1</sup> 2Gb DDR3 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT4JSF12864HZ-1G6__	1GB	128 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT4JSF12864HZ-1G4__	1GB	128 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT4JSF12864HZ-1G1__	1GB	128 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

- Notes:
1. The data sheet for the base device can be found on Micron's Web site.
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT4JSF12864HZ-1G1D1.

## Pin Assignments and Descriptions

**Table 5: Pin Assignments**

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V <sub>REFDQ</sub>	53	DQ19	105	V <sub>DD</sub>	157	DQ42	2	V <sub>SS</sub>	54	V <sub>SS</sub>	106	V <sub>DD</sub>	158	DQ46
3	V <sub>SS</sub>	55	V <sub>SS</sub>	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V <sub>SS</sub>	6	DQ5	58	DQ29	110	RAS#	162	V <sub>SS</sub>
7	DQ1	59	DQ25	111	V <sub>DD</sub>	163	DQ48	8	V <sub>SS</sub>	60	V <sub>SS</sub>	112	V <sub>DD</sub>	164	DQ52
9	V <sub>SS</sub>	61	V <sub>SS</sub>	113	WE#	165	DQ49	10	DQS0#	62	DQS3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V <sub>SS</sub>	12	DQS0	64	DQS3	116	ODT0	168	V <sub>SS</sub>
13	V <sub>SS</sub>	65	V <sub>SS</sub>	117	V <sub>DD</sub>	169	DQS6#	14	V <sub>SS</sub>	66	V <sub>SS</sub>	118	V <sub>DD</sub>	170	DM6
15	DQ2	67	DQ26	119	NF/A13	171	DQS6	16	DQ6	68	DQ30	120	NC	172	V <sub>SS</sub>
17	DQ3	69	DQ27	121	NC	173	V <sub>SS</sub>	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V <sub>SS</sub>	71	V <sub>SS</sub>	123	V <sub>DD</sub>	175	DQ50	20	V <sub>SS</sub>	72	V <sub>SS</sub>	124	V <sub>DD</sub>	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	NC	126	V <sub>REFCA</sub>	178	V <sub>SS</sub>
23	DQ9	75	V <sub>DD</sub>	127	V <sub>SS</sub>	179	V <sub>SS</sub>	24	DQ13	76	V <sub>DD</sub>	128	V <sub>SS</sub>	180	DQ60
25	V <sub>SS</sub>	77	NC	129	DQ32	181	DQ56	26	V <sub>SS</sub>	78	NC	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	NF	132	DQ37	184	V <sub>SS</sub>
29	DQS1	81	V <sub>DD</sub>	133	V <sub>SS</sub>	185	V <sub>SS</sub>	30	RESET#	82	V <sub>DD</sub>	134	V <sub>SS</sub>	186	DQS7#
31	V <sub>SS</sub>	83	A12	135	DQS4#	187	DM7	32	V <sub>SS</sub>	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V <sub>SS</sub>	34	DQ14	86	A7	138	V <sub>SS</sub>	190	V <sub>SS</sub>
35	DQ11	87	V <sub>DD</sub>	139	V <sub>SS</sub>	191	DQ58	36	DQ15	88	V <sub>DD</sub>	140	DQ38	192	DQ62
37	V <sub>SS</sub>	89	A8	141	DQ34	193	DQ59	38	V <sub>SS</sub>	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V <sub>SS</sub>	40	DQ20	92	A4	144	V <sub>SS</sub>	196	V <sub>SS</sub>
41	DQ17	93	V <sub>DD</sub>	145	V <sub>SS</sub>	197	SA0	42	DQ21	94	V <sub>DD</sub>	146	DQ44	198	EVENT#
43	V <sub>SS</sub>	95	A3	147	DQ40	199	V <sub>DDSPD</sub>	44	V <sub>SS</sub>	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V <sub>SS</sub>	202	SCL
47	DQS2	99	V <sub>DD</sub>	151	V <sub>SS</sub>	203	V <sub>TT</sub>	48	V <sub>SS</sub>	100	V <sub>DD</sub>	152	DQS5#	204	V <sub>TT</sub>
49	V <sub>SS</sub>	101	CK0	153	DM5	-	-	50	DQ22	102	CK1	154	DQS5	-	-
51	DQ18	103	CK0#	155	V <sub>SS</sub>	-	-	52	DQ23	104	CK1#	156	V <sub>SS</sub>	-	-

**Table 6: Pin Descriptions**

Symbol	Type	Description
A[13:0]	Input	<b>Address inputs:</b> Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[12:0] address the 1Gb DDR3 devices. A[13:0] address the 2Gb devices.
BA[2:0]	Input	<b>Bank address inputs:</b> BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CK0, CK0#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE0	Input	<b>Clock enable:</b> CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[7:0]	Input	<b>Data input mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
ODT0	Input	<b>On-die termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	<b>Reset:</b> An active LOW CMOS input referenced to V <sub>SS</sub> . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DD}$ .
S0#	Input	<b>Chip select:</b> S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[1:0]	Input	<b>Presence-detect address inputs:</b> These pins are used to configure the temperature sensor/SPD EEPROM address range on the I <sup>2</sup> C bus.
SCL	Input	<b>Serial clock for presence-detect:</b> SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
DQ[63:0]	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQS[7:0], DQS#[7:0]	I/O	<b>Data strobe:</b> DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	<b>Serial data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
EVENT#	Output (open drain)	<b>Temperature event:</b> The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V <sub>DD</sub>	Supply	<b>Power supply:</b> 1.5V $\pm 0.075V$ .
V <sub>DDSPD</sub>	Supply	<b>Serial EEPROM positive power supply:</b> +3.0V to +3.6V.
V <sub>REFCA</sub>	Supply	<b>Reference voltage:</b> Control, command, and address (V <sub>DD</sub> /2).

**Table 6: Pin Descriptions (Continued)**

Symbol	Type	Description
$V_{REFDQ}$	Supply	<b>Reference voltage:</b> DQ, DM ( $V_{DD}/2$ ).
$V_{SS}$	Supply	Ground.
$V_{TT}$	Supply	<b>Termination voltage:</b> Used for control, command, and address ( $V_{DD}/2$ ).
NC	–	<b>No connect:</b> These pins are not connected on the module.
NF	–	<b>No function:</b> Connected within the module, but provides no functionality.

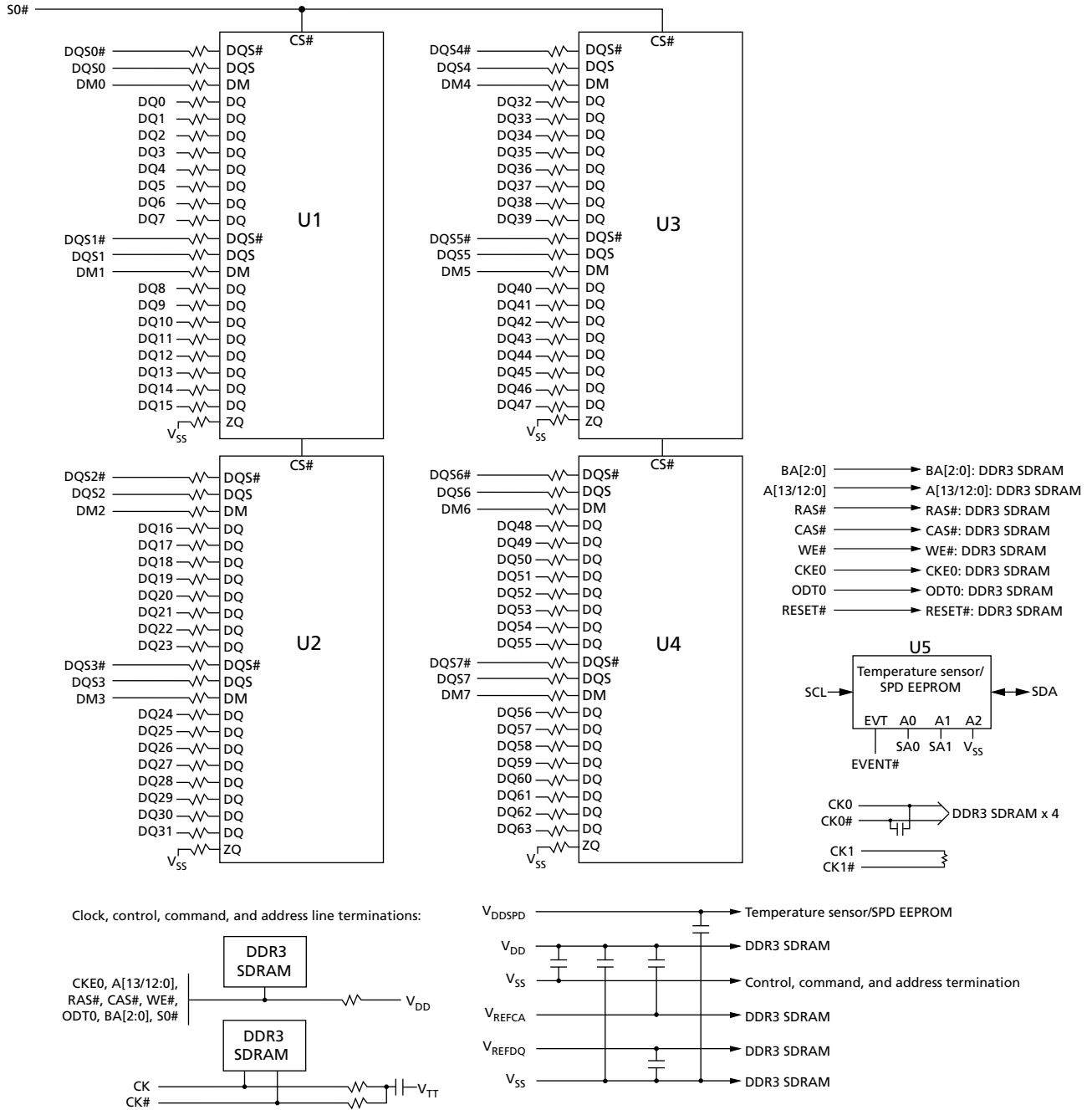
## DQ Map

**Table 7: Component-to-Module DQ Map**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	10	33	U2	0	26	67
	1	13	24		1	29	58
	2	11	35		2	27	69
	3	12	22		3	24	57
	4	14	34		4	30	68
	5	8	21		5	28	56
	6	15	36		6	31	70
	7	9	23		7	25	59
	8	4	4		8	16	39
	9	2	15		9	22	50
	10	0	5		10	20	40
	11	6	16		11	23	52
	12	1	7		12	21	42
	13	3	17		13	18	51
	14	5	6		14	17	41
15	7	18	15	19	53		
U2	0	38	140	U4	0	50	175
	1	37	132		1	53	166
	2	39	142		2	55	176
	3	33	131		3	49	165
	4	34	141		4	54	174
	5	32	129		5	48	163
	6	35	143		6	51	177
	7	36	130		7	52	164
	8	41	149		8	57	183
	9	47	160		9	62	192
	10	44	146		10	56	181
	11	43	159		11	59	193
	12	45	148		12	61	182
	13	42	157		13	58	191
	14	40	147		14	60	180
15	46	158	15	63	194		

## Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

## General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single  $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.



## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 8: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units
$V_{DD}$	$V_{DD}$ supply voltage relative to $V_{SS}$	-0.4	+1.975	V
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.4	+1.975	V

**Table 9: Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units	Notes	
$V_{DD}$	$V_{DD}$ supply voltage	1.425	1.5	1.575	V		
$V_{REFCA(DC)}$	Input reference voltage command/address bus	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V		
$V_{REFDQ(DC)}$	I/O reference voltage DQ bus	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V		
$I_{VTT}$	Termination reference current from $V_{TT}$	-600	-	+600	mA		
$V_{TT}$	Termination reference voltage (DC) – command/address bus	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V	1	
$I_I$	Input leakage current; Any input $0\text{V} \leq V_{IN} \leq V_{DD}$ ; $V_{REF}$ input $0\text{V} \leq V_{IN} \leq 0.95\text{V}$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	-8	0	+8	$\mu\text{A}$	
		DM	-2	0	+2		
$I_{OZ}$	Output leakage current; $0\text{V} \leq V_{OUT} \leq V_{DDQ}$ ; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	-5	0	+5	$\mu\text{A}$	
$I_{VREF}$	$V_{REF}$ supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)		-4	0	+4	$\mu\text{A}$	
$T_A$	Module ambient operating temperature	Commercial	0	-	+70	$^{\circ}\text{C}$	2, 3
$T_C$	DDR3 SDRAM component case operating temperature	Commercial	0	-	+85	$^{\circ}\text{C}$	2, 3, 4

- Notes:
- $V_{TT}$  termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
  - $T_A$  and  $T_C$  are simultaneous requirements.
  - For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
  - The refresh rate is required to double when  $85^{\circ}\text{C} < T_C \leq 95^{\circ}\text{C}$ .

## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

**Table 10: Module and Component Speed Grades**

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

## I<sub>DD</sub> Specifications

**Table 11: DDR3 I<sub>DD</sub> Specifications and Conditions – 512MB**

Values are for the MT41J64M16 DDR3 SDRAM only and are computed from values specified in the 1Gb (64 Meg x 16) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I <sub>DD0</sub>	480	440	400	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub>	680	600	520	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub>	48	48	48	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub>	180	160	140	mA
Precharge quiet standby current	I <sub>DD2Q</sub>	268	240	212	mA
Precharge standby current	I <sub>DD2N</sub>	280	260	220	mA
Precharge standby ODT current	I <sub>DD2NT</sub>	460	420	380	mA
Active power-down current	I <sub>DD3P</sub>	180	160	140	mA
Active standby current	I <sub>DD3N</sub>	260	240	220	mA
Burst read operating current	I <sub>DD4R</sub>	1280	1160	1040	mA
Burst write operating current	I <sub>DD4W</sub>	1720	1420	1180	mA
Refresh current	I <sub>DD5B</sub>	1040	960	880	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub>	24	24	24	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub>	36	36	36	mA
All banks interleaved read current	I <sub>DD7</sub>	1840	1680	1520	mA
Reset current	I <sub>DD8</sub>	56	56	56	mA

**Table 12: DDR3 I<sub>DD</sub> Specifications and Conditions – 1GB**

Values are for the MT41J128M16 DDR3 SDRAM only and are computed from values specified in the 2Gb (128 Meg x 16) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I <sub>DD0</sub>	440	400	360	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub>	540	520	500	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub>	48	48	48	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub>	160	140	120	mA
Precharge quiet standby current	I <sub>DD2Q</sub>	160	140	120	mA
Precharge standby current	I <sub>DD2N</sub>	168	148	128	mA
Precharge standby ODT current	I <sub>DD2NT</sub>	220	200	180	mA
Active power-down current	I <sub>DD3P</sub>	180	160	140	mA
Active standby current	I <sub>DD3N</sub>	180	160	140	mA
Burst read operating current	I <sub>DD4R</sub>	1080	980	800	mA
Burst write operating current	I <sub>DD4W</sub>	1120	1020	840	mA
Refresh current	I <sub>DD5B</sub>	860	800	760	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub>	48	48	48	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub>	60	60	60	mA
All banks interleaved read current	I <sub>DD7</sub>	1900	1700	1500	mA
Reset current	I <sub>DD8</sub>	56	56	56	mA

## Temperature Sensor with Serial Presence-Detect EEPROM

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I<sup>2</sup>C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

### Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via an I<sup>2</sup>C bus. Write protect (WP) is connected to V<sub>SS</sub>, permanently disabling hardware write protect. For further information please refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

**Table 13: Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions**

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V <sub>DDSPD</sub>	+3.0	+3.6	V
Supply current: V <sub>DD</sub> = 3.3V	I <sub>DD</sub>	–	+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V <sub>IH</sub>	+1.45	V <sub>DDSPD</sub> + 1	V
Input low voltage: Logic 0; SCL, SDA	V <sub>IL</sub>	–	+0.55	V
Output low voltage: I <sub>OUT</sub> = 2.1mA	V <sub>OL</sub>	–	+0.4	V
Input current	I <sub>IN</sub>	–5.0	+5.0	μA
Temperature sensing range	–	–40	+125	°C
Temperature sensor accuracy (initial release)	–	–2.0	+2.0	°C
Temperature sensor accuracy (class B)	–	–1.0	+1.0	°C

**Table 14: Sensor and EEPROM Serial Interface Timing**

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	t <sup>BUF</sup>	4.7	–	μs
SDA fall time	t <sup>F</sup>	20	300	ns
SDA rise time	t <sup>R</sup>	–	1,000	ns
Data hold time	t <sup>HD:DAT</sup>	200	900	ns
Start condition hold time	t <sup>H:STA</sup>	4.0	–	μs
Clock HIGH period	t <sup>HIGH</sup>	4.0	50	μs
Clock LOW period	t <sup>LOW</sup>	4.7	–	μs
SCL clock frequency	t <sup>SCL</sup>	10	100	kHz
Data setup time	t <sup>SU:DAT</sup>	250	–	ns

**Table 14: Sensor and EEPROM Serial Interface Timing (Continued)**

Parameter/Condition	Symbol	Min	Max	Units
Start condition setup time	$t_{SU:STA}$	4.7	–	$\mu s$
Stop condition setup time	$t_{SU:STO}$	4.0	–	$\mu s$

### EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated below. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

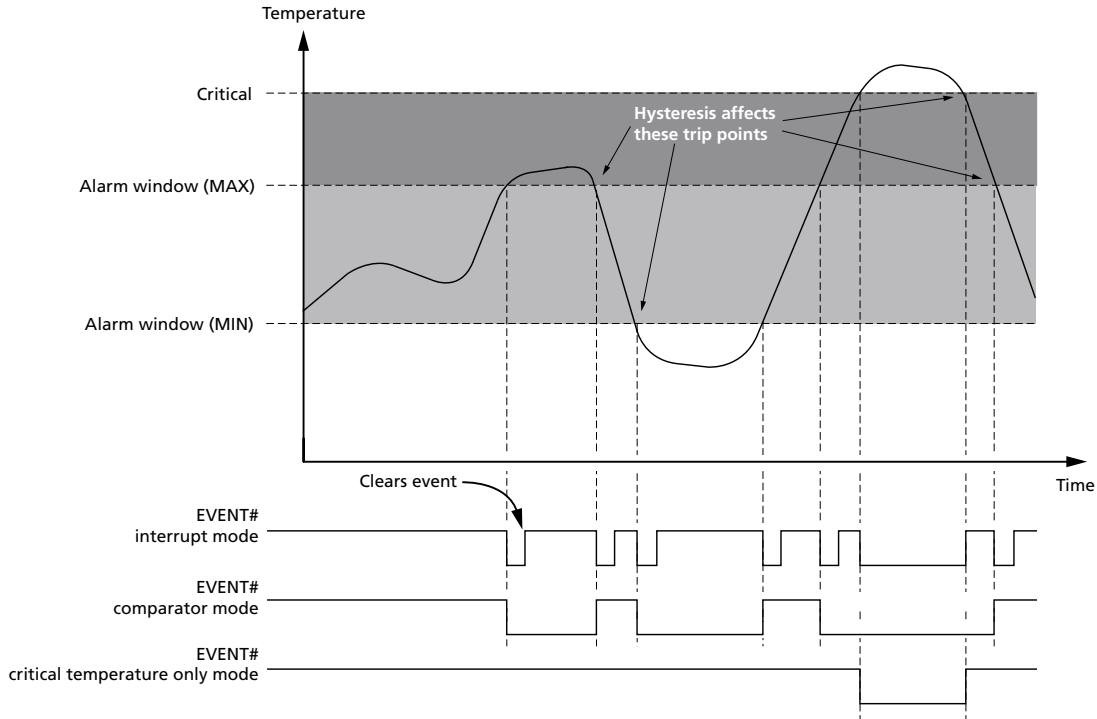
Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

### SMBus Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, and RW#, where A1 and A0 are the two slave subaddress pins, and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the temperature sensor/SPD EEPROM, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

**Figure 3: EVENT# Pin Functionality**



**Table 15: Temperature Sensor Registers**

Name	Address	Power-on Default
Pointer register	Not applicable	Undefined
Capability register	0x00	0x0001
Configuration register	0x01	0x0000
Alarm temperature upper boundary register	0x02	0x0000
Alarm temperature lower boundary register	0x03	0x0000
Critical temperature register	0x04	0x0000
Temperature register	0x05	Undefined

## Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

**Table 16: Pointer Register Bits 0–7**

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	Register select	Register select	Register select	Register select

**Table 17: Pointer Register Bits 0–2 Descriptions**

Bit			Register
2	1	0	
0	0	0	Capability register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary register
0	1	1	Alarm temperature lower boundary register
1	0	0	Critical temperature register
1	0	1	Temperature register

## Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

**Table 18: Capability Register (Address: 0x00)**

Bit							
15	14	13	12	11	10	9	8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit							
7	6	5	4	3	2	1	0
RFU	RFU	RFU	Temperature resolution		Wider range	Precision	Has alarm and critical temperature

**Table 19: Capability Register Bit Description**

Bit	Description
0	Basic capability 1: Has alarm and critical trip point capabilities
1	Accuracy 0: $\pm 2^{\circ}\text{C}$ over the active range and $\pm 3^{\circ}\text{C}$ over the monitor range 1: $\pm 1^{\circ}\text{C}$ over the active range and $\pm 2^{\circ}\text{C}$ over the monitor range
2	Wider range 0: Temperatures lower than $0^{\circ}\text{C}$ are clamped to a binary value of 0 1: Temperatures below $0^{\circ}\text{C}$ can be read



**Table 19: Capability Register Bit Description (Continued)**

Bit	Description
4:3	Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB
15:5	0: Must be set to zero

## Configuration Register

**Table 20: Configuration Register (Address: 0x01)**

Bit							
15	14	13	12	11	10	9	8
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode
Bit							
7	6	5	4	3	2	1	0
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

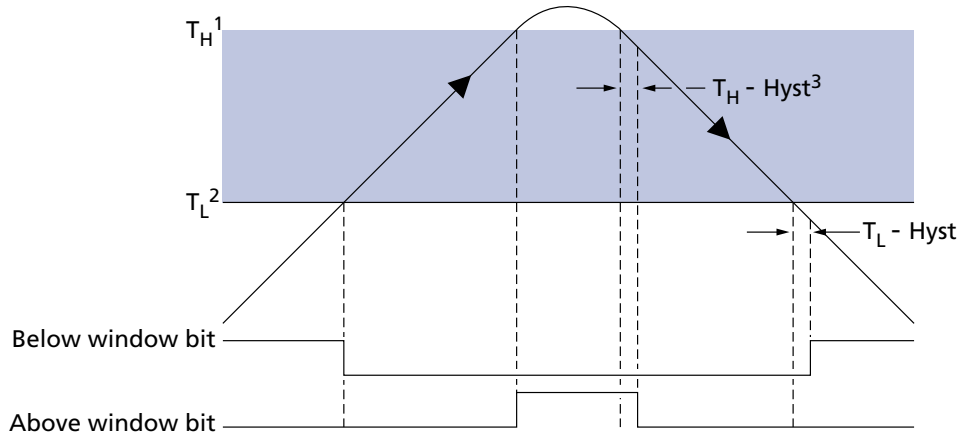
**Table 21: Configuration Register Bit Descriptions**

Bit	Description	Notes
0	Event mode 0: Comparator mode 1: Interrupt mode	Event mode cannot be changed if either of the lock bits is set.
1	EVENT# polarity 0: Active LOW 1: Active HIGH	EVENT# polarity cannot be changed if either of the lock bits is set.
2	Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached	
3	Event output control 0: Event output disabled 1: Event output enabled	
4	Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition	This is a read-only field in the register. The event causing the event can be determined from the read temperature register.
5	Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode	

**Table 21: Configuration Register Bit Descriptions (Continued)**

Bit	Description	Notes
6	Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed	
7	Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed	
8	Shutdown mode 0: Enabled 1: Shutdown	The shutdown mode is a power-saving mode that disables the temperature sensor.
10:9	Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C	<p>When enabled, a hysteresis is applied to temperature movement around the trip points (see Figure 4 (page 19)). As an example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C.</p> <p>The hysteresis is applied to both the above alarm window and the below alarm window bits found in the read-only temperature register (see Table 22 (page 19)). EVENT# is also affected by this register.</p>

Figure 4: Hysteresis Applied to Temperature Around Trip Points



- Notes:
1.  $T_H$  is the value set in the alarm temperature upper boundary trip register.
  2.  $T_L$  is the value set in the alarm temperature lower boundary trip register.
  3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 22: Hysteresis Applied to Alarm Window Bits in the Temperature Register

Condition	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature Gradient	Critical Temperature	Temperature Gradient	Critical Temperature
Sets	Falling	$T_L - \text{Hyst}$	Rising	$T_H$
Clears	Rising	$T_L$	Falling	$T_H - \text{Hyst}$

### Temperature Format

The temperature trip point registers and temperature readout register use a 2's complement format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C, depending on which register is referenced. For example, assuming an LSB of 0.0625°C:

- A value of 0x018C would equal 24.75°C
- A value of 0x06C0 would equal 108°C
- A value of 0x1E74 would equal -24.75°C

## Temperature Trip Point Registers

The upper and lower temperature boundary registers are used to set the maximum and minimum values of the alarm window. LSB for these registers is 0.25°C. All RFU bits in the register will always report zero.

**Table 23: Alarm Temperature Lower Boundary Register (Address: 0x02)**

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
Alarm window upper boundary temperature															

**Table 24: Alarm Temperature Lower Boundary Register (Address: 0x03)**

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
Alarm window lower boundary temperature															

## Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

**Table 25: Critical Temperature Register (Address: 0x04)**

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
Critical temperature trip point															

## Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.



**Table 26: Temperature Register (Address: 0x05)**

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Above critical trip	Above alarm window	Below alarm window	MSB	Temperature											LSB

**Table 27: Temperature Register Bit Descriptions**

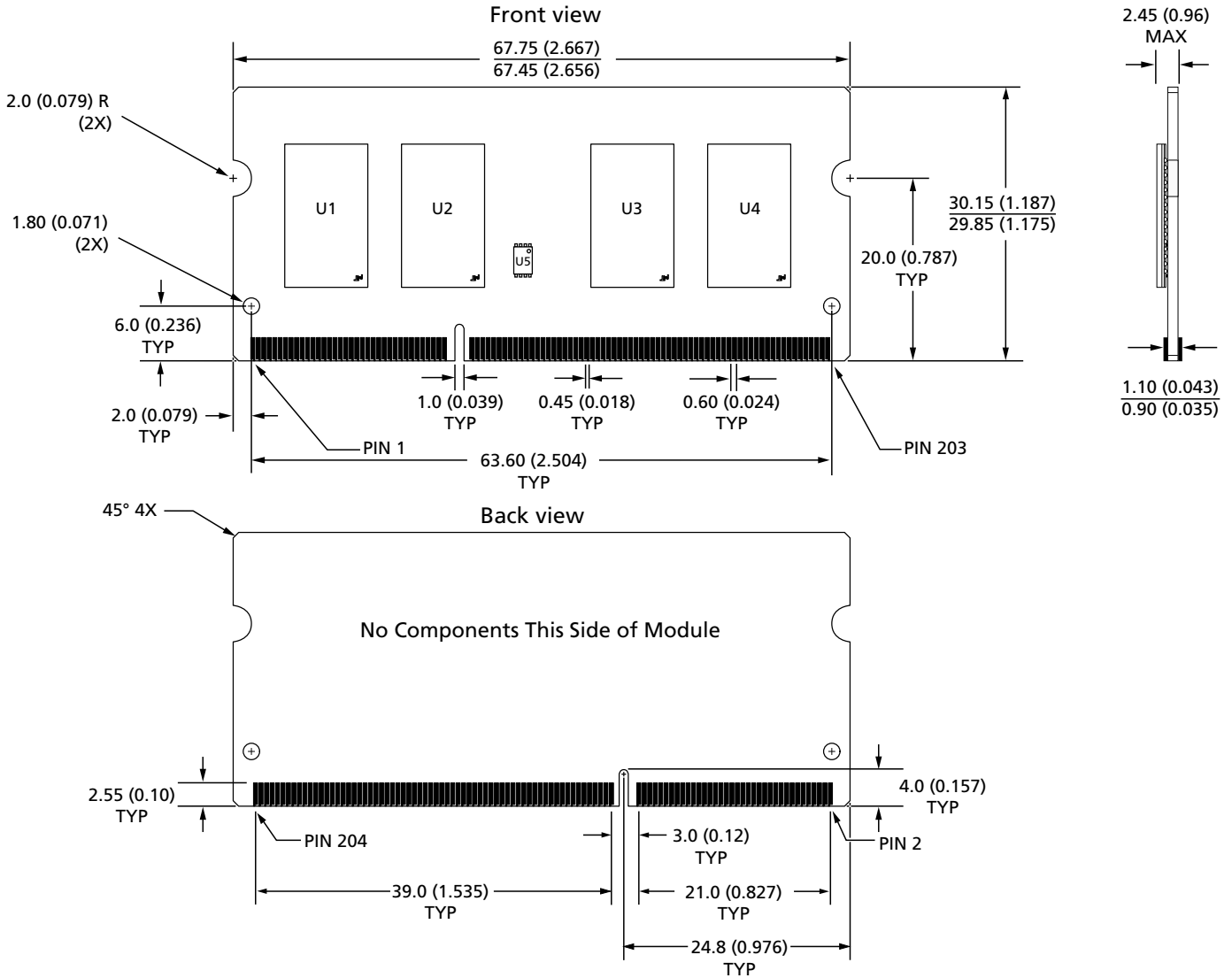
Bit	Description
13	Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window
14	Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window
15	Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point

### Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:  
[www.micron.com/SPD](http://www.micron.com/SPD).

## Module Dimensions

Figure 5: 204-Pin DDR3 SODIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
2. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.