IS42S16400

1 Meg Bits x 16 Bits x 4 Banks (64-MBIT) SYNCHRONOUS DYNAMIC RAM

TARGET SPECIFICATION
JUNE 2000

FEATURES

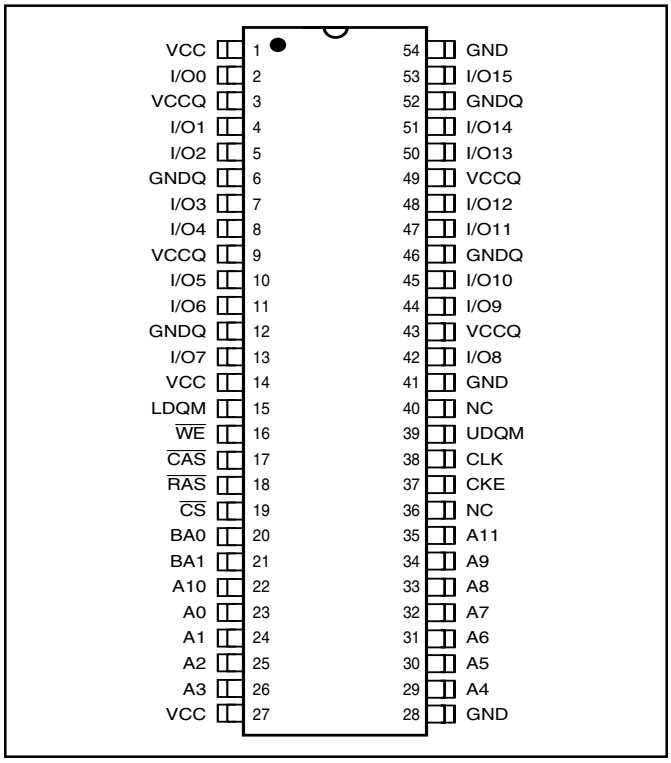
- Clock frequency: 166, 143, 125, 100 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access/precharge
- Single 3.3V power supply
- LVTTL interface
- Programmable burst length
  – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- Self refresh modes
- 4096 refresh cycles every 64 ms
- Random column address every clock cycle
- Programmable $\overline{\text{CAS}}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM
- Industrial temperature availability
- Package 400-mil 54-pin TSOP II

DESCRIPTION

ISSI's 16Mb Synchronous DRAM IS42S16400 is organized as a 1,048,576 bits x 16-bit x 4-bank for improved performance. The synchronous DRAMs achieve high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input.

PIN CONFIGURATIONS

54-Pin TSOP (Type II)



PIN DESCRIPTIONS

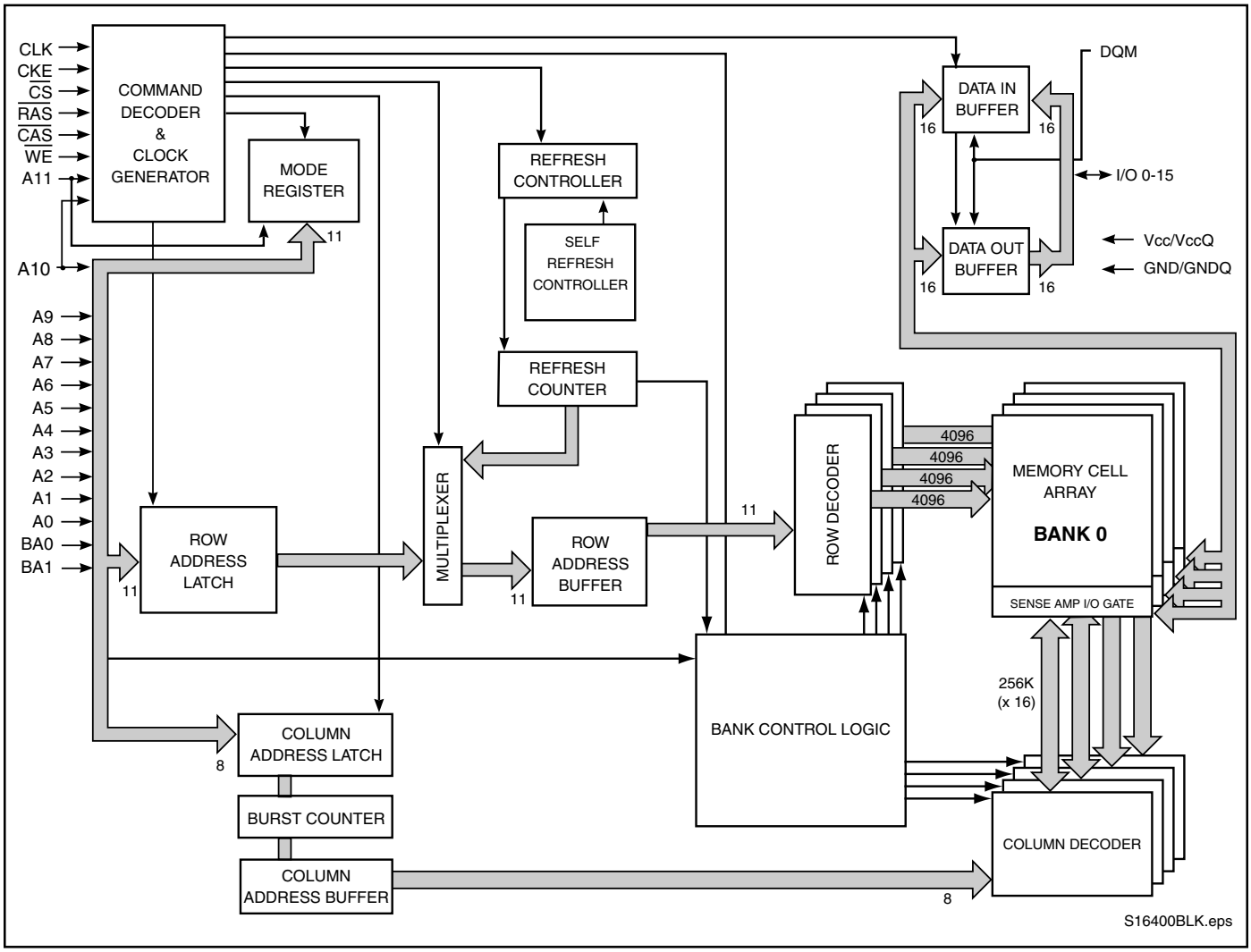
A0-A11	Address Input
BA0, BA1	Bank Select Address
I/O0 to I/O15	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe Command
$\overline{\text{CAS}}$	Column Address Strobe Command

$\overline{\text{WE}}$	Write Enable
LDQM	Lower Bye, Input/Output Mask
UDQM	Upper Bye, Input/Output Mask
Vcc	Power
GND	Ground
VccQ	Power Supply for I/O Pin
GNDQ	Ground for I/O Pin
NC	No Connection

PIN FUNCTIONS

Pin No.	Symbol	Type	Function (In Detail)
23 to 26 29 to 34 22, 35	A0-A11	Input Pin	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (A0-A7 with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
20, 21	BA0, BA1	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
17	$\overline{CAS}$	Input Pin	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
37	CKE	Input Pin	The CKE input determines whether the CLK input is enabled within the device. When is CKE HIGH, the next rising edge of the CLK signal will be valid, and when LOW, invalid. When CKE is LOW, the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE is an asynchronous input.
38	CLK	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
19	$\overline{CS}$	Input Pin	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
2, 4, 5, 7, 8, 10, 11,13, 42, 44, 45, 47, 48, 50, 51, 53	I/O0 to I/O15	I/O Pin	I/O0 to I/O15 are I/O pins. I/O through these pins can be controlled in byte units using the LDQM and UDQM pins.
15, 39	LDQM, UDQM	Input Pin	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state when LDQM/UDQM is HIGH. This function corresponds to $\overline{OE}$ in conventional DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
18	$\overline{RAS}$	Input Pin	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
16	$\overline{WE}$	Input Pin	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
3, 9, 43, 49	VccQ	Power Supply Pin	VccQ is the output buffer power supply.
1, 14, 27	Vcc	Power Supply Pin	Vcc is the device internal power supply.
6, 12, 46, 52	GNDQ	Power Supply Pin	GNDQ is the output buffer ground.
28, 41, 54	GND	Power Supply Pin	GND is the device internal ground.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{CC\ MAX}$	Maximum Supply Voltage		–1.0 to +4.6	V
$V_{CCQ\ MAX}$	Maximum Supply Voltage for Output Buffer		–1.0 to +4.6	V
V_{IN}	Input Voltage		–1.0 to +4.6	V
V_{OUT}	Output Voltage		–1.0 to +4.6	V
$P_{D\ MAX}$	Allowable Power Dissipation		1	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Com. Ind.	0 to +70 –40 to +85	°C
T_{STG}	Storage Temperature		–55 to +150	°C

DC RECOMMENDED OPERATING CONDITIONS(2) (At T_A = 0 to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}, $V_{CC}Q$	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage(3)	2.0	—	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage(4)	-0.3	—	+0.8	V

CAPACITANCE CHARACTERISTICS(1,2) (At T_A = 0 to +25°C, Vcc = VccQ = 3.3 ± 0.3V, f = 1 MHz)

Symbol	Parameter	Typ.	Max.	Unit
$C_{IN}1$	Input Capacitance: A0-A11, BA0, BA1	—	4	pF
$C_{IN}2$	Input Capacitance: (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM)	—	4	pF
CI/O	Data Input/Output Capacitance: I/O0-I/O15	—	5	pF

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to GND.
3. V_{IH} (max) = V_{CCQ} + 2.0V with a pulse width ≤ 3 ns.
4. V_{IL} (min) = GND – 2.0V with a pulse < 3 ns and -1.5V with a pulse < 5ns.

DC ELECTRICAL CHARACTERISTICS (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition		Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}, with pins other than the tested pin at 0V			–5	5	µA
I_{OL}	Output Leakage Current	Output is disabled 0V ≤ V_{OUT} ≤ V_{CC}			–5	5	µA
V_{OH}	Output High Voltage Level	I_{OUT} = –2 mA			2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OUT} = +2 mA			—	0.4	V
I_{CC1}	Operating Current(1,2)	One Bank Operation,	$\overline{CAS}$ latency = 3	-6	—	140	mA
		Burst Length=1		-7	—	125	mA
		t_{RC} ≥ t_{RC} (min.)		-8	—	115	mA
		I_{OUT} = 0mA		-10	—	110	mA
I_{CC2P}	Precharge Standby Current	CKE ≤ V_{IL} (MAX)	t_{CK} = t_{CK} (MIN)	—	—	3	mA
I_{CC2PS}	(In Power-Down Mode)		t_{CK} = ∞	—	—	2	mA
I_{CC2N}	Precharge Standby Current	CKE ≥ V_{IH} (MIN)	t_{CK} = t_{CK} (MIN)	—	—	30	mA
I_{CC2NS}	(In Non Power-Down Mode)		t_{CK} = ∞	—	—	6	mA
I_{CC3P}	Active Standby Current	CKE ≤ V_{IL} (MAX)	t_{CK} = t_{CK} (MIN)	—	—	3	mA
I_{CC3PS}	(In Power-Down Mode)		t_{CK} = ∞	—	—	2	mA
I_{CC3N}	Active Standby Current	CKE ≥ V_{IH} (MIN)	t_{CK} = t_{CK} (MIN)	—	—	40	mA
I_{CC3NS}	(In Non Power-Down Mode)		t_{CK} = ∞	—	—	15	mA
I_{CC4}	Operating Current	t_{CK} = t_{CK} (MIN)	$\overline{CAS}$ latency = 3	-6	—	170	mA
	(In Burst Mode)(1)	I_{OUT} = 0mA		-7	—	150	mA
				-8	—	140	mA
				-10	—	130	mA
			$\overline{CAS}$ latency = 2	-6	—	170	mA
				-7	—	150	mA
				-8	—	140	mA
				-10	—	130	mA
I_{CC5}	Auto-Refresh Current	t_{RC} = t_{RC} (MIN)	$\overline{CAS}$ latency = 3	-6	—	230	mA
				-7	—	230	mA
				-8	—	190	mA
				-10	—	130	mA
			$\overline{CAS}$ latency = 2	-6	—	170	mA
				-7	—	150	mA
				-8	—	140	mA
				-10	—	130	mA
I_{CC6}	Self-Refresh Current	CKE ≤ 0.2V			—	1	mA

Notes:
1. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between Vcc and GND for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.
2. Icc1 and Icc4 depend on the output load. The maximum values for Icc1 and Icc4 are obtained with the output open state.

AC CHARACTERISTICS[1,2,3]

Symbol	Parameter		-6 Min.	-6 Max.	-7 Min.	-7 Max.	Units
$t_{CK}3$	Clock Cycle Time	$\overline{CAS}$ Latency = 3	6	—	7	—	ns
$t_{CK}2$		$\overline{CAS}$ Latency = 2	8	—	8.6	—	ns
$t_{AC}3$	Access Time From CLK[4]	$\overline{CAS}$ Latency = 3	—	5.5	—	6	ns
$t_{AC}2$		$\overline{CAS}$ Latency = 2	—	6	—	6	ns
t_{CHI}	CLK HIGH Level Width		2	—	2.5	—	ns
t_{CL}	CLK LOW Level Width		2	—	2.5	—	ns
$t_{OH}3$	Output Data Hold Time	$\overline{CAS}$ Latency = 3	2.5	—	2.5	—	ns
$t_{OH}2$		$\overline{CAS}$ Latency = 2	2.5	—	2.5	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	ns
$t_{HZ}3$	Output HIGH Impedance Time[5]	$\overline{CAS}$ Latency = 3	—	5.5	—	6	ns
$t_{HZ}2$		$\overline{CAS}$ Latency = 2	—	6	—	6	ns
t_{DS}	Input Data Setup Time		1.5	—	1.5	—	ns
t_{DH}	Input Data Hold Time		0.8	—	0.8	—	ns
t_{AS}	Address Setup Time		1.5	—	1.5	—	ns
t_{AH}	Address Hold Time		0.8	—	0.8	—	ns
t_{CKS}	CKE Setup Time		1.5	—	1.5	—	ns
t_{CKH}	CKE Hold Time		0.8	—	0.8	—	ns
t_{CKA}	CKE to CLK Recovery Delay Time		1CLK+3	—	1CLK+3	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		1.5	—	1.5	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		0.8	—	0.8	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		60	—	63	—	ns
t_{RAS}	Command Period (ACT to PRE)		35	120,000	37	120,000	ns
t_{RP}	Command Period (PRE to ACT)		15	—	15	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		15	—	15	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		14	—	14	—	ns
$t_{DPL}3$	Input Data To Precharge Command Delay time	$\overline{CAS}$ Latency = 3	1CLK	—	1CLK	—	ns
$t_{DPL}2$		$\overline{CAS}$ Latency = 2	1CLK	—	1CLK	—	ns
$t_{DAL}3$	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)	$\overline{CAS}$ Latency = 3	1CLK+t_{RP}	—	1CLK+t_{RP}	—	ns
$t_{DAL}2$		$\overline{CAS}$ Latency = 2	1CLK+t_{RP}	—	1CLK+t_{RP}	—	ns
t_T	Transition Time		1	10	1	10	ns
t_{REF}	Refresh Cycle Time (4096)		—	64	—	64	ms

Notes:
1. When power is first applied, memory operation should be started 100 µs after Vcc and VccQ reach their stipulated voltages. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns.
3. The reference level is 1.4 V when measuring input signal timing. Rise and fall times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Access time is measured at 1.4V with the load shown in the figure below.
5. The time t_{HZ} (max.) is defined as the time required for the output voltage to transition by ± 200 mV from V_{OH} (min.) or V_{OL} (max.) when the output is in the high impedance state.

AC CHARACTERISTICS[1,2,3]

Symbol	Parameter		-8 Min.	-8 Max.	-10 Min.	-10 Max.	Units
$t_{CK}3$	Clock Cycle Time	$\overline{CAS}$ Latency = 3	8	—	10	—	ns
$t_{CK}2$		$\overline{CAS}$ Latency = 2	10	—	10	—	ns
$t_{AC}3$	Access Time From CLK[4]	$\overline{CAS}$ Latency = 3	—	6	—	7	ns
$t_{AC}2$		$\overline{CAS}$ Latency = 2	—	7	—	9	ns
t_{CHI}	CLK HIGH Level Width		3	—	3.5	—	ns
t_{CL}	CLK LOW Level Width		3	—	3.5	—	ns
$t_{OH}3$	Output Data Hold Time	$\overline{CAS}$ Latency = 3	2.5	—	2.5	—	ns
$t_{OH}2$		$\overline{CAS}$ Latency = 2	2.5	—	2.5	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	ns
$t_{HZ}3$	Output HIGH Impedance Time[5]	$\overline{CAS}$ Latency = 3	—	6	—	7	ns
$t_{HZ}2$		$\overline{CAS}$ Latency = 2	—	7	—	9	ns
t_{DS}	Input Data Setup Time		2.0	—	2.0	—	ns
t_{DH}	Input Data Hold Time		1	—	1	—	ns
t_{AS}	Address Setup Time		2.0	—	2.0	—	ns
t_{AH}	Address Hold Time		1	—	1	—	ns
t_{CKS}	CKE Setup Time		2.0	—	2.0	—	ns
t_{CKH}	CKE Hold Time		1	—	1	—	ns
t_{CKA}	CKE to CLK Recovery Delay Time		1CLK+3	—	1CLK+3	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		2.0	—	2.0	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		1	—	1	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		68	—	70	—	ns
t_{RAS}	Command Period (ACT to PRE)		42	120,000	44	120,000	ns
t_{RP}	Command Period (PRE to ACT)		18	—	18	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		18	—	18	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		15	—	15	—	ns
$t_{DPL}3$	Input Data To Precharge Command Delay time	$\overline{CAS}$ Latency = 3	1CLK	—	1CLK	—	ns
$t_{DPL}2$		$\overline{CAS}$ Latency = 2	1CLK	—	1CLK	—	ns
$t_{DAL}3$	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)	$\overline{CAS}$ Latency = 3	1CLK+t_{RP}	—	1CLK+t_{RP}	—	ns
$t_{DAL}2$		$\overline{CAS}$ Latency = 2	1CLK+t_{RP}	—	1CLK+t_{RP}	—	ns
t_T	Transition Time		1	10	1	10	ns
t_{REF}	Refresh Cycle Time		—	64	—	64	ms

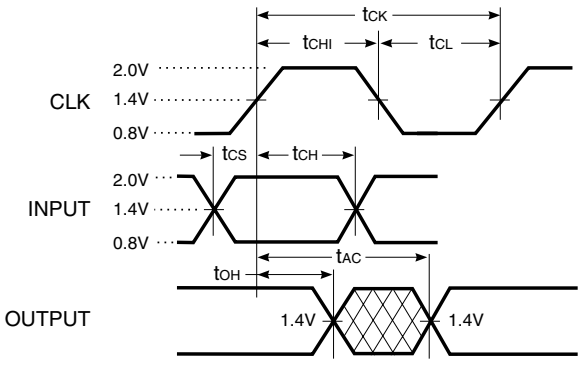
Notes:
1. When power is first applied, memory operation should be started 100 µs after Vcc and VccQ reach their stipulated voltages. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns.
3. The reference level is 1.4 V when measuring input signal timing. Rise and fall times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Access time is measured at 1.4V with the load shown in the figure below.
5. The time t_{HZ} (max.) is defined as the time required for the output voltage to transition by ± 200 mV from V_{OH} (min.) or V_{OL} (max.) when the output is in the high impedance state.

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

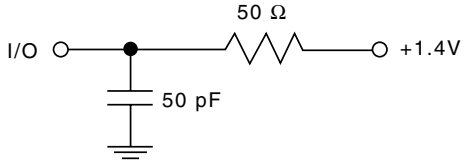
SYMBOL	PARAMETER		-6	-7	-8.	-10.	UNITS
—	Clock Cycle Time		6	7	8	10	ns
—	Operating Frequency		166	143	125	100	MHz
t_{CCD}	READ/WRITE command to READ/WRITE command		1	1	1	1	cycle
t_{CKED}	CKE to clock disable or power-down entry mode		1	1	1	1	cycle
t_{PED}	CKE to clock enable or power-down exit setup mode		1	1	1	1	cycle
t_{DQD}	DQM to input data delay		0	0	0	0	cycle
t_{DQM}	DQM to data mask during WRITEs		0	0	0	0	cycle
t_{DQZ}	DQM to data high-impedance during READs		2	2	2	2	cycle
t_{DWD}	WRITE command to input data delay		0	0	0	0	cycle
t_{DAL}	Data-in to ACTIVE command		5	5	4	4	cycle
t_{DPL}	Data-in to PRECHARGE command		2	2	2	2	cycle
t_{BDL}	Last data-in to burst STOP command		1	1	1	1	cycle
t_{CDL}	Last data-in to new READ/WRITE command		1	1	1	1	cycle
t_{RDL}	Last data-in to PRECHARGE command		2	2	2	2	cycle
t_{MRD}	LOAD MODE REGISTER command to ACTIVE or REFRESH command		2	2	2	2	cycle
t_{ROH}	Data-out to high-impedance from PRECHARGE command	CL = 3 CL = 2	3 2	3 2	3 2	3 2	cycle

AC TEST CONDITIONS (Input/Output Reference Level: 1.4V)

Input



Output Load



OPERATIONAL DESCRIPTION tbd
GENERAL TRUTH TABLE tbd
TIMING DIAGRAMS tbd

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS42S16400-6T	400-mil TSOP II
143MHz	7	IS42S16400-7T	400-mil TSOP II
124MHz	8	IS42S16400-8T	400-mil TSOP II
100 MHz	10	IS42S16400-10T	400-mil TSOP II

Industrial Range: -40°C to 85°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS42S16400-6TI	400-mil TSOP II
143MHz	7	IS42S16400-7TI	400-mil TSOP II
124MHz	8	IS42S16400-8TI	400-mil TSOP II
100 MHz	10	IS42S16400-10TI	400-mil TSOP II

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