

Version	Date/ Datum	Initiated by/ Veranlasser	Reason of modification / Grund der Änderung item, section / Position, Absatz
01	2006-09-11	Lim, Hooi-Bin (OPD - Oled FE Prod. Dev.)	Update product dwg OBS Internal dc products & add handling spec, PPCM-No:NA Detail of Description for Changes please refer to Revision Log
02	2006-10-12	Lim, Hooi-Bin (OPD - Oled FE Prod. Dev.)	Update IC power diagram, PPCM-No:NA Detail of Description for Changes please refer to Revision Log
03	2007-01-03	Lim, Hooi-Bin (OPD - Oled FE Prod. Dev.)	To update product drawings' pin-out, PPCM-No:NA

The document No.
Die Unterlage mit der Nr.:

A63857-H015X-D000-*-7680

Issue:
Version:

02

is no longer valid and must be sent to DocCenter.

Applicable Area - Scope / Gültigkeitsbereich	
Corporation:	OSRAM Opto Semiconductors
Location:	Penang
Cluster:	OLED
Unit:	OLED Module
SubUnit:	Atlanta
Process:	

Function / Funktion	Name & Dienststelle (in Druckschrift) Name & Department (printed letters)	Date / Datum	Signature / Unterschrift
Author/Change-Author	Lim, Hooi-Bin (OPD - Oled FE Prod. Dev.)	2007-01-03	sgd. Livelink WF-ID#7910065
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Product Engineering	Ng, Chee-Pin (OLM - OLED Mfg Support)	2007-01-05	sgd. Livelink WF-ID#7910065
Production QM/QE	Lim, Lim-Ling (QED - Display QE)	2007-01-04	sgd. Livelink WF-ID#7910065

Product Specification for Pictiva TM 128X64 OLED Module, Elegance Yellow, SSD0323,
(Atlanta HX1XX) OS128064PK16MXXXXX

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Revision Log

Rev	Description	Orig. By	ECN # / Date
A	New specification	S. Grespan	ECN# SJ5-1021 6/13/05
B	Removed H00 module, new time table, inspection criteria and title changed.	S. Grespan	ECN# SJ5-1072 11/14/05
01	<ol style="list-style-type: none"> 1. To add HZ150 product to product list 2. To add color products to product list 3. To obsolete H0154 & H0155 Internal DC-DC product 4. To update operating temperature range to -30°C to +70°C 5. To add Graphic Display Ddata RAM (GDDRAM) access 6. To update Parallel Interface Timing Diagram for 68 Series & 80 series MPU 7. To remove potential burn-in precaution 8. To update power up and power down sequence 9. To update module product drawings 10. To add handling spec 11. Change Title 	Lim Hooi-Bin	2006-09-11
02	<ol style="list-style-type: none"> 1. To remove Clarity Orange from spec title 2. To remove Clarity Orange H0170 product 3. To add product Q numbers 4. To update block diagram 5. To update interface diagram 6. To update Zif connection pin out Serial setting 7. To update Initialization settings 8. To add lower luminance settings of 30 nits & 75 nits 9. To update power up and power down sequence 10. To split duration of qualification test to "Guaranteed" & "Capability" 11. To update product marking label height dimension 12. To add LTO to Qualification tests 	Lim Hooi-Bin	2006-10-12

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1. TITLE

- 1.1. Product Specification for Pictiva™ 128X64 OLED Module, Elegance Yellow, SSD0323, (Atlanta HX1XX) OS128064PK16MXXXXX.

2. PURPOSE

- 2.1. This product specification is specifically for OLED Atlanta Module HX1XX.

3. SCOPE

- 3.1. This product specification is applicable to all HX1XX modules.

4. REFERENCE DOCUMENTS

- 4.1. C63062-H0100-A001-D H0150/1 & HZ150 ATLANTA WITH BEZEL MODULE PRODUCT DRAWING
- 4.2. C63062-H0152-A001-C H0152/3 ATLANTA MODULE PRODUCT DRAWING
- 4.3. SOLOMON SSD0323 128 x 80, 16 Gray scale Dot Matrix OLED/PLED Segment/Common Driver with Controller

5. OTHER REQUIREMENTS**5.1. FEATURES, FUNCTIONS, and REQUIREMENTS****5.1.1. Product Summary:****General OLED Module Description**

Part Number	OS128064PK16Mxxxxx
Display Format	128 columns x 64 rows
Pixel Pitch	0.285 (W) x 0.285 (H) mm
Pixel Size	0.255 (W) x 0.255 (H) mm
Display Diagonal	1.6"
Color	Monochrome Elegance Yellow
Grayscale	4 bits
Active Area	36.46 (W) X 18.22 (H) mm
Viewing Area	38.46 (W) X 20.22 (H) mm
Module Size	Varies. Refer to part number table
Glass Size	46.83 (W) X 28.77 (H) X 2.2 (T) mm (including polarizer)
Driver IC	SSD0323
Packaging and interconnect	COF with ZIF tail

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5.1.2. Part Number Options:

Part Number Description

Q Description	Q number	Interface	ROHS/ Non ROHS	Bezel	Color	Factory Code
OS128064PK16MY0A00	Q65110A0950	Parallel	Non-RoHS	Metal	Elegance Yellow	H0150
OS128064PK16MY0Z00	Q65110A5499	Parallel	RoHS	Metal	Elegance Yellow	HZ150
OS128064PK16MY0A01	Q65110A1668	Serial	Non-RoHS	Metal	Elegance Yellow	H0151
OS128064PK16MY0A10	Q65110A1711	Parallel	Non-RoHS	None	Elegance Yellow	H0152
OS128064PK16MY0A11	Q65110A6257	Serial	Non-RoHS	None	Elegance Yellow	H0153
OS128064PK16MR1A00	Q65110A3426	Parallel	Non-RoHS	Metal	Scarlet Red	H1120
OS128064PK16MG1A00	Q65110A3427	Parallel	Non-RoHS	Metal	Lime Green	H1150
OS128064PK16MG2A00	Q65110A3428	Parallel	Non-RoHS	Metal	Jungle Green	H1160
OS128064PK16MO1A00	Q65110A3429	Parallel	Non-RoHS	Metal	Tiger Orange	H1170
OS128064PK16MY1A00	Q65110A3031	Parallel	Non-RoHS	Metal	Light Green	H0160
OS128064PK16MY1A10	Q65110A3030	Parallel	Non-RoHS	None	Light Green	H0162

Note 1 : Please refer to product drawings for Module dimensions

Note 2 : All the above products are External Vcc

Note 3 : Some part numbers in ths specification may become obsolete in the course of product life cycle. Check with Osram for product availability before incorporating a part number into a design

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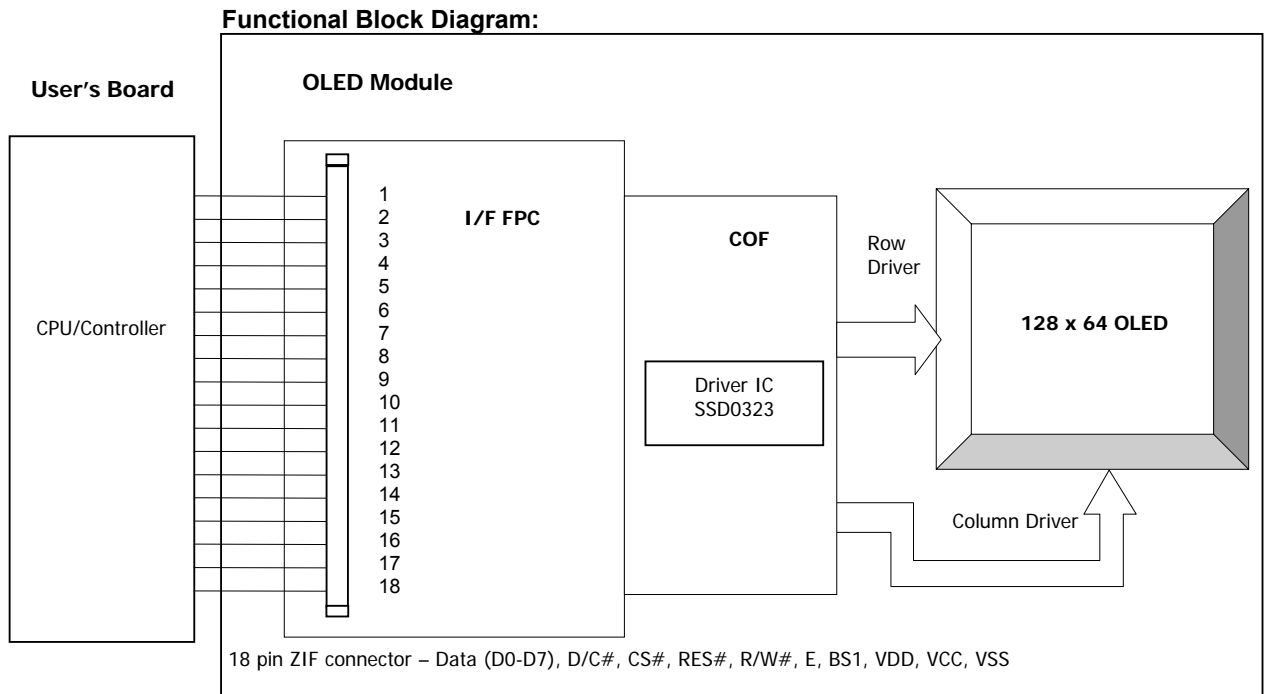
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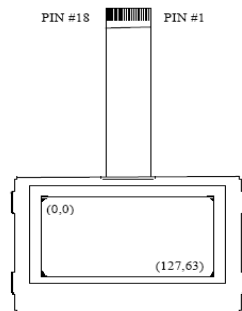
5.1.3. Electrical Characteristics



Overall block diagram of display module assembly and interface

5.1.4. Graphic Area Pixel Mapping:

Rows are designed in the interleave configuration. The COM re-map command allows for proper orientation of the image displayed.



Pixel mapping and glass design layout (top plated contacts)

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5.1.5. Graphic Display Data RAM (GDDRAM) Access

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to table below for GDDRAM address map description)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Row
Outputs Address
(HEX)
(Display Startline=0)

GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124		SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]		D5040[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]		D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	

COM Row
Outputs Address
(HEX)
(Display Startline=0)

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GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	(HEX)
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	

COM Outputs Row Address (HEX)
(Display Startline=0)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
(Display Startline=10H)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00										(HEX)
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										

COM Outputs Row Address (HEX)
(Display Startline=0)

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5.1.6. Duty Cycle:

The pixel rows are multiplexed and will operate at a nominal duty cycle of 1/64. The default duty cycle is 1/80. During initialization a software command must be used to set the required duty cycle.

5.1.7. Interface Pin Out:

There are two interface pin out options corresponding to the parallel and serial interface requirements. The interface is factory-set by jumper JP1 on the FPC; JP1 = 1 for parallel I/F, JP1 = 0 for serial I/F. For the parallel I/F version only, the user can select the interface protocol using pin #3 BS1 (for Motorola 68 series or Intel 80 series).

5.1.7.1. ZIF Connection Pin Out for External Power Supply (Standard)

Pin No.	Parallel I/F		Serial I/F	
	Name	Description	Name	Description
1	CS#	Chip Select	CS#	Chip Select
2	RES#	Reset	RES#	Reset
3	BS1	Parallel I/F protocol Low: 68 series; High: 80 series	BS1	Set to Low or connect to VSS
4	D/C#	High: Data in GDRAM Low: Command	D/C#	High: Data in GDRAM Low: Command
5	R/W# (WR#)	Read/Write selector for 68 series; Write strobe for 80 series	NC	No connect
6	E (RD#)	E clock for 68 series; RD strobe for 80 series	NC	No connect
7	D0	Parallel Data 0	SCLK	Serial Clock Input
8	D1	Parallel Data 1	SDIN	Serial Data Input
9	D2	Parallel Data 2	NC	Must be floating
10	D3	Parallel Data 3	NC	No connect
11	D4	Parallel Data 4	NC	No connect
12	D5	Parallel Data 5	NC	No connect
13	D6	Parallel Data 6	NC	No connect
14	D7	Parallel Data 7	NC	No connect
15	NC	No connect	NC	No connect
16	VDD	Logic Power	VDD	Logic Power
17	VCC	OLED Power Supply	VCC	OLED Power Supply
18	VSS	Ground	VSS	Ground

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5.1.8. Absolute Maximum Ratings:**Absolute Maximum Ratings**

Symbol	Description	Range	Unit
VDD	Supply Voltage for logic	-0.3 to +4.0	V
VCC	Supply Voltage for driver	0 to +16	V
Vin	Input Voltage	VSS-0.3 to VDD+0.4	V
Top	Operating Temperature	-30 to +70	°C
Tstg	Storage Temperature	-40 to +70	°C

5.1.9. DC Characteristics of Complete Module:

(-30°C to +70°C Temperature Range, except as noted)

Recommended DC Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	
Logic operating voltage	VDD	2.4	3.0	3.5	V	
OLED driver input voltage	VCC	12	12.5	13	V	
VDD Operating Current	IDD	-	-	650	µA	
VCC Operating Current (All pixels ON, Luminance at typical value)	ICC ⁽¹⁾	-	22	24	mA	
	ICC ⁽²⁾	28	29	32		
	ICC ⁽³⁾	-	22	25	mA	
Driver Sleep Mode Current (at 25°C)	ISL	-	-	5.0	µA	
Logic input voltage	High	VIH	.8 *VDD	-	VDD	V
	Low	VIL	0	-	.2*VDD	V
Logic output voltage	High (IOH=-.5mA)	VOH	.9 *VDD	-	VDD	V
	Low (IOL=.5mA)	VOL	0	-	.1*VDD	V

Note:

ICC (1)	H0150-OS128064PK16MY0A00
	HZ150-OS128064PK16MY0Z00
	H0151-OS128064PK16MY0A01
	H0152-OS128064PK16MY0A10
	H0153-OS128064PK16MY0A11
ICC (2)	H0150-OS128064PK16MY0A00 (High luminance)
	H1120-OS128064PK16MR1A00
	H1150-OS128064PK16MG1A00
	H1160-OS128064PK16MG2A00
	H1170-OS128064PK16MO1A00
ICC (3)	H0160-OS128064PK16MY1A00
	H0162-OS128064PK16MY1A10

Product Specification for Pictiva TM 128X64 OLED Module, Elegance Yellow, SSD0323,
(Atlanta HX1XX) OS128064PK16MXXXXX

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5.1.10. Power Consumption:

(VDD= 3.0V, VCC = 12.5V, Frame Frequency = 75 Hz, unless otherwise stated)

Power Consumption

Model	Typical Luminance Cd/m ²	Typical Power Consumption* (mW), Dual supply (VDD, VCC) ±10%				
		Power Save mode (Sleep mode)	All pixels ON @ typical luminance	10% ON @ typical luminance	10% ON @ 15% of typ. luminance	2% ON @ 15% of typ. luminance
H0150-OS128064PK16MY0A00	100	0.165	272	33	13	7
HZ150-OS128064PK16MY0Z00	100	0.165	272	33	13	7
H0151-OS128064PK16MY0A01	100	0.165	272	33	13	7
H0152-OS128064PK16MY0A10	100	0.165	272	33	13	7
H0153-OS128064PK16MY0A11	100	0.165	272	33	13	7
H0150-OS128064PK16MY0A00 (High luminance)	150	0.204	360	44	12	5
H1120-OS128064PK16MR1A00	12	0.204	360	44	12	5
H1150-OS128064PK16MG1A00	90	0.204	360	44	12	5
H1160-OS128064PK16MG2A00	20	0.204	360	44	12	5
H1170-OS128064PK16MO1A00	35	0.204	360	44	12	5
H0160-OS128064PK16MY1A00	110	0.204	306	38	11	5
H0162-OS128064PK16MY1A10	110	0.204	306	38	11	5

Product Specification for Pictiva TM 128X64 OLED Module, Elegance Yellow, SSD0323, (Atlanta HX1XX) OS128064PK16MXXXXX

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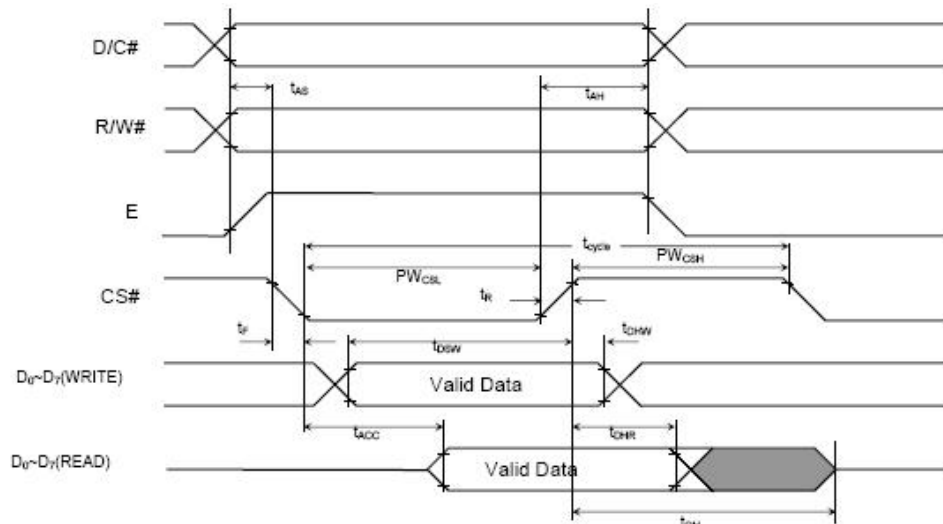
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5.1.11. AC Timing Characteristics:

5.1.11.1. Parallel Interface Timing Characteristics:

Parallel Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	t _{cycle}	300	-	-	ns
Address Setup Time	t _{AS}	0	-	-	ns
Address Hold Time	t _{AH}	0	-	-	ns
Write Data Setup Time	t _{DSW}	40	-	-	ns
Write Data Hold Time	t _{DHW}	15	-	-	ns
Read Data Hold Time	t _{DHR}	20	-	-	ns
Output Disable Time	t _{OH}	-	-	70	ns
Access Time	t _{ACC}	-	-	140	ns
Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	PW _{CSL}	120 60	-	-	ns
Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	PW _{CSH}	60 60	-	-	ns
Rise Time	t _R	-	-	15	ns
Fall Time	t _F	-	-	15	ns
Frame Frequency	t _{FRM}	70	75	85	Hz



Parallel Interface Timing Diagram for 68 Series MPU

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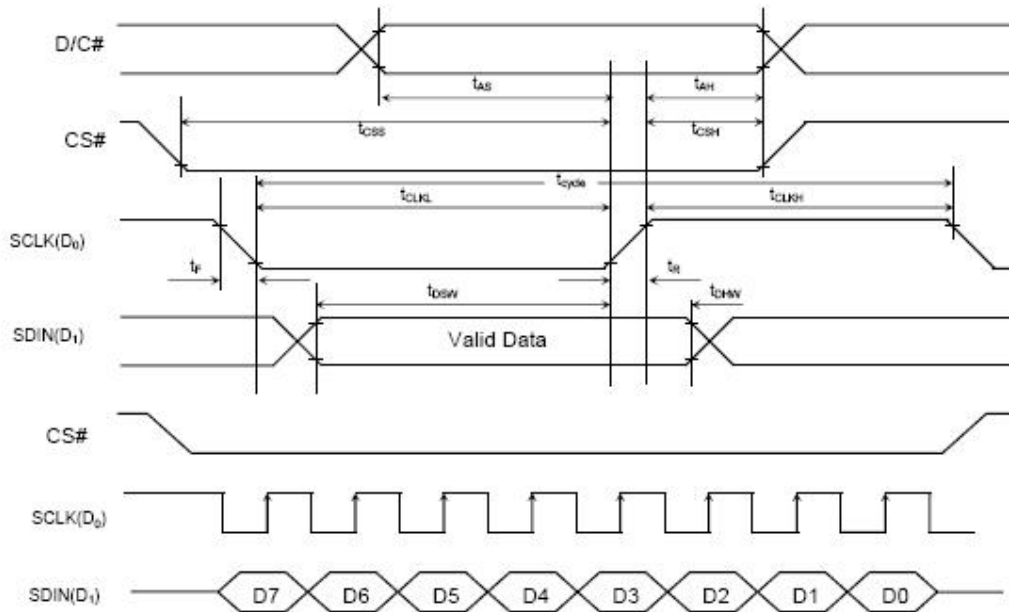
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5.1.11.2. Serial Interface Timing Characteristics:

Serial Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	t _{cycle}	250	-	-	ns
Address Setup Time	t _{AS}	150	-	-	ns
Address Hold Time	t _{AH}	150	-	-	ns
Chip Select Setup Time	t _{CSS}	120	-	-	ns
Chip Select Hold Time	t _{CSH}	60	-	-	ns
Write Data Setup Time	t _{DSW}	100	-	-	ns
Write Data Hold Time	t _{DHW}	100	-	-	ns
Clock Low Time	t _{CLKL}	100	-	-	ns
Clock High Time	t _{CLKH}	100	-	-	ns
Rise Time	t _R	-	-	15	ns
Fall Time	t _F	-	-	15	ns
Frame Frequency	t _{FRM}	70	75	85	Hz



Serial Interface Timing Diagram

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5.2. Display Programming

5.2.1. Programming:

Refer to specification: Solomon SSD0323 OLED/PLED Segment/Common Driver with Controller CMOS

5.2.2. Initialization:

After power up, the commands specified in below Table must be executed during initialization.

Initialization Sequence

Command	Code	Default on POR	Initialization for Module (A)	Initialization For module (B)	Initialization For module (C)
Set Column Address	15	00	Default	Default	Default
		3F	Default	Default	Default
Set Row Address	75	00	Default	Default	Default
		4F	3F	3F	3F
Set Contrast Control**	81	40	33*	4C*	40
Set Current Range	84~86	84	86	86	86
Set Re-map	A0	00	52	52	52
Set Display Start Line	A1	00	Default	Default	Default
Set Display Offset	A2	00	40	40	40
Set Multiplex Ratio	A8	4F	3F	3F	3F
Set Row Period	B2	25	46	46	46
Set Display ON/OFF		AE	AF	AF	AF
Set Display Mode		A4	Default	Default	Default
Set Master Configuration, DC-DC	AD	03	02	02	02
Set Bias Current Setting for DC-DC	CF	F0	Default	Default	Default
Set Pre-charge Compensation Enable	B0	08	Default	Default	Default
Set Pre-charge Compensation Level	B4	00	Default	Default	Default
Set Clock Divide	B3	02	41	41	41
Set Phase Length	B1	53	22	22	22
Set VSL	BF	0E	0D	0D	0D
Set VcomH	BE	11	00	08	03
Set Vprecharge	BC	18	0B	16	11
Set Gray Scale Table	B8	All 1	See Sample Gray Scale Settings	See Sample Gray Scale Settings	See Sample Gray Scale Settings

Note : All in Hex

Note : These settings represent maximum luminance for proper operation of the display. Lower settings can be used for dimming. Higher settings will adversely affect the operating lifetime as defined in this specification.

Product Specification for Pictiva TM 128X64 OLED Module, Elegance Yellow, SSD0323, (Atlanta HX1XX) OS128064PK16MXXXXX

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Module ^(A)	H0150-OS128064PK16MY0A00
	HZ150-OS128064PK16MY0Z00
	H0151-OS128064PK16MY0A01
	H0152-OS128064PK16MY0A10
	H0153-OS128064PK16MY0A11
Module ^(B)	H0150-OS128064PK16MY0A00 (High luminance)
	H1120-OS128064PK16MR1A00
	H1150-OS128064PK16MG1A00
	H1160-OS128064PK16MG2A00
	H1170-OS128064PK16MO1A00
Module ^(C)	H0160-OS128064PK16MY1A00
	H0162-OS128064PK16MY1A10

Sample Gray Scale Settings (Decimal)

GS level	Phase 1	Phase 2	S/W Set	GS Pulse	Total DCLK
L0	2	2	0	0	4
L1	2	2	1	1	5
L2	2	2	1	3	7
L3	2	2	1	5	9
L4	2	2	2	8	12
L5	2	2	2	11	15
L6	2	2	2	14	18
L7	2	2	3	18	22
L8	2	2	3	22	26
L9	2	2	4	27	31
L10	2	2	4	32	36
L11	2	2	5	38	42
L12	2	2	5	44	48
L13	2	2	6	51	55
L14	2	2	6	58	62
L15	2	2	7	66	70

For lower luminance settings of Elegance Yellow products, the command specified in below table must be executed during initialization:

Luminance, cd/m ²	Command	Code	Default on POR	Initialization
75	Set Contrast Control	81	40	22
30	Set Contrast Control	81	40	0D

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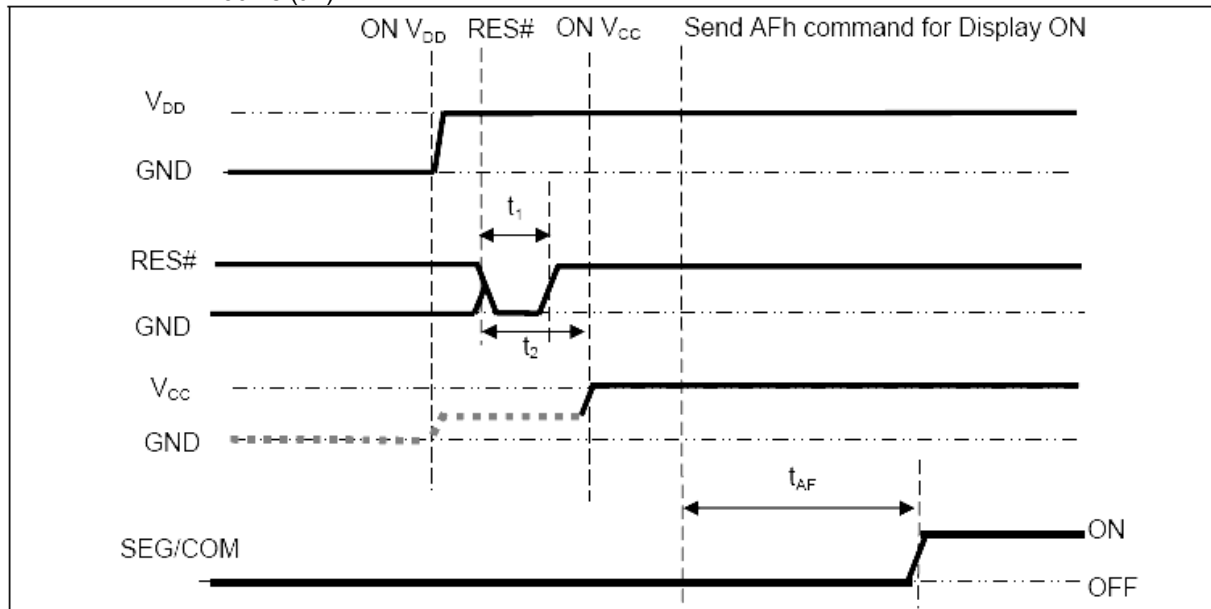
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5.3. Power Up and Power Down Sequence:

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

5.3.1 Power-Up Sequence:

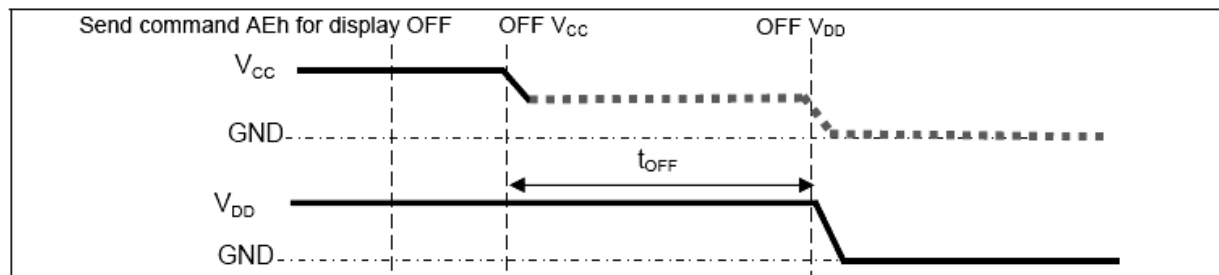
- I. Power-Up Vdd
- II. After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3 μ s (t_1) and then HIGH (logic HIGH)
- III. After set RES# pin LOW (logic LOW), wait for at least 3 μ s (t_2). Then Power ON V_{CC}
- IV. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 30ms (t_{AF}).



Power-Up Diagram

5.3.2 Power-Down Sequence:

- I. Send command AEh for Display off
- II. Wait until panel discharges completely
- III. Power down V_{CC}
- IV. Wait for t_{OFF} . Power OFF V_{DD}. (where Minimum t_{OFF} =0ms, Typical t_{OFF} =30ms)



Power-Down Diagram

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(Atlanta HX1XX) OS128064PK16MXXXXX

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5.4. **Optical and Lifetime Characteristics:**

(Ta = 25°C, unless otherwise stated)

5.4.1. **Optical Characteristics**

		Condition	Min.	Typ.	Max.	Unit
Contrast Ratio	CR	$\nu = \phi = 0^\circ$	2000	-	-	-
		Direct Sun Light	1.05	-	-	
Brightness Uniformity		$\nu = \phi = 0^\circ$	-	-	+20	%
Visible Flicker		$\nu = \phi = 0^\circ$	-	None	-	-
Cross Talk (Brightness variation of non-selected pixels)		$\nu = \phi = 0^\circ$	-	-	10	%

5.4.2. **Lifetime Characteristics:**

Lifetime is measured by luminance as a function of time; based on the display operated at 25°C at typical brightness level with specified software settings, until reaching 50% of initial luminance.

Lifetime Characteristics

Product	Color	X color coordinate 1931 CIE, ± 0.02	X color coordinate 1931 CIE, ± 0.02	Typical Initial Luminance, cd/m ²			Operating Lifetime * Hours, @25°C
				Min.	Typ.	Max.	
H0150-OS128064PK16MY0A00	Elegance Yellow	0.46	0.54	90	100	140	40K
HZ150-OS128064PK16MY0Z00	Elegance Yellow	0.46	0.54	90	100	140	40K
H0151-OS128064PK16MY0A01	Elegance Yellow	0.46	0.54	90	100	140	40K
H0152-OS128064PK16MY0A10	Elegance Yellow	0.46	0.54	90	100	140	40K
H0153-OS128064PK16MY0A11	Elegance Yellow	0.46	0.54	90	100	140	40K
H0150-OS128064PK16MY0A00	Elegance Yellow (High Luminance settings)	0.46	0.54	140	150	160	10K
H1120-OS128064PK16MR1A00	Scarlet Red	0.690	0.310	7	10	15	10K
H1150-OS128064PK16MG1A00	Lime Green	0.370	0.620	90	95	105	10K
H1160-OS128064PK16MG2A00	Jungle Green	0.250	0.730	15	20	25	10K
H1170-OS128064PK16MO1A00	Tiger Orange	0.630	0.370	30	35	40	10K
H0160-OS128064PK16MY1A00	Light Green	0.440	0.560	100	110	125	40K
H0162-OS128064PK16MY1A10	Light Green	0.440	0.560	100	110	125	40K

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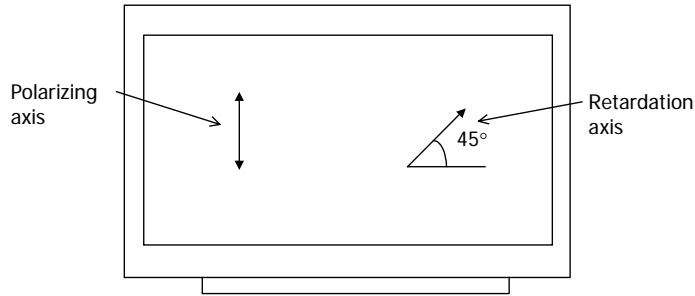
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5.4.3. Polarizing Angle:



Orientation of OLED polarizer angle

5.4.4. Mechanical Characteristics:

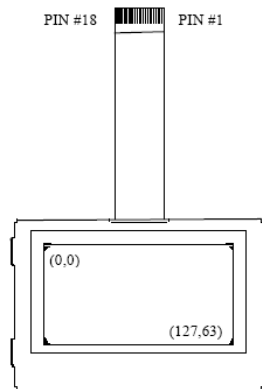
5.4.4.1. Interconnections:

The display module should be electrically connected to a controller on the user's board through the 18-contact pad ZIF tail.

5.4.4.2. Recommended mating connectors:

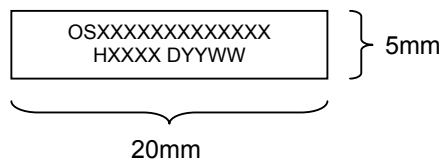
5.4.4.2.1. Top Contact: HIROSE: FH12A-18S-0.5SH, or equivalent

5.4.4.2.2. Bottom Contact: Molex: 52893-1890, HIROSE: FH12-18S-0.5SH, or equivalent



Orientation of ZIF connector tail pin out

5.4.4.3. Product Marking: Parts are marked as shown below in figure.



Legend
 OSRAM P/N & Code
Date Code
 D : Day; YY : Year
 WW : PC Week

Description of part label marking requirements

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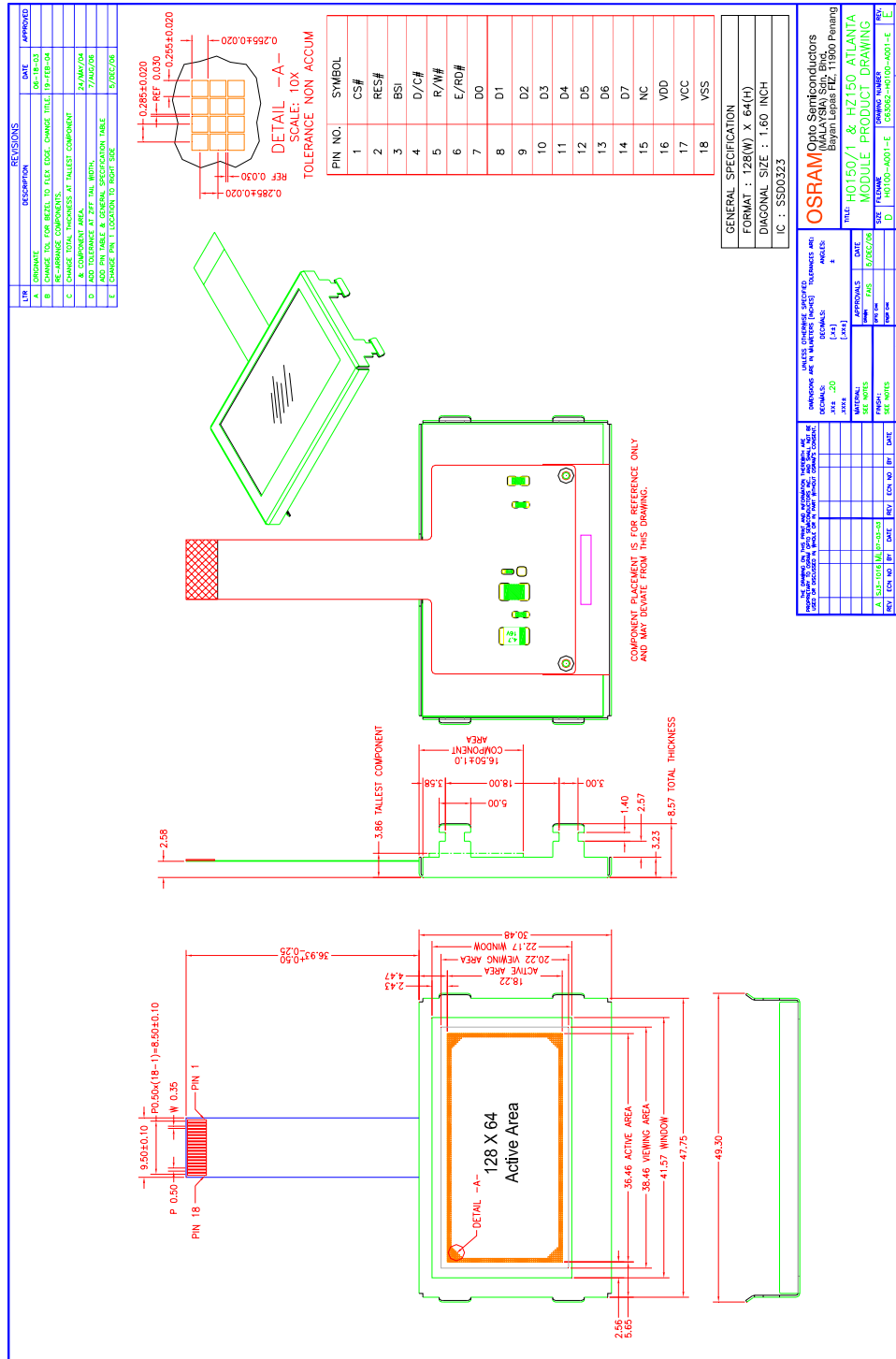
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5.5. Module Mechanical Drawings:

The mechanical drawings shown in below figures are provided for reference.

Module drawing for parts with bezel (external VCC)



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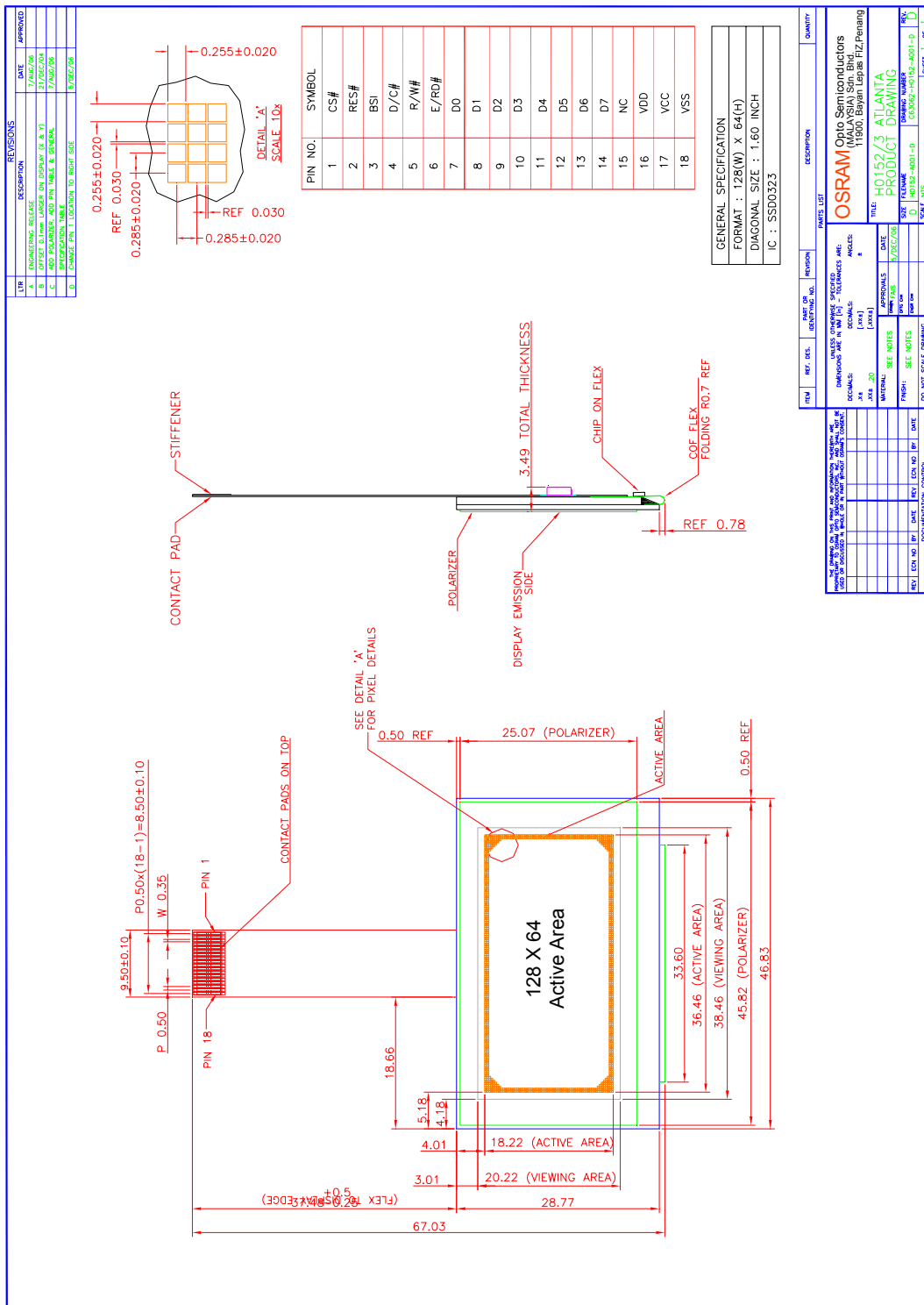
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Module drawing for parts without bezel (external VCC)



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6. QUALIFICATION TESTING:

For reference, the main qualification tests and test criteria done on the OLED module are indicated below in Tables, respectively.

OLED Module Internal Qualification Tests

Test	Condition	Duration	
		Guaranteed	Capability
Temperature and Humidity Bias (THB)*	60°C / 90% RH	250 hrs	504 hrs
Elevated Lifetest (ELT)*	70°C	336 hrs	1000 hrs
	85°C	-	250 hrs
Powered Temperature Cycle (PTC)*	-30°C / 70°C; 30 min. dwell time; 15 min. Transition time	60 cycles	60 cycles
Thermal Shock (TSK)	-40°C / 85°C; 45 min. dwell time; 15 sec. Transition time	100 cycles	100 cycles
Low Temperature Storage (LTS)	-40°C	336 hrs	>1000 hrs
High Temperature Storage (HTS)	70°C	336 hrs	>1000 hrs
	85°C	-	> 500 hrs
Low Temperature Operating (LTO)	-40°C	336 hrs	>> 2000 hrs
Low Air Pressure (LAP) **	15kPa 25°C (0.15bar)	16hrs	16hrs
Mechanical Vibration**	10-58hz 0.75mm 58-150Hz 10g 1oct/min	10 sweeps per X, Y, Z direction	10 sweeps per X, Y, Z direction
Mechanical Shock**	11ms half sine 100g peak	6 shocks per X, Y, Z direction	6 shocks per X, Y, Z direction
Mechanical Bump**	6ms half sine 40g Peak	1000 bumps per X, Y, Z direction	1000 bumps per X, Y, Z direction

***Note 1:** The modules are powered for these tests, with a standard OSRAM pattern (50% emission ratio)

**** Note 2:** These mechanical tests are performed on a representative part of the same product family.

OLED Module Qualification Test Criteria

Acceptance Criteria (without polarizer):	Test Patterns for Powered Tests:
< 50% luminance loss after test	Checkerboard pattern
5 point luminance uniformity <20%	Inverse Checkerboard pattern
No mechanical failure	All pixels On
No electrical failure	All pixels Off
Pixel gap (initial + growth) ≤ 30%	

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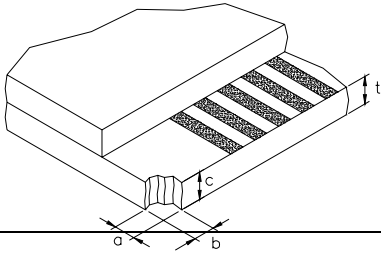
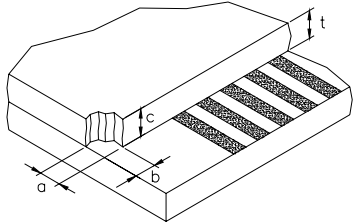
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7. COSMETIC CRITERIA:

Items	Criterion for Defects	Defect Type								
Black / bright spot, particle, pin-hole (on the glass / polarizer), dent on polarizer	<p>Within Viewing Area</p> <table border="1"> <thead> <tr> <th>Size Φ (mm)</th> <th>Acceptable number</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1$</td> <td>Not counted</td> </tr> <tr> <td>$0.1 \leq \Phi \leq 0.2$</td> <td>3</td> </tr> <tr> <td>$\Phi > 0.2$</td> <td>0</td> </tr> </tbody> </table> <p>* $\Phi = (\text{Long diameter} + \text{Short diameter})/2$</p>	Size Φ (mm)	Acceptable number	$\Phi \leq 0.1$	Not counted	$0.1 \leq \Phi \leq 0.2$	3	$\Phi > 0.2$	0	Minor
Size Φ (mm)	Acceptable number									
$\Phi \leq 0.1$	Not counted									
$0.1 \leq \Phi \leq 0.2$	3									
$\Phi > 0.2$	0									
Scratches / lines on the polarizer	<p>Within Viewing Area</p> <table border="1"> <thead> <tr> <th>Size Φ (mm)</th> <th>Acceptable number</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.1$</td> <td>Not counted</td> </tr> <tr> <td>$L \leq 2, 0.1 < W \leq 0.2$</td> <td>3</td> </tr> <tr> <td>$W > 0.2$</td> <td>0</td> </tr> </tbody> </table>	Size Φ (mm)	Acceptable number	$W \leq 0.1$	Not counted	$L \leq 2, 0.1 < W \leq 0.2$	3	$W > 0.2$	0	Minor
Size Φ (mm)	Acceptable number									
$W \leq 0.1$	Not counted									
$L \leq 2, 0.1 < W \leq 0.2$	3									
$W > 0.2$	0									
Polarizer Bubble	<p>Reject if bubble is observed with naked eyes at 30cm distance. with the following criteria</p> <p>Within Viewing Area</p> <table border="1"> <thead> <tr> <th>Size Φ (mm)</th> <th>Acceptable number</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.2$</td> <td>Not counted</td> </tr> <tr> <td>$0.2 \leq \Phi \leq 0.3$</td> <td>3</td> </tr> <tr> <td>$0.3 < \Phi$</td> <td>0</td> </tr> </tbody> </table> <p>Outside Viewing Area – IGNORE</p>	Size Φ (mm)	Acceptable number	$\Phi \leq 0.2$	Not counted	$0.2 \leq \Phi \leq 0.3$	3	$0.3 < \Phi$	0	Minor
Size Φ (mm)	Acceptable number									
$\Phi \leq 0.2$	Not counted									
$0.2 \leq \Phi \leq 0.3$	3									
$0.3 < \Phi$	0									
Polarizer coverage	Reject if the polarizer does not cover the Viewing Area.	Minor								
Corner Chip	<p>Criteria for Corner Chip $t = \text{Glass thickness}$ Accept If $a \leq 1.5 \text{ mm}$ or $b \leq 1.5 \text{ mm}$ $c \leq t$</p> 	Minor								
Corner Chip	<p>Accept If $a \leq 3.0 \text{ mm}$ or $b \leq 3.0 \text{ mm}$</p> 	Minor								

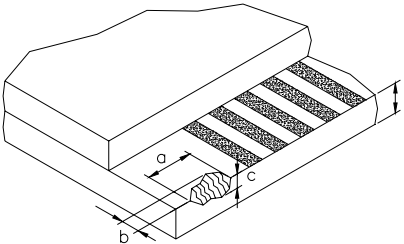
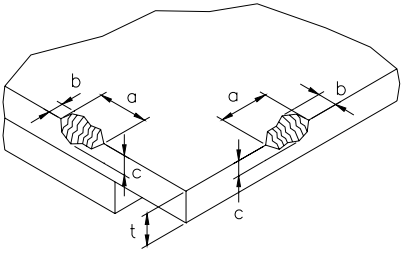
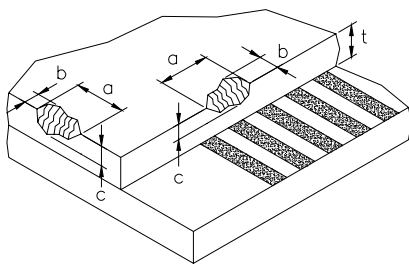
Product Specification for Pictiva TM 128X64 OLED Module, Elegance Yellow, SSD0323, (Atlanta HX1XX) OS128064PK16MXXXXX

OSRAM Opto Semiconductors	03	2007-01-29	A63857-H015X-D000-*-7680
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Items	Criterion for Defects	Defect Type
Chip on contact pad	<p>Criteria for Chips on contact pad</p> <p>t = Glass thickness</p> <p>Accept if</p> <p>$b \leq 1/3$ width of contact ledge</p> 	Minor
Chip on Face of Display	<p>Criteria for Chips on Face of Display</p> <p>Accept if</p> <p>$b \leq 1.5\text{mm}$</p> 	Minor
Chip on Back of Display	<p>Criteria for Chips on Back of Display</p> <p>Accept if</p> <p>$b \leq 3.0\text{ mm}$</p> 	Minor

Definition of W & L & ϕ (Unit: mm)



Note: Distance between any two defects should be over 5 mm

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8. General OLED Module Handling & Care

8.1. Mechanical Handling

- 8.1.1. Avoid mechanical stress, such as shock and pressure. For parts designed without bezel, exercise caution to avoid glass chipping. When handled with bare fingers, pay special attention to sharp glass edges to avoid potential injury.
- 8.1.2. Avoid touching Flex contact pad with bare fingers and avoid mechanical stress and pressure on the flex.
- 8.1.3. Handle the polarizer with care. Avoid hard or sharp objects in contact with the display surface.
- 8.1.4. Store and operate the OLED display within the specified ratings. It is recommended to store them as they have been contained in the inner container at the time of delivery from us.
- 8.1.5. Avoid corner contact to display during assembly or installation to end products.
- 8.1.6. Installation Bending: The flex is generally designed to facilitate mounting to a PCB or connector. It is not a dynamic flex. Therefore, bending should be limited to less than 3 times.
- 8.1.7. Bending Radius: The minimum bending radius is as shown in the product drawing or equal to the thickness of the rear cap glass, whichever is smaller.
- 8.1.8. Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause damage of polarizer or color fading, while an active OLED display with water condensation on its surface will cause corrosion of metal traces.
- 8.1.9. Cleaning:
- 8.1.9.1. Particle/ Foreign materials: Use non-abrasive cloth (Recommended Smartat Cleanroom Wipes WIP-1009 D Series) to gently wipe over the surface of the display in one direction.
- 8.1.9.2. Glue/ Adhesive Residue:
- 8.1.9.2.1. Method 1: Use non-abrasive cloth (Recommended Smartat Cleanroom Wipes WIP-1009 D Series) and applicator (dipped in IPA or ethanol if necessary) to gently wipe over the surface of the display in one direction.
- 8.1.9.2.2. Method 2: Use the finger cot to gently clean the stain on by rubbing it on the polarizer in one direction.

8.2. ESD

- 8.2.1. Electrostatic discharge (ESD): OLED modules are semiconductor devices. Take ESD handling precautions by wearing a ground strap and avoid contacting electrical connections.

Condition	MM	HBM
Vdd mode	200v	2000v
Vss mode	200v	2000v
IO mode	200v	2000v

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