Registered PC-133 SYNCHRONOUS DRAM DIMM

7232ZHSTM4G24TWR-PH0 168 Pin 32Mx72 SDRAM DIMM
Registered, 4k Refresh, 3.3V with SPD

General Description

The module is a 32Mx72 bit, 24 chip, 168 Pin DIMM module consisting of (18) 4Mx8x4 (TSOP) SDRAM, (3) Universal Bus Driver Registers, (1) PLL Clock Driver (1) 5-pin Inverter IC and (1) 256x8 EEPROM for serial presence detect. The module conforms to PC-133 specifications, has byte data masks and supports ECC mode.

Features

- Fully PC-133 Compliant
- JEDEC-Standard 168-pin Dual Inline Memory Module (DIMM)
- Address and Control lines are Registered
- Based on 16Mx8 SDRAM Components
- Power Supply: 3.3V ± 0.3V
- 64ms, 4096-cycle refresh
- Serial Presence Detect (SPD)
- LVTTL Compatible Inputs and Outputs
- Two External Banks
- Four Internal Banks
- Pure Power and Ground Planes
- Gold PCB connector

Pin Assignment

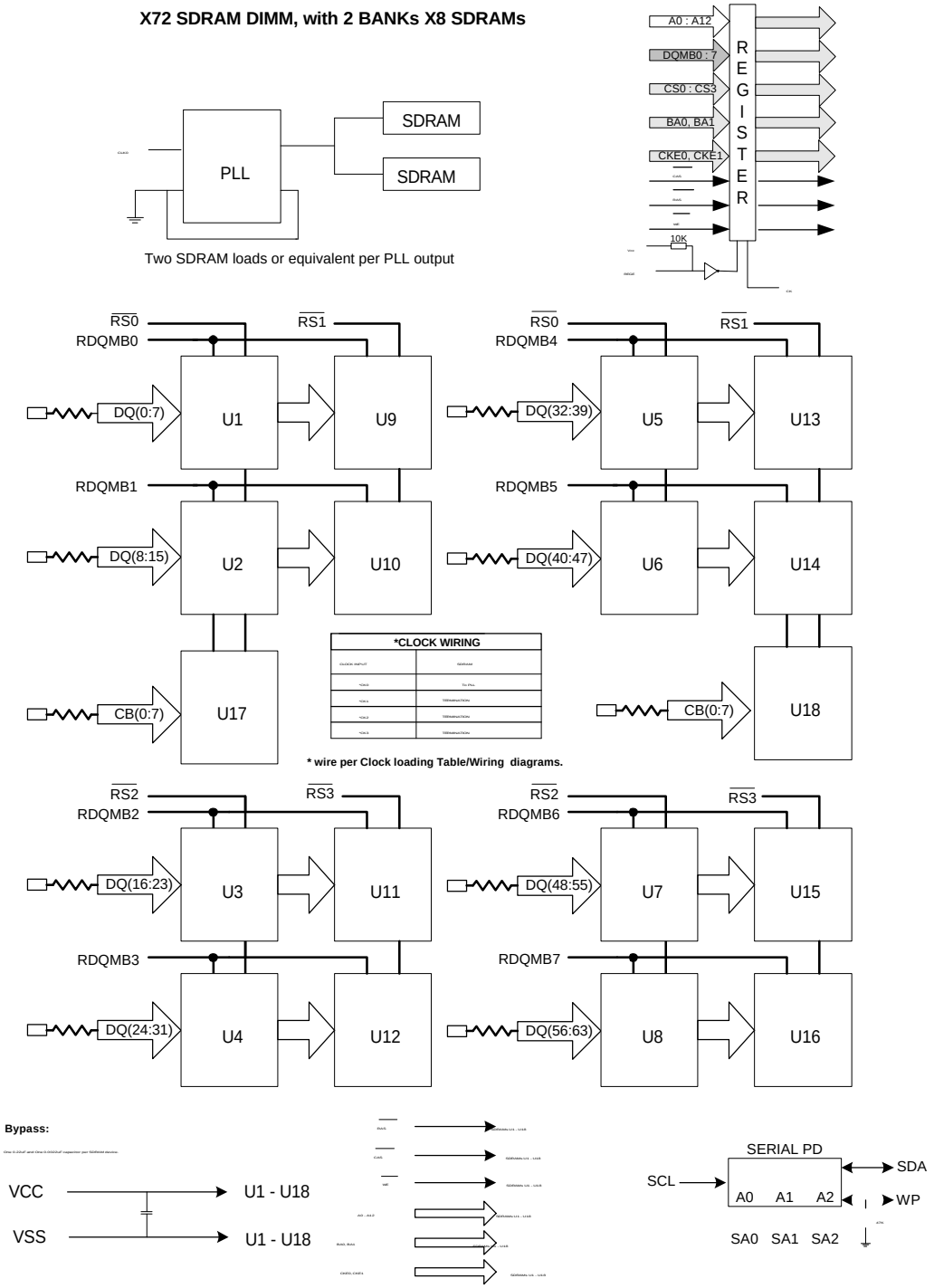
Pin#		Pin#		Pin#		Pin#	
1	Vss	85	Vss	43	Vss	127	Vss
2	DQ0	86	DQ32	44	NC	128	CKE0
3	DQ1	87	DQ33	45	S2*	129	S3*
4	DQ2	88	DQ34	46	DQMB2	130	DQMB6
5	DQ3	89	DQ35	47	DQMB3	131	DQMB7
6	Vcc	90	Vcc	48	NC	132	NC
7	DQ4	91	DQ36	49	Vcc	133	Vcc
8	DQ5	92	DQ37	50	NC	134	NC
9	DQ6	93	DQ38	51	NC	135	NC
10	DQ7	94	DQ39	52	CB2	136	CB6
11	DQ8	95	DQ40	53	CB3	137	CB7
12	Vss	96	Vss	54	Vss	138	Vss
13	DQ9	97	DQ41	55	DQ16	139	DQ48
14	DQ10	98	DQ42	56	DQ17	140	DQ49
15	DQ11	99	DQ43	57	DQ18	141	DQ50
16	DQ12	100	DQ44	58	DQ19	142	DQ51
17	DQ13	101	DQ45	59	Vcc	143	Vcc
18	Vcc	102	Vcc	60	DQ20	144	DQ52
19	DQ14	103	DQ46	61	NC	145	NC
20	DQ15	104	DQ47	62	NC	146	NC
21	CB0	105	CB4	63	CKE1	147	REGE
22	CB1	106	CB5	64	Vss	148	Vss
23	Vss	107	Vss	65	DQ21	149	DQ53
24	NC	108	NC	66	DQ22	150	DQ54
25	NC	109	NC	67	DQ23	151	DQ55
26	Vcc	110	Vcc	68	Vss	152	Vss
27	WE*	111	CAS*	69	DQ24	153	DQ56
28	DQMB0	112	DQMB4	70	DQ25	154	DQ57
29	DQMB1	113	DQMB5	71	DQ26	155	DQ58
30	S0*	114	S1*	72	DQ27	156	DQ59
31	NC	115	RAS*	73	Vcc	157	Vcc
32	Vss	116	Vss	74	DQ28	158	DQ60
33	A0	117	A1	75	DQ29	159	DQ61
34	A2	118	A3	76	DQ30	160	DQ62
35	A4	119	A5	77	DQ31	161	DQ63
36	A6	120	A7	78	Vss	162	Vss
37	A8	121	A9	79	CK2	163	CK3
38	A10/AP	122	BA0	80	NC	164	NC
39	BA1	123	A11	81	WP	165	SA0
40	Vcc	124	Vcc	82	SDA	166	SA1
41	Vcc	125	CK1	83	SCL	167	SA2
42	CK0	126	NC	84	Vcc	168	Vcc

* Active Low

Valid Part Numbers

Part Number	IC Manufacture / Part Number
7232ZHSTM4G24TWR-PH0	INFINEON / HYB39S128800CT-7.5 Rev. C

Block Diagram



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Pin Descriptions

Pin	Name	Function
CLK#	System Clock	All input signals are sampled on the rising edge of clock.
S#	Chip Select	Enables and disables the command decoder. All commands are disabled when S# is high.
CKE	Clock Enable	Masks system clock to freeze current operation on the next clock cycle, also provides access to standby mode (see truth table).
A#	Address Lines	Input lines for Row/Column address.
BA#	Bank Select Lines	Selects the internal bank to be accessed during a row or column address latch.
RAS	Row Address Strobe	Latches the row address on the rising edge of clock when asserted.
CAS	Column Address Strobe	Latches the column address on the rising edge of clock when asserted.
WE	Write Enable	Enables write operation and row precharge.
REGE	Register Enable	Inputs are registered when REGE is high, transparent when REGE is low.
DQM0-DQM7	Data Masks	Provides a byte mask for write operations and a byte enable for read operations.
DQ0-DQ63	Data Lines	Data input/output lines.
CB0-CB7	Check Bit	Check Bit input/output lines, used for ECC.
Vdd	Power Supply	Power Supply 3.3V±0.3V
Vss	Ground	Ground
WP	SPD Write Protect	Serial Presence Detect (SPD) EEPROM write protect. SPD programming is inhibited when asserted.
SDA, SCL	SPD Data/Clock Lines	Serial Presence Detect (SPD) EEPROM bus lines. These lines provide bi-directional data transfer over an I^2C bus.
SA0 – SA2	SPD Address Lines	Serial Presence Detect (SPD) EEPROM address lines. These lines are used to configure the SPD.
NC	No Connection	Line is not connected in DIMM.

Serial Presence Detect Matrix

Byte #	Function	Binary	Hex	Description
		76543210	MS-LS	
0	Define # of bytes written into EEPROM	**10000000**	**80**	128
1	Total # of bytes of SPD memory device	**00001000**	**08**	256
2	Fundamental memory type (EDO,SDRAM...)	**00000100**	**04**	SDRAM
3	# of row addresses	**00001100**	**0C**	12
4	# of column addresses	**00001010**	**0A**	10
5	# of module rows	**00000010**	**02**	2
6	Data width...	**01001000**	**48**	72
7	...Data width continued	**00000000**	**00**	00
8	Voltage interface	**00000001**	**01**	LVTTL
9	SDRAM cycle time	**01110101**	**75**	7.5ns
10	SDRAM access from clock	**01010100**	**54**	5.4ns
11	DIMM configuration type (non-parity,ECC…)	**00000010**	**02**	ECC
12	Refresh rate/type	**10000000**	**80**	Normal/Self
13	Primary SDRAM width	**00001000**	**08**	8
14	Error checking SDRAM width	**00001000**	**08**	8
15	Minimum clock delay back to back random column address	**00000001**	**01**	1
16	Burst lengths supported	**10001111**	**8F**	page/8/4/2/1
17	# of banks on each SDRAM device	**00000100**	**04**	4
18	CAS# latencies supported	**00000110**	**06**	3
19	CS# latency	**00000001**	**01**	CS latency=0
20	Write latency	**00000001**	**01**	WE latency=0
21	SDRAM module attributes	**00011111**	**1F**	Registered
22	SDRAM device attributes: general	**00001110**	**0E**	Write1/Read burst/Precharge
23	Min SDRAM cycle time at CL X-1	**10100000**	**A0**	10ns
24	SDRAM access from clock at CL X-1	**01100000**	**60**	6ns
25	Min SDRAM cycle time at CL X-2	**00000000**	**00**	00
26	Max SDRAM access from clock at CL X-2	**00000000**	**00**	00
27	Min row precharge time	**00010100**	**14**	20ns
28	Min row active to row active	**00001111**	**0F**	15ns
29	Min RAS to CAS delay	**00010100**	**14**	20ns
30	Minimum RAS pulse width	**00101101**	**2D**	45ns
31	Density of each row on module	**00100000**	**20**	128MB
32	Command and Address signal input setup time	**00010101**	**15**	1.5ns
33	Command and Address signal input hold time	**00001000**	**08**	0.8ns
34	Data signal input setup time	**00010101**	**15**	1.5ns
35	Data signal input hold time	**00001000**	**08**	0.8ns
36-61	Superset information (may be used in future)	**00000000**	**00**	Not written
62	SPD data revision code	**00000010**	**02**	2.0
63	Checksum for bytes 0-62	**xxxxxxxx**	**XX**	XX
64-125	Manufacturer's information	**00000000**	**00**	Not written
126	Intel specification frequency	**01100100**	**64**	100Mhz
127	Intel specification CAS# latency support	**10000111**	**87**	CAS latency 3
128-255	Unused storage locations	**00000000**	**00**	Not written

NOTE: 1. x = Variable Data.

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Simplified Truth Table

Command			CKEn-1	CKEn	S*	RAS*	CAS*	WE*	DQM	BA0,1	A10/AP	A11 A9-A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP Code			1
Refresh	Auto refresh		H	H	L	L	L	H	X	X			
	Self Refresh	Entry		L									
		Exit	L	H	H	X	X	X	X	X			
					L	H	H	H					
Bank active & row address			H	X	L	L	H	H	X	V	Row Address		
Read & column address	Auto pre-charge disable		H	X	L	H	L	H	X	V	L	Column addr (A0-A9)	2
	Auto pre-charge enable										H		
Write & column address	Auto pre-charge disable		H	X	L	H	L	L	X	V	L	Column addr (A0-A9)	2
	Auto pre-charge enable										H		
Burst stop			H	X	L	H	H	L	X	X			
Pre-charge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend Mode or active power down		Entry	H	L	X	X	X	X	X	X			
		Exit	L	H	X	X	X	X	X				
Pre-charge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			
No operation command			H	X	L	H	H	H	X	X			

(V=Valid, X=Don't care, H=Logic High, L=Logic Low)

Notes:

1. MRS can be issued only in idle state.
2. A burst read or write with auto pre-charge cannot be interrupted. New commands can be issued t_{RP} after the end of the burst.

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V_{in}	-1.0 to 4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	Pt	10.50	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{st}	-55 to +125	°C

NOTE: Permanent damage may occur if absolute maximum ratings are exceeded.
Device should be operated within recommended operating conditions only.

DC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units	Note
Supply voltage	Vss	0	0	0	V	
Supply voltage	Vcc	3.0	3.3	3.6	V	
Input high voltage	Vih	2.0	-	Vcc+0.3	V	1
Input low voltage	Vil	-	-	0.8	V	2
Output high voltage	Voh	2.4	-	-	V	Ioh=-2mA
Output low voltage	Vol	-	-	0.4	V	Iol=2mA

DC Current Consumption (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	PC133 CL3	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC(min)}$, I_O= 0 mA	2160	mA	4
Precharge standby current in power down mode	I_{CC2P}	CKE0 ≤ V_{IL} (max), t_{CK} = min	32.4	mA	5
	I_{CC2PS}	CKE0,CKE1 ≤ V_{IL} (max), t_{CK} = ∞	43.2		
Precharge standby current in non-power down mode	I_{CC2N}	CKE0,CKE1 ≥ V_{IH} (min), t_{CK} = min, S0*-S3*= V_{IH} (min) Input signals are changed once during 2 clock cycles	864		5
	I_{CC2NS}	CKE0,CKE1 ≥ V_{IH} (min), CK0 ≤ V_{IL} (max), t_{CK} = ∞ Input signals are stable	1080	mA	
Active standby current in non-power down mode	I_{CC3N}	CKE0 ≥ V_{IH} (min), t_{CK} = min, S0*-S3*= V_{IH} (min) Input signals are changed once during 2 clock cycles	1080	mA	5
	I_{CC3NS}	CKE0 ≥ V_{IH} (min), CK0 ≤ V_{IL} (max), t_{CK} = ∞ Input signals are stable	1080		
Burst Operating Current	I_{CC4}	I_O = 0 mA, Page Burst, multiple banks active, t_{CCD} = 2CLK	1512	mA	4
Refresh Current	I_{CC5}	t_{CK} = min , $t_{RC} \geq t_{RC(min)}$	2916	mA	
Self Refresh Current	I_{CC6}	CKE0 ≤ 0.2 V	27	mA	5

CL : CAS Latency

Capacitance (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	Typ	Max	Units	Note
Input capacitance (Am, BA0,CKEm)	C_{I1}	-	68.4	pF	
Input capacitance (DQMBm)	C_{I2}	-	7.6	pF	
Input capacitance (CAS*, RAS*, WE*)	C_{I3}	-	68.4	pF	
Input capacitance (CKm)	C_{I4}	-	25	pF	
Input capacitance (SDA,SCL,SAm)		-	10	pF	
Input/Output capacitance (DQm,CBm)	$C_{I/O}$	-	12	pF	

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AC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	PC133 CL3		Units	Note
CLK Cycle time (CL =3)	t_{CK}	7.5	1000	ns	6,7
CLK Cycle time (CL =2)	t_{CK}	10	1000	ns	6,7
CLK to valid output delay (CL =3)	t_{AC}	-	5.4	ns	6,7
CLK to valid output delay (CL =2)	t_{AC}	-	6	ns	6.7
Output data hold time	t_{OH}	2.7	-	ns	7
Output valid to High-Z	t_{HZ}	-	6.0	ns	7
CLK high pulse width	t_{CH}	2.5	-	ns	7
CLK low pulse width	t_{CL}	2.5	-	ns	7
Command setup time	t_{CMS}	1.5	-	ns	7
Address setup time	t_{AS}	1.5	-	ns	7
Clock enable setup time	t_{CKS}	1.5	-	ns	7
Data input setup time	t_{DS}	1.5	-	ns	7
Command hold time	t_{CMH}	0.8	-	ns	7
Address hold time	t_{AH}	0.8	-	ns	7
Clock enable hold time	t_{CKH}	0.8	-	ns	7
Data input hold time	t_{DH}	0.8	-	ns	7
Power down exit setup time	t_{PDE}	1	-	CLK	7,8
Row active to Row active delay	$t_{RRD\ (min)}$	15	-	ns	6
RAS* to CAS* delay	$t_{RCD\ (min)}$	20	-	ns	6
Row precharge time	$t_{RP\ (min)}$	20	-	ns	6
Row active time	t_{RAS}	45	8000	ns	6
Row cycle time	$t_{RC\ (min)}$	70	-	ns	6
Mode Register set to Active Delay	$t_{RSC\ (min)}$	15	-	ns	

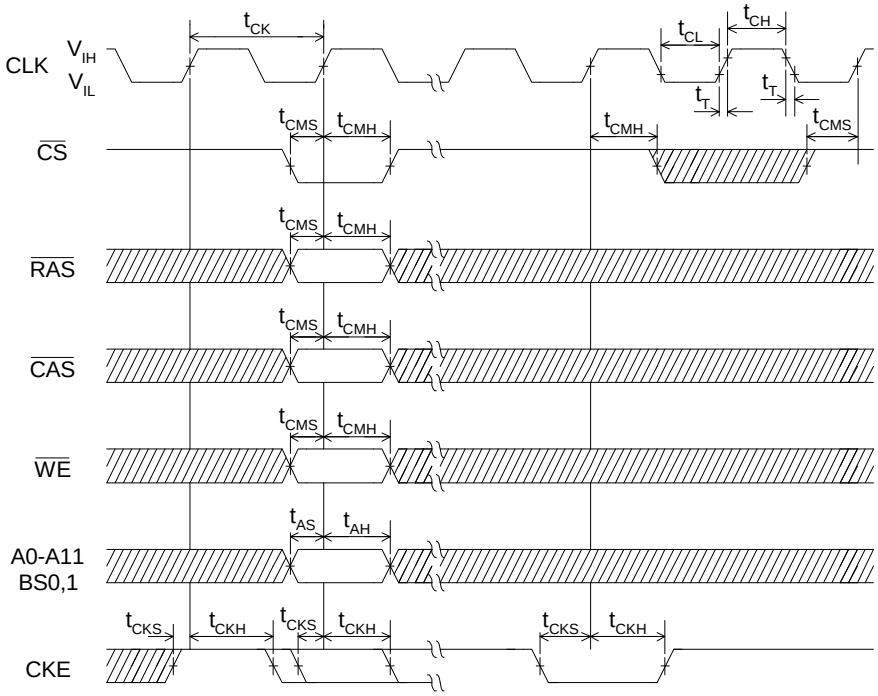
CL : CAS Latency

Notes :

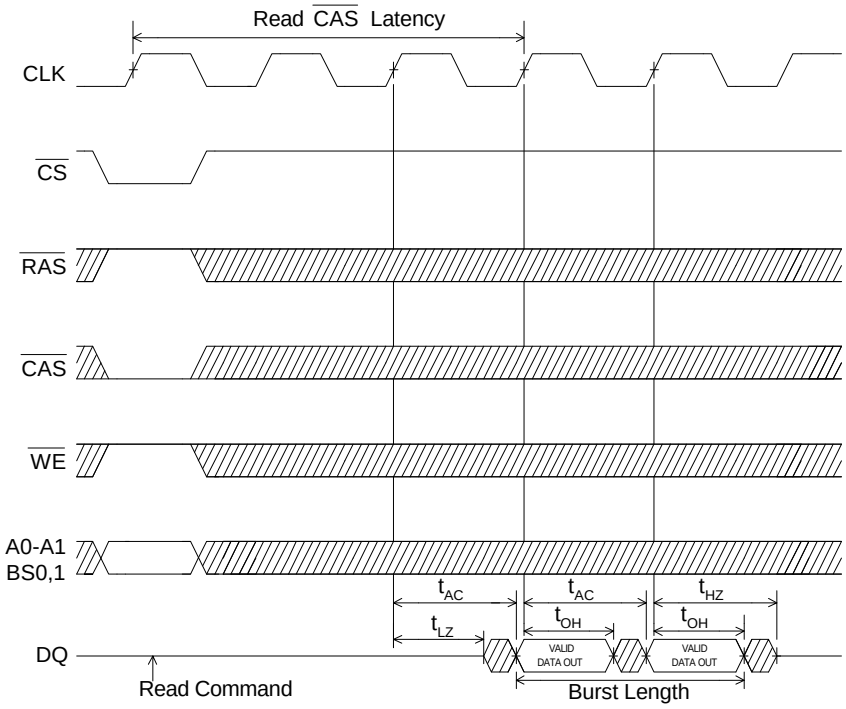
1. Overshoot: Vih $_{(MAX)}$ = Vdd + 2.0V for ≤3ns
2. Undershoot: Vil $_{(MIN)}$ = Vss – 2.0V for ≤3ns
3. Typical peak current consumption.
4. Measured with outputs open.
5. Assumes minimum column address update cycle: t_{CCD}(min).
6. Parameters depend on programmed CAS Latency.
7. Assumed input rise and fall time=1ns.
8. A time of t_{PDE} has to elapse after asserting CKE to resume normal operation when exiting power down mode.

Timings listed are for discrete SDRAM components.
In registered mode, all address & control signals are delayed by one clock cycle.
In buffered mode, all address & control signals must first propagate through the buffer
.

Command Input Timing



Read Timing



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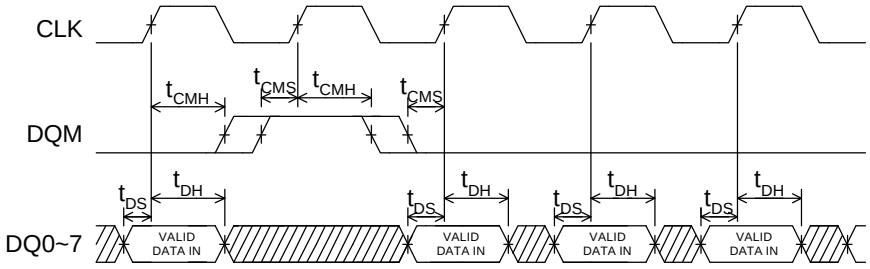
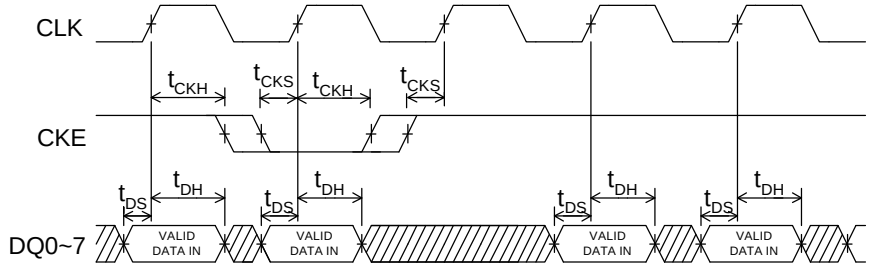
Control Timing of Input Data

(Word Mask)

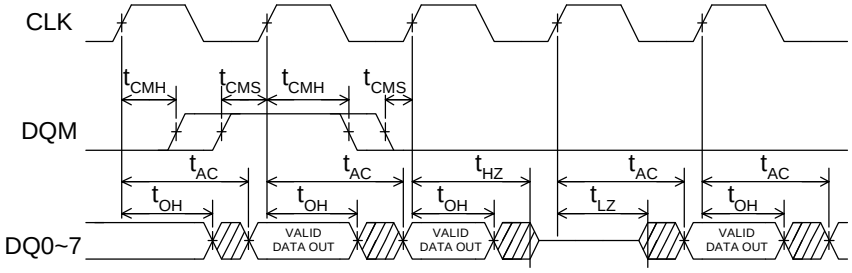


(Clock Mask)

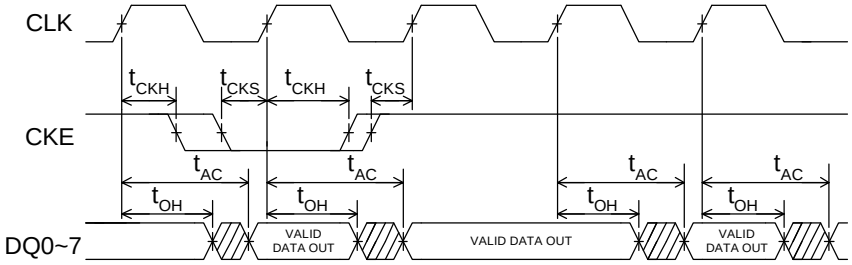


Control Timing of Output Data

(Output Enable)



(Clock Mask)



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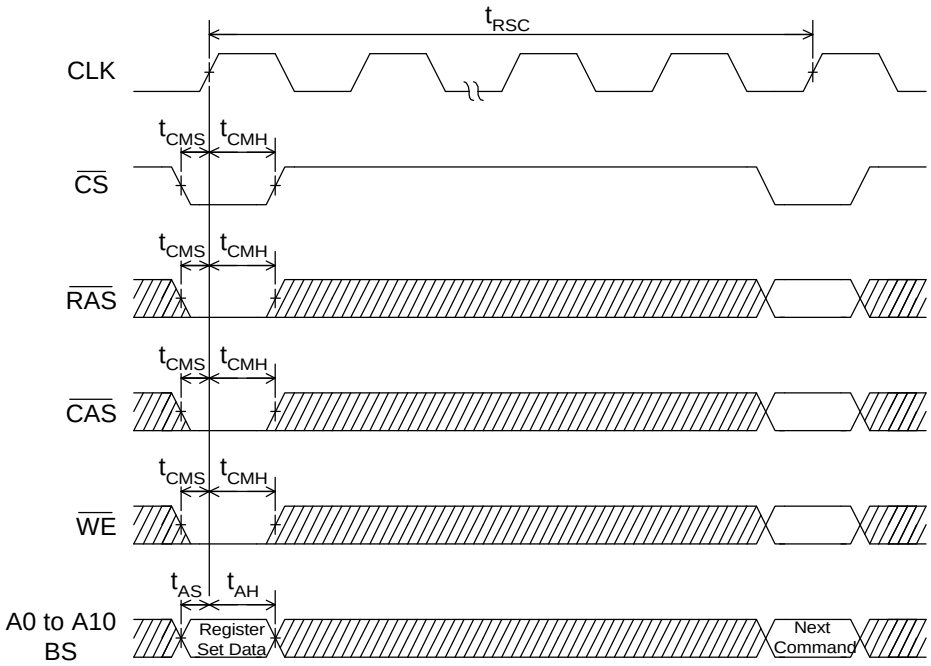
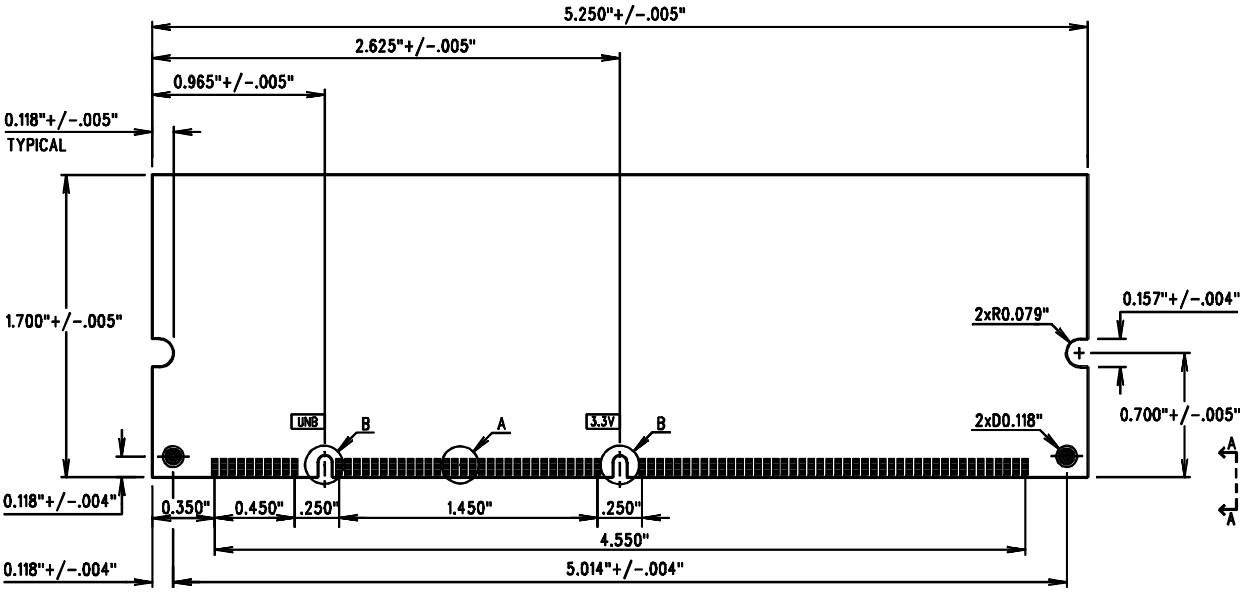
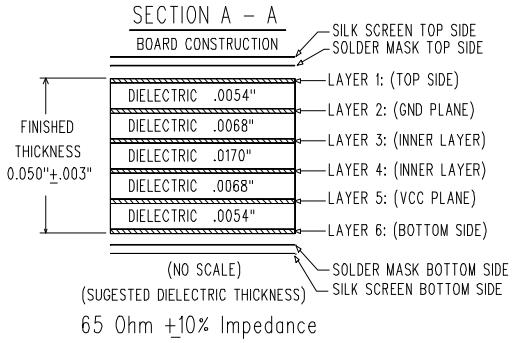
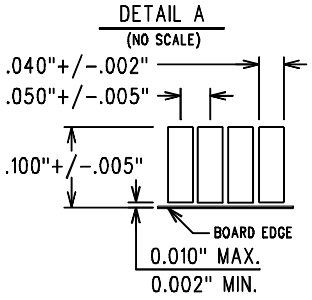
Mode Register Set Cycle

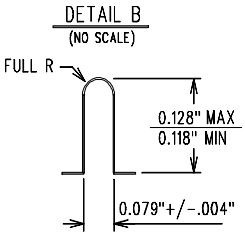


Outline Drawing

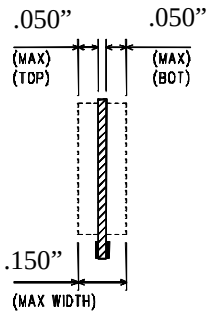


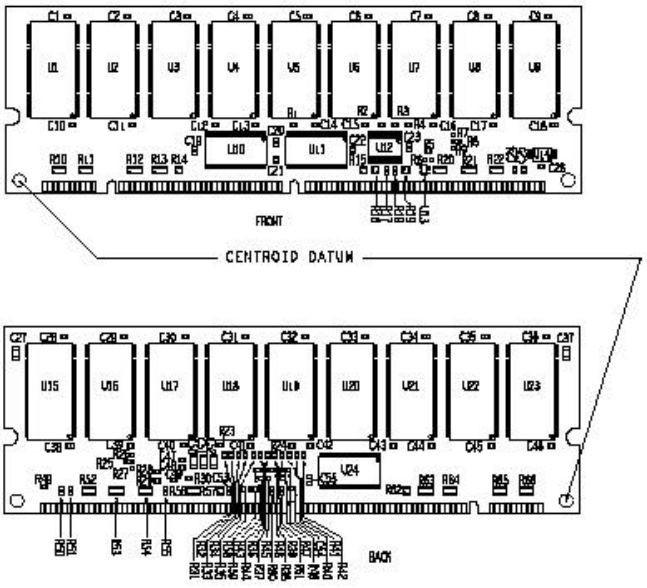






SIDE VIEW





Front Side

Back Side

Note: Drawing is for component location only, assembly may not have all components installed.

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