DDR2 SDRAM VLP SORDIMM

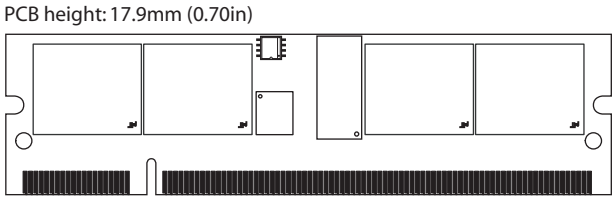
MT9HVF6472RH – 512MB
MT9HVF12872RH – 1GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, very low-profile (ATCA compatible), small-outline registered dual in-line memory module (VLP SORDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 512MB (64 Meg x 72), 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- Vdd = Vddq = +1.8V
- Vddspd = +3.0V to +3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- PLL to reduce system clock line loading
- Gold edge contacts
- Single rank
- I^2C temperature sensor

Figure 1: 200-Pin VLP SORDIMM (ATCA Compatible)



Options	Marking
• Operating temperature[1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 200-pin DIMM (lead-free)	Y
• Frequency/CAS latency[2]	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 2.5ns @ CL = 6 (DDR2-800)	-800
– 3.0ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
– 5.0ns @ CL = 3 (DDR2-400)[3]	-40E
• PCB height	
– 17.9mm (0.70in)	

Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
3. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	16K A[13:0]	16K A[13:0]
Device bank address	4 BA[1:0]	8 BA[2:0]
Device page size per bank	1KB	1KB
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H64M8, 512Mb DDR2 SDRAM[1]

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT9HVF6472RH(I)Y-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HVF6472RH(I)Y-800__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HVF6472RH(I)Y-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HVF6472RH(I)Y-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HVF6472RH(I)Y-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HVF6472RHY-667F1.

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H128M8, 1Gb DDR2 SDRAM[1]

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT9HVF12872RH(I)Y-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HVF12872RH(I)Y-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HVF12872RH(I)Y-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HVF12872RH(I)Y-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HVF12872RH(I)Y-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HVF12872RHY-667E1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin VLP SORDIMM Front								200-Pin VLP SORDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vref	51	DQ18	101	Vdd	151	Vss	2	Vss	52	Vss	102	A6	152	Vss
3	DQ0	53	DQ19	103	A5	153	DQS5#	4	DQ4	54	DQ28	104	A4	154	DM5
5	Vss	55	Vss	105	A3	155	DQS5	6	DQ5	56	DQ29	106	Vdd	156	Vss
7	DQ1	57	DQ24	107	A2	157	Vss	8	Vss	58	Vss	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	Vdd	159	DQ42	10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	Vss	111	A10	161	DQ43	12	Vss	62	Vss	112	BA1	162	Vss
13	Vss	63	DQS3#	113	BA0	163	Vss	14	DQ6	64	DQ30	114	Vdd	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48	16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	Vss	117	Vdd	167	DQ49	18	Vss	68	Vss	118	S0#	168	Vss
19	Vss	69	DQ26	119	CAS#	169	Vss	20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	NC	171	DQS6#	22	DQ13	72	CB5	122	A13	172	Vss
23	DQ9	73	Vss	123	Vdd	173	DQS6	24	Vss	74	Vss	124	Vdd	174	DQ54
25	Vss	75	CB0	125	NC	175	Vss	26	DM1	76	DM8	126	CK0	176	DQ55
27	DQS1#	77	CB1	127	NC	177	DQ50	28	Vss	78	Vss	128	CK0#	178	Vss
29	DQS1	79	Vss	129	DQ32	179	DQ51	30	DQ14	80	CB6	130	Vss	180	DQ60
31	Vss	81	DQS8#	131	Vss	181	Vss	32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56	34	Vss	84	Vss	134	DQ37	184	Vss
35	DQ11	85	Vss	135	DQS4#	185	DQ57	36	DQ20	86	CB2	136	Vss	186	DM7
37	Vss	87	CKE0	137	DQS4	187	Vss	38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	NC	139	Vss	189	DQS7#	40	Vss	90	Vss	140	Vss	190	Vss
41	DQ17	91	EVENT#	141	DQ34	191	DQS7	42	RESET#	92[1]	NF/BA2	142	DQ38	192	DQ63
43	Vss	93	Vdd	143	DQ35	193	DQ58	44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	Vss	195	Vss	46	Vss	96	A11	146	Vss	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59	48	DQ22	98	Vdd	148	DQ44	198	SA1
49	Vss	99	A7	149	DQ41	199	Vddspd	50	DQ23	100	A8	150	DQ45	200	SA0

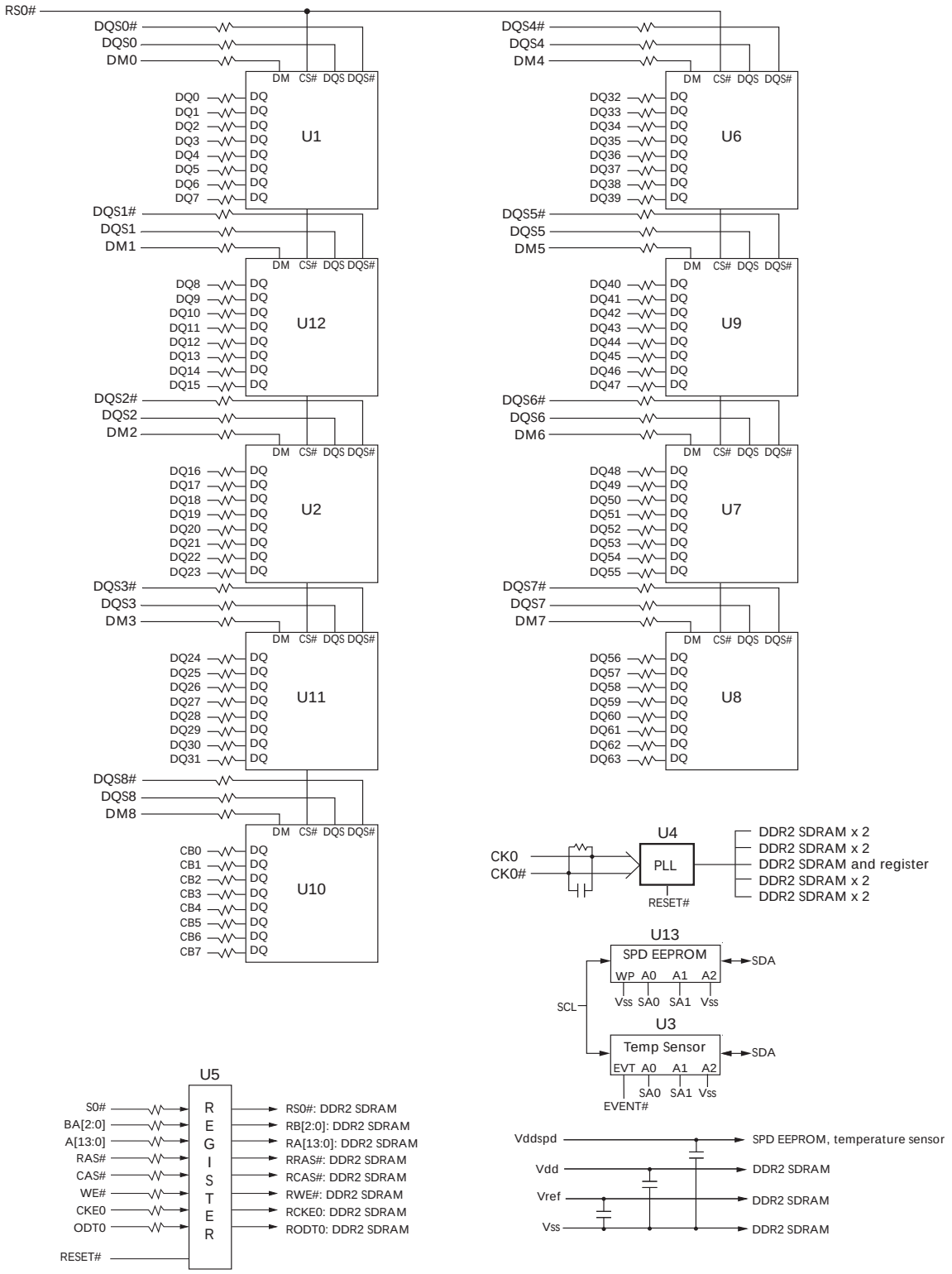
Notes: 1. Pin 92 is NF for 512MB, BA2 for 1GB.

Table 6: Pin Descriptions

Symbol	Type	Description
A[13:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2/1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA[2:0]	Input	**Bank address inputs:** BA[2/1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2/1:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command. BA[1:0] (512MB) and BA[2:0] (1GB).
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ, DQS, and DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DM[8:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[1:0]	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize communication to and from the SPD EEPROM.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I^2C bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
Vdd	Supply	**Power supply:** 1.8V ±0.1V.
Vddspd	Supply	**SPD EEPROM power supply:** +1.7V to +3.6V.
Vref	Supply	**Reference voltage:** Vdd/2.
Vss	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** Connected within the module, but provides no functionality.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT9HVF6472RH and MT9HVF12872RH DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 512MB and 1GB memory modules organized in a x72 configuration. These modules use internally configured, 4-bank (512Mb) or 8-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

These DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Temperature Sensor

An on-board temperature sensor provides the ability to monitor the module temperature along with monitoring alarms. Programmable registers can be used to specify temperature events and critical boundaries. The EVENT# pin is used to signal when different conditions occur based on how the registers are defined.

Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[1:0], which provide four unique DIMM/EEPROM addresses. Write protect (WP) is connected to Vss, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
Vdd/Vddq	Vdd/Vddq supply voltage relative to Vss		–0.5	+2.3	V
Vin, Vout	Voltage on any pin relative to Vss		–0.5	+2.3	V
Ii	Input leakage current; Any input 0V ≤ Vin ≤ Vdd; Vref input 0V ≤ Vin ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, S#, CKE, ODT, BA	–5	+5	µA
		CK0, CK0#	–250	+250	
		DM	–5	+5	
Ioz	Output leakage current; 0V ≤ Vout ≤ Vddq; DQ and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
Ivref	Vref leakage current; Vref = valid Vref level		–18	+18	µA
T_A	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. Refresh rate is required to double when 85°C < T_C ≤ 95°C.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

Idd Specifications

Table 9: DDR2 Idd Specifications and Conditions – 512MB

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from the values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (Idd), ^{t}RC = ^{t}RC (Idd), ^{t}RAS = ^{t}RAS MIN (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		Idd0	900	810	720	720	mA
Operating one bank active-read-precharge current: Iout = 0mA; BL = 4, CL = CL (Idd), AL = 0; ^{t}CK = ^{t}CK (Idd), ^{t}RC = ^{t}RC (Idd), ^{t}RAS = ^{t}RAS MIN (Idd), ^{t}RCD = ^{t}RCD (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as Idd4W		Idd1	1035	945	855	810	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (Idd); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		Idd2P	63	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (Idd); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		Idd2Q	450	405	360	315	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (Idd); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		Idd2N	495	450	405	360	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (Idd); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	Idd3P	360	315	270	225	mA
	Slow PDN exit MR[12] = 1		108	108	108	108	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (Idd), ^{t}RAS = ^{t}RAS MAX (Idd), ^{t}RP = ^{t}RP (Idd); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		Idd3N	630	585	495	405	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (Idd), AL = 0; ^{t}CK = ^{t}CK (Idd), ^{t}RAS = ^{t}RAS MAX (Idd), ^{t}RP = ^{t}RP (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		Idd4W	1755	1530	1260	1035	mA
Operating burst read current: All device banks open; Continuous burst reads; Iout = 0mA; BL = 4, CL = CL (Idd), AL= 0; ^{t}CK = ^{t}CK (Idd), ^{t}RAS = ^{t}RAS MAX (Idd), ^{t}RP = ^{t}RP (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		Idd4R	1845	1620	1305	1035	mA
Burst refresh current: ^{t}CK = ^{t}CK (Idd); REFRESH command at every ^{t}RFC (Idd) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		Idd5	2070	1620	1530	1485	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		Idd6	63	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; Iout = 0mA; BL = 4, CL = CL (Idd), AL = ^{t}RCD (Idd) - 1 × ^{t}CK (Idd); ^{t}CK = ^{t}CK (Idd), ^{t}RC = ^{t}RC (Idd), ^{t}RRD = ^{t}RRD (Idd), ^{t}RCD = ^{t}RCD (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		Idd7	2700	2160	2025	1980	mA

Table 10: DDR2 Idd Specifications and Conditions – 1GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (Idd), ^{t}RC = ^{t}RC (Idd), ^{t}RAS = ^{t}RAS MIN (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		Idd0	810	765	630	630	mA
Operating one bank active-read-precharge current: Iout = 0mA; BL = 4, CL = CL (Idd), AL = 0; ^{t}CK = ^{t}CK (Idd), ^{t}RC = ^{t}RC (Idd), ^{t}RAS = ^{t}RAS MIN (Idd), ^{t}RCD = ^{t}RCD (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as Idd4W		Idd1	990	900	855	810	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (Idd); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		Idd2P	63	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (Idd); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		Idd2Q	450	360	360	315	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (Idd); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		Idd2N	450	360	360	315	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (Idd); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	Idd3P	360	270	270	270	mA
	Slow PDN exit MR[12] = 1		90	90	90	90	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (Idd), ^{t}RAS = ^{t}RAS MAX (Idd), ^{t}RP = ^{t}RP (Idd); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		Idd3N	540	495	405	360	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (Idd), AL = 0; ^{t}CK = ^{t}CK (Idd), ^{t}RAS = ^{t}RAS MAX (Idd), ^{t}RP = ^{t}RP (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		Idd4W	1440	1215	1125	945	mA
Operating burst read current: All device banks open; Continuous burst reads; Iout = 0mA; BL = 4, CL = CL (Idd), AL = 0; ^{t}CK = ^{t}CK (Idd), ^{t}RAS = ^{t}RAS MAX (Idd), ^{t}RP = ^{t}RP (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		Idd4R	1440	1215	1125	945	mA
Burst refresh current; ^{t}CK = ^{t}CK (Idd); REFRESH command at every ^{t}RFC (Idd) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		Idd5	2115	1935	1890	1845	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		Idd6	63	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; Iout = 0mA; BL = 4, CL = CL (Idd), AL = ^{t}RCD (Idd) - 1 × ^{t}CK (Idd); ^{t}CK = ^{t}CK (Idd), ^{t}RC = ^{t}RC (Idd), ^{t}RRD = ^{t}RRD (Idd), ^{t}RCD = ^{t}RCD (Idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		Idd7	3015	2520	2430	2340	mA

Register and PLL Specifications

Table 11: Register Specifications
SSTU32872 devices or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	Vih(DC)	Control, command, address inputs	SSTL_18	Vref(DC) +125	–	mV
DC low-level input voltage	Vil(DC)	Control, command, address inputs	SSTL_18	–	Vref(DC) –125	mV
AC high-level input voltage	Vih(AC)	Control, command, address inputs	SSTL_18	Vref(DC) +250	–	mV
AC low-level input voltage	Vil(AC)	Control, command, address inputs	SSTL_18	–	Vref(DC) –250	mV
Output high voltage	Voh	Parity output	LVCMOS	1.2	–	V
Output low voltage	Vol	Parity output	LVCMOS	–	0.5	V
Input current	Ii	All pins	Vi = Vddq or Vssq	–5	+5	µA
Static standby	Idd	All pins	RESET# = Vssq (Io = 0)	–	200	µA
Static operating	Idd	All pins	RESET# = Vssq; Vi = Vih(AC) or Vil(DC) Io = 0	–	80	mA
Dynamic operating (clock tree)	Iddd	n/a	RESET# = Vdd, Vi = Vih(AC) or Vil(AC), Io = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	Iddd	n/a	RESET# = Vdd, Vi = Vih(AC) or Vil(AC), Io = 0; CK and CK# switching 50% duty cycle; One data input switching at ^{t}CK/2, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	Ci	All inputs except RESET#	Vi = Vref ±250mV; Vddq = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	Ci	RESET#	Vi = Vddq or Vssq	–	Varies by manufacturer	pF

Table 12: PLL Specifications
CUA845 device or JESD82-21 equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	Vih	OE, OS, CK, CK#	LVCMOS	0.65 × Vdd	–	V
DC low-level input voltage	Vil	OE, OS, CK, CK#	LVCMOS	–	0.35 × Vdd	V
Input voltage (limits)	Vin			–0.3	Vddq + 0.3	V
Input differential-pair cross voltage	Vix		Differential input	(Vddq/2) – 0.15	(Vddq/2) + 0.15	V
Input differential voltage	Vid(DC)		Differential input	0.3	Vddq + 0.4	V
Input differential voltage	Vid(AC)		Differential input	0.6	Vddq + 0.4	V
Input current	Ii	OE, OS, FBIN, FBIN#	Vi = Vddq or Vssq	–10	+10	µA
		CK, CK#	Vi = Vddq or Vssq	–250	+250	µA
Output disabled current	Iodl		OE = L, Vddl = 100mV	100	–	µA
Static supply current	Iddld		CK = CK# = 0pf	–	+500	µA
Dynamic supply	Idd	n/a	CK, CK# = 410 MHz, all outputs open (not connected to PCB)	–	+300	mA
Input capacitance	Cin	Each input	Vi = Vddq or Vssq	2	3	pF

Table 13: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^{t}L	–	6	µs
Input clock slew rate	slr(i)	1.0	4.0	V/ns
SSC modulation frequency		30	33	kHz
SSC clock input frequency deviation		0.0	–0.5	%
PLL loop bandwidth (-3db from unity gain)		2	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the SPD EEPROM.

Table 14: Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	Vddspd	+3.0	+3.6	V
Supply current: Vdd = 3.3V	Idd	–	+2.0	mA
Input high voltage: Logic 1; SCL, SDA	Vih	+1.45	Vddspd + 1	V
Input low voltage: Logic 0; SCL, SDA	Vil	–	+0.55	V
Output low voltage: Iout = 2.1mA	Vol	–	+0.4	V
Input current	Iin	–5.0	+5.0	µA
Temperature sensing range	–	–40	+125	°C
Temperature sensor accuracy (class B)	–	–1.0	+1.0	°C

Table 15: Sensor Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^tBUF	4.7	–	µs
SDA fall time	^tF	20	300	ns
SDA rise time	^tR	–	1000	ns
Data hold time	$^tHD:DAT$	200	900	ns
Start condition hold time	$^tH:STA$	4.0	–	µs
Clock HIGH period	^tHIGH	4.0	50	µs
Clock LOW period	^tLOW	4.7	–	µs
SCL clock frequency	^fSCL	10	100	kHz
Data setup time	$^tSU:DAT$	250	–	ns
Start condition setup time	$^tSU:STA$	4.7	–	µs
Stop condition setup time	$^tSU:STO$	4.0	–	µs

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is shown in Figure 3 on page 14. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# triggers whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers at the critical temperature limit and at the MIN and MAX points of the temperature alarm window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature exceeds the programmed critical trip point. When the critical trip point is reached, the temperature sensor goes into comparator mode, and the critical EVENT# signal cannot be cleared through software.

System Management Bus (SMBus) Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, A2, and RW#, where A0, A1, and A2 are the three slave subaddress pins and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the temperature sensor/SPD EEPROM, then pins A[2:0] set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

Figure 3: EVENT# Pin Functionality

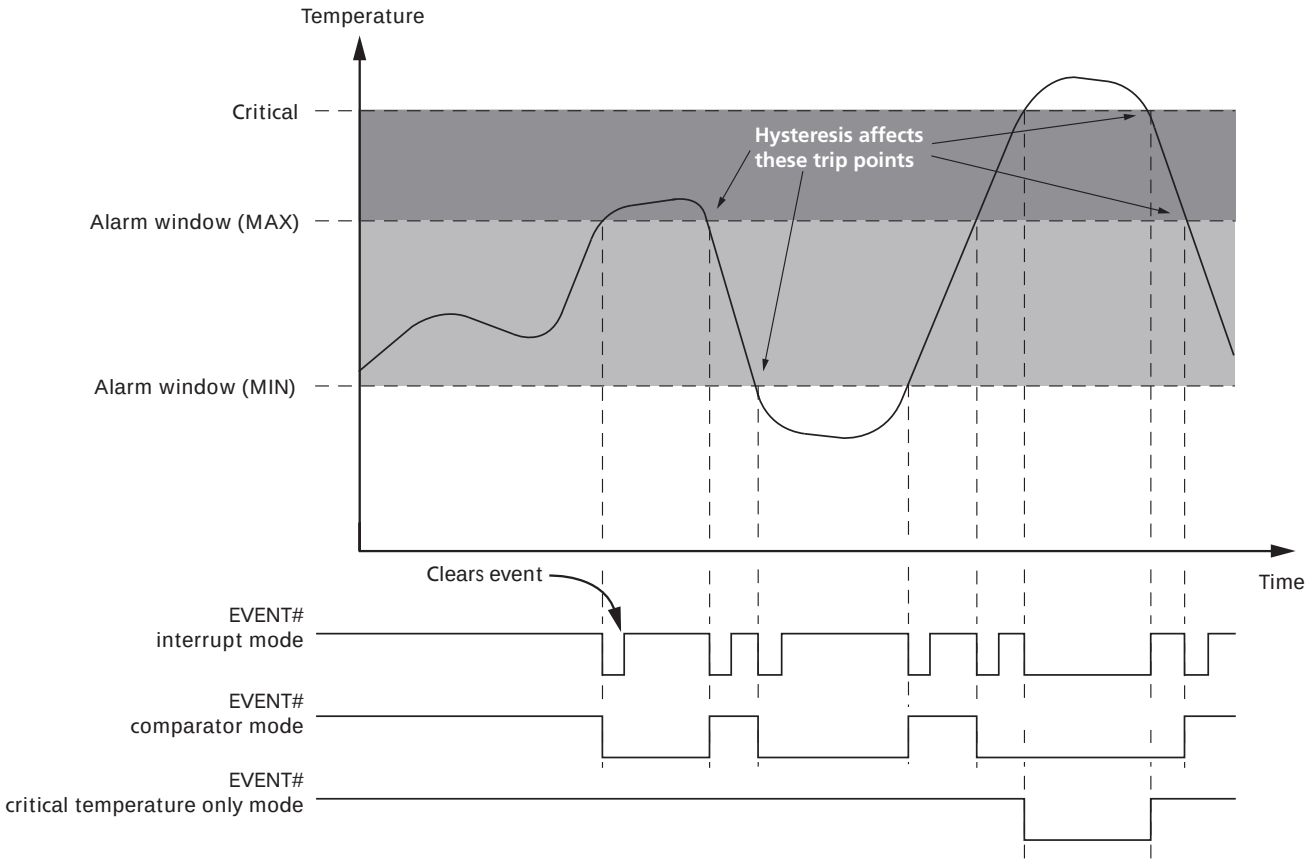


Table 16: Temperature Sensor Registers

Name	Address	Power-On Default
Pointer register	Not applicable	Undefined
Capability register	0x00	0x0001
Configuration register	0x01	0x0000
Alarm temperature upper boundary register	0x02	0x0000
Alarm temperature lower boundary register	0x03	0x0000
Critical temperature register	0x04	0x0000
Temperature register	0x05	Undefined

Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

Table 17: Pointer Register Bits 0–7

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	Register select	Register select	Register select	Register select

Table 18: Pointer Register Bits 0–2 Descriptions

Bit			Register
2	1	0	
0	0	0	Capability register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary register
0	1	1	Alarm temperature lower boundary register
1	0	0	Critical temperature register
1	0	1	Temperature register

Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

Table 19: Capability Register Bits

Bit							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RFU	RFU	RFU	TRES1	TRES0	Wider range	Precision	Alarm and critical temperature

Table 20: Capability Register Bit Descriptions

Bit	Description
0	Basic capability 1: Has alarm and critical trip-point capabilities
1	Accuracy 0: ±2°C over the active range and ±3°C over the monitor range 1: ±1°C over the active range and ±2°C over the monitor range
2	Wider range 0: Temperatures lower than 0°C are clamped to a binary value of 0 1: Temperatures below 0°C can be read
4:3	Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB
15:5	0: Must be set to zero

Configuration Register

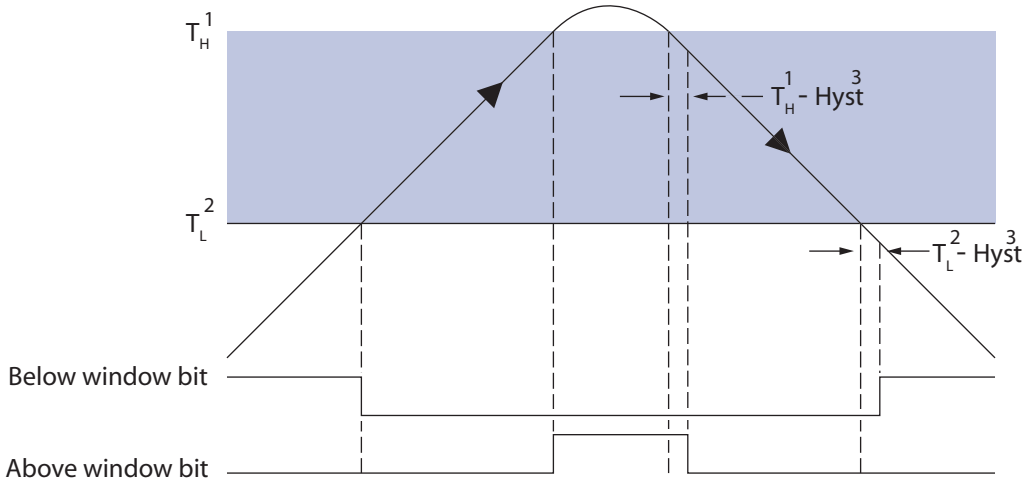
Table 21: Configuration Register(Address: 0x01)

Bit							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

Table 22: Configuration Register Bit Descriptions

Bit	Description	Notes
0	Event mode 0: Comparator mode 1: Interrupt mode	Event mode cannot be changed if either of the lock bits is set.
1	EVENT# polarity 0: Active LOW 1: Active HIGH	EVENT# polarity cannot be changed if either of the lock bits is set.
2	Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached	
3	Event output control 0: Event output disabled 1: Event output enabled	
4	Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition	This is a read-only field in the register. The event causing the event can be determined from the read temperature register.
5	Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode	
6	Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed	
7	Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed	
8	Shutdown mode 0: Enabled 1: Shutdown	The shutdown mode is a power-saving mode that disables the temperature sensor.
10:9	Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C	When enabled, a hysteresis is applied to temperature movement around the trip points (see Figure 4 on page 18). For example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C. The hysteresis is applied to both the above alarm window and the below alarm window bits found in the read-only temperature register (see Table 23 on page 18). EVENT# is also affected by this register.

Figure 4: Hysteresis Applied to Temperature Around Trip Points



Notes:
1. T_H is the value set in the alarm temperature upper boundary trip register.
2. T_L is the value set in the alarm temperature lower boundary trip register.
3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 23: Hysteresis Applied to Alarm Window Bits in the Temperature Register

Condition	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature Gradient	Critical Temperature	Temperature Gradient	Critical Temperature
Sets	Falling	T_L - Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H - Hyst

Temperature Format

The temperature trip point registers and the temperature readout register use a 2's complement format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C, depending on which register is referenced. For example, assuming an LSB of 0.0625°C:

- A value of 0x018C equals 24.75°C
- A value of 0x06C0 equals 108°C
- A value of 0x1E74 equals –24.75°C

Temperature Trip Point Registers

The upper and lower temperature boundary registers are used to set the minimum and maximum values of the alarm window. The LSB for these registers is 0.25°C. All RFU bits in the register will always report 0s.

Table 24: Alarm Temperature Lower Boundary Register (Address: 0x02)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window upper boundary temperature												

Table 25: Alarm Temperature Lower Boundary Register (Address: 0x03)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window lower boundary temperature												

Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report 0s.

Table 26: Critical Temperature Register (Address: 0x04)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Critical temperature trip point												

Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.

Table 27: Temperature Register (Address: 0x05)

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Above critical trip	Above alarm window	Below alarm window	MSB												LSB
			Temperature												

Table 28: Temperature Register Bit Descriptions

Bit	Description
13	Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window
14	Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window
15	Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point

Serial Presence-Detect

Table 29: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage with temperature sensor option	Vddspd	3.0	3.6	V
Input high voltage: Logic 1; All inputs	Vih	2.1	Vddspd + 0.5	V
Input low voltage: Logic 0; All inputs	Vil	–0.6	0.8	V
Output low voltage: Iout = 3mA	Vol	–	0.4	V
SPD input leakage current: Vin = GND to Vdd	Ili	0.10	3	µA
SPD output leakage current: V_{OUT} = GND to Vdd	Ilo	0.05	3	µA
SPD standby current	Isb	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	Iccr	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	Iccw	2	3	mA
Average temperature sensor current	–	–	500	µA

Table 30: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA and SCL fall time	^{t}F	–	300	ns	2
Data-in hold time	^{t}HD:DAT	0	–	µs	
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Clock HIGH period	^{t}HIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SDA and SCL rise time	^{t}R	–	0.3	µs	2
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	^{t}SU:DAT	100	–	ns	
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

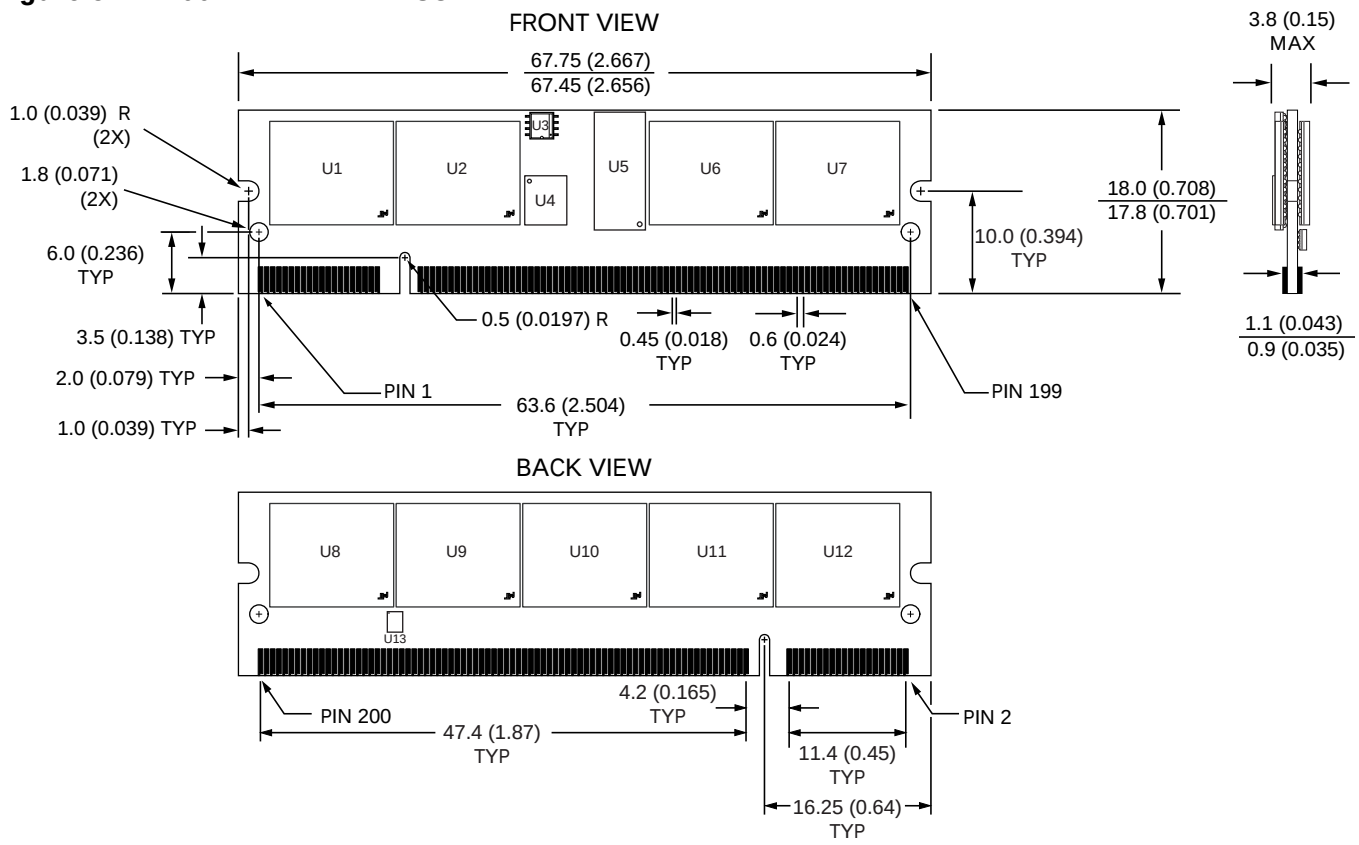
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:
www.micron.com/SPD

Module Dimensions

Figure 5: 200-Pin DDR2 VLP SORDIM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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