

DDR2 SDRAM SORDIMM

MT9HTF6472RH – 512MB

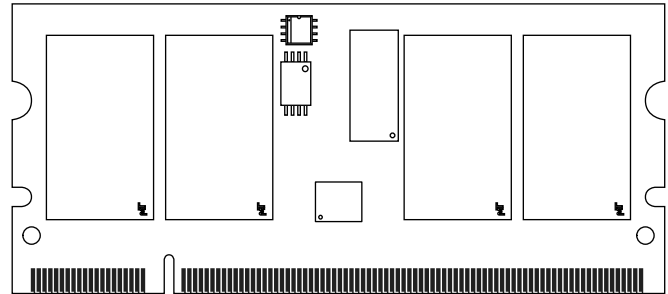
MT9HTF12872RH – 1GB

Features

- 200-pin, small-outline registered dual in-line memory module
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 512MB (64 Meg x 72) or 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = 1.8V$
- $V_{DDSPD} = 3.0\text{--}3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Phase-lock loop (PLL) to reduce system clock line loading
- Gold edge contacts
- Single rank
- I²C temperature sensor

Figure 1: 200-Pin SORDIMM (MO-274 R/C A)

Module height: 30mm (1.18in)



Options

- Operating temperature
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)¹
- Package
 - 200-pin DIMM (lead-free)
- Frequency/CL²
 - 2.5 @ CL = 5 (DDR2-800) -80E
 - 2.5 @ CL = 6 (DDR2-800) -800
 - 3.0ns @ CL = 5 (DDR2-667) -667
 - 3.75ns @ CL = 4 (DDR2-533)³ -53E

Marking

None
I
Y
-80E
-800
-667
-53E

- Notes:
1. Contact Micron for industrial temperature module offerings
 2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
 3. Not recommended for new designs.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | | t _{RCD} (ns) | t _{RP} (ns) | t _{RC} (ns) |
|-------------|-----------------------|------------------|--------|--------|--------|-----------------------|----------------------|----------------------|
| | | CL = 6 | CL = 5 | CL = 4 | CL = 3 | | | |
| -80E | PC2-6400 | 800 | 800 | 533 | 400 | 12.5 | 12.5 | 55 |
| -800 | PC2-6400 | 800 | 667 | 533 | 400 | 15 | 15 | 55 |
| -667 | PC2-5300 | – | 667 | 553 | 400 | 15 | 15 | 55 |
| -53E | PC2-4200 | – | – | 553 | 400 | 15 | 15 | 55 |
| -40E | PC2-3200 | – | – | 400 | 400 | 15 | 15 | 55 |

Table 2: Addressing

| Parameter | 512MB | 1GB |
|----------------------|--------------------|-------------------|
| Refresh count | 8K | 8K |
| Row address | 16K A[13:0] | 16K A[13:0] |
| Device bank address | 4 BA[1:0] | 8 BA[2:0] |
| Device configuration | 512Mb (64 Meg x 8) | 1Gb (128 Meg x 8) |
| Column address | 1K A[9:0] | 1K A[9:0] |
| Module rank address | 1 S0# | 1 S0# |

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H64M8,¹ 512Mb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---|
| MT9HTF6472RH(I)Y-80E__ | 512MB | 64 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT9HTF6472RH(I)Y-800__ | 512MB | 64 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT9HTF6472RH(I)Y-667__ | 512MB | 64 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT9HTF6472RH(I)Y-53E__ | 512MB | 64 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H128M8,¹ 1Gb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---|
| MT9HTF12872RH(I)Y-80E__ | 1GB | 128 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT9HTF12872RH(I)Y-800__ | 1GB | 128 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT9HTF12872RH(I)Y-667__ | 1GB | 128 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT9HTF12872RH(I)Y-53E__ | 1GB | 128 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |

- Notes:
1. The data sheet for the base device can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF12872RHY-667E1.

Pin Assignments

Table 5: Pin Assignments

| 200-Pin SORDIMM Front | | | | | | | | 200-Pin SORDIMM Back | | | | | | | |
|-----------------------|------------------|-----|-----------------|-----|-----------------|-----|--------------------|----------------------|-----------------|-----------------|-----------------|-----|-----------------|-----|-----------------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | V _{REF} | 51 | DQ18 | 101 | V _{DD} | 151 | V _{SS} | 2 | V _{SS} | 52 | V _{SS} | 102 | A6 | 152 | V _{SS} |
| 3 | DQ0 | 53 | DQ19 | 103 | A5 | 153 | DQS5# | 4 | DQ4 | 54 | DQ28 | 104 | A4 | 154 | DM5 |
| 5 | V _{SS} | 55 | V _{SS} | 105 | A3 | 155 | DQS5 | 6 | DQ5 | 56 | DQ29 | 106 | V _{DD} | 156 | V _{SS} |
| 7 | DQ1 | 57 | DQ24 | 107 | A2 | 157 | V _{SS} | 8 | V _{SS} | 58 | V _{SS} | 108 | A1 | 158 | DQ46 |
| 9 | DQS0# | 59 | DQ25 | 109 | V _{DD} | 159 | DQ42 | 10 | DM0 | 60 | DM3 | 110 | A0 | 160 | DQ47 |
| 11 | DQS0 | 61 | V _{SS} | 111 | A10 | 161 | DQ43 | 12 | V _{SS} | 62 | V _{SS} | 112 | BA1 | 162 | V _{SS} |
| 13 | V _{SS} | 63 | DQS3# | 113 | BA0 | 163 | V _{SS} | 14 | DQ6 | 64 | DQ30 | 114 | V _{DD} | 164 | DQ52 |
| 15 | DQ2 | 65 | DQS3 | 115 | RAS# | 165 | DQ48 | 16 | DQ7 | 66 | DQ31 | 116 | WE# | 166 | DQ53 |
| 17 | DQ3 | 67 | V _{SS} | 117 | V _{DD} | 167 | DQ49 | 18 | V _{SS} | 68 | V _{SS} | 118 | S0# | 168 | V _{SS} |
| 19 | V _{SS} | 69 | DQ26 | 119 | CAS# | 169 | V _{SS} | 20 | DQ12 | 70 | CB4 | 120 | ODT0 | 170 | DM6 |
| 21 | DQ8 | 71 | DQ27 | 121 | NC | 171 | DQS6# | 22 | DQ13 | 72 | CB5 | 122 | A13 | 172 | V _{SS} |
| 23 | DQ9 | 73 | V _{SS} | 123 | V _{DD} | 173 | DQS6 | 24 | V _{SS} | 74 | V _{SS} | 124 | V _{DD} | 174 | DQ54 |
| 25 | V _{SS} | 75 | CB0 | 125 | NC | 175 | V _{SS} | 26 | DM1 | 76 | DM8 | 126 | CK0 | 176 | DQ55 |
| 27 | DQS1# | 77 | CB1 | 127 | NC | 177 | DQ50 | 28 | V _{SS} | 78 | V _{SS} | 128 | CK0# | 178 | V _{SS} |
| 29 | DQS1 | 79 | V _{SS} | 129 | DQ32 | 179 | DQ51 | 30 | DQ14 | 80 | CB6 | 130 | V _{SS} | 180 | DQ60 |
| 31 | V _{SS} | 81 | DQS8# | 131 | V _{SS} | 181 | V _{SS} | 32 | DQ15 | 82 | CB7 | 132 | DQ36 | 182 | DQ61 |
| 33 | DQ10 | 83 | DQS8 | 133 | DQ33 | 183 | DQ56 | 34 | V _{SS} | 84 | V _{SS} | 134 | DQ37 | 184 | V _{SS} |
| 35 | DQ11 | 85 | V _{SS} | 135 | DQS4# | 185 | DQ57 | 36 | DQ20 | 86 | CB2 | 136 | V _{SS} | 186 | DM7 |
| 37 | V _{SS} | 87 | CKE0 | 137 | DQS4 | 187 | V _{SS} | 38 | DQ21 | 88 | CB3 | 138 | DM4 | 188 | DQ62 |
| 39 | DQ16 | 89 | NC | 139 | V _{SS} | 189 | DQS7# | 40 | V _{SS} | 90 | V _{SS} | 140 | V _{SS} | 190 | V _{SS} |
| 41 | DQ17 | 91 | EVENT# | 141 | DQ34 | 191 | DQS7 | 42 | RESET# | 92 ¹ | NC/BA2 | 142 | DQ38 | 192 | DQ63 |
| 43 | V _{SS} | 93 | V _{DD} | 143 | DQ35 | 193 | DQ58 | 44 | DM2 | 94 | NC | 144 | DQ39 | 194 | SDA |
| 45 | DQS2# | 95 | A12 | 145 | V _{SS} | 195 | V _{SS} | 46 | V _{SS} | 96 | A11 | 146 | V _{SS} | 196 | SCL |
| 47 | DQS2 | 97 | A9 | 147 | DQ40 | 197 | DQ59 | 48 | DQ22 | 98 | V _{DD} | 148 | DQ44 | 198 | SA1 |
| 49 | V _{SS} | 99 | A7 | 149 | DQ41 | 199 | V _{DDSPD} | 50 | DQ23 | 100 | A8 | 150 | DQ45 | 200 | SA0 |

Note: 1. Pin 92 is NC for 512MB or BA2 for 1GB.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR2 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

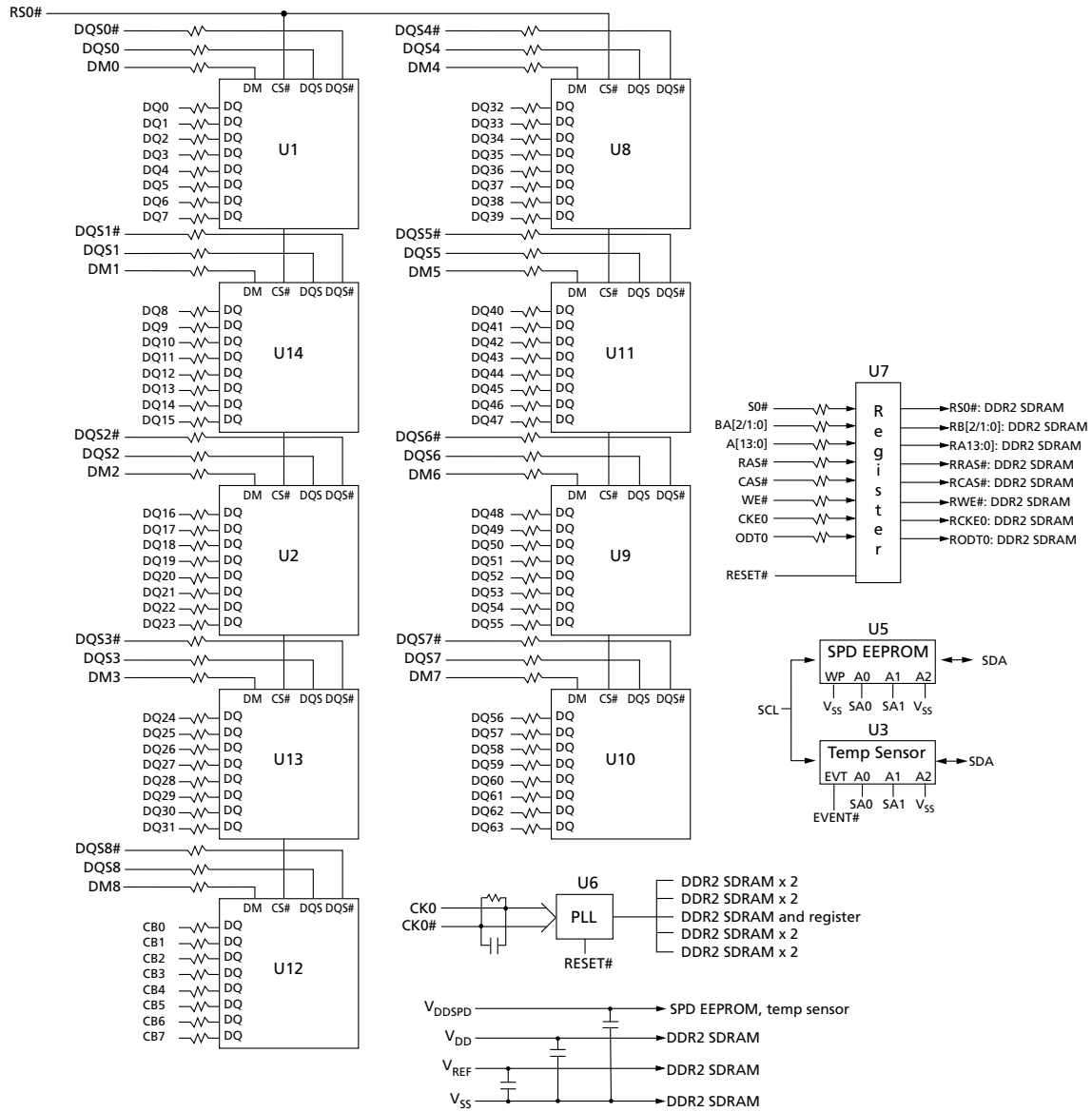
| Symbol | Type | Description |
|-----------------|-------|---|
| Ax | Input | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information. |
| BAx | Input | Bank address inputs: Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. |
| CKx, CK#x | Input | Clock: Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. |
| CKEx | Input | Clock enable: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM. |
| DMx, | Input | Data mask (x8 devices only): DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. |
| ODTx | Input | On-die termination: Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| Par_In | Input | Parity input: Parity bit for Ax, RAS#, CAS#, and WE#. |
| RAS#, CAS#, WE# | Input | Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input | Reset: Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z. |
| S#x | Input | Chip select: Enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SAx | Input | Serial address inputs: Used to configure the SPD EEPROM address range on the I ² C bus. |
| SCL | Input | Serial clock for SPD EEPROM: Used to synchronize communication to and from the SPD EEPROM on the I ² C bus. |
| CBx | I/O | Check bits. Used for system error detection and correction. |
| DQx | I/O | Data input/output: Bidirectional data bus. |
| DQSx, DQS#x | I/O | Data strobe: Travels with the DQ and is used to capture DQ at the DRAM or the controller. Output with read data; input with write data for source synchronous operation. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |

Table 6: Pin Descriptions (Continued)

| Symbol | Type | Description |
|-----------------------------------|------------------------|---|
| SDA | I/O | Serial data: Used to transfer addresses and data into and out of the SPD EEPROM on the I ² C bus. |
| RDQSx, RDQS#x | Output | Redundant data strobe (x8 devices only): RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, RDQS becomes data mask (see DMx). RDQS# is only used when RDQS is enabled and differential data strobe mode is enabled. |
| Err_Out# | Output (open drain) | Parity error output: Parity error found on the command and address bus. |
| V _{DD} /V _{DDQ} | Supply | Power supply: 1.8V ±0.1V. The component V _{DD} and V _{DDQ} are connected to the module V _{DD} . |
| V _{DDSPD} | Supply | SPD EEPROM power supply: 1.7–3.6V. |
| V _{REF} | Supply | Reference voltage: V _{DD} /2. |
| V _{SS} | Supply | Ground. |
| NC | – | No connect: These pins are not connected on the module. |
| NF | – | No function: These pins are connected within the module, but provide no functionality. |
| NU | – | Not used: These pins are not used in specific module configurations/operations. |
| RFU | – | Reserved for future use. |

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

DDR2 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR2 SDRAM devices. DDR2 SDRAM modules use DDR architecture to achieve high-speed operation. DDR2 architecture is essentially a $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR2 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection.

Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Temperature Sensor

An on-board temperature sensor provides the ability to monitor the module temperature along with monitoring alarms. Programmable registers can be used to specify temperature events and critical boundaries. An EVENT# pin is used to signal when different conditions occur based on how the registers are defined.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | |
|-------------------|--|---|------|---------|-------------|
| V_{DD} | V_{DD} supply voltage relative to V_{SS} | -0.5 | 2.3 | V | |
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.5 | 2.3 | V | |
| I_I | Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; V_{REF} input $0V \leq V_{IN} \leq 0.95V$; (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA | -5 | 5 | μA |
| | | CK0, CK0# | -250 | 250 | |
| | | DM | -5 | 5 | |
| I_{OZ} | Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQ and ODT are disabled | -5 | 5 | μA | |
| I_{VREF} | V_{REF} leakage current; V_{REF} = valid V_{REF} level | -18 | 18 | μA | |
| T_A | Module ambient operating temperature | Commercial | 0 | 70 | $^{\circ}C$ |
| | | Industrial | -40 | 85 | $^{\circ}C$ |
| T_C^1 | DDR2 SDRAM component operating temperature ² | Commercial | 0 | 85 | $^{\circ}C$ |
| | | Industrial | -40 | 95 | $^{\circ}C$ |

- Notes:
1. The refresh rate is required to double when T_C exceeds 85 $^{\circ}C$.
 2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades.

Table 8: Module and Component Speed Grades

DDR2 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -1GA | -187E |
| -80E | -25E |
| -800 | -25 |
| -667 | -3 |
| -53E | -37E |
| -40E | -5E |

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 9: DDR2 I_{DD} Specifications and Conditions – 512MB

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

| Parameter | Symbol | -80E/-800 | -667 | -53E | Units | |
|--|-----------------------------|--------------------|------|------|-------|----|
| Operating one bank active-precharge current: $t^{CK} = t^{CK} (I_{DD})$, $t^{RC} = t^{RC} (I_{DD})$, $t^{RAS} = t^{RAS} \text{ MIN} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | I _{DD0} | 900 | 810 | 720 | mA | |
| Operating one bank active-read-precharge current: I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; $t^{CK} = t^{CK} (I_{DD})$, $t^{RC} = t^{RC} (I_{DD})$, $t^{RAS} = t^{RAS} \text{ MIN} (I_{DD})$, $t^{RCD} = t^{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I _{DD4W} | I _{DD1} | 1035 | 945 | 855 | mA | |
| Precharge power-down current: All device banks idle; $t^{CK} = t^{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | I _{DD2P} | 63 | 63 | 63 | mA | |
| Precharge quiet standby current: All device banks idle; $t^{CK} = t^{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | I _{DD2Q} | 450 | 405 | 360 | mA | |
| Precharge standby current: All device banks idle; $t^{CK} = t^{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | I _{DD2N} | 495 | 450 | 405 | mA | |
| Active power-down current: All device banks open; $t^{CK} = t^{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | I _{DD3PF} | 360 | 315 | 270 | mA |
| | Slow PDN exit MR[12] = 1 | I _{DD3PS} | 108 | 108 | 108 | mA |
| Active standby current: All device banks open; $t^{CK} = t^{CK} (I_{DD})$, $t^{RAS} = t^{RAS} \text{ MAX} (I_{DD})$, $t^{RP} = t^{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | I _{DD3N} | 630 | 585 | 495 | mA | |
| Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I _{DD}), AL = 0; $t^{CK} = t^{CK} (I_{DD})$, $t^{RAS} = t^{RAS} \text{ MAX} (I_{DD})$, $t^{RP} = t^{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | I _{DD4W} | 1755 | 1530 | 1260 | mA | |
| Operating burst read current: All device banks open; Continuous burst read, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; $t^{CK} = t^{CK} (I_{DD})$, $t^{RAS} = t^{RAS} \text{ MAX} (I_{DD})$, $t^{RP} = t^{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | I _{DD4R} | 1845 | 1620 | 1305 | mA | |
| Burst refresh current: $t^{CK} = t^{CK} (I_{DD})$; REFRESH command at every $t^{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | I _{DD5} | 2070 | 1620 | 1305 | mA | |
| Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | I _{DD6} | 63 | 63 | 63 | mA | |

Table 9: DDR2 I_{DD} Specifications and Conditions – 512MB (Continued)

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

| Parameter | Symbol | -80E/-800 | -667 | -53E | Units |
|--|------------------|-----------|------|------|-------|
| Operating bank interleave read current: All device banks interleaving reads; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = ^t RCD (I _{DD}) - 1 × ^t CK (I _{DD}); ^t CK = ^t CK (I _{DD}), ^t RC = ^t RC (I _{DD}), ^t RRD = ^t RRD (I _{DD}), ^t RCD = ^t RCD (I _{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | I _{DD7} | 2700 | 2160 | 2025 | mA |

Table 10: DDR2 I_{DD} Specifications and Conditions – 1GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

| Parameter | Symbol | -80E/ 800 | -667 | -53E | Units | |
|--|-----------------------------|--------------------|------|------|-------|----|
| Operating one bank active-precharge current: $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | I _{DD0} | 810 | 765 | 630 | mA | |
| Operating one bank active-read-precharge current: I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$, $t_{RCD} = t_{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I _{DD4W} | I _{DD1} | 990 | 900 | 855 | mA | |
| Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | I _{DD2P} | 63 | 63 | 63 | mA | |
| Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | I _{DD2Q} | 450 | 360 | 360 | mA | |
| Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | I _{DD2N} | 450 | 360 | 360 | mA | |
| Active power-down current: All device banks open; $t_{CK} = t_{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | I _{DD3PF} | 360 | 270 | 270 | mA |
| | Slow PDN exit MR[12] = 1 | I _{DD3PS} | 90 | 90 | 90 | mA |
| Active standby current: All device banks open; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | I _{DD3N} | 540 | 495 | 405 | mA | |
| Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | I _{DD4W} | 1440 | 1215 | 1125 | mA | |
| Operating burst read current: All device banks open; Continuous burst read, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | I _{DD4R} | 1440 | 1215 | 1125 | mA | |
| Burst refresh current: $t_{CK} = t_{CK} (I_{DD})$; REFRESH command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | I _{DD5} | 2115 | 1935 | 1890 | mA | |
| Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | I _{DD6} | 63 | 63 | 63 | mA | |
| Operating bank interleave read current: All device banks interleaving reads; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$; $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RRD} = t_{RRD} (I_{DD})$, $t_{RCD} = t_{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | I _{DD7} | 3015 | 2520 | 2430 | mA | |

Register and PLL Specifications

Table 11: Register Specifications

SSTU32872 devices or equivalent

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---|--------------|---------------------------|---|---------------------|------------------------|------------------|
| DC high-level input voltage | $V_{IH(DC)}$ | Control, command, address | SSTL_18 | $V_{REF(DC)} + 125$ | $V_{DDQ} + 250$ | mV |
| DC low-level input voltage | $V_{IL(DC)}$ | Control, command, address | SSTL_18 | 0 | $V_{REF(DC)} - 125$ | mV |
| AC high-level input voltage | $V_{IH(AC)}$ | Control, command, address | SSTL_18 | $V_{REF(DC)} + 250$ | V_{DD} | mV |
| AC low-level input voltage | $V_{IL(AC)}$ | Control, command, address | SSTL_18 | 0 | $V_{REF(DC)} - 250$ | mV |
| Output high voltage | V_{OH} | Parity output | SSTL_18 | 1.2 | – | V |
| Output low voltage | V_{OL} | Parity output | SSTL_18 | – | 0.5 | V |
| Input current | I_I | All pins | $V_I = V_{DDQ}$ or V_{SSQ} | –5 | 5 | μA |
| Static standby | I_{DD} | All pins | RESET# = V_{SSQ} ($I_O = 0$) | – | 200 | mA or μA ?? |
| Static operating | I_{DD} | All pins | RESET# = V_{SSQ} ; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$, $I_O = 0$ | – | 80 | mA |
| Dynamic operating (clock tree) | I_{DDD} | N/A | RESET# = V_{DD} ; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O = 0$; CK and CK# switching 50% duty cycle | – | Varies by manufacturer | μA |
| Dynamic operating (per each input) | I_{DDD} | N/A | RESET# = V_{DD} ; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O = 0$; CK and CK# switching 50% duty cycle; One data input switching at $t^{CK}/2$, 50% duty cycle | – | Varies by manufacturer | μA |
| Input capacitance (per device, per pin) | C_I | All inputs except RESET# | $V_I = V_{REF} \pm 250mV$; $V_{DDQ} = 1.8V$ | 2.5 | 3.5 | pF |
| Input capacitance (per device, per pin) | C_I | RESET# | $V_I = V_{DDQ}$ or V_{SSQ} | – | Varies by manufacturer | pF |

Table 12: PLL Specifications

CUA845 device or JEDEC82-21 equivalent

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---------------------------------------|--------------|---------------------|---|----------------------|----------------------|---------|
| DC high-level input voltage | V_{IH} | OE, OS, CK, CK# | LVC MOS | $0.65 \times V_{DD}$ | – | V |
| DC low-level input voltage | V_{IL} | OE, OS, CK, CK# | LVC MOS | – | $0.35 \times V_{DD}$ | V |
| Input voltage (limits) | V_{IN} | | | –0.3 | $V_{DD} + 0.3$ | V |
| Input differential-pair cross voltage | V_{IX} | | Differential input | $(V_{DD}/2) - 0.15$ | $(V_{DD}/2) + 0.15$ | V |
| Input differential voltage | $V_{ID(DC)}$ | | Differential input | 0.3 | $V_{DD} + 0.4$ | V |
| Input differential voltage | $V_{ID(AC)}$ | | Differential input | 600 | $V_{DD} + 0.4$ | V |
| Input current | I_I | OE, OS, FBIN, FBIN# | $V_I = V_{DD}$ or V_{SS} | –10 | 10 | μA |
| | | CK, CK# | $V_I = V_{DD}$ or V_{SS} | –250 | 250 | μA |
| Output disabled current | I_{ODL} | | OE = L, $V_{ODL} = 100mV$ | 100 | – | μA |
| Static supply current | I_{DDLD} | | $C_L = 0pf$ | – | 500 | μA |
| Dynamic supply | I_{DD} | N/A | CK and CK# = 410 MHz, all outputs open (not connected to PCB) | – | 300 | mA |
| Input capacitance | C_{IN} | Each input | $V_I = V_{DD}$ or V_{SS} | 2 | 3 | pF |

Table 13: PLL Clock Driver Timing Requirements and Switching Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|--------|-----|------|---------|
| Stabilization time | t_L | – | 6.0 | μs |
| Input clock slew rate | slr(i) | 1.0 | 4.0 | V/ns |
| SSC modulation frequency | – | 30 | 33.0 | kHz |
| SSC clock input frequency deviation | – | 0.0 | –0.5 | % |
| PLL loop bandwidth (–3dB from unity gain) | – | 2.0 | – | MHz |

Note: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82.

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I²C bus shared with the SPD EEPROM.

Table 14: Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|--|--------------------|-------|------------------------|-------|
| Supply voltage | V _{DDSPD} | +3.0 | +3.6 | V |
| Supply current: V _{DD} = 3.3V | I _{DD} | – | +2.0 | mA |
| Input high voltage: Logic 1; SCL, SDA | V _{IH} | +1.45 | V _{DDSPD} + 1 | V |
| Input low voltage: Logic 0; SCL, SDA | V _{IL} | – | +0.55 | V |
| Output low voltage: I _{OUT} = 2.1mA | V _{OL} | – | +0.4 | V |
| Input current | I _{IN} | –5.0 | +5.0 | μA |
| Temperature sensing range | – | –40 | +125 | °C |
| Temperature sensor accuracy (class B) | – | –1.0 | +1.0 | °C |

Table 15: Sensor and EEPROM Serial Interface Timing

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---------------------|-----|------|-------|
| Time bus must be free before a new transition can start | t _{BUF} | 4.7 | – | μs |
| SDA fall time | t _F | 20 | 300 | ns |
| SDA rise time | t _R | – | 1000 | ns |
| Data hold time | t _{HD:DAT} | 200 | 900 | ns |
| Start condition hold time | t _{H:STA} | 4.0 | – | μs |
| Clock HIGH period | t _{HIGH} | 4.0 | 50 | μs |
| Clock LOW period | t _{LOW} | 4.7 | – | μs |
| SCL clock frequency | t _{SCL} | 10 | 100 | kHz |
| Data setup time | t _{SU:DAT} | 250 | – | ns |
| Start condition setup time | t _{SU:STA} | 4.7 | – | μs |
| Stop condition setup time | t _{SU:STO} | 4.0 | – | μs |

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated below. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

SM Bus Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, A2, and RW#, where A2, A1, and A0 are the three slave subaddress pins and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the temperature sensor/SPD EEPROM, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

Figure 3: EVENT# Pin Functionality

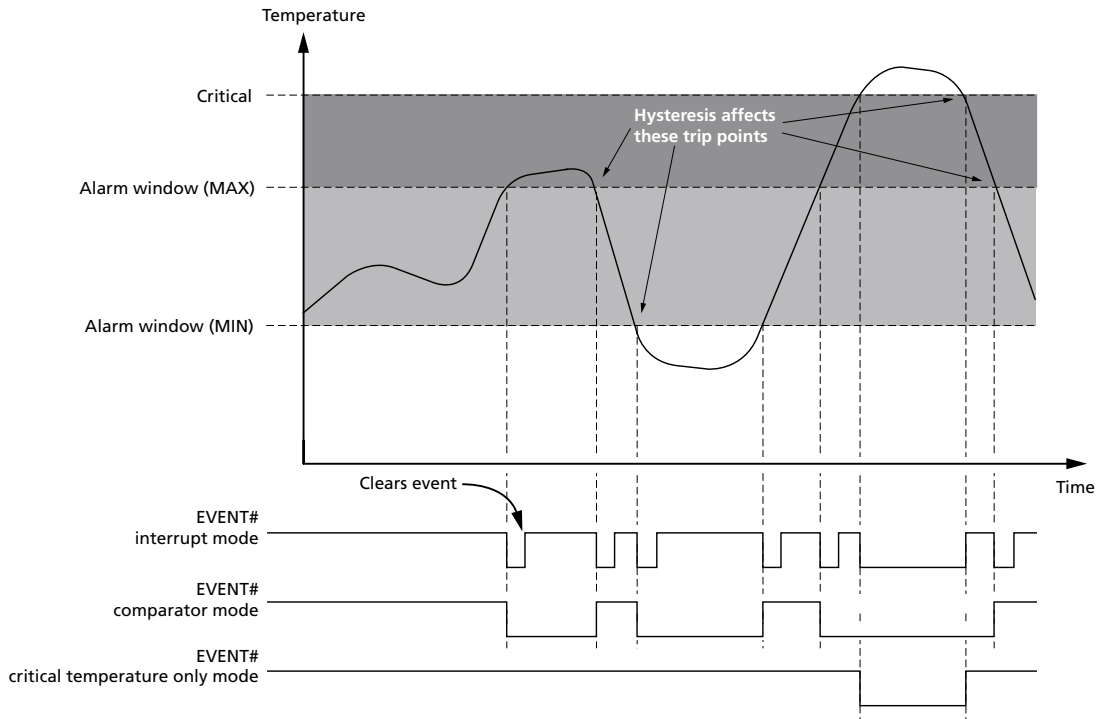


Table 16: Temperature Sensor Registers

| Name | Address | Power-on Default |
|---|----------------|------------------|
| Pointer register | Not applicable | Undefined |
| Capability register | 0x00 | 0x0001 |
| Configuration register | 0x01 | 0x0000 |
| Alarm temperature upper boundary register | 0x02 | 0x0000 |
| Alarm temperature lower boundary register | 0x03 | 0x0000 |
| Critical temperature register | 0x04 | 0x0000 |
| Temperature register | 0x05 | Undefined |

Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

Table 17: Pointer Register Bits 0–7

| Bit | | | | | | | |
|-----|---|---|---|-----------------|-----------------|-----------------|-----------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | Register select | Register select | Register select | Register select |

Table 18: Pointer Register Bits 0–2 Descriptions

| Bit | | | Register |
|-----|---|---|---|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | Capability register |
| 0 | 0 | 1 | Configuration register |
| 0 | 1 | 0 | Alarm temperature upper boundary register |
| 0 | 1 | 1 | Alarm temperature lower boundary register |
| 1 | 0 | 0 | Critical temperature register |
| 1 | 0 | 1 | Temperature register |

Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

Table 19: Capability Register (Address: 0x00)

| Bit | | | | | | | |
|-----|-----|-----|------------------------|-----|-------------|-----------|------------------------------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU |
| Bit | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RFU | RFU | RFU | Temperature resolution | | Wider range | Precision | Has alarm and critical temperature |

Table 20: Capability Register Bit Description

| Bit | Description |
|-----|--|
| 0 | Basic capability 1: Has alarm and critical trip point capabilities |
| 1 | Accuracy 0: $\pm 2^{\circ}\text{C}$ over the active range and $\pm 3^{\circ}\text{C}$ over the monitor range 1: $\pm 1^{\circ}\text{C}$ over the active range and $\pm 2^{\circ}\text{C}$ over the monitor range |
| 2 | Wider range 0: Temperatures lower than 0°C are clamped to a binary value of 0 1: Temperatures below 0°C can be read |

Table 20: Capability Register Bit Description (Continued)

| Bit | Description |
|------|--|
| 4:3 | Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB |
| 15:5 | 0: Must be set to zero |

Configuration Register

Table 21: Configuration Register (Address: 0x01)

| Bit | | | | | | | |
|-------------------|----------------|-------------|---------------------|----------------------|---------------------|----------------|---------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RFU | RFU | RFU | RFU | RFU | Hysteresis | | Shutdown mode |
| Bit | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Critical lock bit | Alarm lock bit | Clear event | Event output status | Event output control | Critical event only | Event polarity | Event mode |

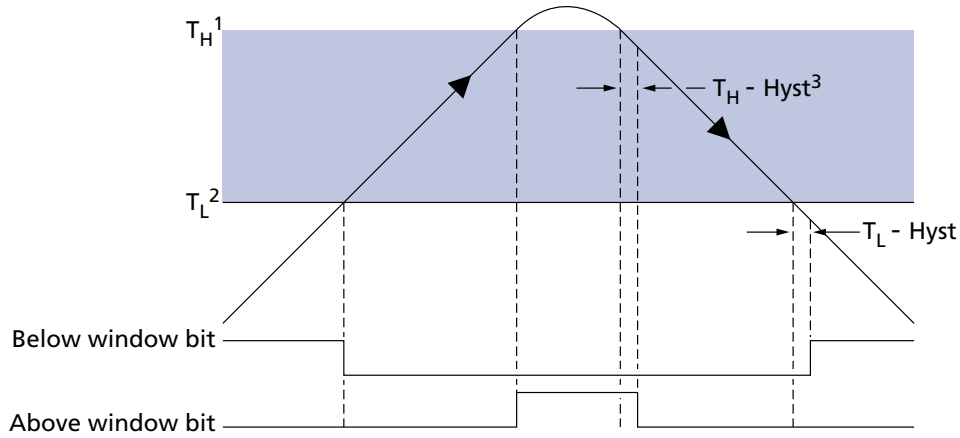
Table 22: Configuration Register Bit Descriptions

| Bit | Description | Notes |
|-----|--|--|
| 0 | Event mode 0: Comparator mode 1: Interrupt mode | Event mode cannot be changed if either of the lock bits is set. |
| 1 | EVENT# polarity 0: Active LOW 1: Active HIGH | EVENT# polarity cannot be changed if either of the lock bits is set. |
| 2 | Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached | |
| 3 | Event output control 0: Event output disabled 1: Event output enabled | |
| 4 | Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition | This is a read-only field in the register. The event causing the event can be determined from the read temperature register. |
| 5 | Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode | |

Table 22: Configuration Register Bit Descriptions (Continued)

| Bit | Description | Notes |
|------|---|---|
| 6 | Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed | |
| 7 | Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed | |
| 8 | Shutdown mode 0: Enabled 1: Shutdown | The shutdown mode is a power-saving mode that disables the temperature sensor. |
| 10:9 | Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C | When enabled, a hysteresis is applied to temperature movement around the trip points (see Figure 4 (page 21)). As an example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C. The hysteresis is applied to both the above alarm window and the below alarm window bits found in the read-only temperature register (see Table 23 (page 21)). EVENT# is also affected by this register. |

Figure 4: Hysteresis Applied to Temperature Around Trip Points



- Notes: 1. T_H is the value set in the alarm temperature upper boundary trip register.
 2. T_L is the value set in the alarm temperature lower boundary trip register.
 3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 23: Hysteresis Applied to Alarm Window Bits in the Temperature Register

| Condition | Below Alarm Window Bit | | Above Alarm Window Bit | |
|-----------|------------------------|----------------------|------------------------|----------------------|
| | Temperature Gradient | Critical Temperature | Temperature Gradient | Critical Temperature |
| Sets | Falling | $T_L - \text{Hyst}$ | Rising | T_H |
| Clears | Rising | T_L | Falling | $T_H - \text{Hyst}$ |

Temperature Format

The temperature trip point registers and temperature readout register use a 2's complement format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C, depending on which register is referenced. For example, assuming an LSB of 0.0625°C:

- A value of 0x018C would equal 24.75°C
- A value of 0x06C0 would equal 108°C
- A value of 0x1E74 would equal -24.75°C

Temperature Trip Point Registers

The upper and lower temperature boundary registers are used to set the maximum and minimum values of the alarm window. LSB for these registers is 0.25°C. All RFU bits in the register will always report zero.

Table 24: Alarm Temperature Lower Boundary Register (Address: 0x02)

| Bit | | | | | | | | | | | | | | | |
|---|----|----|-----|----|----|---|---|---|---|---|---|---|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | MSB | | | | | | | | | | LSB | RFU | RFU |
| Alarm window upper boundary temperature | | | | | | | | | | | | | | | |

Table 25: Alarm Temperature Lower Boundary Register (Address: 0x03)

| Bit | | | | | | | | | | | | | | | |
|---|----|----|-----|----|----|---|---|---|---|---|---|---|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | MSB | | | | | | | | | | LSB | RFU | RFU |
| Alarm window lower boundary temperature | | | | | | | | | | | | | | | |

Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 26: Critical Temperature Register (Address: 0x04)

| Bit | | | | | | | | | | | | | | | |
|---------------------------------|----|----|-----|----|----|---|---|---|---|---|---|---|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | MSB | | | | | | | | | | LSB | RFU | RFU |
| Critical temperature trip point | | | | | | | | | | | | | | | |

Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.



Table 27: Temperature Register (Address: 0x05)

| Bit | | | | | | | | | | | | | | | |
|---------------------|--------------------|--------------------|-----|-------------|----|---|---|---|---|---|---|---|---|---|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Above critical trip | Above alarm window | Below alarm window | MSB | Temperature | | | | | | | | | | | LSB |

Table 28: Temperature Register Bit Descriptions

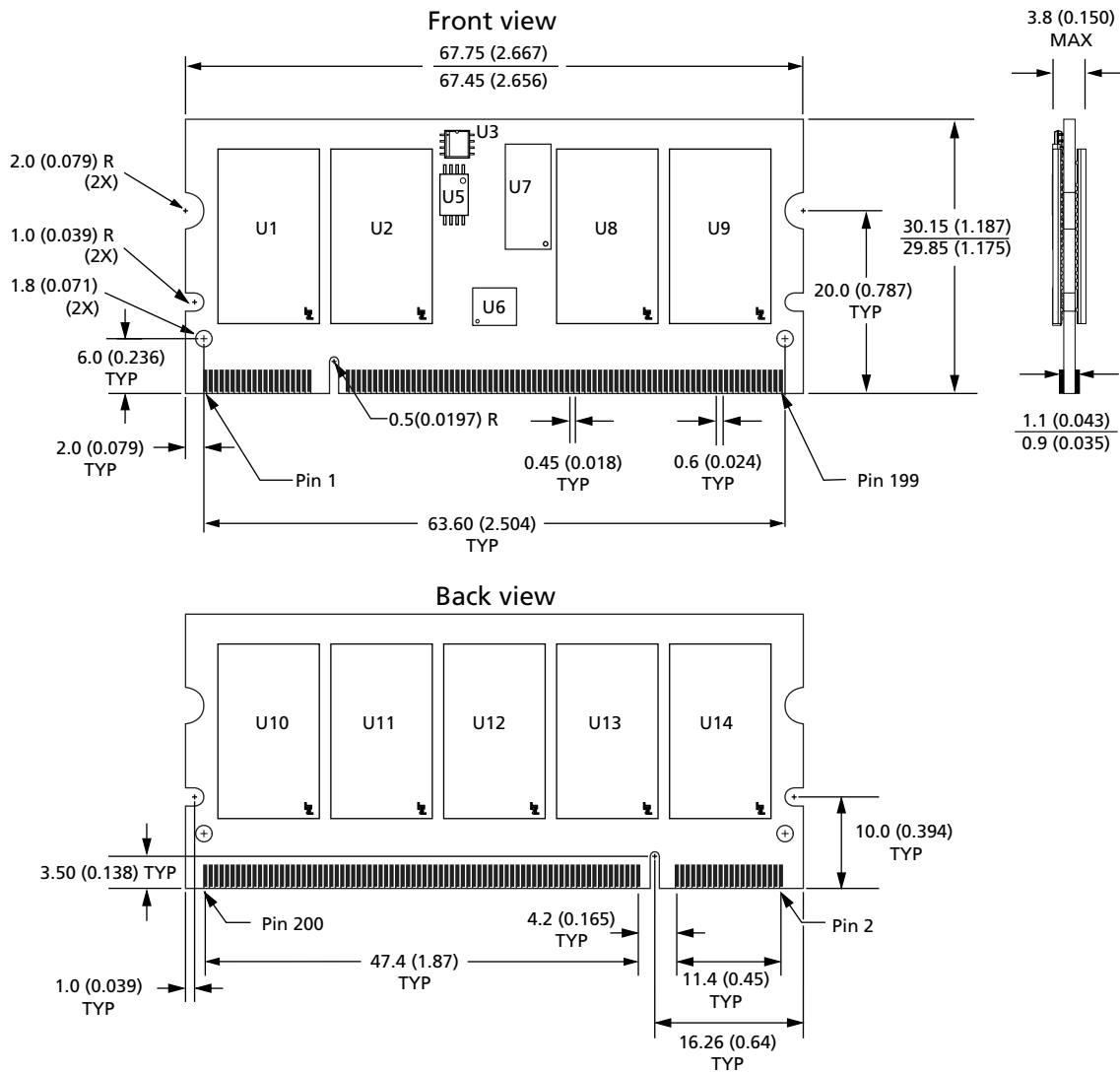
| Bit | Description |
|-----|---|
| 13 | Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window |
| 14 | Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window |
| 15 | Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point |

Serial Presence-Detect Data

For the latest SPD, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 5: 200-Pin DDR2 SORDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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