Intel® IXP28XX Network Processors

Hardware Design Guide

August 2005

Order Number: 309192-002US

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Revision History

Date	Revision	Description
August 2005	002	Updates to Chapter 4 QDR SRAM.
December 2004	001	Initial release

Introduction 1

The purpose of this manual is to accelerate the development of Intel® IXP28XX Network Processor hardware designs. The manual provides the hardware developer general design guidelines and includes specific design implementations used on the IXDP2800 Advanced Development Platform.

These guidelines have been developed to ensure maximum flexibility for board designers and to reduce board-related problems. The design information in this document is in two categories:

- **Design Recommendations**, based on Intel's simulations and lab debugging experience to date, and are strongly recommended (or necessary) to meet timing and signal quality specifications.
- **Design Considerations** or suggestions, based on the development platforms designed by Intel. They should be used as examples, but may not be applicable to particular designs.

Note: The guidelines recommended in this document are based on simulation work completed by Intel. This work is ongoing, and recommendations are subject to change.

Note: General information regarding certain artwork in this document. Due to differences in output devices, some figures may display inconsistently. For example, viewing a figure on a computer screen and producing hardcopy to a printer can result in the screen providing finer resolution than the printer.

1.1 System Overview

The IXP28XX network processors enable fast deployment of complete content processing by providing unlimited programming flexibility, code re-use, and high-performance processing. These network processors support a wide variety of WAN and LAN applications that require a broad range of speeds, currently ranging from OC-3 through OC-192. High performance and scalability is achieved through an innovative Microengine architecture that includes a multi-threaded distribution cache architecture that enables pipeline features in software.

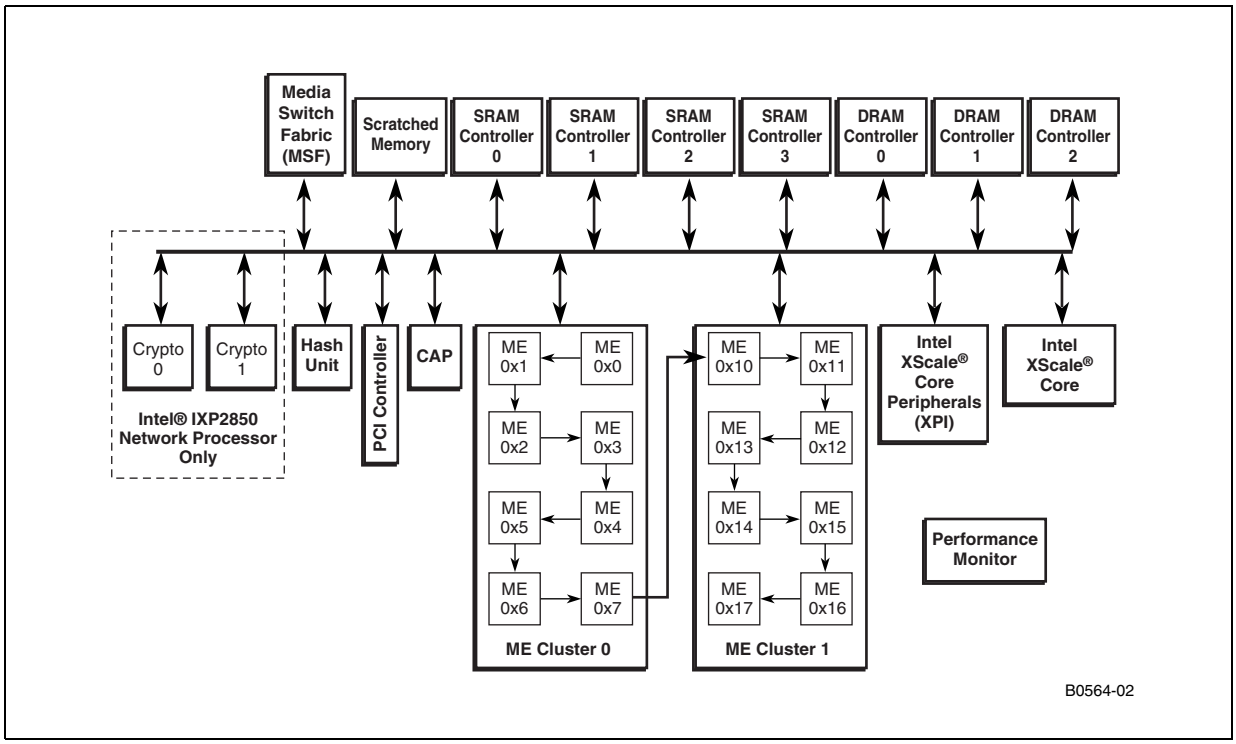
In addition to the standard feature set available with the Intel® IXP2800 Network Processor, the Intel® IXP2850 Network Processor integrates functionality for secure network traffic at 10 Gbytes/sec. This enables the up-front design of secure network equipment and results in lower power consumption and more efficient use of space on the printed circuit board.

Table 1 summarizes the product features. Figure 1 provides a functional overview of the Intel® IXP2800 Network Processor and Intel® IXP2850 Network Processor internal hardware, showing the major internal blocks.

Table 1. Product Features of IXP28XX Network Processors

Feature	Description
Sixteen integrated Microengines (Version 2)	• Operating frequency of up to 1.4 GHz • Configurable to four or eight threads per Microengine • 640 Dwords of local memory per Microengine • Sixteen-entry CAM per Microengine, with single cycle lookup • Next Neighbor bus accessing adjacent Microengines • CRC unit per Microengine • 8K instructions control store per Microengine • Support for Generalized Thread Signaling
Integrated Intel XScale® core	• Operating frequency of up to 700 MHz • High performance, low power 32-bit embedded RISC processor • 32-Kbyte instruction cache • 32-Kbyte data cache
Two integrated Cryptographic units (Intel® IXP2850 Network Processor only)	• Operating frequency of 700 MHz • Support for DES, 3DES, AES, and SHA-1 algorithms • Support for AES 128-, 192-, and 256-bit keys
Three industry-standard RDRAM interfaces	• Peak bandwidth of 2.1 Gbytes/sec • 800-MHz and 1066-MHz RDRAM • Error Correction Code (ECC) • Addressable from Intel XScale® core, Microengines, and PCI
Four industry-standard 32-bit QDR SRAM interfaces	• Peak bandwidth of 1.9 Gbytes/sec per channel • 233-MHz SRAM • Hardware support for Linked List and Ring operations • Atomic bit operations • Atomic arithmetic support • Addressable from Intel XScale® core, Microengines, and PCI
Integrated Media Switch Fabric interface	• Two unidirectional 16-bit Low-Voltage Differential Signaling (LVDS) data interfaces • Up to 500 MHz per channel • Separately configurable for either SPI-4 or CSIX protocols
Industry-standard PCI Bus	• *PCI Local Bus Specification, Version 2.2** interface for 64-bit, 66-MHz I/O
Additional integrated features	• Hardware Hash Unit (48-, 64-, and 128-bit) • 16-KByte Scratchpad Memory • Serial UART port for debug • Eight general-purpose I/O pins • Four 32-bit timers
1356 Ball FCBGA package	• Dimensions of 37.5mm x 37.5mm • 1 mm solder ball pitch

Figure 1. IXP2800/IXP2850 Network Processor Functional Block Diagram



1.2 In This Guide

This document comprises the following chapters and appendixes that describe the IXP28XX network processor:

- Chapter 2, “Power Ratings and Requirements,” describes the minimum and maximum operating voltages and temperatures.
- Chapter 3, “RDRAM,” describes the IXP28XX network processor’s Rambus* DRAM implementation.
- Chapter 4, “QDR SRAM,” describes the IXP28XX network processor’s four independent SRAM controllers, each of which supports pipelined QDR synchronous static RAM (SRAM).
- Chapter 5, “MSF (SPI-4/CSIX/FC),” describes the Media and Switch Fabric (MSF) interface.
- Chapter 6, “PCI,” describes the use of the PCI controller to provide a 64-bit, 66-MHz-capable *PCI Local Bus Specification, Version 2.2** interface for the IXP28XX network processor.
- Chapter 7, “Slowport,” describes the Slowport external interface to the IXP28XX network processor.
- Chapter 8, “Mechanical/Packaging,” describes the dimensions of the IXP28XX network processor and package markings for the processor chip.

1.2.1 Typographical Conventions

This guide contains the following text and typography conventions:

Table 2. Guide Conventions

Convention	Description
Italics	New terms and titles of documents or help systems appear in italics.
bold	Special text for labels of items appears in bold type.
`monospace`	Code and names of drives, pathnames, directories, and filenames appear in Courier monospace type.
`monospace bold`	Example commands given to show user input.
table of contents table of figures table of tables	Each item in the tables of contents, figures, and tables is a hyperlink.
>	Indicates the sequential choice of menu items. For example, the menu items for the Developers Workbench are **Start > IXA SDK 4.1 > DevWorkbench**.

1.2.2 Acronyms and Terminology

Table 3 defines the acronyms and terminology that are used throughout this document.

Table 3. Acronyms and Terminology (Sheet 1 of 3)

Acronym/Terminology	Definition
AES	Advanced Encryption Standard
ATM	Asynchronous Transfer Mode
BGA	ball grid array
BWE	Byte Write Enable, a type of control signal that is active low
CFM	Clock-to-Master, positive polarity
CFMN	Clock-to-Master, negative polarity
Clamshelling	Locating two devices on opposite sides of the printed circuit board
cPCI	Compact PCI, a 32- or 64-bit bus, operating at either 33 or 66 MHz
CPIX	Common Programming Interface Forum
CSIX	Common Switch Interface
CPLD	Complex Programmable Logic Device
CSR	Control Status Register
CTM	Clock-to-Master, positive polarity
CTMN	Clock-to-Master, negative polarity
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Dynamic Link Library
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory

Table 3. Acronyms and Terminology (Sheet 2 of 3)

Acronym/Terminology	Definition
DRCG	Direct Rambus* Clock Generator
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-only Memory
LVDS	Low-Voltage Differential Signaling
MAC	Medium Access Control, a 48-bit number unique to each LAN network interface card (NIC)
MSF	Media Switch Fabric
NA	Not applicable
NIC	Network Interface Card
NPF	Network Processor Forum; organized to facilitate the development of next-generation networking and telecommunications products based on network processing technologies
OIF	Optical Internetworking Forum
PCB	Printed circuit board
PCI	Peripheral Component Interconnect
PHY	physical layer device
PGA	pin grid array
PLL	Phase Lock Loop
POS	Packet over SONET
PPCI	Primary PCI, a 64-bit PCI bus operating at 33 or 66 MHz. This bus connects the ingress and egress IXP28XX network processor to the master and slave PCI-PCI bridge chips.
PVT	Process/Voltage/Temperature
QDR SRAM	Quad Data Rate Static Random Access Memory
RDRAM	Rambus* Dynamic Random Access Memory
RIMM*	Rambus* In-line Memory Module used with RDRAM chips developed by Rambus, Inc.
RPE	Read Port Enable, a type of control signal that is active low
RSL	Rambus* Signaling Level
SDH	Synchronous Digital Hierarchy, a set of international fiber optic transmission standards
SF	Switch Fabric
SHA-1	Secure Hash Algorithm 1
SPCI	Secondary PCI, a 32-bit bus operating at 33 MHz
SPI-4	Interface for packet and cell transfer between a physical layer (PHY) device and a link layer device (the IXP28XX network processor), for aggregate bandwidths of OC-192 ATM and Packet over SONET/SDH (POS), as well as 10 Gb/s Ethernet applications.
Striping	Hardware interleaving of addresses to provide balanced access to all populated channels; the interleave size is 128 bytes. Interleaving helps to maintain utilization of available bandwidth by spreading consecutive accesses to multiple channels. The interleaving is done in the hardware so that the three channels appear to software as a single contiguous memory space.

Table 3. Acronyms and Terminology (Sheet 3 of 3)

Acronym/Terminology	Definition
TCAM	Ternary Content Addressable Memory
TM	Traffic Manager
UART	Universal Asynchronous Receiver-Transmitter
VOQ	Virtual output queue
VRM	Voltage Regulator Module
WPE	Write Port Enable, a type of control signal that is active low

1.3 Related Documentation

Refer to the following documents or models for more information. All Intel-issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel. Contact your field representative for information on obtaining Intel-issued documentation.

- *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*
- *Intel® IXP2800 and Intel® IXP2850 Network Processors Datasheet*
- *Intel® IXP2800 Network Processor Hardware Reference Manual*
- *Intel® IXP2800 Network Processor Hardware Initialization Reference Manual*
- *Intel® IXP2800 and Intel® IXP2850 Network Processors Interfacing Devices to the Slowport Application Note*
- *Intel® IXP2800 Network Processor Electrical, Mechanical, and Thermal Specification (EMTS) Application Note*
- *Intel® IXP2800 Network Processor IBIS Model*
- *Intel® IXP2800 Network Processor BSDL File*
- *PCI Local Bus Specification, Version 2.2**

1.4 Contacting Intel®

Networking and Communications Building Blocks Site	http://www.intel.com/design/network
Intel Internet Exchange Architecture Site	http://www.intel.com/IXA
Other Intel Support	http://developer.intel.com/design/litcentr
Intel Literature Center	(800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
General Information Hotline	(800) 628-8686 or (916) 356-3104 5 a.m. to 5 p.m. PST

Power Ratings and Requirements 2

The following sections describe power ratings and requirements for the Intel® IXP2800 and Intel® IXP2850 Network Processors.

2.1 Power Ratings

Operation beyond the functional operating temperature range (see Table 5) is not recommended and extended exposure beyond this range may affect reliability. Table 7 and Table 8 list the functional operating voltage ranges; Table 9 through Table 11 provide example power values.

Note: Under all operating conditions, the 3.3 V – 1.35/1.3/1.2 V and 3.3 V – 2.5 V supply voltage difference (V_{DELTA}) must *not* be exceeded; otherwise, permanent damage to the device may result. Also, the Core/PLL supply voltage must never be less than 1.1 V (see Table 4).

Table 4. Absolute Maximum/Minimum Ratings Table

Parameter	Minimum	Maximum	Comment
Junction Temp Tj (Commercial)	—	120° C	
Junction Temp Tj (Extended)	—	120° C	
Storage Temperature Range	-55° C	125° C	
Supply Voltage Difference V_{DELTA}	—	2.7 V	• 3.3 V to 2.5 V rail difference • 3.3 V to 1.35/1.3/1.2 V rail difference
V_{CORE} (1.35/1.3 V) Minimum Operating Voltage	1.1 V	—	
V_{CORE} (1.2 V) Minimum Operating Voltage	1.1 V	—	
Maximum power-up time	—	700 ms	It is expected that all supplies will be up and stable within 700 milliseconds.

Table 5. Functional Operating Temperature Range

Parameter	Minimum	Maximum	Comment
Commercial temperature operating range	0° C	70° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.
Extended temperature operating range	-40° C	85° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.
Maximum Junction Temperature (Extended)	—	120° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.
Maximum Junction Temperature (Commercial)	—	120° C	Refer to the *Intel® IXP2800 Network Processor Thermal/Mechanical Design Guideline Application Note*.

Table 6. Typical and Maximum Power[1]

Device[2]	Typical	Maximum	Frequency
IXP2800 - B*n*[3]	25.5 W	31.5 W	1.4 GHz
IXP2800 - B*n*	18.5 W	23 W	1.0 GHz
IXP2800 - B*n*	12.5 W	16 W	650 MHz
IXP2850 - B*n*	27.5 W	34 W	1.4 GHz
IXP2850 - B*n*	20.5 W	25 W	1.0 GHz
IXP2850 - B*n*	14 W	17.5 W	650 MHz

1. The maximum power parameters represent the worst-case power consumption as measured by running the Intel packet over SONET (POS) reference design processing minimum-size packets (49 bytes) running at full OC-192 line rate.
2. Total power.
3. B*n* refers to B0 and B1.

Table 7. Functional Operating Voltage Range – 1.4/1.0 GHz

Interface	Supply Name	Description	Voltage (V)	Tolerance (+/-%)	Notes 1,2,3,4,5
Core	VCC VSS	Core power supply Core ground	1.3 V GND	5% N/A	3
Clock/PLL	VCC_PLL VSS VCC_CLK VREFHI_CLK VREFLO_CLK	PLL power PLL ground Ref. Clock power (also for GPIO) Clock reference voltage Clock reference voltage	1.3 V GND 2.50 V 1.40 V 1.00 V	5% N/A 5% 5% 5%	1,3
SPI-4/CSIX/FLOW	VCC25V VCCA_FC VCCA_SPI4 VREFHI VREFLO	SPI-4 supply (also for PCI) DLL power DLL power SPI-4/flow reference voltage SPI-4/flow reference voltage	2.50 V 1.3 V 1.3 V 1.40 V 1.00 V	5% 5% 5% 5% 5%	1 1 4 4
GPIO	VCC33	GPIO, JTAG, SP power	3.30 V	5%	
PCI	VCC33_PCI	PCI power supply	3.30 V	5%	5
QDR	VDDQ PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	QRD power supply DLL power DLL power DLL power DLL power QDR reference voltage QDR reference voltage QDR reference voltage QDR reference voltage	1.50 V 1.3 V 1.3 V 1.3 V 1.3 V 0.75 V 0.75 V 0.75 V 0.75 V	1.4 V to 1.6 V 5% 5% 5% 5% 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V	 1 1 1 1 2 2 2 2
RDR	VCCR VCCRA VCCRIO PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	RDRAM core processor RDRAM clean power RDRAM I/O power RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage	1.3 V 1.3 V 1.80 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V	5% 5% 1.7 V to 1.9 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V	1
FUSE	VCC_FUSE	Fuse power supply	1.3 V	5%	

1. These supplies can be derived from core Vcc, but should be filtered appropriately.
2. QDR references should be derived from Vddq so that they track fluctuations in Vddq.
3. During power-up, after NRESET is de-asserted, the device will experience an increase in current consumption after the PLL locks and the system clocks begin to operate at full speed. During this time a droop on the core power supply may occur due to this increase in current consumption. It is acceptable that the core power supply droop a maximum of 100 mV to a minimum of 1.2 V during this time. It is expected that the device be Idle during this time and that no instructions be executing until the power is within the 5% regulation specification. The behavior is undefined if instructions are executed while the power is not within the 5% regulation specification.
4. SPI-4 reference should be derived from VCC25V so that they track fluctuations in VCC25V.
5. The tolerance on the PCI supply is tighter than specified in the *PCI Local Bus Specification, Version 2.2**.

Table 8. Functional Operating Voltage Range – 650 MHz

Interface	Supply Name	Description	Voltage (V)	Tolerance (+/-%)	Notes 1,2,3,4
Core	VCC VSS	Core power supply Core ground	1.2 V GND	5% N/A	
Clock/PLL	VCC_PLL VSS VCC_CLK VREFHI_CLK VREFLO_CLK	PLL power PLL ground Ref. Clock power (also for GPIO) Clock reference voltage Clock reference voltage	1.2 V GND 2.50 V 1.40 V 1.00 V	5% N/A 5% 5% 5%	1
SPI-4/CSIX/FLOW	VCC25V VCCA_FC VCCA_SPI4 VREFHI VREFLO	SPI-4 supply (also for PCI) DLL power DLL power SPI-4/flow reference voltage SPI-4/flow reference voltage	2.50 V 1.2 V 1.2 V 1.40 V 1.00 V	5% 5% 5% 5% 5%	1 1 3 3
GPIO	VCC33	GPIO, JTAG, SP power	3.30 V	5%	
PCI	VCC33_PCI	PCI power supply	3.30 V	5%	4
QDR	VDDQ PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	QRD power supply DLL power DLL power DLL power DLL power QDR reference voltage QDR reference voltage QDR reference voltage QDR reference voltage	1.50 V 1.2 V 1.2 V 1.2 V 1.2 V 0.75 V 0.75 V 0.75 V 0.75 V	1.4 V to 1.6 V 5% 5% 5% 5% 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V 0.7 V to 0.85 V	 1 1 1 1 2 2 2 2
RDR	VCCR VCCRA VCCRIO PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	RDRAM core processor RDRAM clean power RDRAM I/O power RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage RDRAM reference voltage	1.2 V 1.2 V 1.80 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V 1.40 V	5% 5% 1.7 V to 1.9 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V 1.2 V to 1.6 V	1
FUSE	VCC_FUSE	Fuse power supply	1.2 V	5%	

1. These supplies can be derived from core Vcc, but should be filtered appropriately.
2. QDR references should be derived from Vddq so that they track fluctuations in Vddq.
3. SPI-4 reference should be derived from VCC25V so that they track fluctuations in VCC25V.
4. The tolerance on the PCI supply is tighter than specified in the *PCI Local Bus Specification, Version 2.2**.

Table 9. Example Power by Supply – 1.4 GHz

Type	Group	Names	Max Power[1]	
			IXP2800	IXP2850
Power Supplies	1.3 V logic	VCC VCCR VCCRA VCC_FUSE	25.5 W	28.0 W
	1.3 V PLL/DLL	VCC_PLL VCCA_FC VCCA_SPI4 PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA	1.0 W	1.0 W
	1.50 V	VDDQ	2.0 W	2.0 W
	1.80 V	VCCRIO	0.5 W	0.5 W
	2.5 V	VCC_CLK VCC25V	1.8 W	1.8 W
	3.3 V	VCC33 VCC33_PCI	0.7 W	0.7 W
Voltage References	0.75	VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	< 0.01 W	< 0.01 W
	1.0 V	VREFLO_CLK VREF_LO	< 0.01 W	< 0.01 W
	1.4 V	VREFHI_CLK VREFHI PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	< 0.01 W	< 0.01 W

1. Power specified is in the total for all the supplies/references in each group.

Table 10. Example Power by Supply – 1.0 GHz

Type	Group	Names	Max Power[1]	
			IXP2800	IXP2850
Power Supplies	1.3 V logic	VCC VCCR VCCRA VCC_FUSE	17.0 W	19.0 W
	1.3 V PLL/DLL	VCC_PLL VCCA_FC VCCA_SPI4 PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA	1.0 W	1.0 W
	1.50 V	VDDQ	2.0 W	2.0 W
	1.80 V	VCCRIO	0.5 W	0.5 W
	2.5 V	VCC_CLK VCC25V	1.8 W	1.8 W
	3.3 V	VCC33 VCC33_PCI	0.7 W	0.7 W
Voltage References	0.75 V	VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	< 0.01 W	< 0.01 W
	1.0 V	VREFLO_CLK VREF_LO	< 0.01 W	< 0.01 W
	1.4 V	VREFHI_CLK VREFHI PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	< 0.01 W	< 0.01 W

1. Power specified is in the total for all the supplies/references in each group.

Table 11. Example Power by Supply – 650 MHz

Type	Group	Names	Max Power[1]	
			IXP2800	IXP2850
Power Supplies	1.2 V logic	VCC VCCR VCCRA VCC_FUSE	10.4 W	11.8 W
	1.2 V PLL/DLL	VCC_PLL VCCA_FC VCCA_SPI4 PAS0_VCCA PAS1_VCCA PAS2_VCCA PAS3_VCCA	1.0 W	1.0 W
	1.50 V	VDDQ	1.9 W	1.9 W
	1.80 V	VCCRIO	0.4 W	0.4 W
	2.5 V	VCC_CLK VCC25V	1.7 W	1.7 W
	3.3 V	VCC33 VCC33_PCI	0.7 W	0.7 W
Voltage References	0.75 V	VREF_QDR0 VREF_QDR1 VREF_QDR2 VREF_QDR3	< 0.01 W	< 0.01 W
	1.0 V	VREFLO_CLK VREF_LO	< 0.01 W	< 0.01 W
	1.4 V	VREFHI_CLK VREFHI PAR0_PADVREFA PAR0_PADVREFB PAR1_PADVREFA PAR1_PADVREFB PAR2_PADVREFA PAR2_PADVREFB	< 0.01 W	< 0.01 W

1. Power specified is in the total for all the supplies/references in each group.

2.2 Supply Voltage Power-up Sequence

Caution: The IXP28XX network processors each have a prescribed supply voltage bring-up sequence that must be followed, or permanent damage to the device may result. This section provides the bring-up sequence for 1.4 /1.0 GHz devices (Section 2.2.1) and 650 MHz devices (Section 2.2.2).

2.2.1 Sequence for 1.4 / 1.0 GHz Devices

The sequence for the 1.4 / 1.0 GHz B-stepping devices is as follows:

1. The 2.5 V supply must come up before the 1.3 V supply.
2. The 1.3 V supply must come up after the 2.5 V supply and must not start to ramp until the 2.5-V supply has exceeded 1 V.
3. The 3.3 V supply must come up only after the 2.5 V and 1.3 V supplies are up and stable.

It is expected that all supplies will be up and stable within the maximum power-up time requirement of 700 ms. Additionally, the maximum time from when the 2.5 V supply is up and stable to when the 1.3 V supply begins to ramp should not exceed 200 ms.

Note: The 1.8 V and 1.5 V supplies can come up in any order before or after the 2.5 V, 1.3 V, and 3.3 V supplies.

Note: No 3.3 V devices should drive any of the IXP2800/IXP2850 pins until its 3.3 V supply is up and stable.

2.2.2 Sequence for 650 MHz Devices

The sequence for the 650 MHz B-stepping devices is as follows:

1. The 2.5 V supply must come up before the 1.2 V supply.
2. The 1.2 V supply must come up after the 2.5 V supply and must not start to ramp until the 2.5 V supply has exceeded 1 V.
3. The 3.3 V supply should begin to ramp after the 2.5 V and 1.2 V supplies are up and stable.

   It is acceptable to ramp the 1.2 V and 3.3 V supplies together as long as the two supplies rise linearly together and do not deviate by more than 10% of the nominal ramp rate until both supplies reach their respective final voltage levels.

It is expected that all supplies will be up and stable within the maximum power-up time requirement of 700 ms. Additionally, the maximum time from when the 2.5 V supply is up and stable to when the 1.2 V supply begins to ramp should not exceed 200 ms.

Note: The 1.8 V and 1.5 V supplies can come up in any order before or after the 2.5 V, 1.2 V, and 3.3 V supplies.

Note: No 3.3 V devices should drive any of the IXP2800/IXP2850 pins until its 3.3 V supply is up and stable.

2.2.3 Power Supply Regulation

2.2.3.1 Power-Up Power Supply Regulation

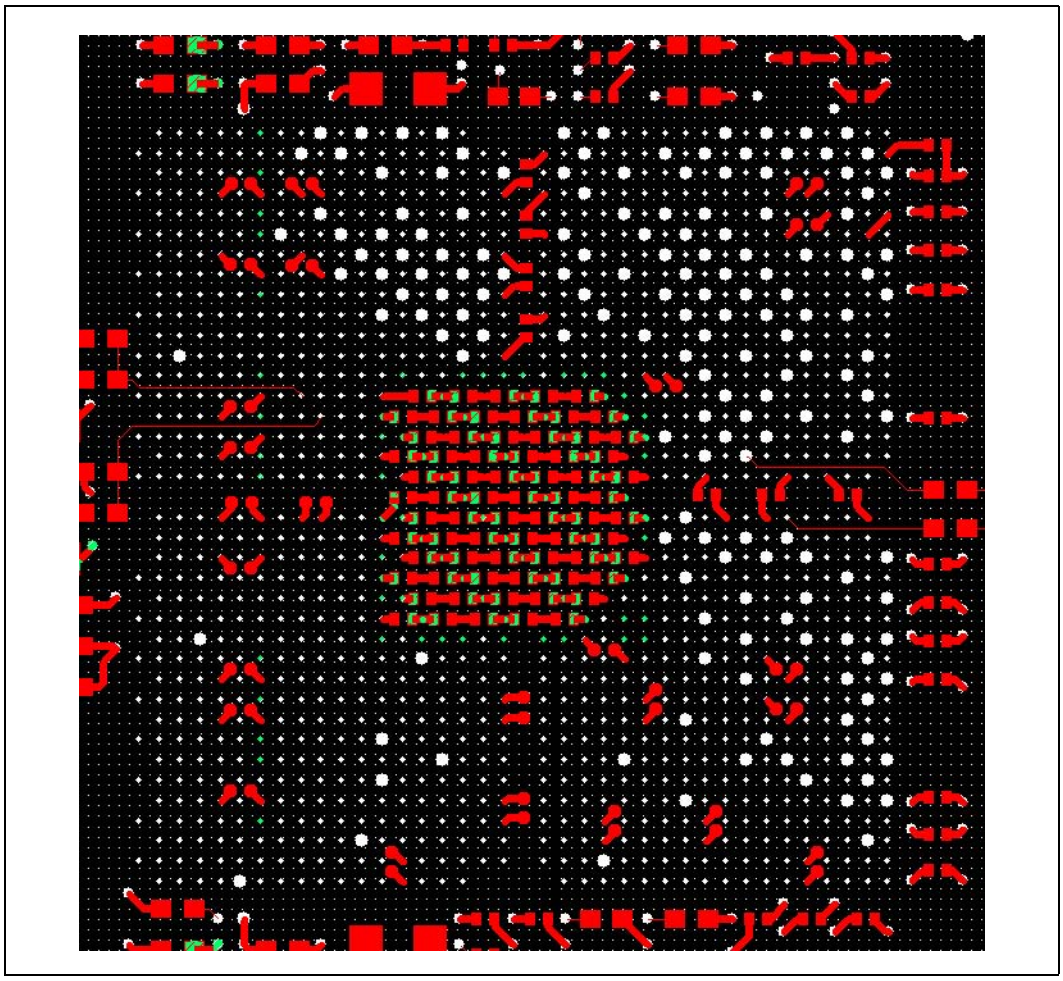
During power-up, after NRESET is de-asserted, the device will experience an increase in current consumption after the PLL locks and the system clocks begin to operate at full speed. During this time, a droop on the core power supply may occur due to this increase in current consumption. It is acceptable that the core power supply droop a maximum of 100 mV to a minimum of 1.2 V during this time. It is expected that the device is Idle during this time and that no instructions are executing until the power is within the 5% regulation specification. The behavior is undefined if instructions are executed while the power is not within the 5% regulation specification.

2.2.3.2 Power Supply Decoupling

To maintain supply regulation during power-up and during normal operation sufficient de-coupling, mid-frequency and bulk capacitors should be used to account for transient power steps. The number and size of decoupling capacitors required for a particular implementation depends on the board stack-up and power-delivery circuitry, so a single solution will not work for all implementations. Note that the worst case transient occurs when the device comes out of reset as explained in Section 2.2.3.1. The IXDP2800 decoupling design implements a via-sharing mechanism that maximizes the number of decoupling capacitors that can be accommodated under the device while minimizing the number of vias. This reduces the amount of holes in the power and ground planes. The decoupling layout from the IXDP2800 Advanced Development System is shown in Figure 2.

The IXDP2800 development platform uses 63 0.22 uF 0402 AVX* capacitors for the core supply decoupling. A 1uF 0402 capacitor is now available from AVX* which can be substituted for the 0.22 uF capacitor. This will provide better regulation stability during the power-on transient event. Refer to Section 2.5 for details of the power-on transient event.

Figure 2. IXDP2800 Decoupling Implementation

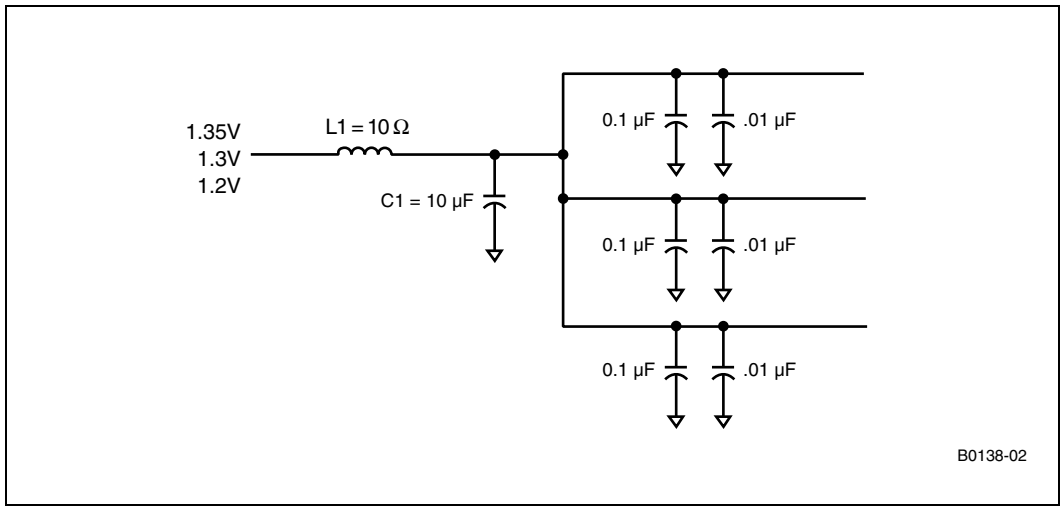


2.3 LC Filter Network

Figure 3 shows an example of an LC filter design that can be used to derive the power for the analog and DLL power supplies for the IXP2800 or IXP2850 network processor. For L1, a 10-Ω ferrite bead with a DCR of less than 0.1 Ω should be used. For C1, a 10 µF capacitor should be used and each analog V_{CC} pin should be decoupled with a 0.1 µF and a 0.01 µF capacitor.

The IXDP2800 Advanced Development Platform uses analog power for all PLL/DL pins.

Figure 3. LC Filter Network



2.4 IXDP2800 Advanced Development Platform Power Supply Subsystem

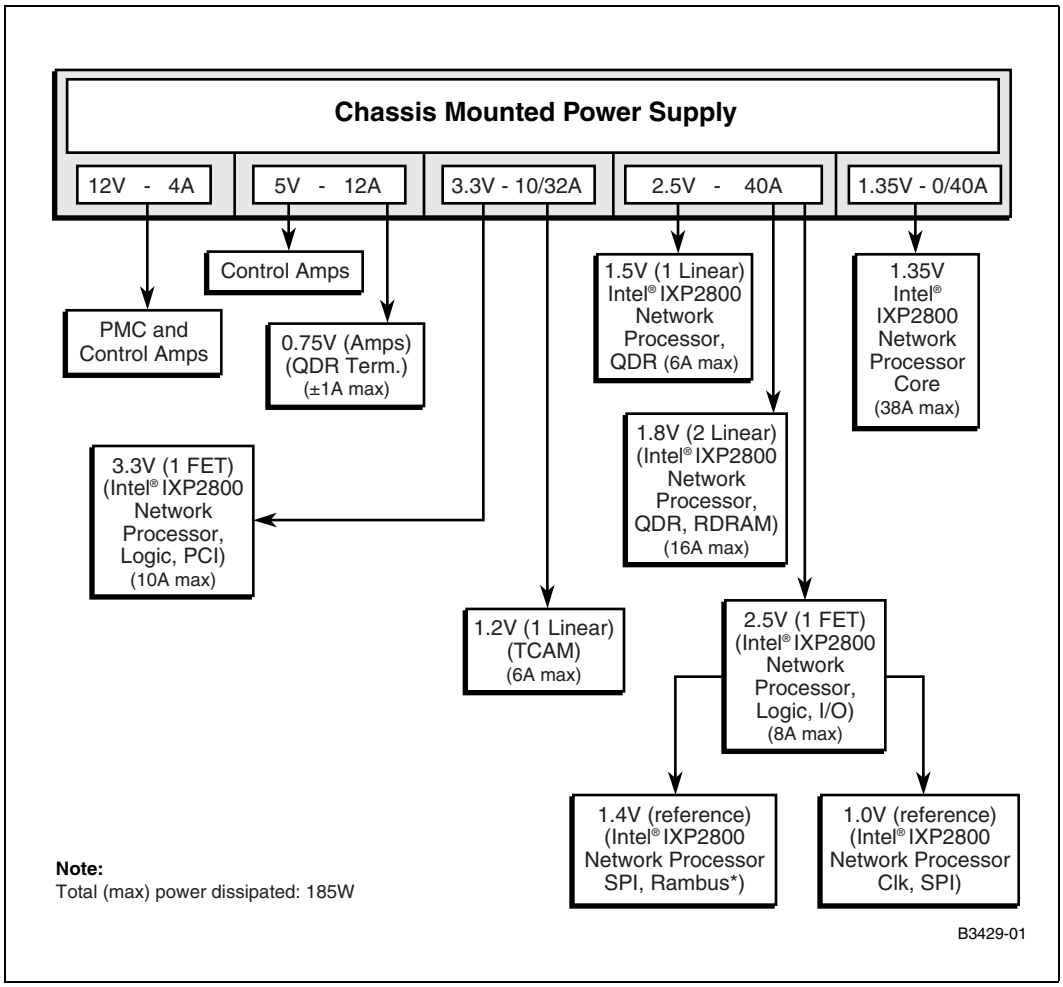
In the following sections, the IXDP2800 Advanced Development Platform power supply subsystem is described with a block diagram and a power-up sequence:

- Section 2.4.1, “Subsystem Block Diagram”
- Section 2.4.2, “Power-up Sequence”

2.4.1 Subsystem Block Diagram

Figure 2 is a block diagram for the IXDP2800 Advanced Development Platform power supply subsystem.

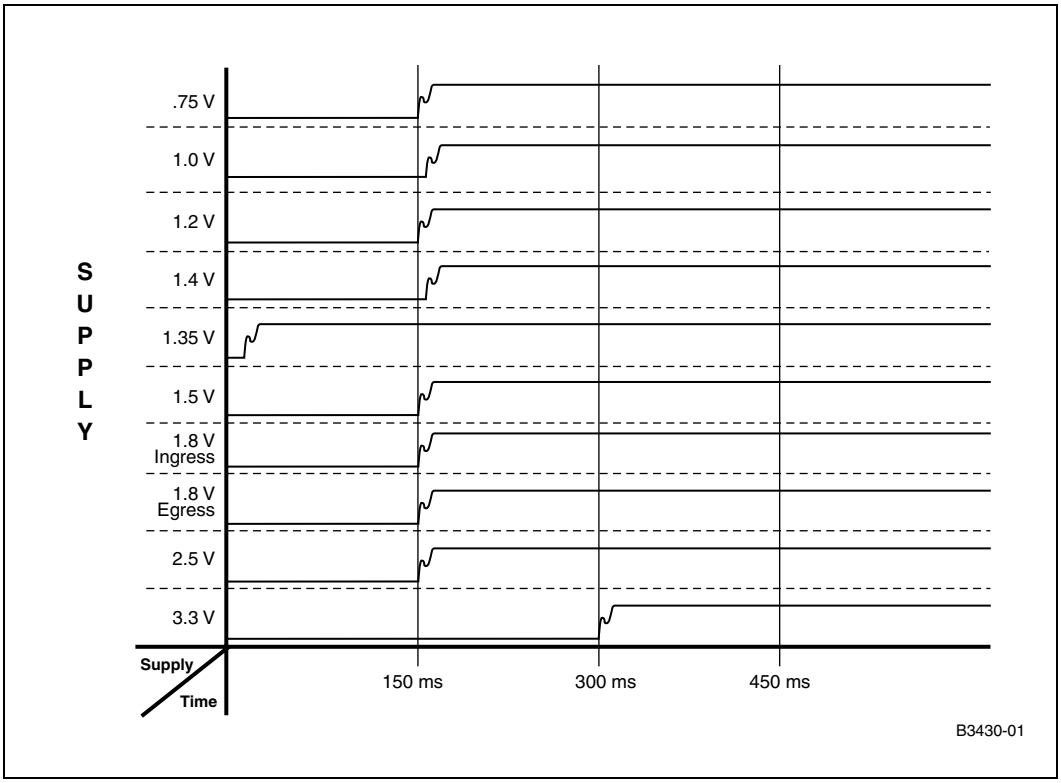
Figure 4. IXDP2800 Advanced Development Platform Power Supply Subsystem



2.4.2 Power-up Sequence

Figure 5 illustrates the power-up sequence for the IXDP2800 Advanced Development Platform power supply.

Figure 5. IXDP2800 Advanced Development Platform Power-up Sequence

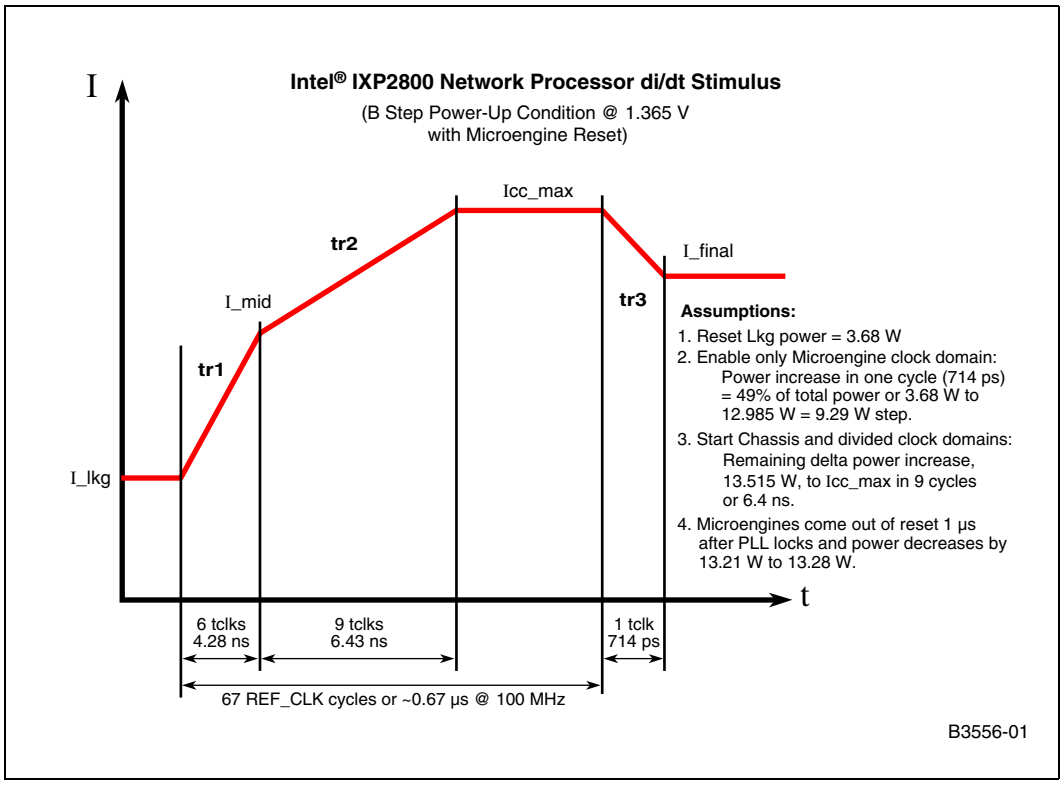


2.5 IXP28XX Network Processor Power-On di/dt Profiles

Figure 6 illustrates IXP28XX network processor worst case power-up di/dt stimulus. The characteristics of this transient event are as follows:

- Reset leakage power is 3.68 W (2.7 A at 1.365 V).
- Maximum power is 26.5 W.
- After PLL locks the Microengine (1.4/1.0 GHz) the clock starts in 6 cycles as follows:
  - Power ramps from leakage to approximately 49% of maximum power, or 12.985 W.
  - The di/dt slope for step tr1 (see Figure 6) represents a 9.29-W step (i.e., the transient step) over 6 cycles at a 1.4-GHz clock rate (1592 A per µs at VDD_{MAX}).
- Remaining clocks are started over 9 cycles as follows:
  - Power ramps remaining rise to maximum power.
  - The di/dt slope for step tr2 (see Figure 6) represents a 13.515-W step (i.e., the transient step) over 9 cycles at a 1.4-GHz clock rate (1540 A per µs at VDD_{MAX}).
- Power decreases by 13.21 W to 13.28 W, approximately 67 REF_CLK cycles after PLL locks in one cycle
  - Sensitivity analysis shows that a duration of tr2 (see Figure 6) does not affect the first, second, or third droop.

Figure 6. IXP28XX Network Processor di/dt Stimulus



2.5.1 di/dt Droop Analysis Results

An exhaustive droop analysis was performed using an Intel system validation platform. The goal of analysis was to correlate the measured power-on di/dt with the theoretical design values. A detailed model of the system board, power delivery circuit and package were developed and simulated using the theoretical di/dt transient events to predict the voltage droop measured at the pins of the device. Several correlation analysis were performed to ensure the integrity of the models. Once the models were validated the simulation results were compared with measured results from the system validation platform. The final step of the analysis was to perform a sensitivity analysis by varying the di/dt stimulus to match the simulated results to the measured results.

The outcome of the analysis is the transient curve shown Figure 6. The following items summarize the findings of the correlation study:

- The First Droop magnitude is 34 mV (tr1 = 6 cycles, tr2 = 9 cycles, and tr3 = 1 cycle), which occurs at 8 ns after transient is applied.
  - The magnitude and time of the first droop depends on the combination of tr1 and tr2 transient events.
- The Second Droop magnitude is 78.4 mV, which occurs at 0.67 µs after transient.
  - The second droop depends on when the Microengines come out of reset, specifically how much time this occurs after PLL locks and power starts decreasing.
- The Third Droop magnitude is 67.6 mV, which occurs between 10.1 – 13.1 µs after transient.
  - Assuming Voltage Regulator Bandwidth = 10 KHz.
  - Cbulk is *only* 50% of its total capacitance.
  - I_final = 10.703 A (10% more than 9.73 A measured value).
  - The number of clock cycles for tr3 does not impact the third droop.
  - The amount of final current load and Cbulk will impact the amplitude of the third droop.
- The first, second, and third droops are not affected by the duration of tr3.

2.5.2 Recommendations From Droop Analysis

There are two major recommendations from the correlation study:

- Increase the system board cavity (under the processor) capacitors to address the second droop amplitude. To reduce the magnitude of the second droop in the 0.67us timeframe, sufficient decoupling capacitors should be placed under the processor; refer to Figure 2.
- Increase bulk capacitors to address the third droop amplitude. As shown in Figure 6 the current will decrease after the PLL locks and the MicroEngines are taken out of reset, therefore sufficient bulk capacitance is required to ride through the ~1uS high current transient event.

RDRAM 3

The Intel® IXP2800 and Intel® IXP2850 Network Processors have controllers for three Rambus* DRAM (RDRAM) channels. Each of the controllers independently accesses its own RDRAMs, and can operate concurrently with the other controllers (i.e., they are not operating as a single, wider memory). DRAM provides high-density, high-bandwidth storage and is often used for data buffers.

RDRAM sizes of 64, 128, 256, and 512 Mbytes, and 1 Gbyte are supported. However, each of the channels must have the same number, size, and speed of RDRAMs populated. Each channel can be populated with one to four per bank for short-channel, and one RIMM for long-channel.

Up to two Gbytes of DRAM are supported. If less than two Gbytes of memory is available, the upper part of the address space is not used. It is also possible (for system cost and area savings) to have channels 0 and 1 populated with channel 2 empty, or channel 0 populated with channels 1 and 2 empty.

Reads and writes to RDRAM are generated by Microengines, Intel XScale® core, and PCI (external Bus Masters and DMA Channels). The controllers also do refresh and calibration cycles to the RDRAMs, transparently to software.

Note: RDRAM Powerdown and Nap modes are *not* supported.

Hardware interleaving of addresses (also called striping) provides balanced access to all populated channels; the interleave size is 128 bytes. Interleaving helps to maintain utilization of available bandwidth by spreading consecutive accesses to multiple channels. The interleaving is done in the hardware so that the three channels appear to software as a single, contiguous memory space.

ECC (Error Correcting Code) is supported, but can be disabled. Enabling ECC or parity requires that x18 RDRAMs be used; if ECC is disabled, x16 RDRAMs can be used. ECC can detect and correct all single-bit errors, and detect all double-bit errors. When ECC is enabled, partial writes (of less than eight bytes) must be done as read-modify-writes.

It is not required to implement all three RDRAM channels, however if only a single channel is implemented it MUST be channel 0. If two channels are implemented then it MUST be channels 0 and 1. No other channels are supported in these modes. Note that unused RSL I/Os do not require termination. Also note that designs that do not implement all channels are still required to provide power to all of the RSL I/O power pins as this is a common supply with the device.

3.1 IXMB2800 RDRAM Subsystem Design

The IXMB2800 network processor base card RDRAM subsystem design is implemented using NexMod* memory module solution from High Connection Density, Inc. This solution provides a scalable, high-speed memory in space-constrained applications for networking, communications, and other markets. Using this solution minimizes the amount of space required to get the maximum amount of memory, in this case 256 MB per channel, and facilitates the RDRAM interface design.

The multi-tiered NexMod* module contains all of the circuitry for an entire Rambus* channel in a single module. The NexMod* module can be attached either to the main board with pin grid array (PGA) connectors or soldered with ball grid array (BGA) technology. The module incorporates termination resistors, the Direct Rambus* Clock Generator (DRCG), and a Voltage Regulator Module (VRM) on the same modular subsystem as the memory chips.

In summary, its features are:

- Density up to 256 Mbytes per channel
- Built-in termination and clock generation
- With its 1.1 in. x 2.0 in. size, NexMod* is very space-efficient (compared to SO-RIMM and RIMM solutions)
- Stacked assembly

The NexMod* modules are also available from Samsung and Viking. The IXMB2800 layout details are provided in Section 3.5.

3.1.1 RDRAM Subsystem Implementation Options

Table 12 describes RDRAM subsystem implementation options.

Table 12. RDRAM Subsystem Implementation Options (Sheet 1 of 2)

Option	Memory per NPU		Comments
	Using 256-Mbyte part	Using 512-Mbyte part	
Short channel with two devices	192 Mbytes	384 Mbytes	• Clam-shell configuration helps in layout. • Observability of clam-shell components is an issue. • Must follow all design rules defined in the *Rambus* Short Channel Design Guide*.
Short channel with four devices	384 Mbytes	768 Mbytes	• Clam-shell configuration helps in layout. • Observability of clam-shell components is an issue. • Must follow all design rules defined in the *Rambus* Short Channel Design Guide.*
HCD NexMOD* (eight devices per channel)	768 Mbytes	1.5 Gbytes	• HCD module contains VRM and terminators on the module, making it very space-efficient. • HCD also simplifies channel design since many of the Rambus* design rules are handled on the module.
SO-RIMM* (eight devices per channel)	768 Mbytes	1.5 Gbytes	• SO-RIMM* mounting is horizontal. • Must follow all design rules defined in the *Rambus* Long Channel Design Guide*.
Standard RIMM* (eight devices per channel)	768 Mbytes	1.5 Gbytes	• RIMM* mounting is vertical, but the connector is very long. • Board placement for a dual-NPU design is challenging. • Vendors: Samsung*, Elpida*

Table 12. RDRAM Subsystem Implementation Options (Sheet 2 of 2)

Option	Memory per NPU		Comments
	Using 256-Mbyte part	Using 512-Mbyte part	
Dual-channel RIMM* (eight devices per channel)	768 Mbytes	1.5 Gbytes	• Vendors: Elpida*, Samsung*
Quad-channel RIMM* (four devices per channel)	384 Mbytes	768 Mbytes	• Vendor: Samsung*. • Rambus* is working with vendors to establish a standard.

3.2 Rambus* Channel Design

The following sections provide a high-level overview of Rambus* channel design. For complete design and layout details please refer to the Rambus* design guidelines which can be found on the Rambus* website at www.rambus.com.

3.2.1 RSL Trace Requirements and Recommendations

The following is a list of RSL (Rambus* Signaling Level) trace requirements and recommendations for Rambus* designs:

- All signals must be length-matched (RSL and clock signals) from the IXP28XX network processor to each RDRAM pin. Signals are then length-matched for RDRAM to RDRAM pin.
- Lines should be matched to within 10 mils.
- No length-match requirement is necessary from the last RDRAM pin to the termination island.
- Length matching must compensate for controller package substrate routing. These lengths are provided in Section 3.7.
  - Note that the flight time of the package is 154ps/in and is typically 180ps/in on a standard FR4 PCB. Hence the trace lengths provided in Section 3.7 must be adjusted to reflect the flight delay of the target PCB. An example of this is provided in Section 3.7.
- For impedance control, use the following guidelines:
  - 34 Ω for a short channel and 28 Ω for a long channel.
  - Trace widths for the desired impedance should be obtained from the manufacturer of the PCB as field solvers may not be accurate.
  - Device loading is compensated by narrowing (necking) the trace width in the vicinity of RDRAM.
  - The recommended electrical pitch is:
    15 mm - 18 mm for a 128-Mbyte RDRAM and
    12 mm - 18 mm for a 256-Mbyte RDRAM
- Post layout simulations are strongly recommended to ensure proper signal integrity.
  - Fine tuning of signal lengths may be required to meet timing and signal integrity requirements.

3.2.2 Unused Channel Guidelines

It is not a requirement to implement all three RDRAM channels available on the IXP28XX network processor. However, if only a single channel is implemented it MUST be channel 0. If two channels are implemented then they MUST be channels 0 and 1. No other channel combinations are supported in these modes.

The unused Rambus* I/Os for unused channels do not require termination as the I/O are powered down by default.

Note: Designs that do not implement all channels are still required to provide power to all of the RSL I/O power pins since this is a common supply with the device.

3.2.3 Crosstalk

Recommendations for avoiding crosstalk are as follows:

- Use adequate line spacing and shielding of signal vias.
  - — Use a 2x - 3x trace-width separation.
  - — Place GND vias near signal vias for a good return current path.
  - — Ground flood may also be used between RSL signals to minimize crosstalk. Examples of ground floods are provided in the various Rambus* layout guides.
- Avoid routing over plane splits and voids.

3.2.4 Third-party Sources

Detailed design and layout guides are available from Rambus* for short channel, RIMM, and SO-RIMM designs; the information is not provided in this document since many third-party vendors change information from time to time and could result in inconsistencies between the documents. Please refer to the following third-party sources for Rambus* channel design guidelines for the latest information:

- Design Guides and design examples provided by Rambus*, available at www.rambus.com.
- Design Guides for connection density provided by High Connection Density, Inc., available at www.hcdcorp.com.

3.2.5 IXP28XX Network Processor Power-Up Sequence

Note: The 1.8 V and 1.5 V supplies can come up in any order before or after the 2.5 V, 1.3 V, and 3.3 V supplies.

For Rambus* channel designs, perform the following steps to power up the IXP28XX network processor:

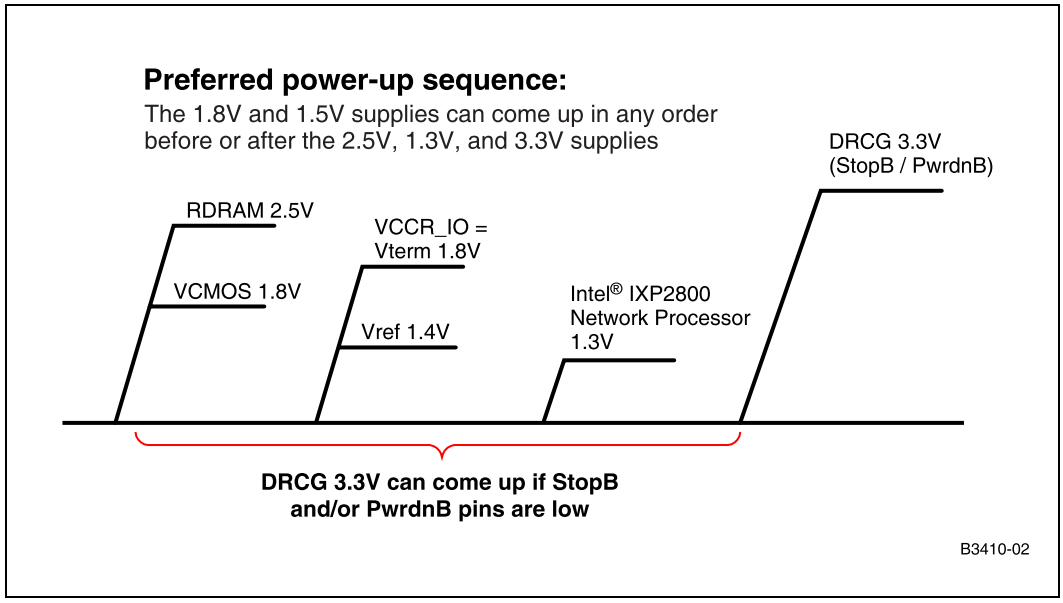
1. Power up the RDRAM to 2.5 V.
   - — V_{CMOS} (1.8 V) is raised simultaneously with 2.5 V through a voltage divider.
   - — Each RDRAM draws only 10 µA V_{CMOS} of current.

2. Power up the V_{CCR_IO} to 1.8 V and V_{TERM} to 1.8 V.
   — Both V_{CCR_IO} and V_{TERM} must be raised simultaneously and tied to the same 1.8 V power supply.
   — V_{REF} should be generated through a voltage divider from V_{TERM}.
3. Power up the IXP28XX network processor to 1.35 V (V_{CCR} and V_{CCR_A}).
   — V_{CCR} is connected to V_{CCR_A} through an LC filter.
4. Enable the DRCG clock output.
   — Apply 3.3 V after V_{CCR_IO}, with StopB and PwrdnB pins high.

Note: DRCG 3.3 V can come up if StopB and/or PwrdnB pins are low.

Figure 7 illustrates the power-up sequence.

Figure 7. Power-up Sequence



3.2.6 IXP28XX Network Processor Power-Up Considerations when using NexMod* Memory Modules

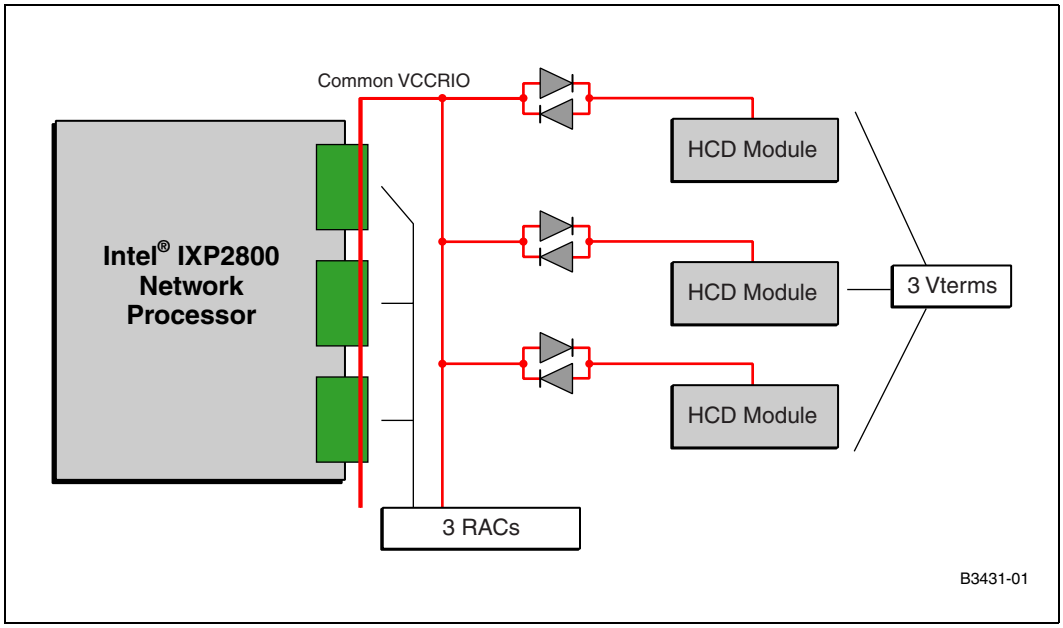
The following are additional design considerations for the IXP28XX network processor's power-up sequence when using NexMod* modules. Because each channel can have a separate power source for V_{TERM} and V_{CMOS} when using the HCD memory modules and V_{CCR_IO}, the RDRAM I/O supply for the IXP28XX network processor, is common to all three channels as shown in Figure 8, the following requirement must be satisfied by the power delivery design:

- The system designer must ensure that V_{CCR_IO} and V_{TERM} never differ by more than 1.6 V.
  — In most cases this can be guaranteed by the power sequence order.

If the requirement cannot be guaranteed by the power sequence design then the following recommendations can be used to meet the requirement:

- Each channel's V_{TERM} can be linked to V_{CCR_IO} with back-to-back Schottkey diodes. An example of this implementation is shown in Figure 8.
- The RDRAM V_{CMOS} can be connected to V_{CCR_IO} because V_{CMOS} draws only a few µA.

Figure 8. Common V_{CCR_IO} for All Three RACs in the IXP28XX® Network Processor



3.3 IXP28XX Network Processor Rambus* Controller Footprint and Via Placement

The following figures illustrate the IXP28XX network processor Rambus* controller footprint and via placement:

- Figure 9, "Rambus* Controller Footprint and Via Placement Showing Alternating Dogbone Orientation"
- Figure 10, "Rambus* Controller Footprint and Via Placement Showing Exploded View of Checkerboard Detail"

Figure 9 illustrates the IXP28XX network processor Rambus* controller footprint and via placement. The checkerboard GND-signal via placement is achieved by alternating the orientation of the dogbones.

Figure 9. Rambus* Controller Footprint and Via Placement Showing Alternating Dogbone Orientation

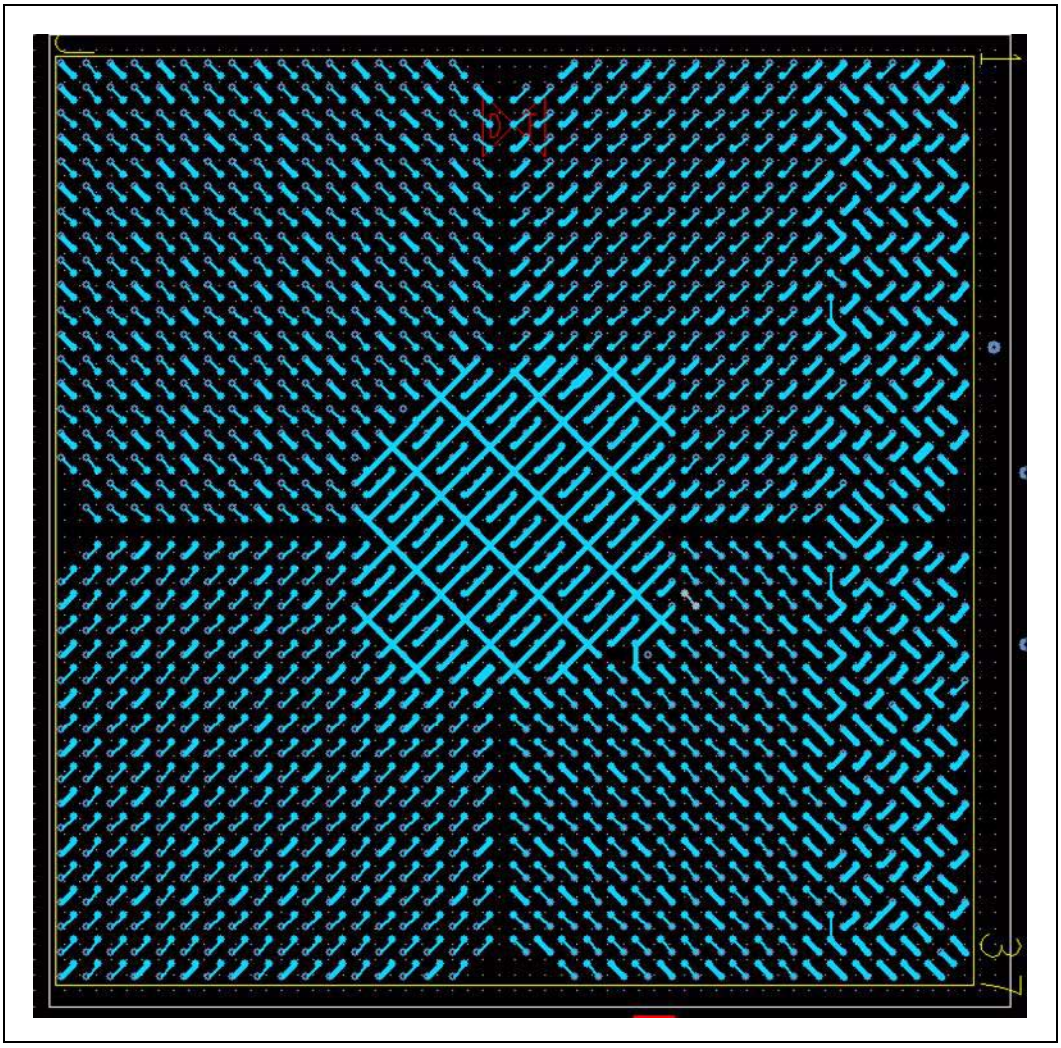
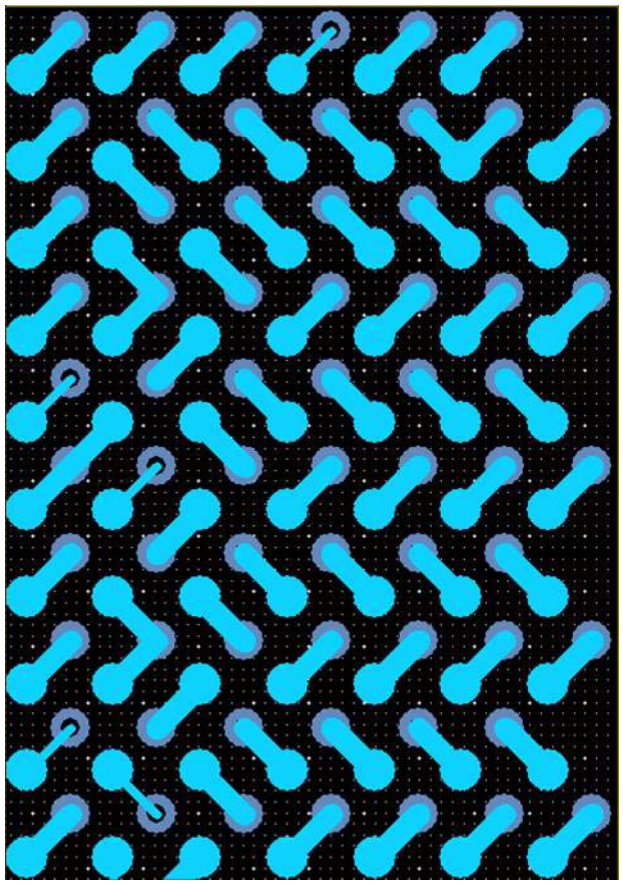


Figure 10 illustrates the IXP28XX network processor Rambus* controller footprint and via placement, showing an exploded view of checkerboard detail.

Figure 10. Rambus* Controller Footprint and Via Placement Showing Exploded View of Checkerboard Detail



3.4 IXP28XX Network Processor Controller Escape Routing

The following figures illustrate IXP28XX Network Processor controller escape routing as implemented on the IXMB2800 development system:

- Figure 11, “Network Processor Controller Escape Routing - Layer 4”
- Figure 12, “Network Processor Controller Escape Routing - Layer 6”
- Figure 13, “Network Processor Controller Escape Routing - Layer 13”
- Figure 14, “Network Processor Controller Escape Routing - SCK/CMD Signals Routed on Layer 12”
- Figure 15, “Network Processor Controller Escape Routing - SCK/CMD Signals Routed on Layer 16”

Figure 11 illustrates layer 4 of the IXP28XX network processor controller escape routing, using 28-Ω, 11-mil-wide traces.

Figure 11. Network Processor Controller Escape Routing - Layer 4

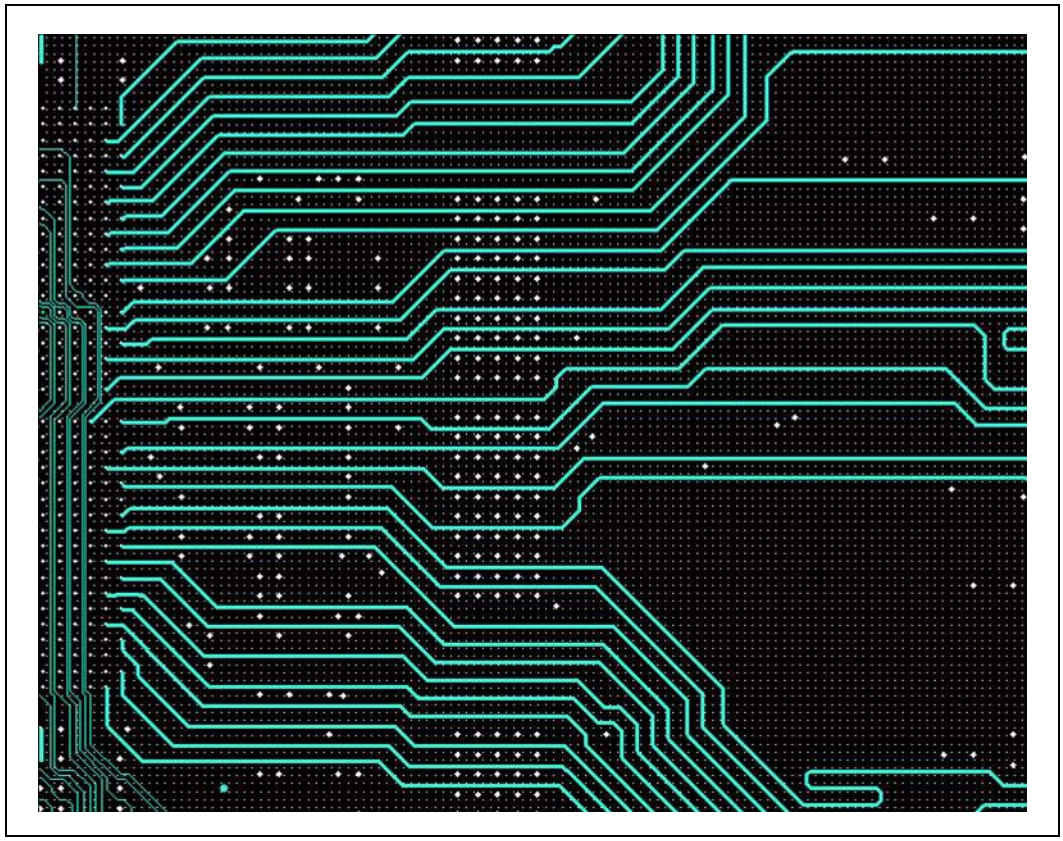


Figure 12 illustrates layer 6 of the IXP28XX network processor controller escape routing, using 28-Ω, 11-mil-wide traces.

Figure 12. Network Processor Controller Escape Routing - Layer 6

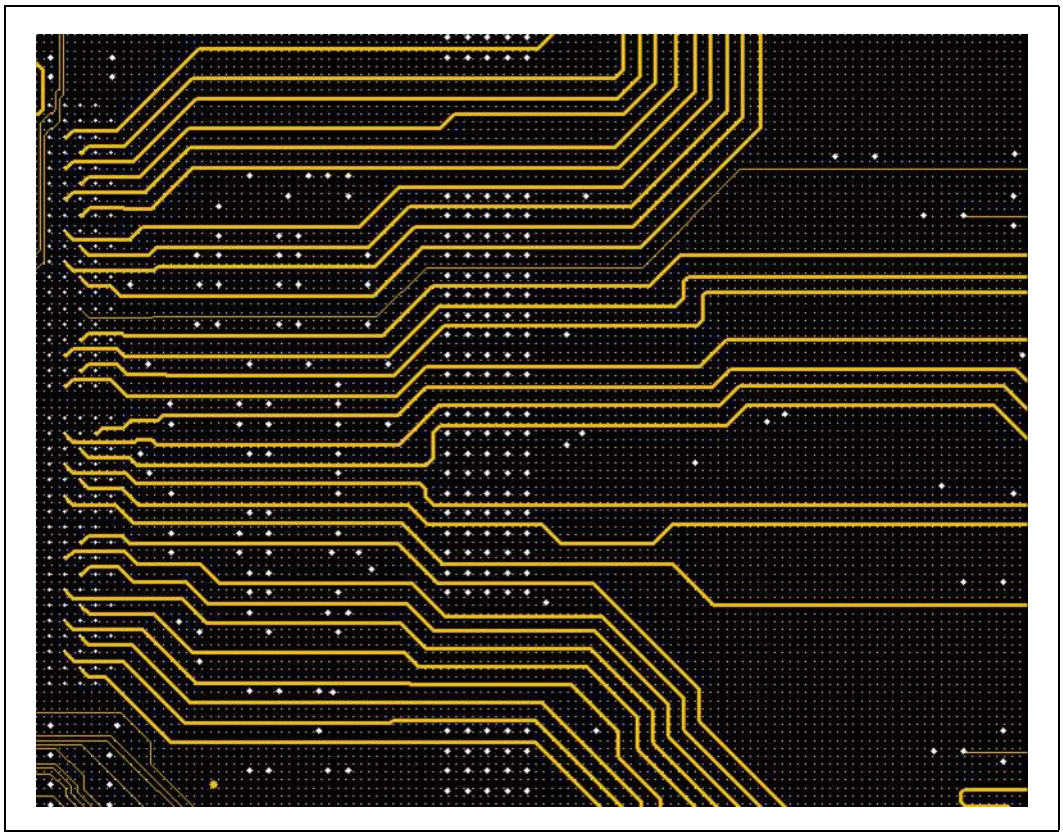


Figure 13 illustrates layer 13 of the IXP28XX network processor controller escape routing, using 28-Ω, 11-mil-wide traces.

Figure 13. Network Processor Controller Escape Routing - Layer 13

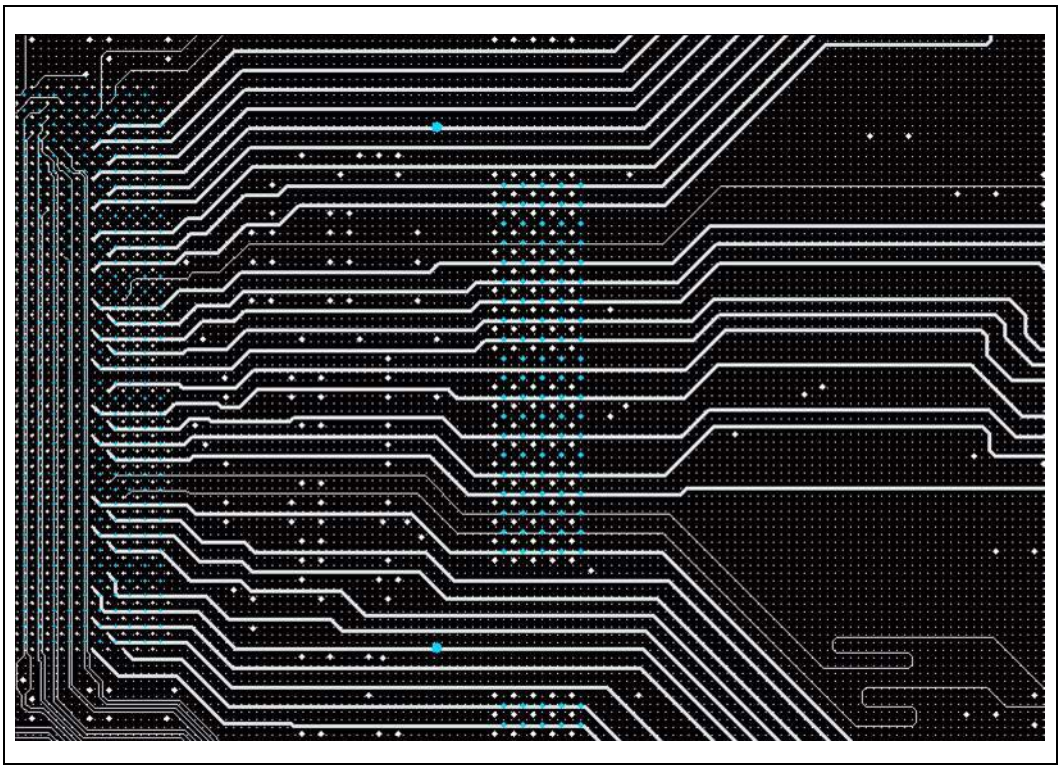


Figure 14 illustrates IXP28XX network processor controller escape routing on layer 12, with SCK/CMD signals, using 28-Ω, 11-mil-wide traces.

Figure 14. Network Processor Controller Escape Routing - SCK/CMD Signals Routed on Layer 12

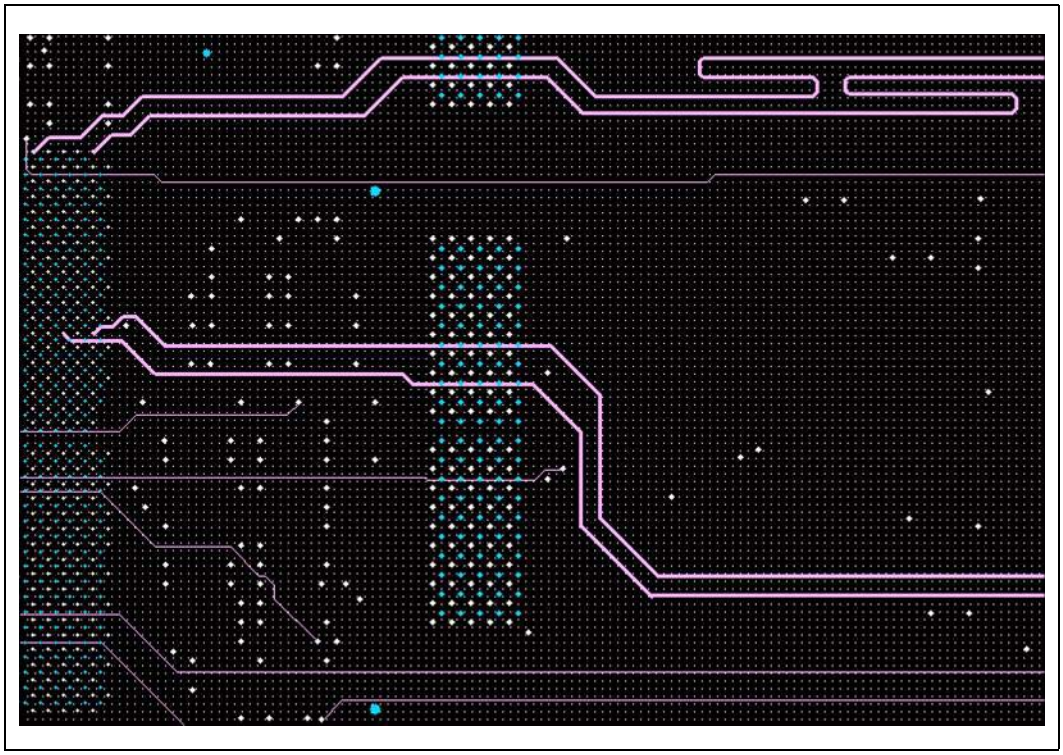
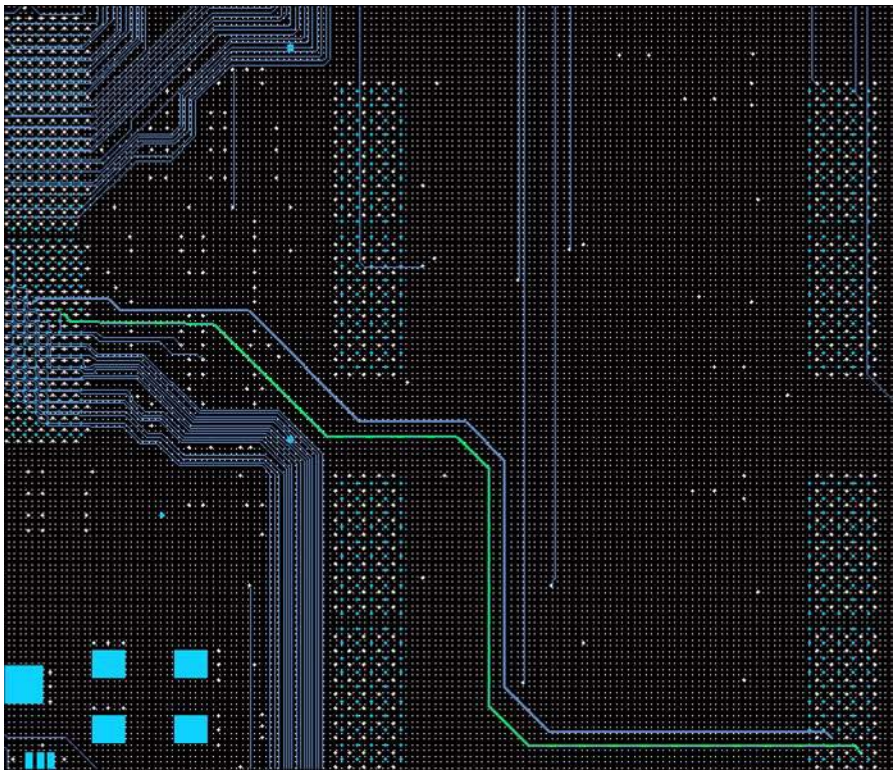


Figure 15 illustrates IXP28XX network processor controller escape routing on layer 16, with SCK/CMD signals, using 28-Ω, 11-mil-wide traces.

Figure 15. Network Processor Controller Escape Routing - SCK/CMD Signals Routed on Layer 16



3.5 IXP28XX Network Processor Three-Channel Controller to HCD NexMod* RDRAM Routing

The following figures illustrate routing with the IXP28XX network processor's three-channel controller to HCD NexMod* RDRAM as implemented on the IXMB2800 development system.

- Figure 16, "Three-Channel Controller to HCD NexMod* RDRAM Routing - Layer 4"
- Figure 17, "Three-Channel Controller to HCD NexMod* RDRAM Routing - Layer 6"
- Figure 18, "Three-Channel Controller to HCD NexMod* RDRAM Routing - Layer 13"
- Figure 19, "Three-Channel Controller to HCD NexMod* RDRAM Routing - SCK/CMD Layer 12"

Figure 16. Three-Channel Controller to HCD NexMod* RDRAM Routing - Layer 4

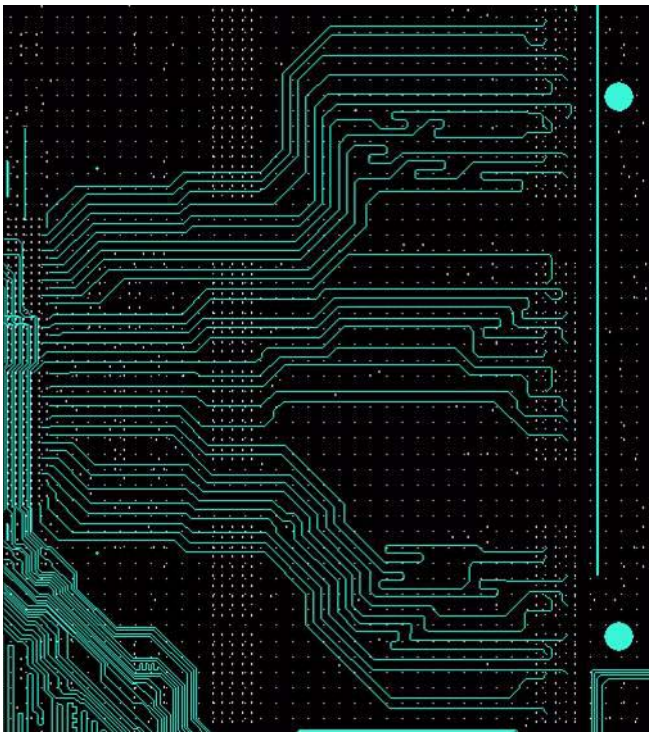


Figure 17. Three-Channel Controller to HCD NexMod* RDRAM Routing - Layer 6

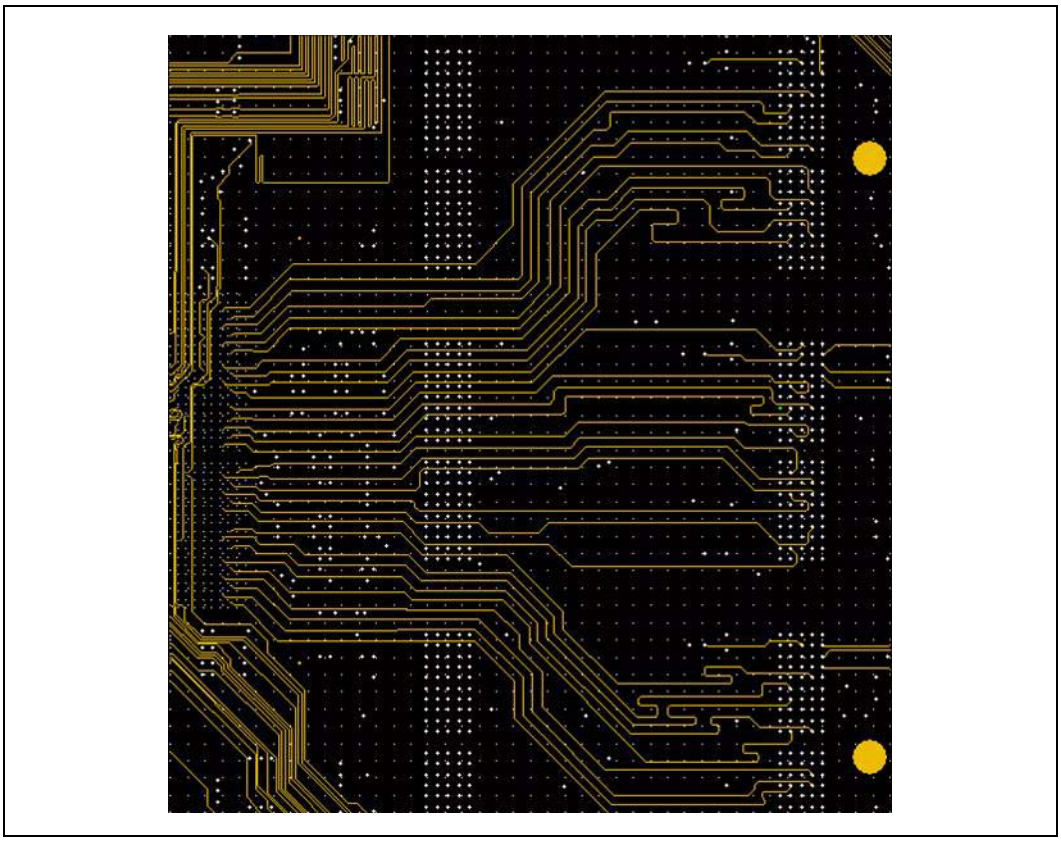


Figure 18. Three-Channel Controller to HCD NexMod* RDRAM Routing - Layer 13

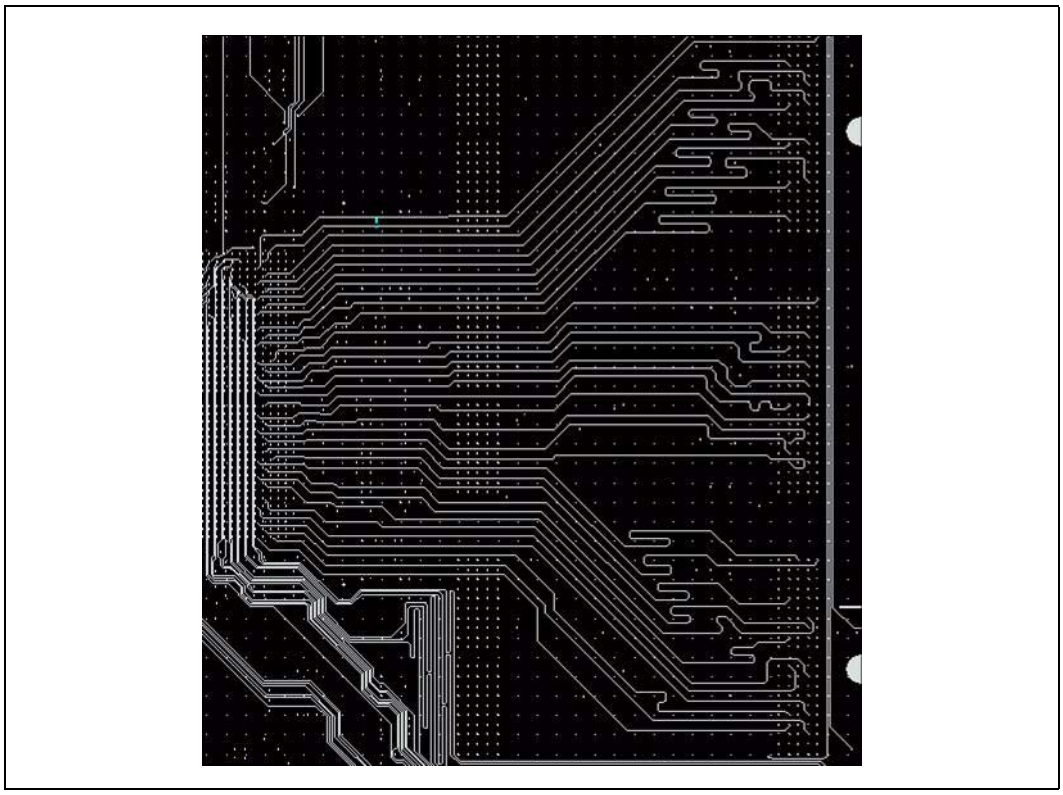
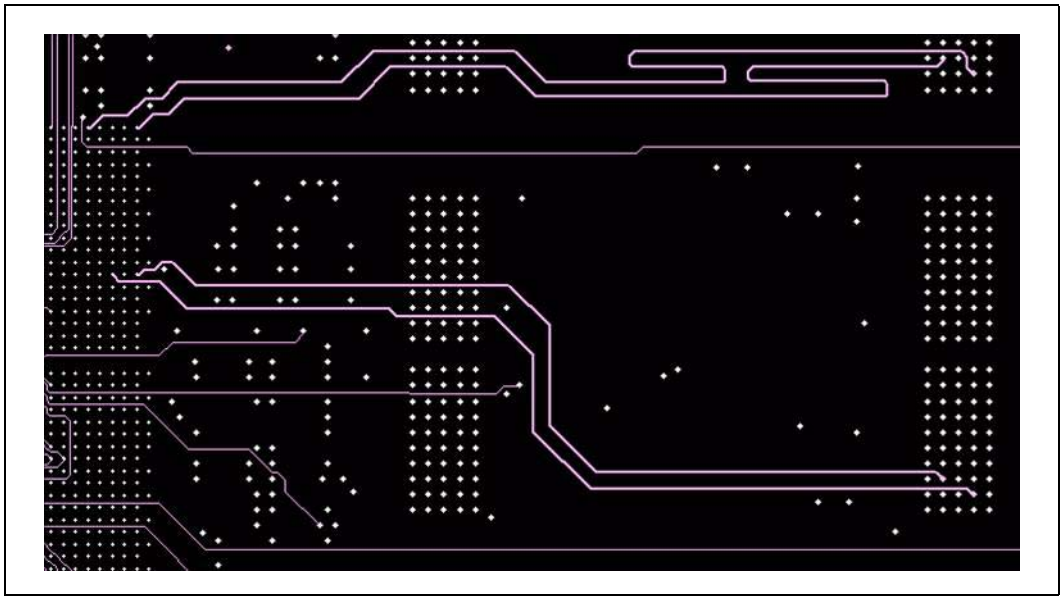


Figure 19. Three-Channel Controller to HCD NexMod* RDRAM Routing - SCK/CMD Layer 12

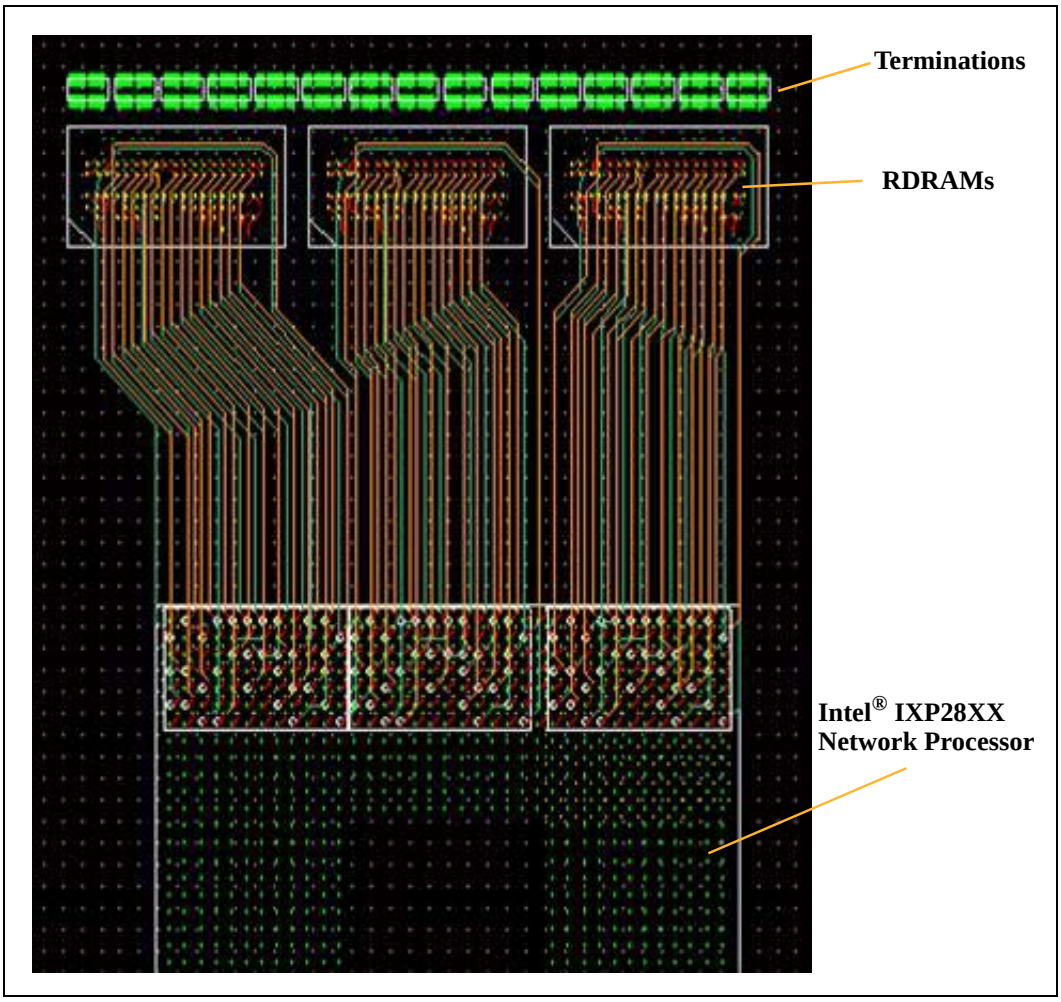


3.6 IXP28XX Network Processor Short Channel Routing

Figure 20 illustrates an IXP28XX network processor short channel routing example

Note: The layout example depicted in Figure 20 was implemented only as a routing study and has not been validated.

Figure 20. IXP28XX Network Processor Short Channel Routing



3.7 Package Trace Lengths for RDRAM Signals

Table 13 provides package trace lengths for RDRAM signals, listed by decreasing lengths in a given logical grouping.[1]

The flight time on the package substrate is 154ps/in which differs from the flight delay of standard FR4, typical 180ps/in. As a result the package routing lengths in Table 13 must be adjusted to compensate for the difference in flight delay between the package and the PCB. For example RDR0_CMD has a package length of 0.697 in, and the target PCB has a flight delay of 180ps/in. In order to adjust the package length to match the PCB flight delay this length must be multiplied by the ratio of 154/180 or the difference between the package and PCB flight delays. Therefore the trace package routing length that must be accounted for on the PCB is 0.697*(154/180) or 0.596 in.

Note: If the flight delay of the target PCB is not 180 ps/in then the ratio, (154/180), must be modified accordingly, i.e., the denominator would be changed to reflect the actual flight delay.

Table 13. Package Trace Lengths for RDRAM Signals (Sheet 1 of 2)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
RDR0_CMD	17.709	0.697	**RDR1_CTM**	12.634	0.497	**RDR2_DQA[3]**	19.161	0.754
RDR0_DQB[8]	17.39	0.685	RDR1_CTMN	12.634	0.497	RDR2_DQA[0]	18.843	0.742
RDR0_DQB[5]	17.071	0.672	RDR1_DQA[2]	12.549	0.494	RDR2_DQA[8]	18.573	0.731
RDR0_RQ[3]	16.938	0.667	RDR1_CMD	12.436	0.490	RDR2_CTM	18.264	0.719
RDR0_DQB[2]	16.78	0.661	RDR1_DQA[6]	11.982	0.472	RDR2_CTMN	18.264	0.719
RDR0_RQ[0]	16.517	0.650	RDR1_DQA[0]	11.567	0.455	RDR2_DQA[6]	17.226	0.678
RDR0_DQB[6]	15.93	0.627	RDR1_DQB[8]	11.316	0.446	RDR2_DQA[4]	16.687	0.657
RDR0_RQ[5]	15.727	0.619	RDR1_DQB[7]	11.167	0.440	RDR2_DQA[1]	16.358	0.644
RDR0_SIO	15.466	0.609	RDR1_RQ[5]	10.884	0.429	RDR2_RQ[4]	16.105	0.634
RDR0_DQB[3]	15.411	0.607	RDR1_DQA[8]	10.782	0.424	RDR2_DQA[5]	16.087	0.633
RDR0_PCLKM	14.94	0.588	RDR1_DQB[4]	10.741	0.423	RDR2_RQ[0]	16.028	0.631
RDR0_SCK	14.294	0.563	RDR1_SCLKN	10.609	0.418	RDR2_DQA[7]	15.997	0.630
RDR0_DQB[1]	13.979	0.550	RDR1_RQ[0]	10.391	0.409	RDR2_DQA[2]	15.843	0.624
RDR0_RQ[2]	13.743	0.541	RDR1_DQA[4]	9.992	0.393	RDR2_CFM	15.645	0.616
RDR0_RQ[6]	13.651	0.537	RDR1_CFMN	9.67	0.381	RDR2_CFMN	15.645	0.616
RDR0_SCLKN	13.646	0.537	RDR1_CFM	9.668	0.381	RDR2_RQ[1]	15.448	0.608
RDR0_DQB[7]	13.607	0.536	RDR1_DQA[1]	9.603	0.378	RDR2_RQ[5]	15.271	0.601
RDR0_CTM	13.321	0.524	RDR1_RQ[1]	9.432	0.371	RDR2_RQ[7]	14.707	0.579
RDR0_CTMN	13.32	0.524	RDR1_DQB[5]	9.223	0.363	RDR2_RQ[2]	14.637	0.576
RDR0_DQA[2]	13.006	0.512	RDR1_RQ[3]	8.712	0.343	RDR2_DQB[4]	13.402	0.528
RDR0_DQA[5]	12.952	0.510	RDR1_SCK	8.639	0.340	RDR2_DQB[1]	13.239	0.521
RDR0_DQB[4]	12.898	0.508	RDR1_DQB[2]	8.627	0.340	RDR2_DQB[7]	13.103	0.516
RDR0_CFM	12.636	0.497	RDR1_DQB[1]	8.481	0.334	RDR2_DQB[3]	12.978	0.511
RDR0_CFMN	12.636	0.497	RDR1_PCLKM	8.465	0.333	RDR2_SIO	12.902	0.508
RDR0_DQB[0]	12.49	0.492	RDR1_DQA[5]	8.443	0.332	RDR2_RQ[6]	12.633	0.497
RDR0_DQA[6]	11.797	0.464	RDR1_DQA[7]	8.292	0.326	RDR2_DQB[8]	12.463	0.491

1. Signals in boldface type indicate the start of a logical grouping.

Table 13. Package Trace Lengths for RDRAM Signals (Sheet 2 of 2)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
RDR0_RQ[1]	11.432	0.450	RDR1_DQB[6]	8.247	0.325	RDR2_RQ[3]	11.952	0.471
RDR0_RQ[4]	10.75	0.423	RDR1_RQ[7]	8.192	0.323	RDR2_DQB[6]	11.63	0.458
RDR0_DQA[1]	10.516	0.414	RDR1_RQ[2]	8.141	0.321	RDR2_DQB[2]	11.486	0.452
RDR0_RQ[7]	10.342	0.407	RDR1_RQ[6]	7.645	0.301	RDR2_DQB[0]	11.046	0.435
RDR0_DQA[4]	10.206	0.402	RDR1_DQB[3]	7.565	0.298	RDR2_SCK	10.513	0.414
RDR0_DQA[7]	9.961	0.392	RDR1_DQA[3]	7.273	0.286	RDR2_PCLKM	10.254	0.404
RDR0_DQA[0]	8.655	0.341	RDR1_DQB[0]	6.813	0.268	RDR2_DQB[5]	9.806	0.386
RDR0_DQA[8]	8.306	0.327	RDR1_SIO	6.608	0.260	RDR2_SCLKN	9.157	0.361
RDR0_DQA[3]	8.001	0.315	RDR1_RQ[4]	6.421	0.253	RDR2_CMD	8.958	0.353

QDR SRAM 4

The Intel® IXP2800 and Intel® IXP2850 Network Processors have four independent SRAM controllers, each of which supports pipelined QDR synchronous static RAM (SRAM) and/or a coprocessor that adheres to QDR signaling. Any or all controllers can be left unpopulated if the application does not need to use them. SRAM is accessible by the Microengines, the Intel XScale® core, and the PCI Unit (external bus masters and DMA).

The memory is logically four bytes (32 bits) wide; physically, the data pins are two bytes wide and are double-clocked. Byte parity is supported, and each of the four bytes has a parity bit, which is written when the byte is written and checked when the data is read. There are byte-enables that select the bytes to be written, for writes of less than 32 bits.

Each of the four QDR ports are QDR- and QDRII-compatible, and each port implements the "_K" and "_C" output clocks and the "_CIN" clock (and their inversions) as inputs.

Note: The "_C" and "_CIN" clocks are optional. Extensive work has been done to provide impedance controls within the IXP28XX network processors for the signals initiated by the network processor driving to QDR parts. A clean signaling environment is critical to achieving 200- to 233-MHz QDRII data transfers.

The configuration assumptions for the network processor I/O driver and/or receiver development include four QDR loads and the network processor. The network processor supports bursts of two SRAMs; four-SRAM bursts are not supported.

The SRAM controller can also be configured to interface to an external coprocessor that adheres to the QDR electricals and protocol. Each SRAM controller can also interface to an external coprocessor through its standard QDR interface, which enables SRAM devices and coprocessors to operate on the same bus. The coprocessor behaves as a memory-mapped device on the SRAM bus.

4.1 Introduction

This is a design guide for the QDR interface of IXP28XX NPU. It is intended to guide board designers using IXP28XX network processor in their designs employing 4 SRAM loads or less at a clock frequency of 233/250MHz. If a much lower frequency is to be used then it is recommended that the developer consult with the SRAM vendor to ensure that the SRAM operates at that intended frequency.

These guidelines are based on a set of simulations that were performed under optimum or close to optimum conditions. The QDR section of the base board of IXDP2400 platform has been used to simulate all IXP28XX QDR signals. The routing guidelines in this guide are modified from those employed in IXDP2400 platform. It is very important that these guidelines be observed and adhered to as closely as possible to obtain working designs.

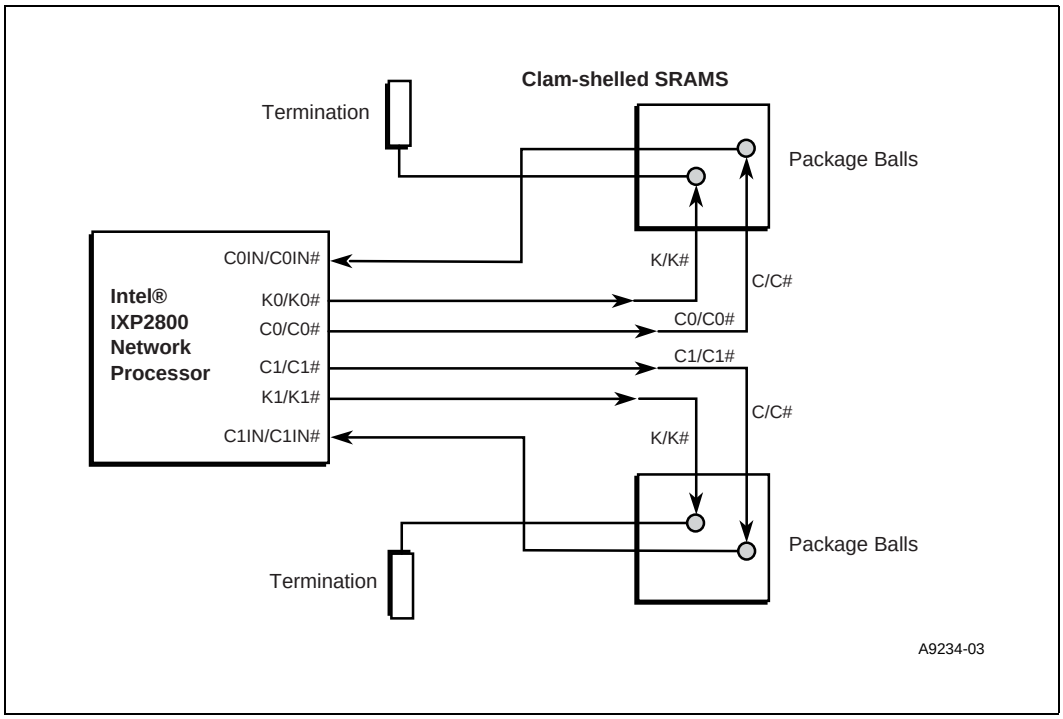
However, **if the customer is interested in using a different design scheme then we strongly recommend the customer to do full extended simulations on the intended design scheme**.Any changes or modifications to the design guidelines described here in this document may lead to

significant changes in results or may lead to non-working design altogether. That is why it is strongly recommended that developers thoroughly simulate any new designs or modifications before committing to any new modifications.

4.2 QDR Clocking Scheme

The controller drives out a pair of K clocks (K and K#), and a pair of C clocks (C and C#). The C and C# clocks externally return to the controller for reading data. Figure 21 shows the clock diagram of the clocking scheme for a QDR interface driving four SRAM chips.

Figure 21. Clocking Scheme for a QDR Interface Driving Four SRAMs



4.2.1 SRAM Controller Configurations

Each channel has enough address pins (24) to support up to 64 Mbytes of SRAM. The SRAM controllers can directly generate multiple port enables (up to four pairs) to allow for depth expansion; two pairs of pins are dedicated for port-enables. Smaller RAMs use fewer address signals than the number provided to accommodate the largest RAMs, so some address pins – 23:20 – are configurable as either address or port-enable, based on the control status register (CSR) setting, as shown in Table 14.

Note: All of the SRAMs on a given channel must be the same size.

Table 14. SRAM Controller Configurations

SRAM Configuration	SRAM Size	Addresses Needed to Index SRAM	Addresses Used as Port-enables	Total Number of Port-select Pairs Available
512K x 18	1 Mbyte	17:0	23:22, 21:20	4
1M x 18	2 Mbytes	18:0	23:22, 21:20	4
2M x 18	4 Mbytes	19:0	23:22, 21:20	4
4M x 18	8 Mbytes	20:0	23:22	3
8M x 18	16 Mbytes	21:0	23:22	3
16M x 18	32 Mbytes	22:0	None	2
32M x 18	64 Mbytes	23:0	None	1

Each channel can be expanded by depth, according to the number of port-enables available. If external decoding is used, then the number of SRAMs used is not limited by the number of port enables generated by the SRAM controller.

Note: External decoding may require external pipeline registers to account for the decode time, depending on the desired frequency.

Table 15 lists the QDR Address and Read Port Enable (RPE)/Write Port Enable (WPE) mapping.

Table 15. QDR Address/RPE/WPE Mapping

SRAM Configuration/Size	SRAM_CONTROL [SRAM_SIZE][9:7]	SRAM_CONTROL [PORT_CTL][5:4]	RPE[2]/WPE[2]	RPE[3]/WPE[3]
512K x 18 - 1 Mbyte	000	11	QDR_ADDR[23:22]	QDR_ADDR[21:20]
1Mb x 18 - 2 Mbytes	001	11	QDR_ADDR[23:22]	QDR_ADDR[21:20]
2Mb x 18 - 4 Mbytes	010	11	QDR_ADDR[23:22]	QDR_ADDR[21:20]
4Mb x 18 - 8 Mbytes	011	10	QDR_ADDR[23:22]	N/A
8Mb x 18 - 16 Mbytes	100	10	QDR_ADDR[23:22]	N/A
16Mb x 18 - 32 Mbytes	101	00	N/A	N/A
32Mb x 18 - 64 Mbytes	110	00	N/A	N/A

Table 16 shows maximum SRAM system sizes. Shaded entries require external decoding, because they use more port-enables than the SRAM controller can supply directly.

Table 16. Total Memory per Channel (Sheet 1 of 2)

SRAM Size	Number of SRAMs on Channel							
	1	2	3	4	5	6	7	8
512K x 18	1 Mbyte	2 Mbytes	3 Mbytes	4 Mbytes	5 Mbytes	6 Mbytes	7 Mbytes	8 Mbytes
1M x 18	2 Mbytes	4 Mbytes	6 Mbytes	8 Mbytes	10 Mbytes	12 Mbytes	14 Mbytes	16 Mbytes
2M x 18	4 Mbytes	8 Mbytes	12 Mbytes	16 Mbytes	20 Mbytes	24 Mbytes	28 Mbytes	32 Mbytes
4M x 18	8 Mbytes	16 Mbytes	24 Mbytes	32 Mbytes	64 Mbytes	NA	NA	NA

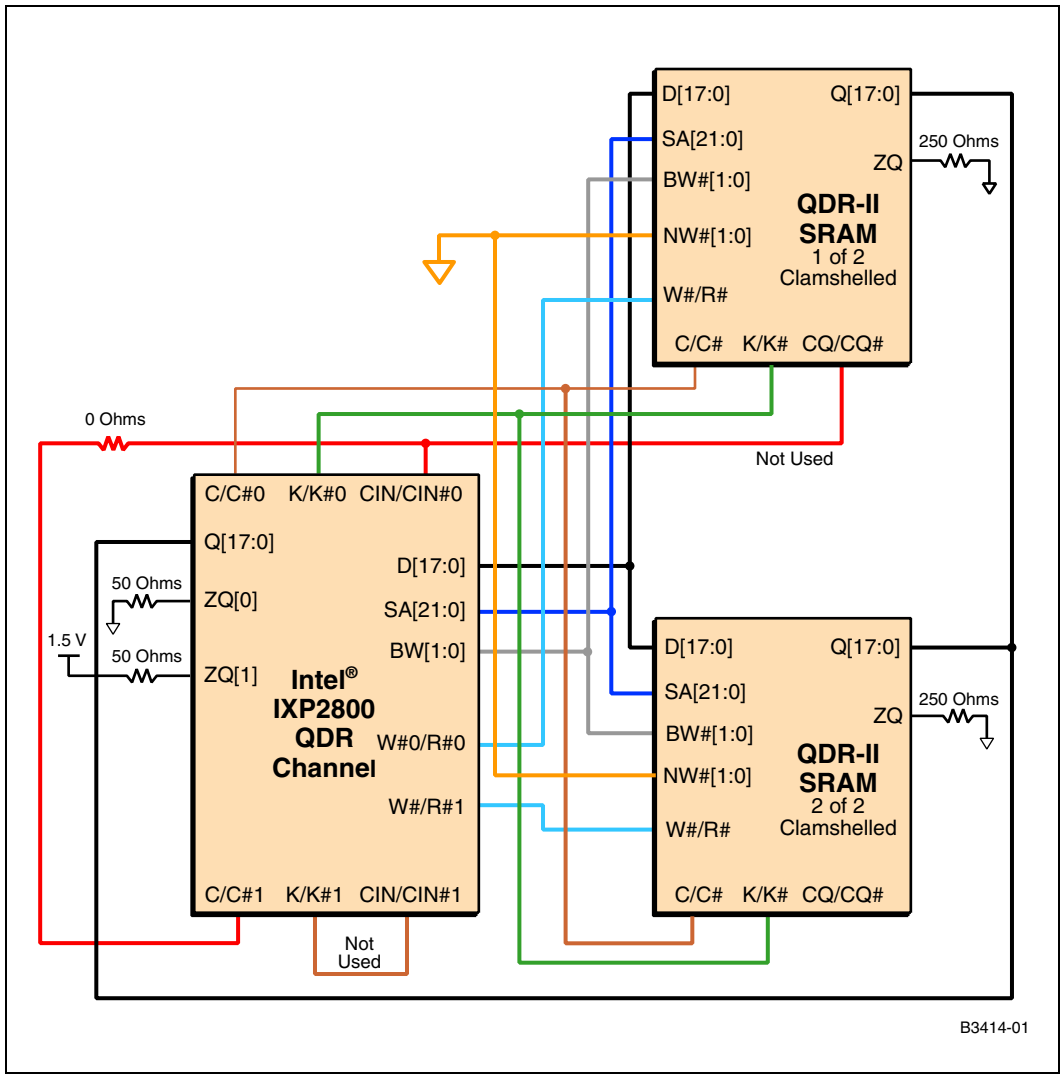
Table 16. Total Memory per Channel (Sheet 2 of 2)

SRAM Size	Number of SRAMs on Channel							
	1	2	3	4	5	6	7	8
8M x 18	16 Mbytes	32 Mbytes	48 Mbytes	64 Mbytes	NA	NA	NA	NA
16M x 18	32 Mbytes	64 Mbytes	NA	NA	NA	NA	NA	NA
32M x 18	64 Mbytes	NA	NA	NA	NA	NA	NA	NA

4.3 QDR SRAM Connections

Figure 22 illustrates the QDR SRAM connections.

Figure 22. QDR SRAM Connections



4.4 QDR SRAM Interface

The IXP28XX network processor has four independent SRAM subsystems, each of which supports pipelined QDRII-synchronous static RAM (QDRII SRAM). There may also be – in addition to or as a replacement for the pipelined QDR SRAM – a coprocessor with QDR signaling capability.

The IXP2800 SRAM memory interface is logically 32 bits wide. The read and write data buses are physically two bytes wide each and are double-clocked. Each byte has a parity bit written and checked on data writes and reads, respectively. The byte enables select bytes to write for data that is less than 32 bits. The SRAM controller supports QDRII two-word bursts at speeds of up to 233 MHz.

4.4.1 Using x9 Versus x18 QDR SRAM Parts

When using x18 parts with four-SRAM load topology, there are serious signal integrity issues in the DATA-READ cycle when one of the SRAMs is sending data and the IXP28XX network processor is receiving (reading) the data from the SRAM that is driving. For example, the three stubs of the other non-sending SRAMs could cause severe signal reflections that would deteriorate the noise margin as well as the timing in the signal.

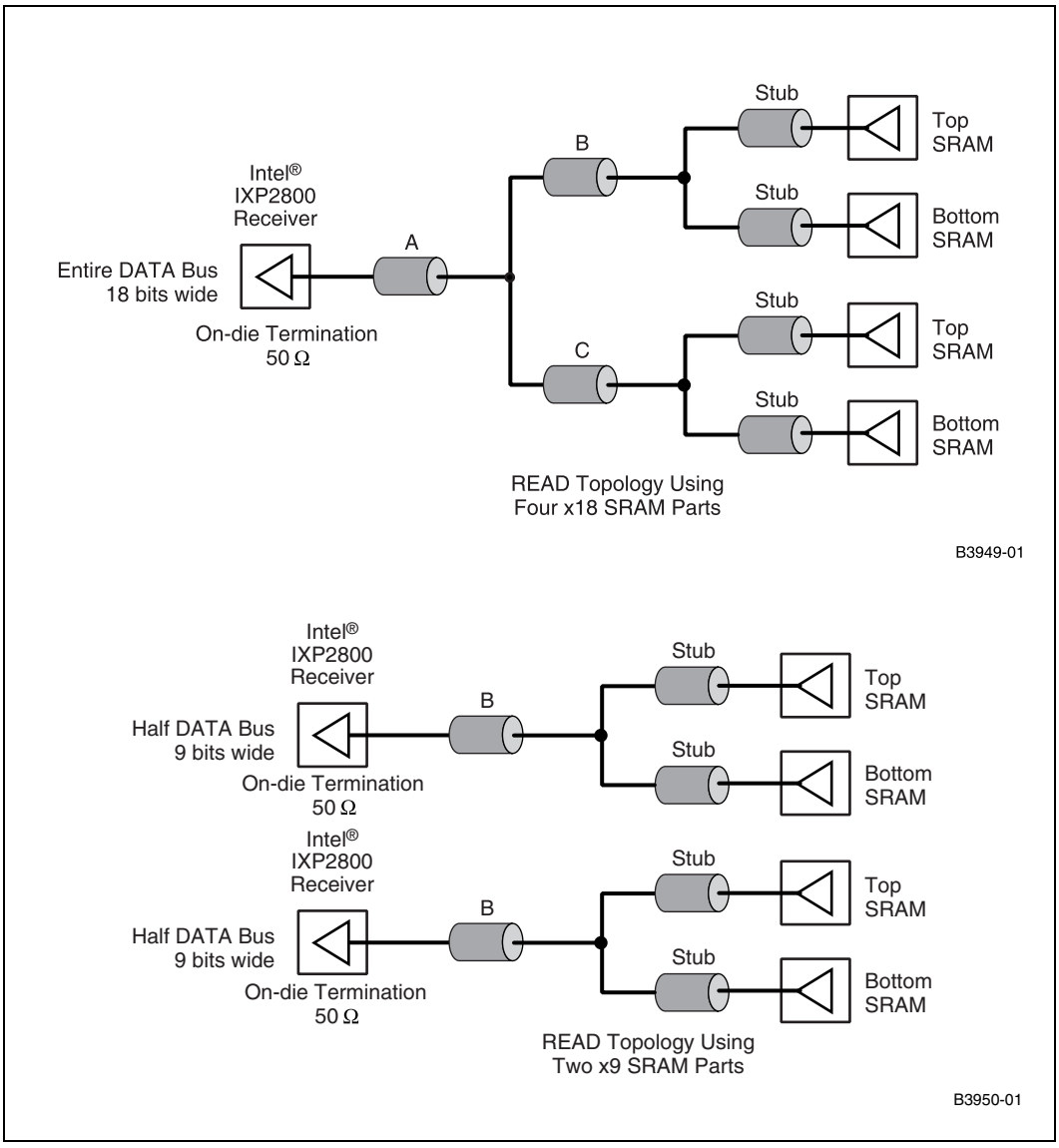
Using “star” topology, four electrical loads can be achieved on one side of the PCB; however, it is recommended that simulation first verify that timing meets the specification and that signal integrity is maintained.

With a two-SRAM load topology, the DATA-READ cycle’s signal integrity issue is less serious than in the four-SRAM load because there is only one stub hanging on the net. The more stubs the net has, the more serious and severe the reflections become due to serious mismatching in the line impedance.

During the DATA-WRITE cycle or in the ADDRESS net, the IXP28XX network processor sends data to all of the SRAMs and thus, there are no hanging stubs that would cause severe reflections. This means that performance is acceptable with four SRAM loads in the WRITE and ADDRESS operations, but not in the DATA-READ operation.

For these reasons, it was necessary to split the DATA bus — that is, DATA-READ and DATA-WRITE — into halves, each with a 2-SRAM load that is nine bits wide for designs that implement a four-SRAM load topology. Using x9 SRAM devices provides clean signalling during READ operations; see Figure 23.

Figure 23. Topologies for Using x9 Versus x18 QDR SRAM Parts



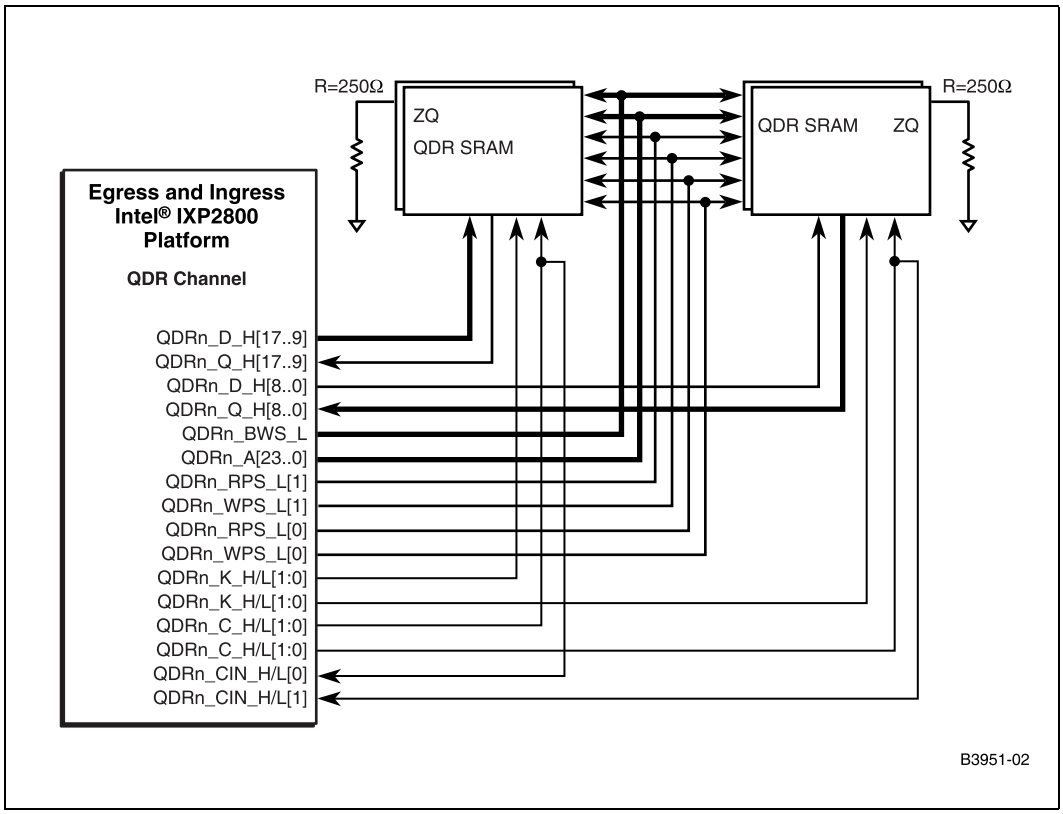
When it is necessary to use more than one SRAM device to achieve a certain memory size capacity, the SRAMs can be arranged in either a Width-Expansion configuration or a Depth-Expansion configuration. Clamshelling — that is, locating two devices on opposite sides of the PCB — is possible with either width-expansion or depth-expansion.

4.4.1.1 Examples of the QDR Interface

The following figures illustrate examples of the QDR interface:

- Figure 24, “IXP2800 Width-Expanded QDR Interface”
- Figure 25, “Ingress IXP28XX Network Processor QDR Modular Channel Depth-Expanded QDR Interface”
- Figure 26, “Ingress IXP2800 Network Processor QDR Modular Channel, Four-Load QDR Interface”

Figure 24. IXP2800 Width-Expanded QDR Interface[1]



1. On egress channels 1 and 2 and ingress channel 1.

Figure 25. Ingress IXP28XX Network Processor QDR Modular Channel Depth-Expanded QDR Interface

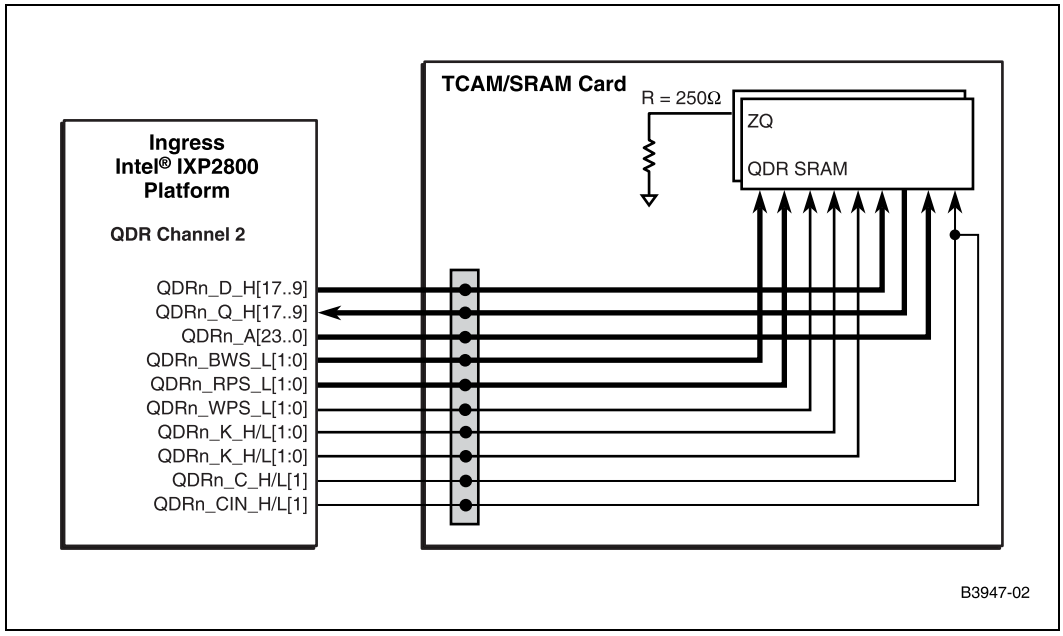
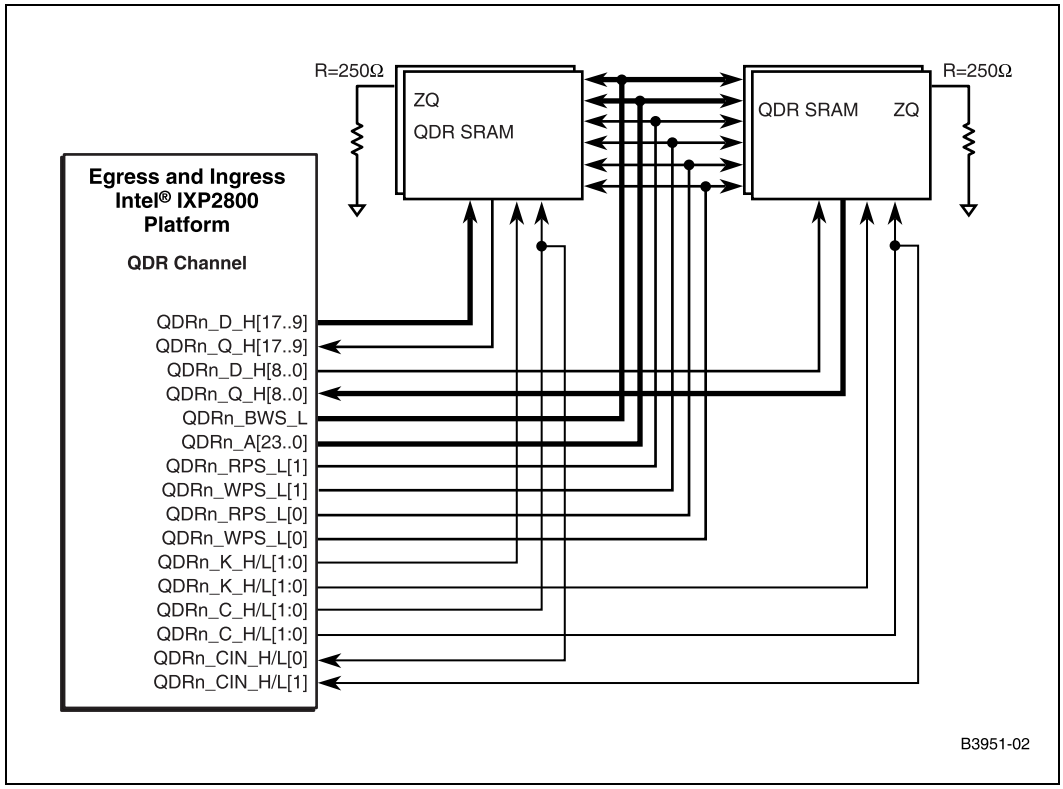


Figure 26. Ingress IXP2800 Network Processor QDR Modular Channel, Four-Load QDR Interface



4.4.2 Signal Groups

The QDR interface has six groups of signals. These are the K-Clocks, the C-Clocks, Address, Data-OUT or WRITE, Data-IN or READ, and Control. The Control group has three signals, the WRITE PORT ENABLE Active Low, the READ PORT ENABLE Active Low, and the BYTE WRITE ENABLE Active Low. The Address, Data-OUT, Data-IN, and the BYTE WRITE ENABLE are all Double Data Rate, while the WRITE PORT ENABLE and the READ PORT ENABLE are single data rate.

An overall summary of these signal groups with topology details is depicted in Table 17 below.

Table 17. An Overview of QDR signal groups

Signals	Topology	Driver	Trace Impedance	No of Loads	Termination	Termination Position
Address	T-Topology	30 Ohm Driver	34 Ohm	4 SRAMs	35 Ohm	Center @ T Point
K Clocks	Point-to-Point	50 Ohm Driver	50 Ohm	2 SRAMs	50 Ohm	@SRAM Input
C Clocks	Point-to-Point	50 Ohm Driver	50 Ohm	2 SRAMs	50 Ohm	On Die @ IXP2800 (CIN Inputs)
D (Write)	T-Topology/Daisy-Chain	50 Ohm Driver	50 Ohm	2 SRAMs	50 Ohm	@ T Point
Q (Read)	T-Topology	SRAM	50 Ohm	2 SRAMs	50 Ohm	On Die @ IXP2800
Control WPE/RPE	T-Topology	30 Ohm Driver	34 Ohm	2 SRAMs	35 Ohm	@ T Point
Control BWE	T-Topology/Daisy-Chain	30 Ohm Driver	34 Ohm	2 SRAMs	35 Ohm	@ T Point

4.4.3 QDR Signal Mapping

Table 18. QDR SRAM Signal Mapping (Sheet 1 of 2)

IXP28XX Signals	Top SRAM 1 (2Mx9)	Bottom SRAM 2 (2Mx9)	Termination V_{TT}=0.75 V	Top SRAM 3 (2Mx9)	Bottom SRAM 4 (2Mx9)	Termination V_{TT}=0.75 V
QDRn_A[23:0]	A[23..0]	A[23..0]	–	A[23..0]	A[23..0]	PU35Ω Center Termination at T-junction[1]
QDRn_K_H[1:0] QDRn_K_L[1:0]	K0, K0#	K0, K0#	PU50Ω	–	–	–
QDRn_K_H[1:0] QDRn_K_L[1:0]	–	–	–	K1, K1#	K1, K1#	PU50Ω
QDRn_C_H[1:0] QDRn_C_L[1:0]	C0, C0#	C0, C0#	On-die at IXP28XX Receiver	–	–	–
QDRn_C_H[1:0] QDRn_C_L[1:0]	–	–	–	C1, C1#	C1, C1#	On-die at IXP28XX Receiver

Table 18. QDR SRAM Signal Mapping (Sheet 2 of 2)

IXP28XX Signals	Top SRAM 1 (2Mx9)	Bottom SRAM 2 (2Mx9)	Termination V_{TT}=0.75 V	Top SRAM 3 (2Mx9)	Bottom SRAM 4 (2Mx9)	Termination V_{TT}=0.75 V
QDRn_Q_H[16:9]	–	–	–	Q[7:0]	Q[7:0]	On-die at IXP28XX Receiver
QDRn_Q_H[8]	–	–	–	Q[8]	Q[8]	On-die at IXP28XX Receiver
QDRn_Q_H[7:0]	Q[7:0]	Q[7:0]	On-die at IXP28XX Receiver	–	–	–
QDRn_Q_H[8]	Q[8]	Q[8]	On-die at IXP28XX Receiver	–	–	–
QDRn_D_H[16:9]	–	–	–	D[7:0]	D[7:0]	PU50Ω
QDRn_D_H[17]	–	–	–	D[8]	D[8]	PU50Ω
QDRn_D_H[7:0]	D[7..0]	D[7..0]	PU50Ω	–	–	–
QDRn_D_H[8]	D[8]	D[8]	PU50Ω	–	–	–
QDRn_RPS_L[0]	R#	–	–	R#	–	PU35Ω Center Termination at T-junction
QDRn_WPS_L[0]	W#	–	–	W#	–	PU35Ω Center Termination at T-junction
QDRn_RPS_L[1]	–	R#	–	–	R#	PU35Ω Center Termination at T-junction
QDRn_WPS_L[0]	–	W#	–	–	W#	PU35Ω
QDRn_BWS_L[0]	BW#	BW#	PU35Ω	–	–	–
QDRn_BWS_L[1]	–	–	–	BW#	BW#	PU35Ω
V_{DDQ}= 1.5	V_{DDQ}=1.5 V	V_{DDQ}=1.5 V	–	V_{DDQ}=1.5 V	V_{DDQ}=1.5 V	–
V_{DD_Core}=1.3 V	V_{DD_Core}= 1.8 V	V_{DD_Core}= 1.8 V	–	V_{DD_Core}= 1.8 V	V_{DD_Core}= 1.8 V	–
QDRn_ZQ[1:0]	Z_Q=250Ω to GND	Z_Q=250Ω to GND	–	Z_Q=250Ω to GND	Z_Q=250Ω to GND	–
VREF_QDRn	V_{ref}=0.75	V_{ref}=0.75	–	V_{ref}=0.75	V_{ref}=0.75	–

1. Termination is not required for all topologies. Signal Integrity simulations should be performed to determine if the termination is required.

4.4.4 ClamShell Configuration of SRAMs

When it is necessary to use more than one SRAM device to achieve a certain memory size capacity, the SRAMs can be arranged in either a Width-Expansion configuration or a Depth-Expansion configuration. Clam-shelling—that is, locating two devices on opposite sides of the PCB—is possible in either case of width-expansion or depth-expansion. However, it is important to check whether the particular signal addressed is properly mirrored or no in the SRAM part used so that it can be routed properly. If it is not mirrored then the signal can be routed as is where one SRAM is

accessed first and second last leading to a daisy-chain configuration. Alternatively, a via could be inserted in between the two SRAMs to create a T-Topology configuration which might be the proper choice.

4.4.5 QDR SRAM Input/Output Timing Specifications

The following sections describe the input and output timing requirements for the IXP28XX network processor QDR I/O buffer. All timings are with respect to a 233-MHz clock and the QDR interface running at 466 MT/s. The timing is referenced from the rising edge of C/C# or K/K# for the receiver and the transmitter, respectively.

4.4.5.1 IXP2800 Input Timing

The IXP28XX network processor input timings provide for the setup and hold-time requirements of the network processor's receiver only when it is receiving data from the QDR SRAM (Driver) during the READ cycle operation. The output timing needed for this operation for the driver side (QDR SRAM), is described in the specification sheet of the SRAM provided by the SRAM manufacturer.

For further information about IXP2800 input timing, refer to the *Intel® IXP2800 and IXP2850 Network Processors Datasheet*.

4.4.5.2 IXP2800 Output Timing

The IXP28XX network processor output timings provide for the output timing requirements of the network processor's driver when it is sending data to the QDR SRAM (Receiver) in the ADDRESS, WRITE, and CONTROL operations. The setup-and-hold time requirements of the receiver (QDR SRAM) side needed for these operations is described in the specification sheet of the SRAM provided by the SRAM manufacturer.

For further information regarding IXP2800 output timing, refer to the *Intel® IXP2800 and IXP2850 Network Processors Datasheet*.

4.4.6 QDR Signal Group Package Trace Length

In order to obtain the best timing margin, trace length-match all signals to within ±25 mils including the package substrate trace routing length. All QDR package trace lengths are provided in Table 35.

4.5 QDR SRAM Routing Rules

4.5.1 QDR Trace Requirements

The most important design detail of the QDR interface is to accurately length-match all signals from the controller to the pins of the SRAM device. This allows the control and data signals to reach the pins of the SRAM and the IXP28XX network processor (for read) at the same time. In the case of read data being returned to the IXP28XX network processor this makes it easy to find a common data valid window for all signals to be captured by the controller. During initialization of the QDR channel the DLL in the receive path can be programmed to find a suitable capture clock to strobe the read data. Refer to the *IXP2800 Hardware Initialization Reference Manual* for more details.

It is important to note here that ALL nets within one signal group must be length matched among each other to within ±25mils, or preferably to within ±10mils. This is achievable and has been done. This means that all Address signals must have the same length to within ±25mils and similarly for the rest of the signal groups. This requirement is more critical in the K-Clock and C-Clock signals which have to be routed with extreme care.

What is meant by length here is the total length of the net including the package trace length plus the PCB board trace length from the Driver Die-Pad to the Receiver Die-Pad. This total length on one net must be matched to the total length of each net in the same group. In essence, the Address nets must be length matched together, the Data-OUT nets must be matched together, and so on. However, the length of a Data-OUT net, for example, needs does not need to be matched to an Address net etc.

A complete listing of package trace lengths for all nets in all groups would be available in a separate spreadsheet. This spreadsheet can be used to do the length matching of the nets.

The following are QDR trace requirements:

- All signals must be length-matched from the controller to each QDR SRAM pin.
  - For topologies that implement a balance “T” topology, you only account for the length of one arm of the “T” when performing the length matching.
- All signal lines must be matched to within 25 mils.
  - You must compensate for controller package substrate routing, otherwise signal lines must be matched to within 25 mils. The package substrate lengths are provided in Section 4.12.

Note: It is strongly recommended that a simulation analysis of the final layout be performed to ensure all timing requirements are being satisfied. This will catch any length-matching mistakes that may have been introduced during trace length matching.

4.5.2 QDR SRAM Address Topology

The Address signals are properly mirrored in the SRAM part. This makes the balanced T-Topology with matched branches the favorable configuration for Address signals. However, some Address pins may not lend themselves to be routed as a balanced T-topology. A T-topology with un-matched branches might become necessary in this case leading to a T-topology with daisy-chain branches. We recommend to exert every effort to use balanced T-topology for the address with 4 SRAM loads for adequate signal integrity and timing margin.

Figure 27 illustrates T-topology for QDR address signals.

Figure 27. QDR Address Signals — Balanced T-Topology

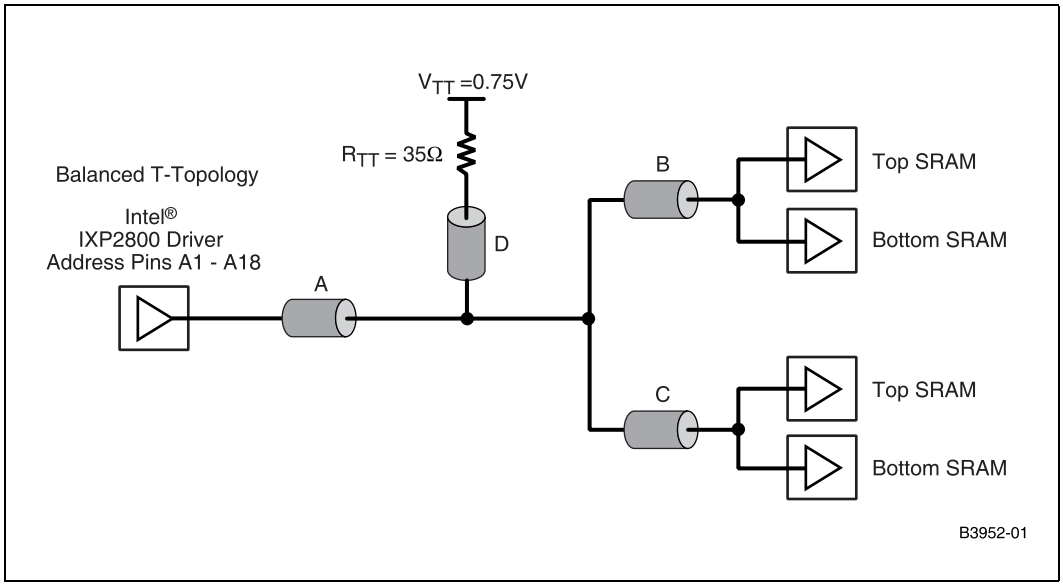


Figure 28. QDR Address Routing — T-Topology with Daisy-Chain Branches

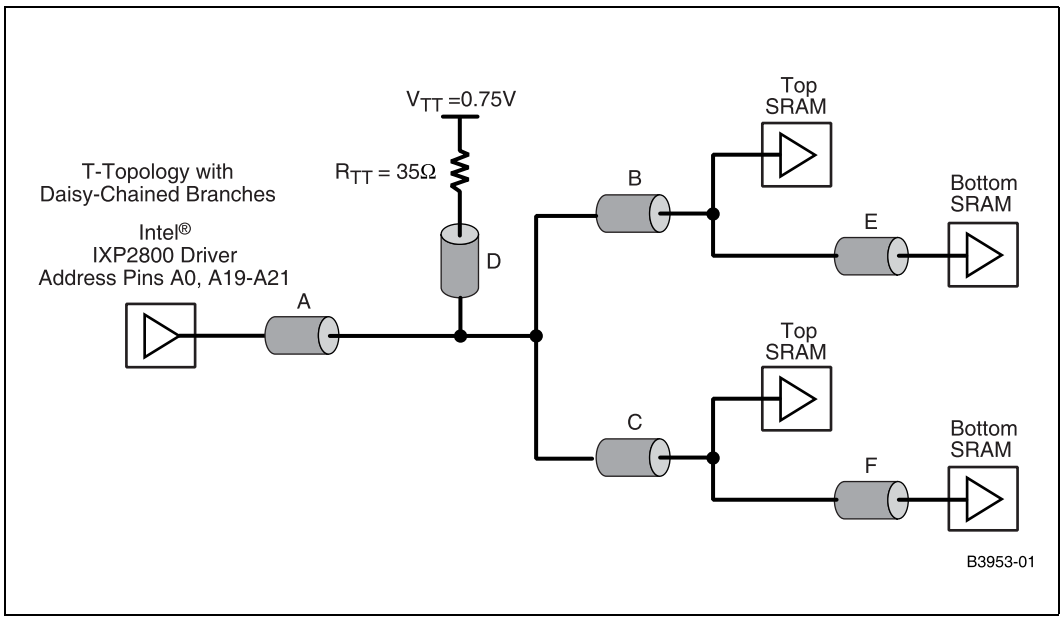


Table 19 provides routing guidelines for the QDR address signal group.

Table 19. QDR Address Signal Group Routing Guidelines

Parameter	Routing Guideline
Signal Group	Address
Topology	Balanced-T topology
Reference Plane	Ground
Characteristic Trace Impedance	
Main Trunk	34 Ω ±5%
Branches	60 Ω ±5%
RTT	35 Ω ±1%
Nominal Trace Width	
Main Trunk	10 mils
Arms of the T	3.5 mils
Nominal Trace Separation	15 - 20 mils
Group Spacing	Isolation from all other signals is 20 - 25mils.
Trace length P[1] +A to SRAMs	Should be matched to K-Clk trace length minus 0.9 inches. Maximum = 11.0 inches Trace length from ball to ball for all Address nets should be matched for the entire group to within 25 mils.
Trace length B, C	As short as possible; B and C should match. Maximum B + E = 1.0 inches Maximum C + F = 1.0 inches
Trace length D	As short as possible; Maximum = 100 mils
Trace length E, F	As short as possible. Maximum B + E = 1.0 inches Maximum C + F = 1.0 inches
Maximum via count per signal	As small as possible; Maximum = 12 vias
Length tuning method	All address signals matched within ±25 mils, where length includes package length compensation (P+A)

1. P refers to the package length.

Figure 29 illustrates routing for a QDR address signal trace width/spacing.

Figure 29. QDR Address Signal Trace Width/Spacing Routing

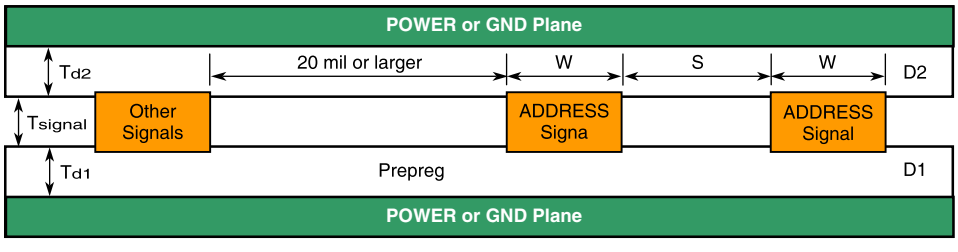


Table 20 lists the QDR address stack-up signal cross-section details.

Table 20. QDR Address Stack-up Signal Cross-section Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	Address	Main Trunk = 10 Branches = 3.5	0.5	15 - 20	5.0	5.7	3.5	3.8	20 - 25

4.5.3 QDR SRAM D (Data Out) Topology

For Data Bus to work successfully at 233MHz only x9 SRAM parts need to be used and not x18 parts for multiple loads applications. Thus the data bus (READ and WRITE) should be split in two halves each with a 9bit including the parity bit. The loads for each Data signal must be maintained at 2 SRAMs only that are clam-shelled together so that they electrically constitute one load only.

As mentioned in section 3 on SRAM clam-shelling, some signals are not fully mirrored in the SRAM part. Data-OUT is an example of these un-mirrored signals. Therefore, for Data-OUT signals a daisy-chain configuration would be used for its topology. A better choice, however, is to use a T-topology for Data-OUT whenever it is possible.

Figure 30 illustrates the routing topology for QDR SRAM D (Data Out).

Figure 30. D (Data Out) Routing Topology

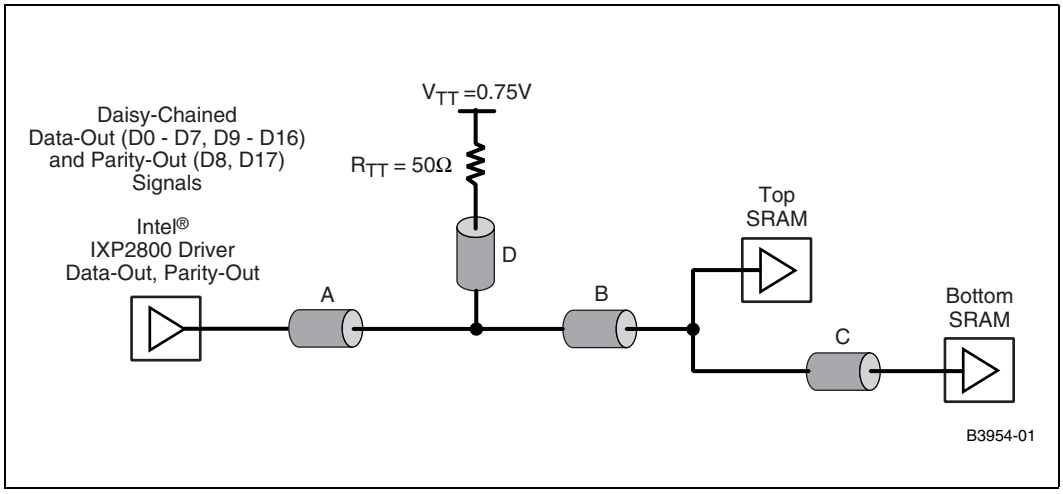


Table 21 provides routing guidelines for the QDR D signal group.

Table 21. QDR D Signal Group Routing Guidelines

Parameter	Routing Guideline
Signal Group	D
Topology	Daisy Chain or Matched-T topology
Reference Plane	Ground
Characteristic Trace Impedance	50 Ω ±10%
RTT	50 Ω ±1%
Nominal Trace Width	5 mils
Nominal Trace Separation	8 - 15 mils
Group Spacing	Isolation from all other signals is 20 mils.
Trace length P[1] +A to SRAMs	Should be matched to K-Clk trace length minus 0.5 inches. Maximum = 11.0 inches
Trace length B	As short as possible. Maximum = 0.4 inches
Trace length C	Maximum = 0.5 inches
Trace length D	As short as possible; Maximum = 1.0 inch
Maximum via count per signal	As small as possible; Maximum = 7 vias
Length tuning method	All D signals matched within ±25 mils, where length includes package length compensation (P+A)

1. P refers to the package length.

Figure 31 illustrates the routing for QDR D signal trace width/spacing.

Figure 31. QDR D Signal Trace Width/Spacing Routing

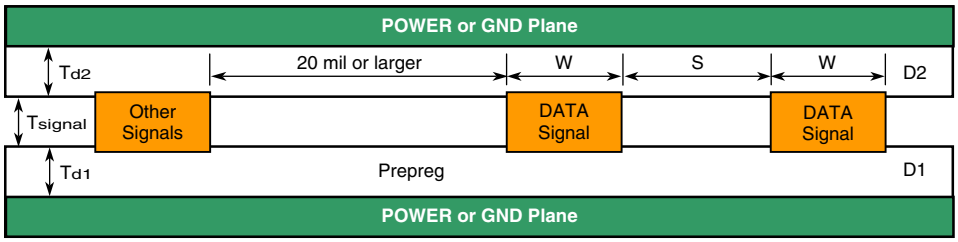


Table 22 lists the QDR D stack-up signal cross-section details.

Table 22. QDR D Stack-up Signal Cross-section Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	D	5	0.5	8 - 15	5.0	5.7	3.5	3.8	20 - 25

4.5.4 QDR SRAM Q (Data In) Topology

For Data Bus to work successfully at 233MHz, especially the READ signal, only x9 SRAM parts need to be used and not x18 parts for multiple loads. Thus the data bus (READ and WRITE) should be split in two halves each with a 9bit including the parity bit. The loads for each Data signal must be maintained at 2 SRAMs only that are clam-shelled together so that they electrically constitute one load only.

Figure 32 illustrates QDR SRAM Q (Data In) topology.

Figure 32. Q (Data In) Routing Topology

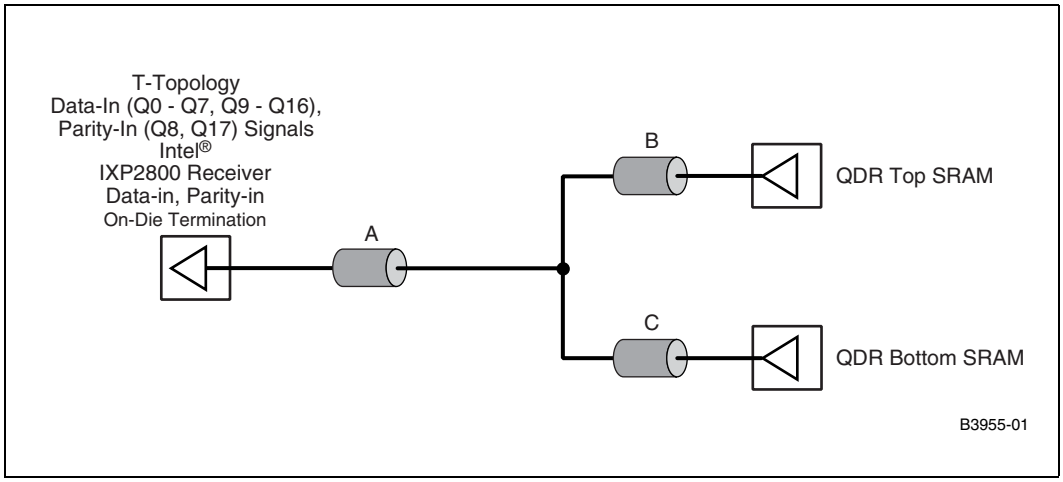


Table 23 provides routing guidelines for the QDR Q (Data In) signal group.

Table 23. QDR Q (Data In) Signal Group Routing Guidelines

Parameter	Routing Guideline
Signal Group	Q
Topology	Matched T-topology
Reference Plane	Ground
Characteristic Trace Impedance	50 Ω ±10%
RTT	50 Ω ±1% on-die termination at the IXP28XX receiver
Nominal Trace Width	5 mils
Nominal Trace Separation	8 - 15 mils
Group Spacing	Isolation from all other signals is 20 - 25 mils.
Trace length P[1] +A to SRAMs	Should be matched to CIN-Clk (return clock) trace length. Maximum = 11.0 inches
Trace length B, C	As short as possible. B and C must match. Maximum B = 0.25 inches Maximum C= 0.25 inches
Maximum via count per signal	As small as possible; Maximum = 7 vias
Length tuning method	All Q signals matched within ±25 mils, where length includes package length compensation (P+A)

1. P refers to the package length.

Figure 33 illustrates routing for QDR Q signal trace width/spacing.

Figure 33. QDR Q Signal Trace Width/Spacing Routing

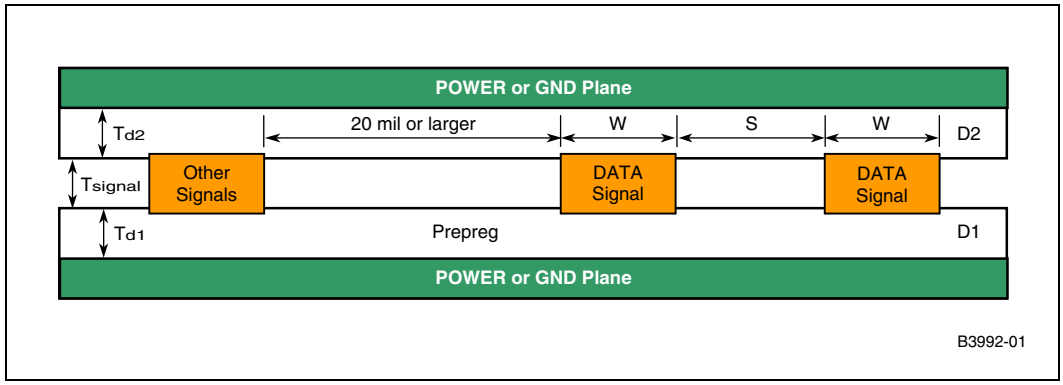


Table 24 lists the QDR Q stack-up signal cross-section details.

Table 24. QDR Q Stack-up Signal Cross-section Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	Q	5	0.5	20 - 25	5.0	5.7	3.5	3.8	20 - 25

4.5.5 QDR SRAM K, K# Clock Topologies

The K input clock registers address and control inputs on the rising edge. Data is registered on the rising edge of K and the rising edge of K#, which is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock's rising edges.

The K-Clock signals have 2 SRAM loads and the signals are mirrored in the SRAM part. Thus, the topology of choice for the K-Clocks is a point-to-point topology with two SRAMs clam-shelled.

Figure 34 illustrates the routing topology for QDR K and K#.

Figure 34. QDR K and K# Routing Topology

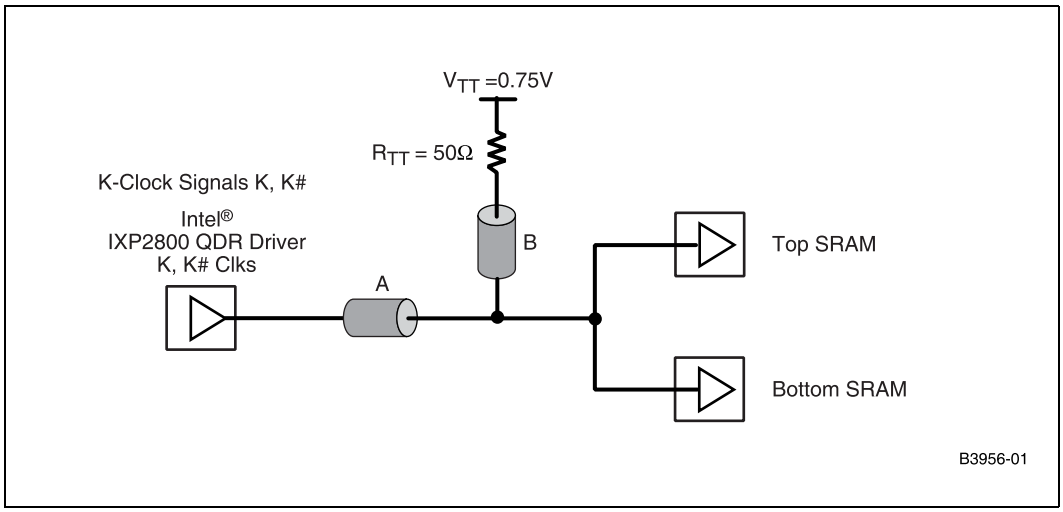


Table 25 provides routing guidelines for the QDR K and K# signal groups.

Table 25. QDR K and K# Signal Group Routing Guidelines

Parameter	Routing Guideline
Signal Group	K, K#
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	50 Ω ±10%
RTT	50 Ω ±1%
Nominal Trace Width	5 mils
Nominal Trace Separation	20 mils
Group spacing	Isolation from all other signals is 20 - 25 mils
Trace length P[1] +A to SRAMs	Trace length from ball to ball should be within 25 mils for all K, K# nets.
Trace length B	As short as possible. Maximum = 1.0 inches
Maximum via count per signal	As short as possible. Maximum = 6 vias
Length tuning method	K and K# signals matched within ±25 mils to (Data-Out + 0.5 in.), (Address + 0.9 in.), and (Control + 0.5 in.) signals, where length includes package length compensation (P+A)

1. P refers to the package length.

Figure 35 illustrates routing for QDR K and K# signal trace width/spacing.

Figure 35. QDR K and K# Signal Trace Width/Spacing Routing

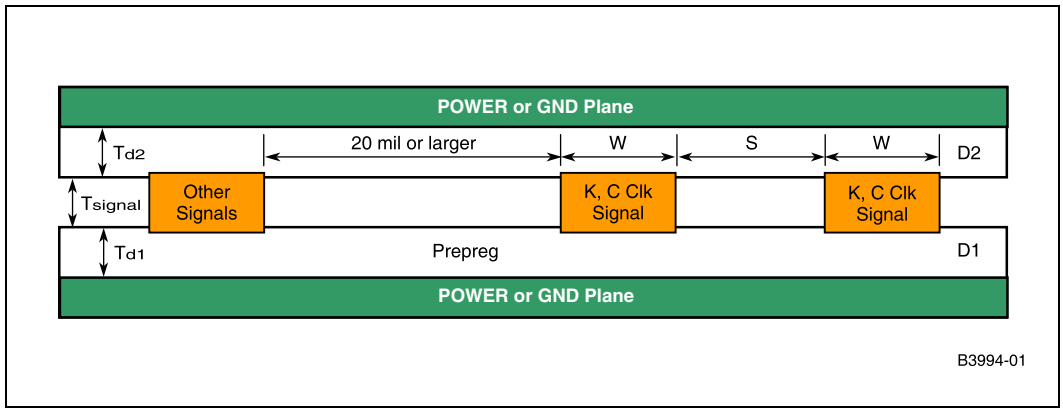


Table 26 lists the QDR K-Clock stack-up signal cross-section details.

Table 26. QDR K-Clock Stack-up Signal Cross-section Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	K-Clock	5	0.5	20 - 25	5.0	5.7	3.5	3.8	20 - 25

4.5.5.1 Relationship between Address, Control, Data-OUT and K-Clock

The trace lengths of all members the K-Clocks net group should be matched to each other to within ±10 mils. The K-Clock is used to sample Address, CONTROL, and Data-OUT simultaneously.

The K-Clock has only two SRAM loads with no stubs (point-to-point topology). The Data-OUT has two SRAM loads. However, it has either one long stub between the two SRAMs in case of daisy chain configuration, or two shorter stubs in case of a T-Topology configuration. The Address signal has 4 SRAM loads in a T-Topology configuration. The CONTROL signals are similar in topology to the Data-OUT signal.

Because these signals have different topology and/or different number of loads, the flight time of each would be different. However, the K-Clock must be used to sample the Data-OUT, CONTROL, and Address at the same time. Therefore it becomes necessary to match their flight times with respect to each other. Matching their flight times means adjusting their trace lengths with respect to each accordingly. If the trace length of on of these three signals is fixed the individual trace length of each one of the other signals must be controlled according to the following K-Clk to Data-Out relationship formula:

K-Clk-Pkg-trace-length + K-Clk-trunk-length =
D-Pkg-trace-length + D-trunk-length + 500 mil

Similarly, the following formula applies for the *K-Clk/Address* relationship:

K-Clk-Pkg-trace-length + K-Clk-trunk-length =
Address-Pkg-trace-length + Address-trunk-length + 900 mil

It is important to mention that the above two formulas are not independent but rather interrelated and must be satisfied simultaneously. If adjustments are made to the lengths or topologies of these signals then it is strongly recommended that simulations are performed to ensure that the signals are properly aligned.

4.5.6 QDR SRAM C, C#, CIN, CIN# Clock Topologies

This output clock pair provides a user-controlled means of tuning SRAM device output data. The rising edge of C is used as the output timing reference for first output data. The rising edge of C# is used as the output reference for second output data. Ideally, C# is 180 degrees out of phase with C.

Figure 36 illustrates the routing topology for QDR C, C#, CIN, and CIN#.

Figure 36. QDR C, C#, CIN, and CIN# Routing Topology

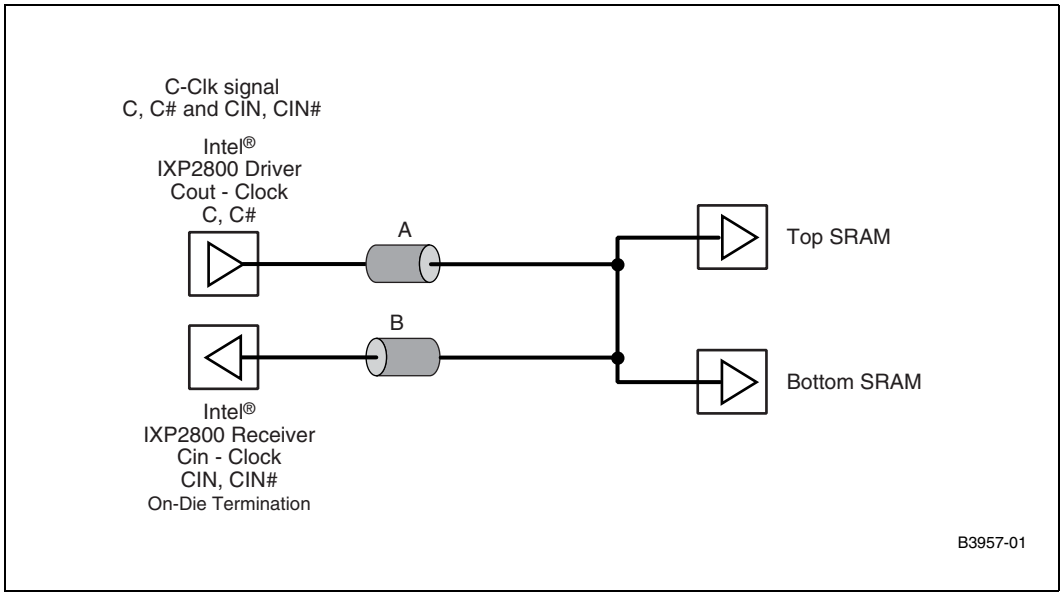


Table 27 provides routing guidelines for the QDR C, C#, CIN, and CIN# signal groups.

Table 27. QDR C, C#, CIN, and CIN# Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guideline
Signal Group	C, C#, CIN, CIN#
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	50 Ω ±10%
RTT	50 Ω ±1% on-die termination at IXP28XX receiver
Nominal Trace Width	5 mils
Nominal Trace Separation	20 - 25 mils
Group spacing	Isolation from all other signals is 20 mils

Table 27. QDR C, C#, CIN, and CIN# Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guideline
Trace length Pkg[1] + A to SRAMs	Roughly matched to B Maximum = 11.0 inches.
Trace length B	Should be matched to Q trace length Maximum = 11.0 inches
Maximum via count per signal	As small as possible. Maximum = 6 vias
Length tuning method	All C and C# signals should be length-matched among each other to within ±25 mils

Figure 37 illustrates the routing for QDR C, C#, CIN, and CIN# signal trace width/spacing.

Figure 37. QDR C, C#, CIN, CIN# Signal Trace Width/Spacing Routing

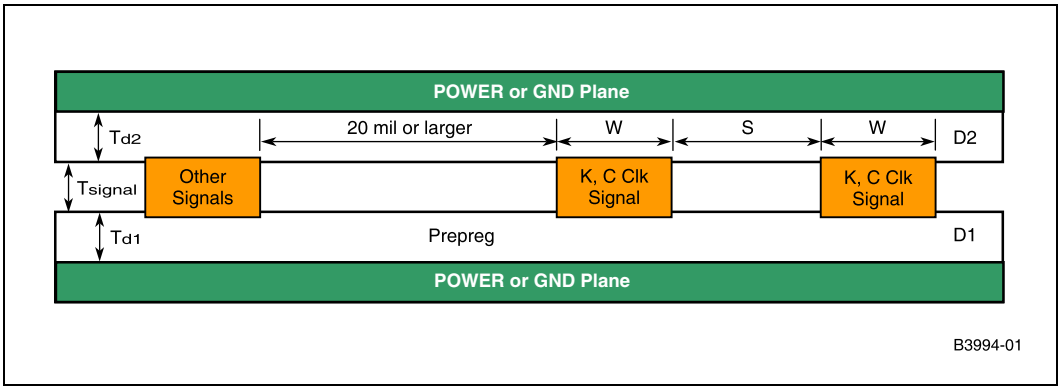


Table 28 lists the QDR C and CIN clock signal trace width/spacing routing details.

Table 28. QDR C and CIN Clock Signal Trace Width/Spacing Routing Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	C-Clock	5	0.5	20 - 25	5.0	5.7	3.5	3.8	20 - 25

The trace lengths of the *C-Clocks (*C0, C0#, C1, and C1#) should be matched to each other to within ±25 mils. Similarly, the trace lengths of the *CIN-Clocks (*CIN0, CIN0#, CIN1, and CIN1#) should be matched to each other to within ±25 mils. However, the individual trace length of each *CIN-Clock* must be controlled according to the following *CIN-Clk/Q* relationship formula:

CIN/CIN#-Clk-trace-length (SRAM pin to IXP28XX C-IN pin)
= Q-trace-length

4.5.7 QDR SRAM RPE#, WPE#, BWE# Control Topologies

There are three types of control signals, and each is active low: Write Port Enable (WPE#), Read Port Enable (RPE#), and Byte Write Enable (BWE#). These signals have to be carefully connected, depending on how the four SRAMs are configured. The Read and the Write Port Enables can be thought of as Address. For example, the lower read port would go to the lower address SRAMs. The byte-writes go with groups of nine bits of data, and the use of byte-write replaces a read-modified write operation.

Control signals are usually grouped with the Address signals because of the functional similarity between the two groups. However they have two SRAM loads only rather than 4 as it is the case for Address. Thus the driver buffer strength, termination resistance, trace impedance, and trace spacing would be the same as in the Address. Only the trace length would be different and similar to the Data-OUT for flight time matching purposes.

Alternatively, these signals can be treated as the Data-OUT signals due to their similarity in the number of loads. In this case, the driver buffer strength, the termination resistance, the trace impedance, and the trace spacing, and trace length would be similar to those of the Data-OUT signal.

Figure 38 illustrates the routing topology for the QDR control RPE# and WPE# signals.

Figure 38. QDR Control RPE# and WPE# Signals Routing Topology

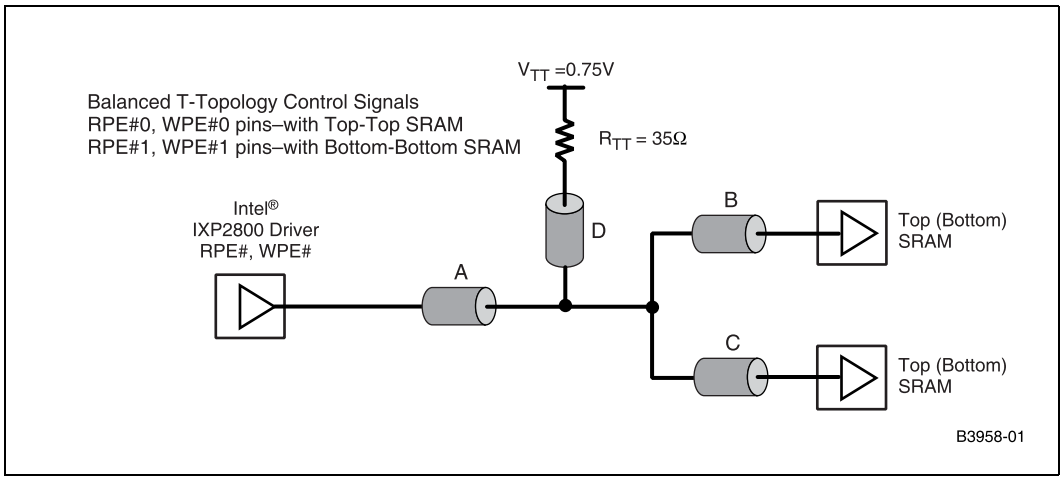


Table 29 provides routing guidelines for the QDR control RPE# and WPE# signal groups.

Table 29. QDR Control RPE# and WPE# Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guideline
Signal Group	CONTROL RPE#, WPE#
Topology	Balanced-T topology
Reference Plane	Ground
Characteristic Trace Impedance	33 Ω ±10%
RTT	35 Ω ±1%
Nominal Trace Width	5 mils
Nominal Trace Separation	15 mils or more

Table 29. QDR Control RPE# and WPE# Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guideline
Group Spacing	Isolation from all other signals is 20 - 25mils.
Trace length P[1] +A to SRAMs	Should be matched to K-Clk trace length minus 0.5 inches. Maximum = 11.0 inches
Trace length B, C	As short as possible. Maximum B = 1.0 inches Maximum C = 1.0 inches
Trace length D	As short as possible; Maximum = 1.0 inch
Maximum via count per signal	As small as possible; Maximum = 7 vias
Length tuning method	All CONTROL signals matched within ±25 mils, where length includes package length compensation (P+A)

1. P refers to the package length.

Figure 39 illustrates routing for QDR control RPE# and WPE# signal trace width/spacing.

Figure 39. QDR Control RPE# and WPE# Signal Trace Width/Spacing Routing

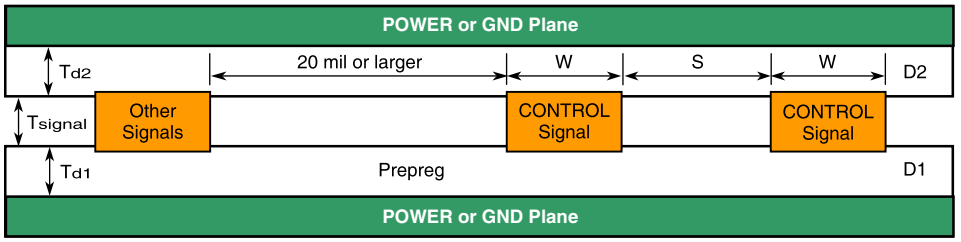


Table 30 lists the QDR CONTROL stack-up signal cross-section details.

Table 30. QDR CONTROL Stack-up Signal Cross-section Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	CONTROL	5	0.5	8 - 15	5.0	5.7	3.5	3.8	20 - 25

Figure 40 illustrates the routing topology for QDR control BWE# signals.

Figure 40. QDR Control BWE# Signals Routing Topology

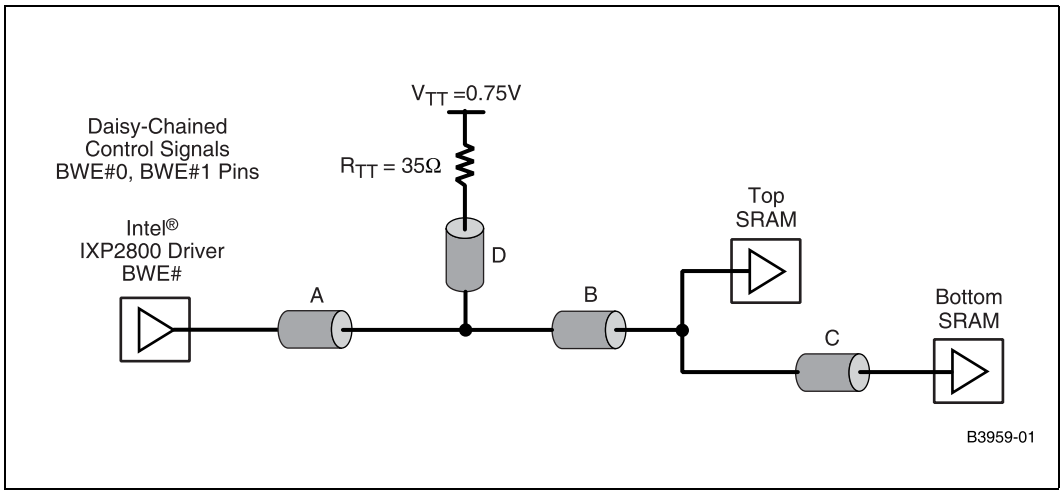


Table 31 provides routing guidelines for the QDR control BWE# signal group.

Table 31. QDR Control BWE# Signal Group Routing Guidelines

Parameter	Routing Guideline
Signal Group	CONTROL BWE#
Topology	Daisy Chain or Balanced-T topology
Reference Plane	Ground
Characteristic Trace Impedance	33 Ω ±10%
RTT	35 Ω ±1%
Nominal Trace Width	5 mils
Nominal Trace Separation	15 mils or more
Group Spacing	Isolation from all other signals is 20 - 25mils.
Trace length P[1] +A to SRAMs	Should be matched to K-Clk trace length minus 0.5 inches. Maximum = 11.0 inches
Trace length B	As short as possible. Maximum = 0.4 inches
Trace length C	Maximum = 0.5 inches
Trace length D	As short as possible; Maximum = 1.0 inch
Maximum via count per signal	As small as possible; Maximum = 7 vias
Length tuning method	All CONTROL signals matched within ±25 mils, where length includes package length compensation (P+A)

1. P refers to the package length.

Figure 41 illustrates routing for control BWE# signal trace width/spacing.

Figure 41. Control BWE# Signal Trace Width/Spacing Routing

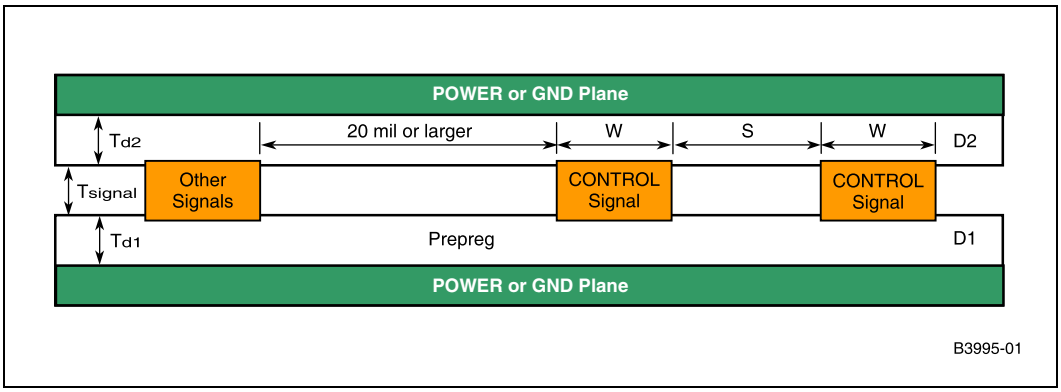


Table 32 lists the QDR CONTROL stack-up signal cross-section details.

Table 32. QDR CONTROL Stack-up Signal Cross-section Details

Parameter	QDR Signal	Trace Width (W) [mils]	Trace Thickness (Tsignal) [mils]	Trace Spacing (S) [mils]	D1 Thickness (TD1) [mils]	D2 Thickness (Td2) [mils]	Er(D1)	Er(D2)	Spacing between signal groups [mils]
Value	CONTROL	5	0.5	8 - 15	5.0	5.7	3.5	3.8	20 - 25

4.6 QDR SRAM V_{REF} Generation

The best known method for V_{REF} generation is to derive the 0.75-V reference through a resistive divider from the 1.5-V QDR supply. The following solutions can be used to generate the V_{REF} supply:

- Figure 42 depicts a circuit that creates V_{REF} through a resistive divider which is then fed through an optical amplifier to create a noise-sensitive voltage reference.
- Figure 43 and Figure 44 show a resistor divider circuit to generate the V_{REF} supply.

Figure 42. QDR SRAM V_{REF} Generation

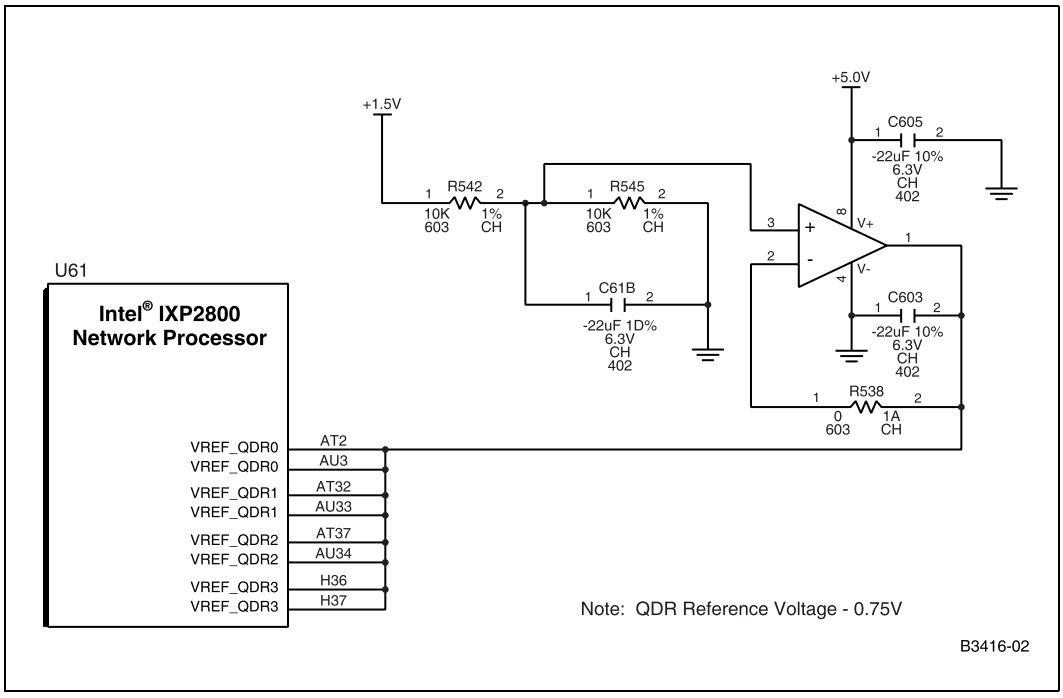
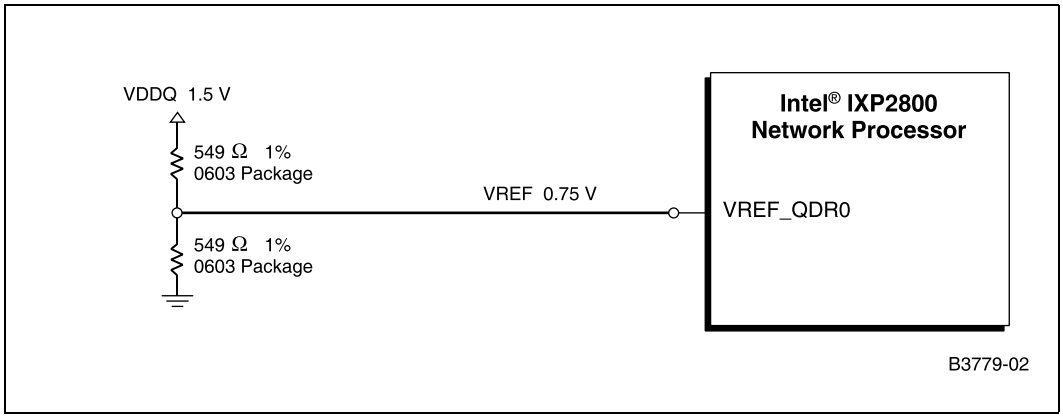
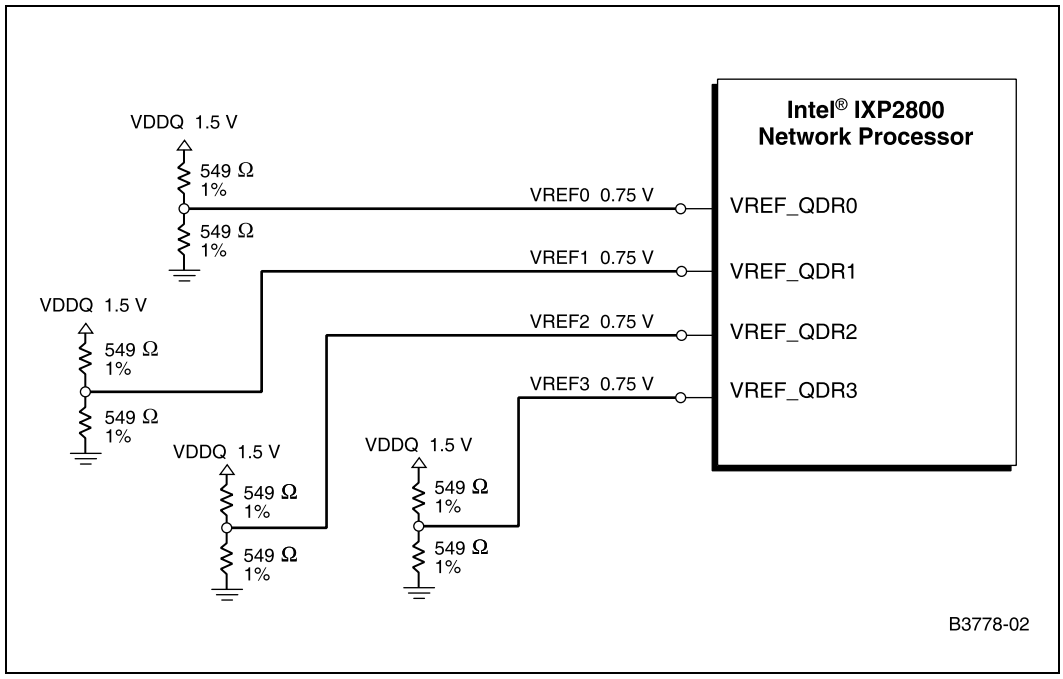


Figure 43. Resistive QDR V_{REF} Divider Example



Note: A separate resistive voltage divider should be used for each QDR SRAM channel; Figure 44 shows an example of a voltage QDR V_{REF} divider for each QDR channel.

Figure 44. Voltage QDR V_{REF} Divider Example for Each QDR Channel



4.7 TCAM/SRAM/Coprocessor Interface

In certain cases it may be desirable to implement a connector in the QDR interface to accommodate a third-party QDRII-LA1-compliant coprocessor or an upgradable QDR memory module. The Intel BKM for this is to provide the IXP28XX QDR interface through a 2 x 57 shrouded 114-pin Mictor* connector. The connector has all the QDR signals from a single channel and JTAG interface. In addition, power is provided in the form of 1.5 V, 1.8 V, and 3.3 V. The current for the 1.5 V and 1.8 V is limited to 0.5 A and 2.5 A, respectively. This current supply provides the power support for up to four QDRII SRAMs.

4.7.1 TCAM/SRAM/Coprocessor Interface — Base Card Side

This part of the interface runs between the ingress IXP28XX network processor and the Mictor* connector on the base card side. All traces are matched in length to within ±10 mils and have the same nominal line impedance of 50 Ω.

4.7.1.1 Interface Topologies

This part of the interface has a topology of a point-to-point configuration between the IXP28XX network processor's I/O buffer and the Mictor* connector. The rest of the topologies are found on the TCAM/SRAM/coprocessor card and are different for different signals (Address, D, etc.).

4.7.1.1.1 Address, D, CONTROL, Q, and K-Clocks Signals

Figure 45 illustrates topologies for address, D, CONTROL, Q, and K-clocks.

Figure 45. Address, D, CONTROL, Q, and K-Clocks Topologies

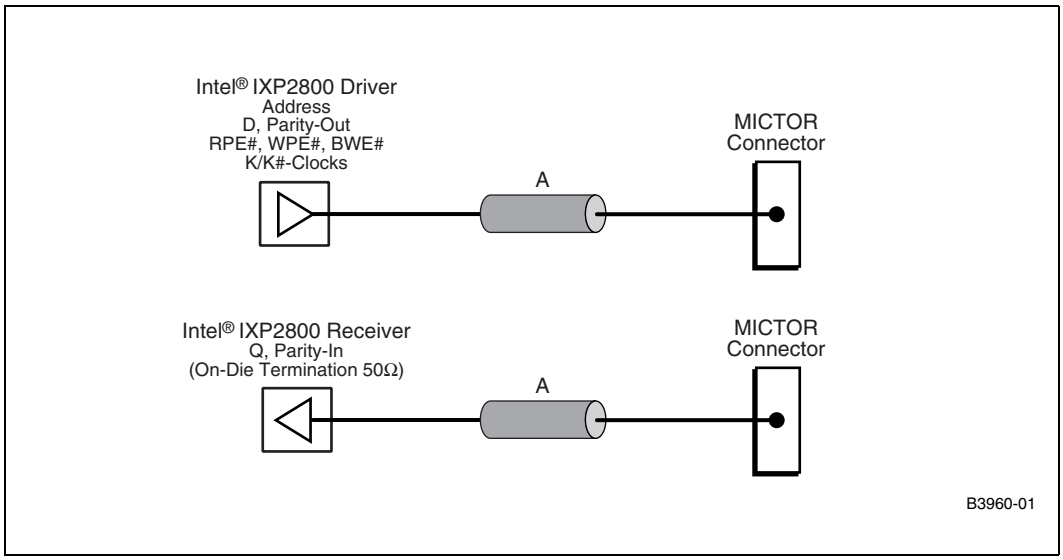


Table 33 provides routing guidelines for the TCAM/SRAM/coprocessor interface base card.

Table 33. TCAM/SRAM/Coprocessor Interface Guidelines (Address, D, CONTROL, Q, and K-Clocks)

Parameter	Routing Guideline
Signal Group	TCAM/SRAM/coprocessor Address, D, CONTROL, Q, and K-Clocks
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	50 Ω ±5%
Nominal Trace Width	5 mils
Nominal Trace Separation for group	8 to 15 mils
Group spacing	Isolation from non-QDR and non-group-related signals is 20 mils.
IXP28XX breakout guideline	3.5 mils with 4 mil space for a maximum of 400 mils
A or B trace length	Maximum = 5.0 inches (IXP28XX pin to Mictor* pin) The trace length from ball-to-ball should be within 25 mils.

4.7.1.1.2 C, C#, CIN, and CIN# Clocks Signals

Figure 46 illustrates the topologies for the C, C#, CIN, and CIN# clocks.

Figure 46. C, C#, CIN, and CIN# Clocks Topologies

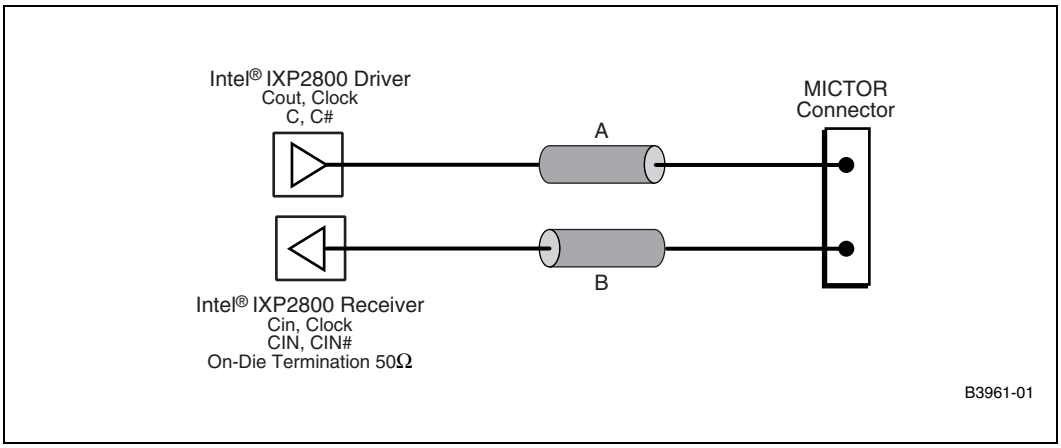


Table 34 provides routing guidelines for the TCAM/SRAM/coprocessor interface base card.

Table 34. TCAM/SRAM/Coprocessor Interface Guidelines (C, C#, CIN, and CIN# Clocks)

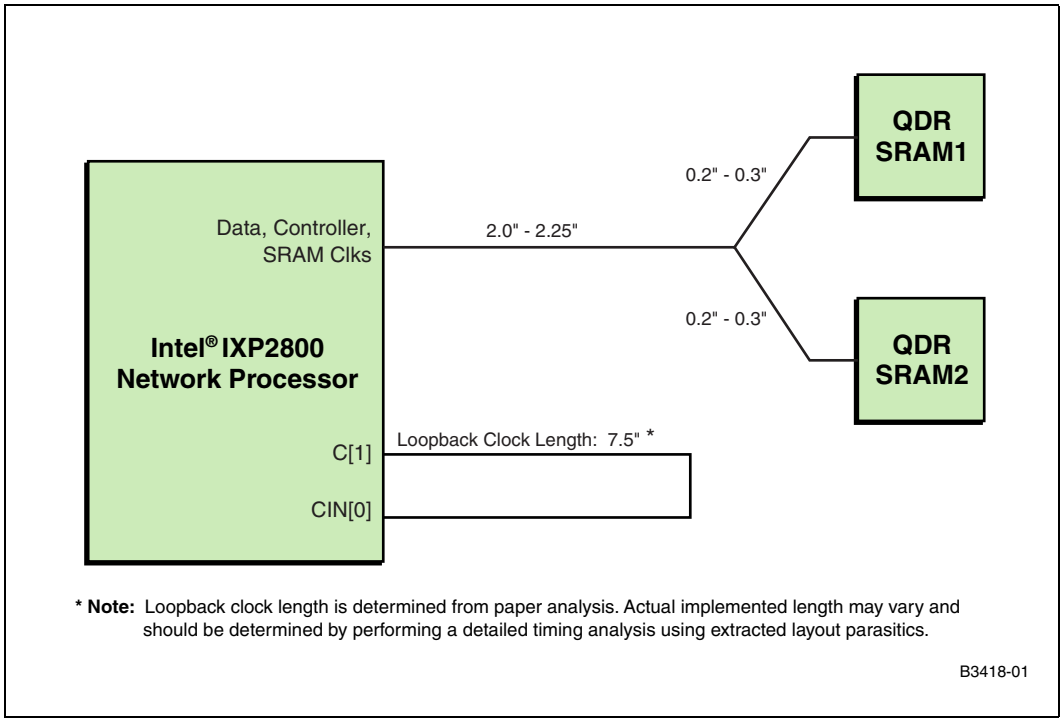
Parameter	Routing Guideline
Signal Group	TCAM/SRAM/coprocessor C, C#, CIN, and CIN# Clocks
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	50 Ω ±5%
Nominal Trace Width	5 mils
Nominal Trace Separation for group	8 to 15 mils
Group spacing	Isolation from non-QDR and non-group-related signals is 20 mils.
IXP28XX breakout guideline	3.5 mils with 4-mil space for a maximum of 400 mils
A or B trace length	Maximum = 5.0 inches (IXP28XX pin to Mictor* pin) The trace length from ball-to-ball should be within 25 mils.

4.8 IXDP2800 QDR Implementation Guidelines

The following is a list of QDR SRAM routing topologies that have been implemented on the IXDP2800 Advanced Development Platform:

- Simulation shows that no termination is required for two-device “clamshell” topology, as shown in Figure 47.
- Performance is at 250+ MHz.

Figure 47. QDR SRAM Routing Recommendations



4.8.1 Routing for a Four-QDR SRAM Topology

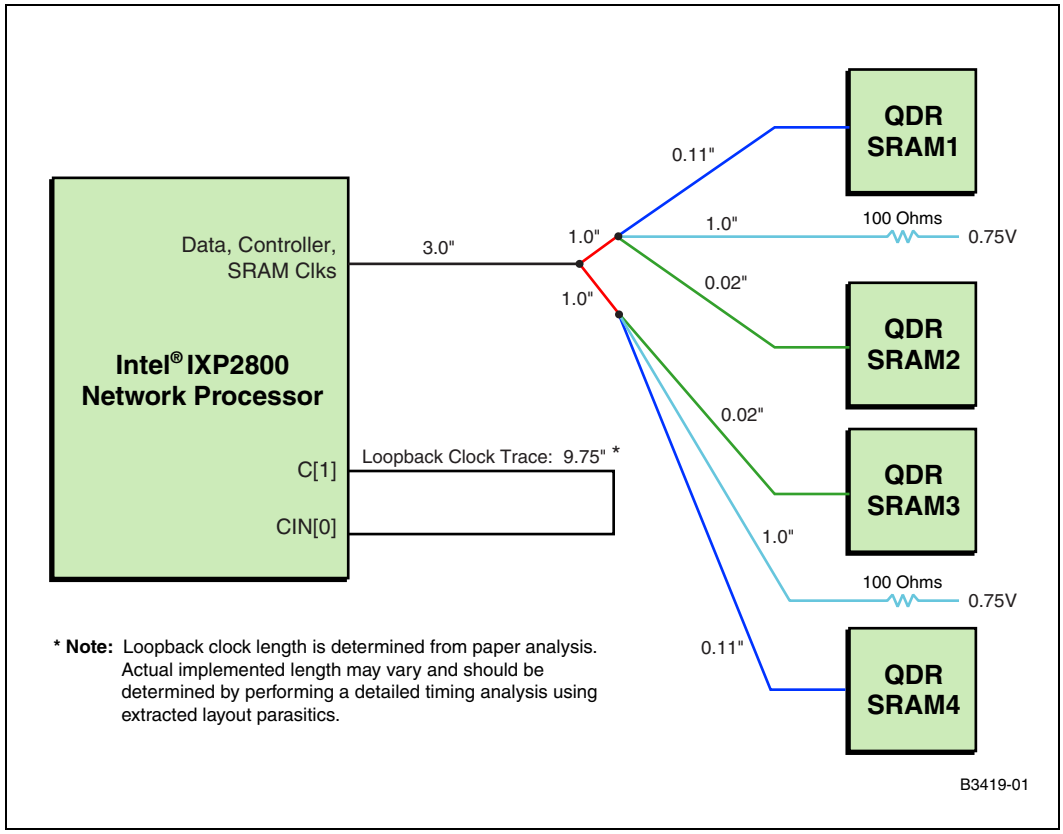
For topologies using four loads during a read, only one SRAM drives the bus, and the stub to the other SRAM causes a reflection that effectively reduces the data-valid window. The maximum operating frequency is effectively, approximately 167 MHz.

The following are routing recommendations for four QDR SRAM topologies:

- Only terminate lines on IXP28XX network processor drives.
- OUTCLK/OUTCLK_L is 4.5 inches.
- The x9 devices are recommended for topologies that use four loads, and for 200+ MHz operations.
- The x18 devices are recommended for 167+ MHz operations.

Figure 48 illustrates routing recommendations for a four-QDR SRAM load.

Figure 48. Four-QDR SRAM Load Routing Recommendations



4.8.2 Determining Loopclock Length for QDRII SRAM Used by IXDP2800 Advanced Development Platform

This section describes how to determine functional platforms with the best possible timing margin by using two- and four-load examples. Although SRAM devices are used in the examples, the principles and calculations described apply to any load on the channel, including TCAM.

Figure 49 shows the optimal interconnections for the two QDR load conditions. It is optimal in that no termination resistors are required. By removing termination resistors, power is conserved, BOM count is reduced, and board layout is simplified. Using one clock pair (C_H[0], C_L[0], K_H[0], K_L[0]) from the IXP28XX network processor to drive the SRAM devices and the other pair (C_H[1], C_L[1]) to clock the Q data back into the IXP28XX network processor, provides the widest timing margin. Each clock is effectively point-to-point, reducing the load of each clock and decreasing uncertainty.

Figure 49. Example Interconnects on the IXP28XX Network Processor, with a Two-QDRII SRAM Load per Channel

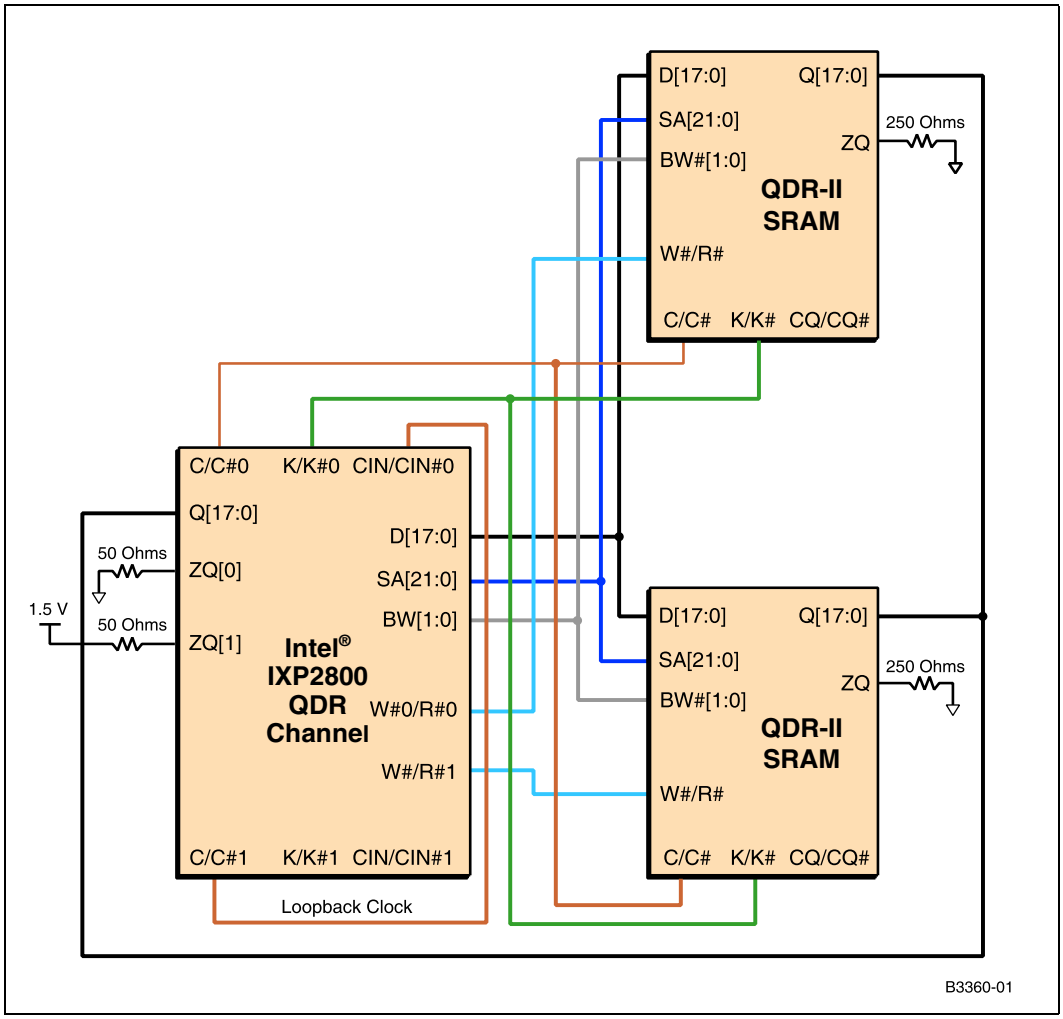


Figure 50 illustrates the trace length from the IXP28XX network processor to SRAM (C, K, SA, D, and R/W_BW).

Figure 51 illustrates the trace length from SRAM to the IXP28XX network processor (Q data).

Figure 50. Trace Length from IXP28XX Network Processor to SRAM (C, K, SA, D, and R/W_BW)

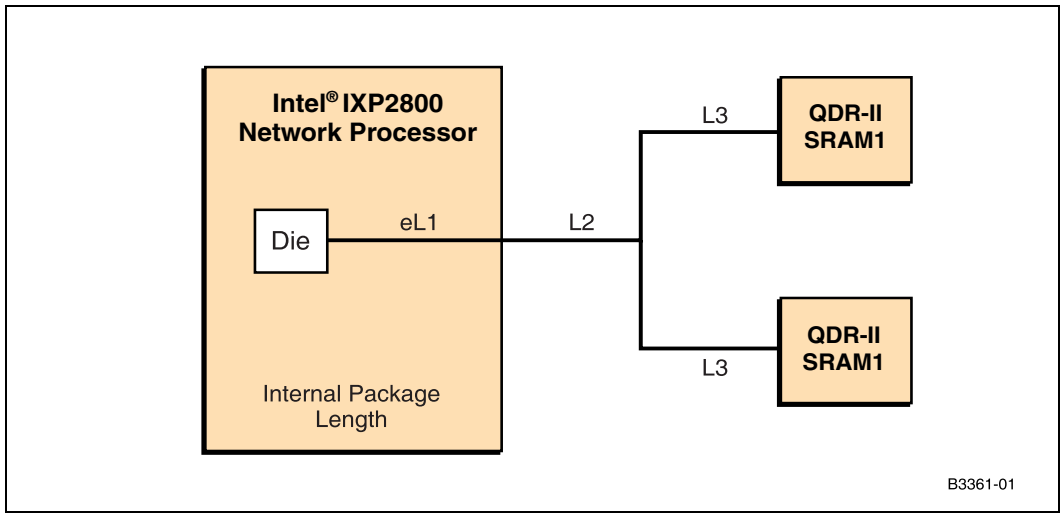
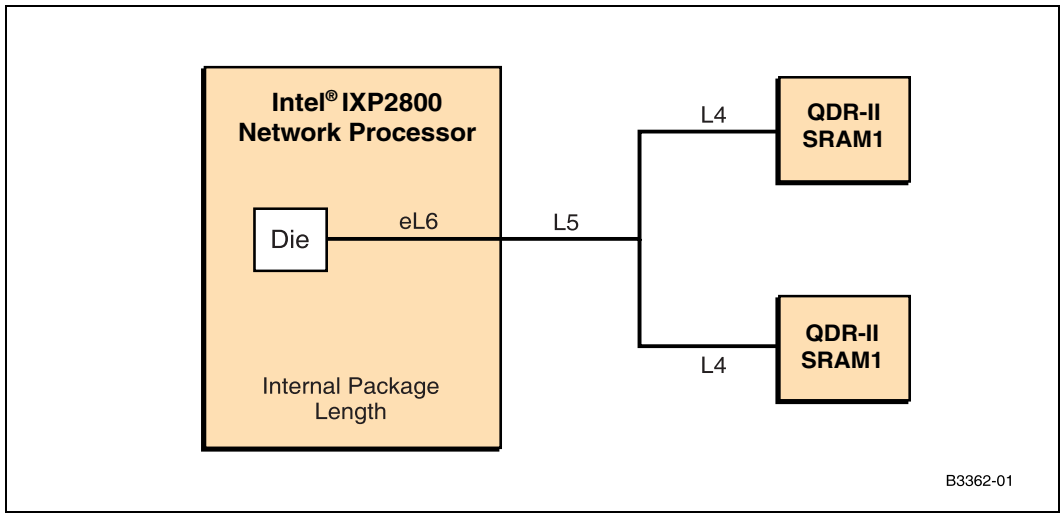


Figure 51. Trace Length from SRAM to IXP28XX Network Processor (Q Data)



In Figure 50 and Figure 51 L# is the length of etch on the printed circuit board (PCB). The label, eL# is the effective length of internal etch. Effective length must be considered since the signals propagate faster in the package than on the PCB, due to the materials used in each. The QDRII SRAM internal package length need not be considered, because the package is internally matched by length.

Each channel is independent; therefore, only one channel needs to be considered at a time. Ideally, the rising edge of the CIN clock is coincident with the rising edge of Q data, i.e., the loopback clock should arrive at the network processor die at the same time as the Q data, even though they follow different paths.

In the case of the loopback clock, only the C clock length from the IXP28XX network processor to SRAM and the Q data length from SRAM to the network processor need to be considered. It is assumed that the total C and C_N etch lengths are identical. In practice, they may vary by a mil or

two, in which case the average should be used. Further, the Q data total length is the average of all Q lengths, so Q Length = avg(eL6 + L5 + L4). The Q length should not be allowed to vary by more than ±0.10 inches.

The basic method for determining the length of the loopback clock is C Length + Q Length + Capacitive Load Delta C&Q. The maximum length in any case cannot be more than one bit-time. This must then be further constrained to allow for PVT variations; hence, at 200 MHz or for a bit-time of 2.5 ns, the total flight time delay must not exceed 2.0 ns, i.e., (2.5 ns bit-time – 500ps PVT).

The effective internal package length of the IXP28XX network processor can be calculated. The propagation delay in the network processor package is approximately 154 ps/inch. The propagation delay on a PCB can be calculated as 84.735 * Square Root (Er) where Er is the Dielectric Permittivity of the substrate. For FR4 epoxy glass at 250 MHz, the delay calculation is approximately 4.2, meaning that the propagation delay of a generic PCB is approximately 174 ps/inch. Consult your PCB vendor for the recommended Er at a specific frequency. Knowing this, eL can be calculated in inches. The IXP28XX network processor internal package length is given in µm and the conversion is inches = µm/1000/25.4. Hence:

eL = (package_length/1000/25.4) * (154 / 174)

where 174 is substituted with a value based on the user's PCB.

So, if an IXP2800 package length were 18863 µm, eL = 0.657 inches.

L2, L3, L4, and L5 are the actual lengths of the PCB etch in inches.

Now that we know how to calculate lengths, we need to discuss the Capacitive Load Delta term. Since C[0] and Q lines have more capacitance loading than C[1] (loopclock), C[0] and Q slew rates are slower with respect to C[1]. The capacitance per pin for a Micron QDRII SRAM is 5 pF (minimum) to 6 pF (maximum), and the capacitance for an IXP28XX network processor input pin is 5 pF (minimum) to 10 pF (maximum). Therefore, the total capacitive load at the end of the line on C[0] is two SRAMs for 10 pF (minimum) and 12 pF (maximum). The total capacitive load at the end of the line on Q is one IXP28XX network processor for 5 pF (minimum) and 10 pF (maximum). The total capacitive load at the end of the line on C[1] is one IXP28XX network processor for 5 pF (minimum) and 10 pF (maximum). C[0] + Q load is therefore 15 pF minimum, and 22 pF maximum.

The boundary condition deltas (minimum and maximum differences between C[0]+Q – C[1]) are 12 pF (maximum) and 10 pF (minimum). To center the error, select the mean case of 11 pF Capacitive Load Delta C&Q. This delta in capacitance load can be converted to an effective length. It is generally accepted that for a transmission line, Co = Td/Zo where Td was calculated above at 174 ps/inch and Zo is 50 Ω — so the intrinsic capacitance Co = 3.48 pF/inch. Then, the delta load of 11 pF translates into 3.1 extra inches of etch for Capacitive Load Delta C. Effectively, the difference in capacitance is translated into an additional three inches of trace length that must be accounted for in the overall loopclock length. This is a *very important* consideration.

If the user is using a similar PCB dielectric, the formula can be simplified to:

Loopclock Length=[Mean(eL1 + L2 + L3)] + [Mean(L4 + L5 + eL6)] + 3.1 in.

Note: This length can be used as a starting point for layout; however, the final overall length values should be determined by simulating with extracted parasitics from the layout.

4.8.3 QDR SRAM Alternating Routing Layers

The following figures illustrate QDR SRAM alternating routing layers for adjacent QDR clamshell pairs, as implemented on the IXDP2800 Advanced Development Platform:

- Figure 52, “QDR 0 Routing on Layer 13 - Adjacent QDR Clamshell Pairs”
- Figure 53, “QDR 1 Routing on Layer 12 - Adjacent QDR Clamshell Pairs”

Figure 52. QDR 0 Routing on Layer 13 - Adjacent QDR Clamshell Pairs

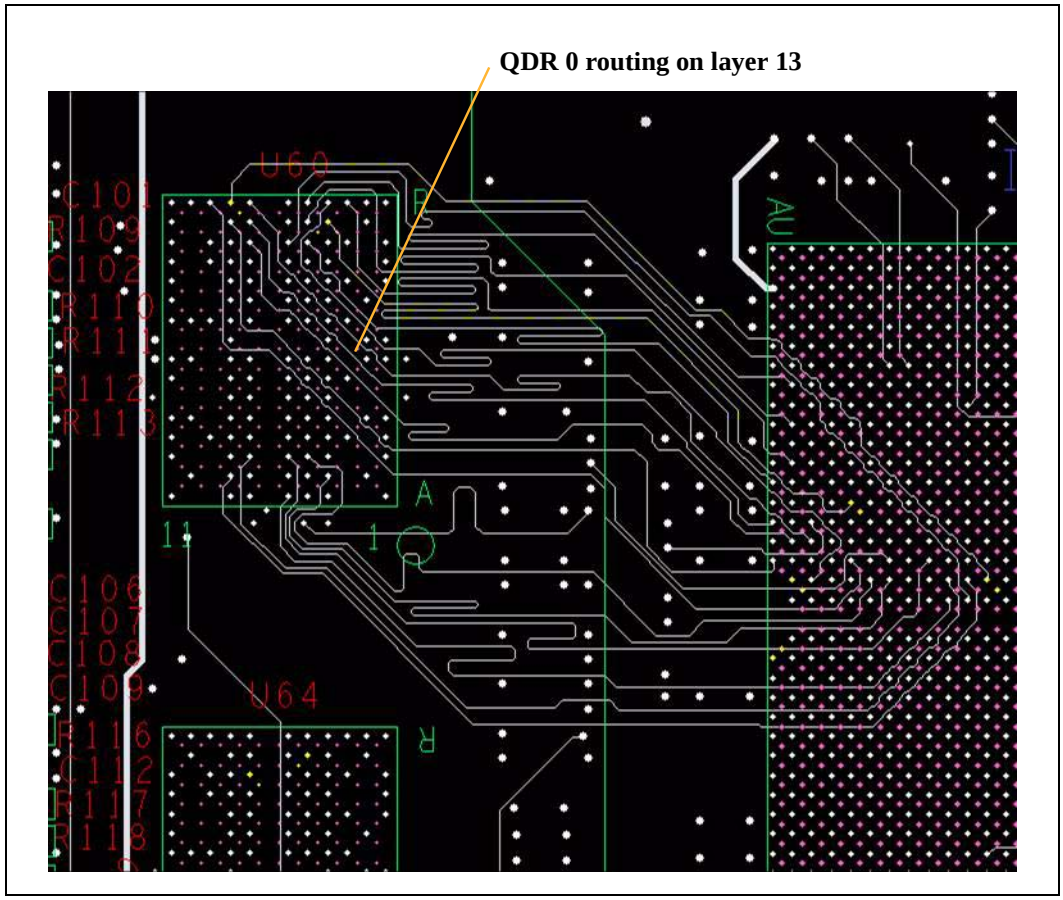
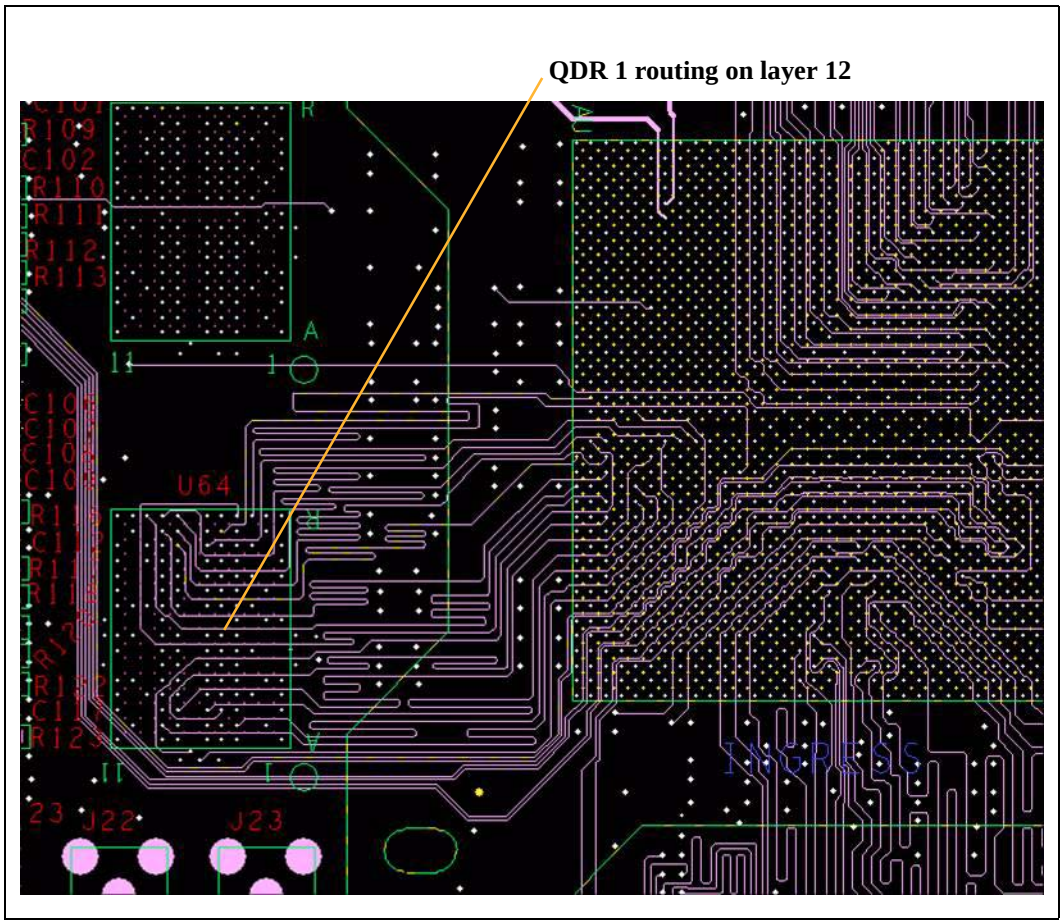


Figure 53. QDR 1 Routing on Layer 12 - Adjacent QDR Clamshell Pairs



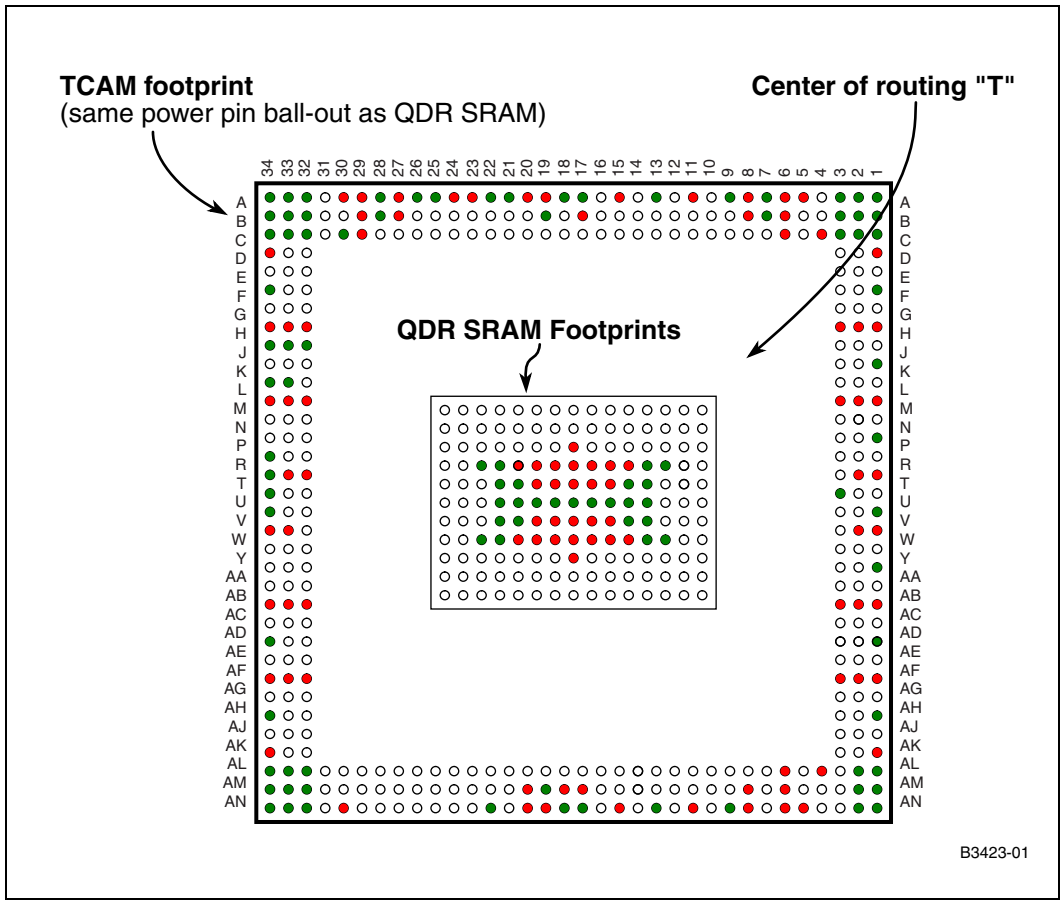
4.9 IXDP2800 TCAM Implementation

This section describes the placement and routing implementation for the TCAM and QDR SRAM.

4.9.1 TCAM and QDR SRAM Placement

Figure 54 illustrates TCAM and QDR SRAM placement.

Figure 54. TCAM and QDR SRAM Placement

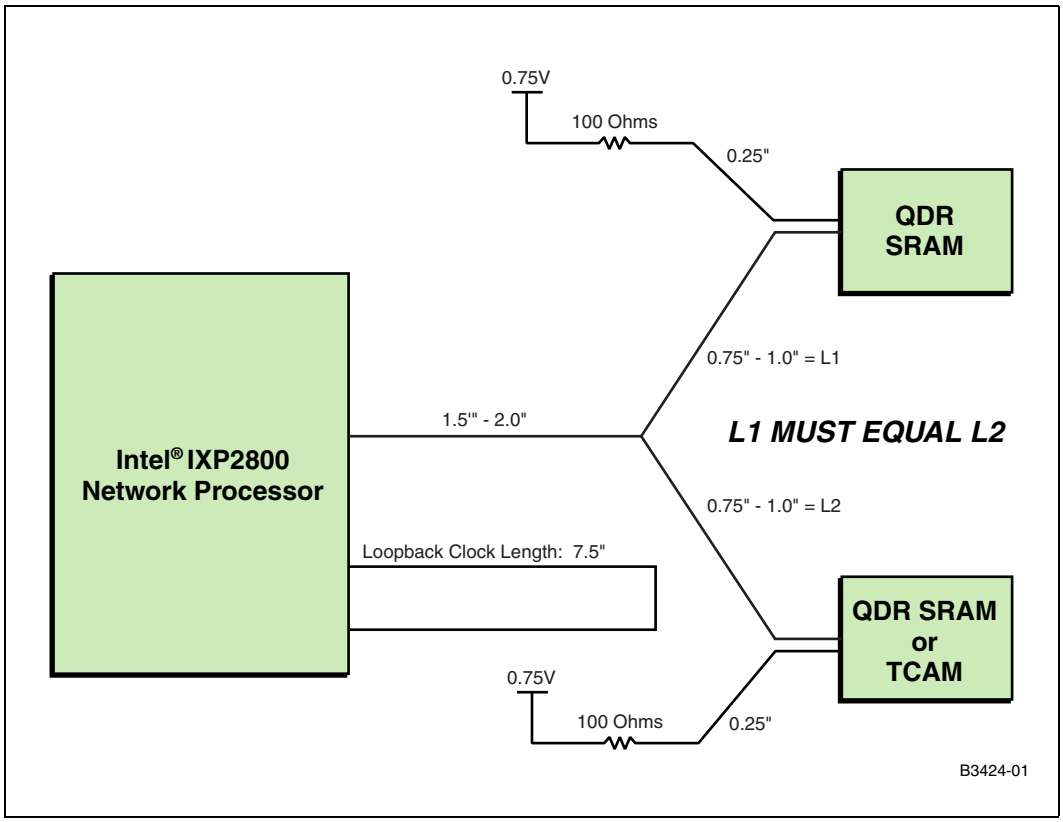


4.9.2 QDR SRAM and TCAM Routing Implementation

Figure 55 illustrates the routing recommendations for QDR SRAM and TCAM, implemented as follows:

- Only terminate lines on IXP28XX network processor drives
- OUTCLK/OUTCLK_L is 4 – 4.5 inches
- 250+ MHz performance

Figure 55. Routing Recommendations for QDR SRAM and TCAM Routing



4.10 QDR SRAM and TCAM Routing

The following figures illustrate QDR SRAM and TCAM routing:

- Figure 56, “QDR Signal from IXP28XX Network Processor to Tee Point on Layer 12”
- Figure 57, “QDR Signal Tee Point Arms Routed on Signal Layers 4 and 13”

Figure 56. QDR Signal from IXP28XX Network Processor to Tee Point on Layer 12

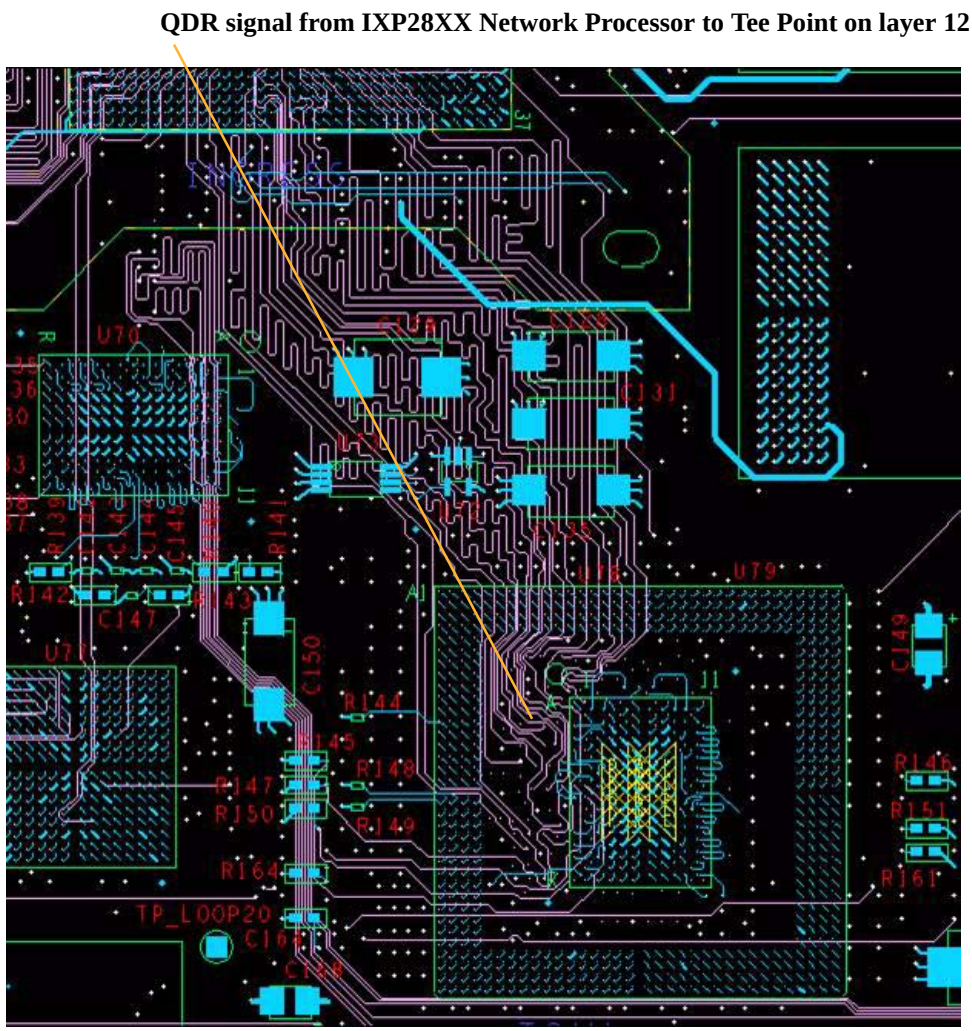
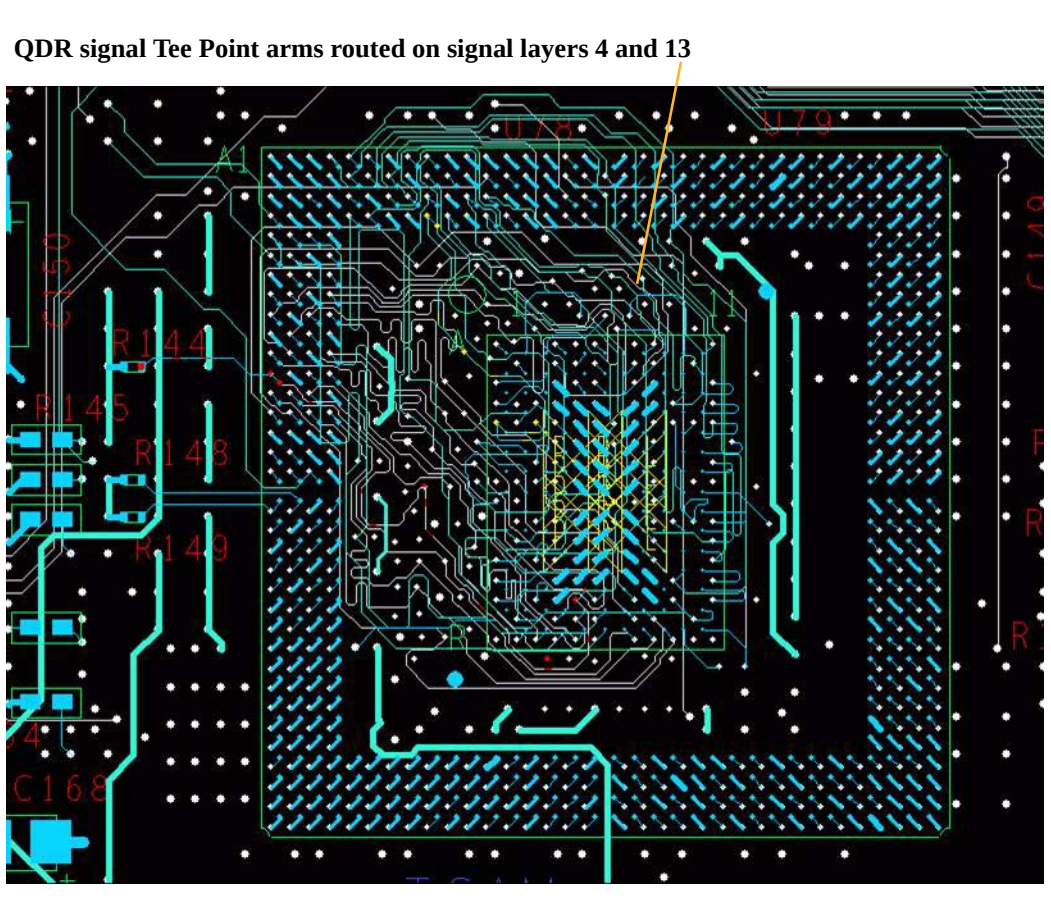


Figure 57. QDR Signal Tee Point Arms Routed on Signal Layers 4 and 13



4.11 QDR SRAM Design Review Checklist

Use the following design review checklist for QDR SRAM schematic reviews:

- For clamshell pairs, the data bus pins are flipped, so the BWS_N signals also must be flipped.
- The byte parity is DQ8 for byte 0.
- The byte parity is DQ17 for byte 1.
- Check for proper ZQ resistor: 50 Ω.
- QDR JTAG pins are 3.3 V on the IXP28XX network processor, but 1.5 V on QDR devices, i.e., a level-shift is necessary.
- The IXP28XX network processor CIN[1] pins are NC from the I/O pad to the SRAM controller internally. Only CIN[0] is used to derive the read capture clock.
  - The CIN[1] pin can be used to terminate the clock and this I/O pad is controllable via the RCOMP registers. Refer to the *Intel® IXP2400 and IXP2800 Network Processor Programmer's Reference Manual* for more details.

4.12 Package Trace Lengths for QDR Signals

Table 35 provides package trace lengths for QDR signals, listed by decreasing lengths in a given logical grouping. Signals in boldface type within the table indicate the start of a logical grouping.

The flight time on the package substrate is 154ps/in which differs from the flight delay of standard FR4, typical 180ps/in. As a result the package routing lengths in Table 35 must be adjusted to compensate for the difference in flight delay between the package and the PCB. For example QDR0_Q_H[16] has a package length of 0.628 in, and the target PCB has a flight delay of 180ps/in. In order to adjust the package length to match the PCB flight delay this length must be multiplied by the ratio of 154/180 or the difference between the package and PCB flight delays. Therefore the trace package routing length that must be accounted for on the PCB is 0.628*(154/180) or 0.537 in.

Note: If the flight delay of the target PCB is not 180 ps/in then the ratio, (154/180), must be modified accordingly, i.e., the denominator would be changed to reflect the actual flight delay.

Table 35. Package Trace Lengths for QDR Signals (Sheet 1 of 4)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
QDR0_Q_H[16]	15.959	0.628	**QDR1_C_H[1]**	12.5	0.492	**QDR2_Q_H[2]**	15.36	0.605
QDR0_Q_H[2]	14.754	0.581	QDR1_C_L[1]	12.5	0.492	QDR2_C_H[1]	15	0.591
QDR0_Q_H[3]	14.63	0.576	QDR1_Q_H[12]	11.965	0.471	QDR2_C_L[1]	15	0.591
QDR0_C_H[1]	13.75	0.541	QDR1_Q_H[10]	11.853	0.467	QDR2_CIN_H[0]	14.5	0.571
QDR0_C_L[1]	13.75	0.541	QDR1_C_H[0]	11.5	0.453	QDR2_CIN_H[1]	14.5	0.571
QDR0_CIN_H[0]	13.5	0.531	QDR1_C_L[0]	11.5	0.453	QDR2_CIN_L[0]	14.5	0.571
QDR0_CIN_H[1]	13.5	0.531	QDR1_Q_H[6]	11.143	0.439	QDR2_CIN_L[1]	14.5	0.571
QDR0_CIN_L[0]	13.5	0.531	QDR1_Q_H[5]	10.627	0.418	QDR2_Q_H[16]	14.295	0.563
QDR0_CIN_L[1]	13.5	0.531	QDR1_Q_H[11]	10.15	0.400	QDR2_Q_H[14]	14.051	0.553
QDR0_Q_H[14]	12.682	0.499	QDR1_CIN_H[0]	10	0.394	QDR2_Q_H[17]	13.729	0.541
QDR0_Q_H[15]	11.914	0.469	QDR1_CIN_H[1]	10	0.394	QDR2_Q_H[3]	12.564	0.495
QDR0_Q_H[1]	11.594	0.456	QDR1_CIN_L[0]	10	0.394	QDR2_Q_H[0]	12.485	0.492
QDR0_C_H[0]	11.5	0.453	QDR1_CIN_L[1]	10	0.394	QDR2_Q_H[1]	11.56	0.455
QDR0_C_L[0]	11.5	0.453	QDR1_Q_H[1]	8.684	0.342	QDR2_C_H[0]	11.1	0.437
QDR0_Q_H[17]	11.359	0.447	QDR1_Q_H[15]	8.362	0.329	QDR2_C_L[0]	11.1	0.437
QDR0_Q_H[0]	10.095	0.397	QDR1_Q_H[13]	7.899	0.311	QDR2_Q_H[15]	9.226	0.363
QDR0_Q_H[4]	9.898	0.390	QDR1_Q_H[8]	7.434	0.293	QDR2_Q_H[13]	8.981	0.354
QDR0_Q_H[13]	8.977	0.353	QDR1_Q_H[16]	7.343	0.289	QDR2_Q_H[4]	8.958	0.353
QDR0_Q_H[5]	8.552	0.337	QDR1_Q_H[9]	7.03	0.277	QDR2_Q_H[5]	8.782	0.346
QDR0_Q_H[11]	7.371	0.290	QDR1_Q_H[3]	6.98	0.275	QDR2_Q_H[12]	7.911	0.311
QDR0_Q_H[8]	7.288	0.287	QDR1_Q_H[17]	6.878	0.271	QDR2_Q_H[8]	7.529	0.296
QDR0_Q_H[10]	7.263	0.286	QDR1_Q_H[7]	6.861	0.270	QDR2_Q_H[11]	7.48	0.294
QDR0_Q_H[12]	7.208	0.284	QDR1_Q_H[4]	6.173	0.243	QDR2_Q_H[10]	6.607	0.260
QDR0_Q_H[7]	6.953	0.274	QDR1_Q_H[14]	6.126	0.241	QDR2_Q_H[7]	6.245	0.246
QDR0_Q_H[6]	6.18	0.243	QDR1_Q_H[0]	5.996	0.236	QDR2_Q_H[9]	6.201	0.244
QDR0_Q_H[9]	5.969	0.235	QDR1_Q_H[2]	5.789	0.228	QDR2_Q_H[6]	6.024	0.237

Table 35. Package Trace Lengths for QDR Signals (Sheet 2 of 4)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
QDR3_Q_H[13]	14.583	0.574	**QDR0_D_H[1]**	15.574	0.613	QDR0_A_H[11]	6.387	0.251
QDR3_CIN_H[0]	13.5	0.531	QDR0_D_H[3]	15.234	0.600	QDR0_WPS_L[1]	6.368	0.251
QDR3_CIN_H[1]	13.5	0.531	QDR0_A_H[5]	13.956	0.549	QDR0_D_H[6]	6.312	0.249
QDR3_CIN_L[0]	13.5	0.531	QDR0_D_H[16]	13.738	0.541	QDR0_A_H[20]	6.193	0.244
QDR3_CIN_L[1]	13.5	0.531	QDR0_A_H[9]	13.512	0.532	QDR0_A_H[8]	6.18	0.243
QDR3_Q_H[4]	13.434	0.529	QDR0_A_H[4]	13.361	0.526	QDR0_BWS_L[1]	6.156	0.242
QDR3_Q_H[5]	11.944	0.470	QDR0_A_H[1]	12.612	0.497	QDR0_A_H[12]	6.043	0.238
QDR3_Q_H[10]	11.479	0.452	QDR0_K_H[1]	12.5	0.492	QDR0_D_H[8]	6.04	0.238
QDR3_Q_H[9]	10.802	0.425	QDR0_K_L[1]	12.5	0.492	QDR0_D_H[10]	6.01	0.237
QDR3_Q_H[6]	10.055	0.396	QDR0_A_H[2]	11.945	0.470	QDR0_A_H[3]	6.004	0.236
QDR3_C_H[0]	10	0.394	QDR0_D_H[12]	11.435	0.450	QDR0_D_H[11]	6	0.236
QDR3_C_H[1]	10	0.394	QDR0_A_H[15]	11.342	0.447	QDR0_A_H[7]	5.997	0.236
QDR3_C_L[0]	10	0.394	QDR0_BWS_L[0]	11.267	0.444	QDR0_D_H[7]	5.992	0.236
QDR3_C_L[1]	10	0.394	QDR0_D_H[4]	10.73	0.422	QDR0_D_H[9]	5.991	0.236
QDR3_Q_H[12]	9.758	0.384	QDR0_D_H[13]	10.495	0.413	QDR0_K_H[0]	1.85	0.073
QDR3_Q_H[11]	9.718	0.383	QDR0_A_H[21]	10.105	0.398	QDR0_K_L[0]	1.85	0.073
QDR3_Q_H[7]	8.695	0.342	QDR0_A_H[22]	9.924	0.391			
QDR3_Q_H[14]	8.056	0.317	QDR0_A_H[6]	9.863	0.388			
QDR3_Q_H[15]	7.971	0.314	QDR0_A_H[13]	9.798	0.386			
QDR3_Q_H[17]	7.617	0.300	QDR0_A_H[16]	9.728	0.383			
QDR3_Q_H[0]	7.132	0.281	QDR0_A_H[19]	9.267	0.365			
QDR3_Q_H[8]	6.984	0.275	QDR0_D_H[15]	8.652	0.341			
QDR3_Q_H[1]	6.465	0.255	QDR0_D_H[2]	8.547	0.336			
QDR3_Q_H[16]	6.308	0.248	QDR0_RPS_L[1]	8.424	0.332			
QDR3_Q_H[3]	6.118	0.241	QDR0_D_H[14]	8.391	0.330			
QDR3_Q_H[2]	6.07	0.239	QDR0_A_H[0]	8.094	0.319			
			QDR0_D_H[17]	7.796	0.307			
			QDR0_D_H[5]	7.775	0.306			
			QDR0_RPS_L[0]	7.722	0.304			
			QDR0_A_H[18]	7.554	0.297			
			QDR0_A_H[23]	7.147	0.281			
			QDR0_A_H[10]	6.968	0.274			
			QDR0_A_H[14]	6.962	0.274			
			QDR0_A_H[17]	6.88	0.271			
			QDR0_WPS_L[0]	6.861	0.270			
			QDR0_D_H[0]	6.521	0.257			

Table 35. Package Trace Lengths for QDR Signals (Sheet 3 of 4)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
QDR1_K_H[1]	11.5	0.453	QDR1_WPS_L[0]	11.256	0.443	QDR2_A_H[2]	9.901	0.390
QDR1_K_L[1]	11.5	0.453	QDR1_A_H[9]	11.255	0.443	QDR2_D_H[0]	9.844	0.388
QDR1_D_H[7]	11.265	0.444	QDR1_D_H[4]	11.255	0.443	QDR2_D_H[3]	9.839	0.387
QDR1_A_H[4]	11.264	0.443	QDR1_D_H[17]	11.25	0.443	QDR2_WPS_L[1]	9.809	0.386
QDR1_A_H[13]	11.257	0.443	QDR1_BWS_L[0]	11.221	0.442	QDR2_D_H[12]	9.755	0.384
QDR1_D_H[9]	11.257	0.443	QDR1_D_H[0]	11.184	0.440	QDR2_A_H[1]	9.603	0.378
QDR1_WPS_L[1]	11.257	0.443	QDR1_K_H[0]	8.5	0.335	QDR2_A_H[20]	9.339	0.368
QDR1_A_H[0]	11.256	0.443	QDR1_K_L[0]	8.5	0.335	QDR2_BWS_L[1]	9.102	0.358
QDR1_A_H[10]	11.256	0.443	QDR1_A_H[15]	7.161	0.282	QDR2_D_H[16]	9.083	0.358
QDR1_A_H[11]	11.256	0.443	QDR1_D_H[6]	6.683	0.263	QDR2_D_H[7]	8.343	0.328
QDR1_A_H[12]	11.256	0.443	QDR1_A_H[5]	6.681	0.263	QDR2_D_H[13]	8.164	0.321
QDR1_A_H[14]	11.256	0.443	QDR1_D_H[2]	6.076	0.239	QDR2_D_H[5]	8.125	0.320
QDR1_A_H[16]	11.256	0.443	QDR1_A_H[23]	6.006	0.236	QDR2_A_H[7]	8.053	0.317
QDR1_A_H[17]	11.256	0.443	QDR1_A_H[19]	6005	0.236	QDR2_A_H[12]	7.756	0.305
QDR1_A_H[18]	11.256	0.443	QDR1_A_H[1]	6.002	0.236	QDR2_A_H[0]	7.345	0.289
QDR1_A_H[2]	11.256	0.443	QDR1_D_H[10]	6	0.236	QDR2_D_H[2]	7.338	0.289
QDR1_A_H[20]	11.256	0.443				QDR2_A_H[22]	7.313	0.288
QDR1_A_H[21]	11.256	0.443	**QDR2_K_H[1]**	16	0.630	QDR2_D_H[11]	7.213	0.284
QDR1_A_H[22]	11.256	0.443	QDR2_K_L[1]	16	0.630	QDR2_BWS_L[0]	6.842	0.269
QDR1_A_H[3]	11.256	0.443	QDR2_D_H[17]	15.997	0.630	QDR2_D_H[8]	6.781	0.267
QDR1_A_H[6]	11.256	0.443	QDR2_D_H[15]	15.403	0.606	QDR2_A_H[14]	6.485	0.255
QDR1_A_H[7]	11.256	0.443	QDR2_A_H[17]	15.149	0.596	QDR2_A_H[19]	6.479	0.255
QDR1_A_H[8]	11.256	0.443	QDR2_D_H[1]	14.881	0.586	QDR2_A_H[18]	6.477	0.255
QDR1_BWS_L[1]	11.256	0.443	QDR2_K_H[0]	14	0.551	QDR2_A_H[9]	6.476	0.255
QDR1_D_H[1]	11.256	0.443	QDR2_K_L[0]	14	0.551	QDR2_A_H[21]	6.475	0.255
QDR1_D_H[11]	11.256	0.443	QDR2_A_H[5]	13.256	0.522	QDR2_D_H[10]	6.475	0.255
QDR1_D_H[12]	11.256	0.443	QDR2_A_H[6]	13.242	0.521	QDR2_A_H[11]	6.474	0.255
QDR1_D_H[13]	11.256	0.443	QDR2_A_H[4]	12.689	0.500	QDR2_D_H[6]	6.474	0.255
QDR1_D_H[14]	11.256	0.443	QDR2_D_H[4]	12.684	0.499	QDR2_D_H[9]	6.474	0.255
QDR1_D_H[15]	11.256	0.443	QDR2_D_H[14]	12.501	0.492	QDR2_RPS_L[1]	6.474	0.255
QDR1_D_H[16]	11.256	0.443	QDR2_A_H[15]	12.346	0.486	QDR2_RPS_L[0]	6.47	0.255
QDR1_D_H[3]	11.256	0.443	QDR2_A_H[16]	11.767	0.463	QDR2_A_H[3]	6.246	0.246
QDR1_D_H[5]	11.256	0.443	QDR2_A_H[13]	11.271	0.444	QDR2_A_H[23]	6.168	0.243
QDR1_D_H[8]	11.256	0.443	QDR2_A_H[8]	11.12	0.438			
QDR1_RPS_L[0]	11.256	0.443	QDR2_WPS_L[0]	10.027	0.395			
QDR1_RPS_L[1]	11.256	0.443	QDR2_A_H[10]	9.927	0.391			

Table 35. Package Trace Lengths for QDR Signals (Sheet 4 of 4)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
QDR3_D_H[9]	15.749	0.620	QDR3_RPS_L[0]	6.957	0.274			
QDR3_K_H[1]	14.5	0.571	QDR3_A_H[9]	6.873	0.271			
QDR3_K_L[1]	14.5	0.571	QDR3_D_H[17]	6.737	0.265			
QDR3_D_H[11]	14.024	0.552	QDR3_D_H[1]	6.659	0.262			
QDR3_A_H[20]	13.941	0.549	QDR3_D_H[15]	6.482	0.255			
QDR3_D_H[10]	13.838	0.545	QDR3_D_H[16]	6.331	0.249			
QDR3_A_H[21]	13.417	0.528	QDR3_D_H[3]	6.247	0.246			
QDR3_A_H[0]	13.118	0.516	QDR3_A_H[3]	6.007	0.236			
QDR3_K_H[0]	12.7	0.500	QDR3_RPS_L[1]	6.007	0.236			
QDR3_K_L[0]	12.7	0.500	QDR3_A_H[19]	6.003	0.236			
QDR3_WPS_L[1]	12.488	0.492	QDR3_A_H[16]	6.002	0.236			
QDR3_A_H[23]	12.2	0.480	QDR3_A_H[7]	6.001	0.236			
QDR3_WPS_L[0]	12.036	0.474	QDR3_A_H[13]	6	0.236			
QDR3_D_H[13]	11.307	0.445	QDR3_A_H[8]	6	0.236			
QDR3_A_H[10]	11.28	0.444	QDR3_A_H[11]	5.996	0.236			
QDR3_A_H[22]	11.264	0.443	QDR3_D_H[2]	5.981	0.235			
QDR3_D_H[12]	11.137	0.438						
QDR3_A_H[6]	10.963	0.432						
QDR3_A_H[1]	10.703	0.421						
QDR3_A_H[4]	10.654	0.419						
QDR3_BWS_L[1]	10.4	0.409						
QDR3_A_H[15]	10.328	0.407						
QDR3_A_H[17]	10.067	0.396						
QDR3_D_H[4]	9.077	0.357						
QDR3_D_H[5]	8.933	0.352						
QDR3_D_H[7]	8.916	0.351						
QDR3_D_H[6]	8.884	0.350						
QDR3_A_H[2]	8.856	0.349						
QDR3_A_H[5]	8.474	0.334						
QDR3_A_H[18]	8.27	0.326						
QDR3_D_H[0]	8.201	0.323						
QDR3_D_H[8]	8.117	0.320						
QDR3_A_H[14]	7.613	0.300						
QDR3_BWS_L[0]	7.177	0.283						
QDR3_D_H[14]	7.148	0.281						
QDR3_A_H[12]	7.102	0.280						

MSF (SPI-4/CSIX/FC) 5

5.1 Media and Switch Fabric Interface

The Media and Switch Fabric (MSF) Interface connects the Intel® IXP2800 or Intel® IXP2850 Network Processor to a physical layer device (PHY) and/or a Switch Fabric Interface. The MSF consists of the following external interfaces:

- Receive and transmit interfaces, each of which can be individually configured for either the SPI-4 Phase 2 (System Packet Interface) to a PHY or the CSIX-L1 protocol to a switch fabric.
- A Flow Control Interface, which provides a point-to-point connection used primarily to pass CSIX-L1 flow control C-Frames either between two network processors or between a network processor and a switch fabric.

The MSF supports 16-bit DDR LVDS signaling for the SPI-4 data path channel and can be configured to support either LVTTL or LVDS (Low-Voltage Differential Signal) signaling for the SPI-4 FIFO status channel. The MSF supports 16-bit LVDS signaling for CSIX-L1 protocol and 4-bit LVDS signaling for the Flow Control interface.

5.1.1 SPI-4.2

SPI-4.2 is an interface for packet and cell transfer between a physical layer (PHY) device and a link layer device (network processor) for aggregate bandwidths of OC-192 ATM and Packet over SONET/SDH (POS), as well as 10 Gbyte/sec Ethernet applications.

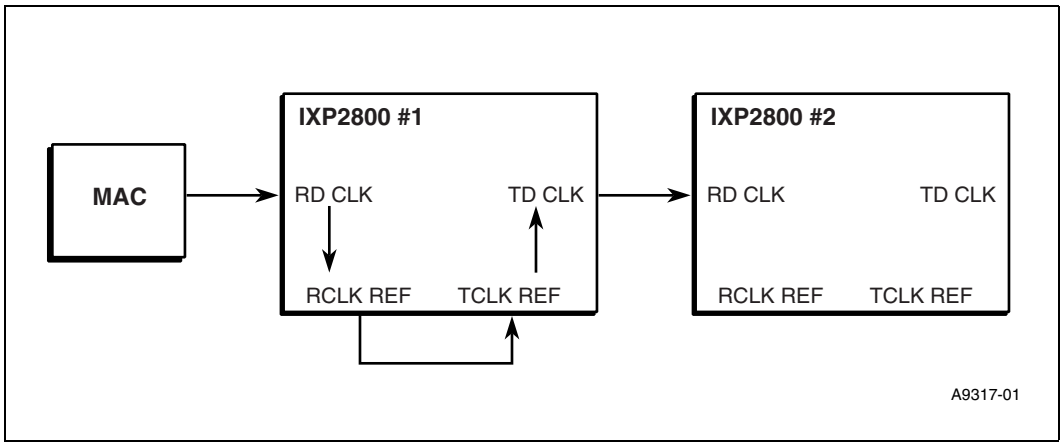
The SPI-4.2 protocol transfers data in bursts of variable length. Associated with each burst is information such as port number (for a multi-port device such as a 10 x 1 GbE), SOP, and EOP. This information is collected by the MSF and passed to the Microengines.

The following implementations do *not* require an extra oscillator to provide a clock for the data that moves between two network processors on the same line card:

- The TD_CLK from network processor 1 to network processor 2 can be created by dividing network processor 1's internal fast clock. The multiplex that selects between the two possible sources of TD_CLK is controlled by a bit in the MSF_Tx_Control control status register (CSR). This option is the more desirable of these implementations.
- Optionally, the MAC device creates an RD_CLK to the first network processor, as shown in Figure 58. RCLK_REF loops back into TCLK_REF for network processor 1 and TCLK_REF is used as the source of the TD_CLK to network processor 2. ***Note*** that this implementation is provided for documentation completeness; while it is feasible, it is not the more desirable solution since the accumulated jitter from the source (MAC), PCB, and forwarding must be accounted. The cumulative effect may result in the clock violating the duty cycle and/or exceeding the jitter specification of the receiving device.

The Optical Internetworking Forum (OIF) controls the SPI-4.2 Implementation Agreement document (available at http://www.oiforum.com).

Figure 58. SPI-4 Clock Configuration for Dual Network Processors[1]



1. Note that when chaining clocks the jitter accumulated from the MAC, PCB, and RCLK/TCLK_REF pins must be accounted in addition to the duty-cycle distortion.

5.1.2 CSIX

CSIX-L1 (Common Switch Interface, Level 1) defines an interface between a Traffic Manager (TM) and a Switch Fabric (SF) for ATM, IP, MPLS, and Ethernet, or similar data communication applications.

The Network Processor Forum (NPF) controls the CSIX-L1 specification (available at http://www.npforum.org and www.csix.org).

The unit of information transferred between Traffic Managers and Switch Fabrics is called a CFrame, of which there are three categories:

- Data
- Control (for example, flow control)
- Idle

The MSF automatically discards any Idle CFrames that it receives from the SF, and transmits Idle CFrames to the SF when required. The MSF stores Data and Control CFrames in buffers during transmit and receive operations. The buffers may be partitioned according to CFrame category — guaranteeing that neither control nor data CFrames block each other.

There are two types of CSIX-L1 flow control:

- Link Level
- Virtual Output Queue (VOQ)

Every CFrame Base Header contains a Ready Field, which contains two Link Level flow control bits: one for Flow Control traffic and one for Data traffic. Due to the CSIX-L1 requirement for bounded response to Link Level flow control, the MSF manages all Link Level flow control.

Virtual Output Queue Flow Control is carried in Flow Control CFrames. As with Data CFrames, the MSF places Flow Control CFrames in internal buffers before passing them to the Microengines for processing.

5.1.3 Flow Control Bus

The MSF Flow Control Bus passes CSIX-L1 flow control CFrames between two network processors or between a Switch Fabric and a single network processor. The bus is implemented as two independent unidirectional buses. It uses LVDS signaling with the same clocking rate as the MSF receive and transmit channels and has a 4-bit data bus — yielding an available bandwidth equal to 25 percent of the receive and transmit channels.

The Flow Control Bus can be configured in one of two modes:

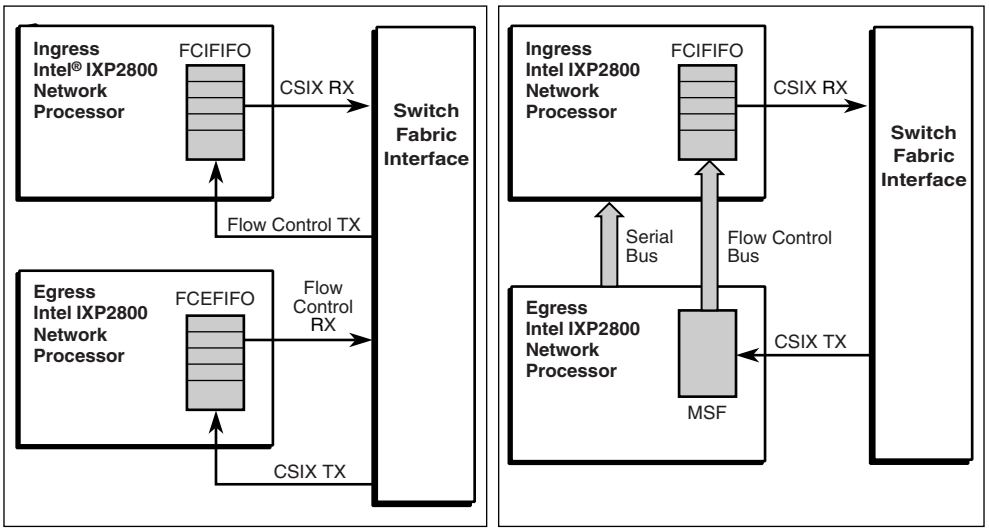
- Dual Chip, Full Duplex Mode for applications where the Fabric Interface uses the transmit and receive channels to pass flow control CFrames.
- Simplex Mode for applications where the Fabric Interface is designed to use the Flow Control Bus to pass flow control CFrames.

When the IXP2800 or IXP2850 network processor is configured in Dual Chip, Full Duplex Mode, the egress IXP28XX network processor automatically forwards CFrames received from the Switch Fabric across the Flow Control Bus to the ingress IXP28SS network processor. Additionally, the egress IXP2800 or IXP2850 network processor sends incoming and outgoing Link Level flow control information across the Flow Control Serial Bus to the ingress IXP28XX network processor.

When the IXP2800 or IXP2850 network processor is configured in Simplex Mode, the Flow Control Bus signals are connected directly to the Switch Fabric. The egress IXP2800 or IXP2850 network processor sends flow control CFrames directly to the Switch Fabric, and the Switch Fabric sends flow control CFrames directly to the ingress IXP2800 or IXP2850 network processor.

Figure 59 shows the IXP28XX network processor connected in both modes.

Figure 59. CSIX Flow Control Interfaces: Simplex and Full Duplex Modes



5.2 Routing Recommendations for LVDS Signals

5.2.1 LVDS Trace Requirements

The following is a list of LVDS trace requirements:

- Differential signals must be routed as pairs with a 100-Ω differential impedance.
- Each *leg* of a differential pair should be matched by length, within a tolerance of 10 mils.
- A differential pair should be matched by length, within a tolerance of 100 mils.
- Connectors can be used, but must be simulated.
- Differential pair signals should be routed entirely on a single layer on inner layers of the PCB

5.2.2 LVDS Trace Characteristics for IXDP2800 Advanced Development Platform

The LVDS trace characteristics are implemented as follows on the IXDP2800 Advanced Development Platform:

- The differential pair was routed with a minimum 4-mil trace width and a 10-mil trace pitch (6-mil spacing between lines); these characteristics provide a 50-Ω trace and a 92-Ω differential impedance.
- Routing the differential pair with a 4-mil trace width and a 15-mil trace pitch between signal pairs (11-mil spacing between lines) yields a better impedance match at the expense of routing density.

5.2.3 Design Review Checklist

The following is a list of items that should be reviewed when implementing the LVDS interface schematic design:

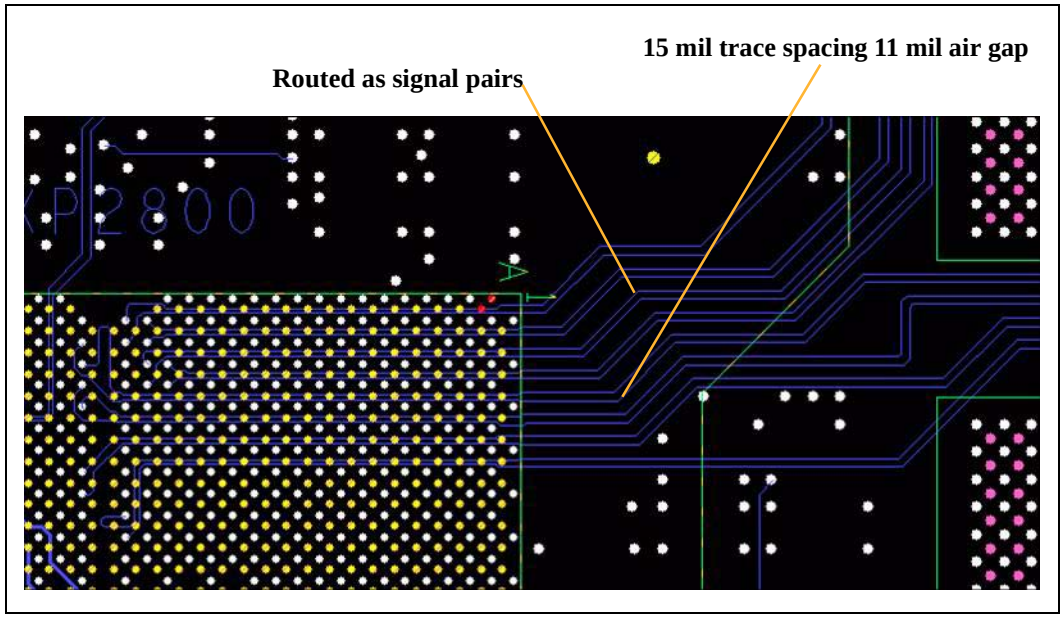
- ZQ pins must be tied together through a 100-Ω resistor.
- PREEMP pins must be terminated to V_{SS}.
- Unused Receive Parity pins RPAR_H/L must be tied to logic 1 – i.e., RPAR_H = 1, RPAR_L = 0.
- Receive Protocol RPROT_H/L must be set accordingly for protocol that is being implemented. For SPI-4 the differential pair must be set to a logic 0 and for CSIX to a logic 1 state:
  - SPI-4 = 0, i.e., RPROT_H = 0, RPROT_L = 1
  - CSIX = 1, i.e., RPROT_H = 1, RPROT_L = 0

- Unused inputs must be terminated; this can be implemented one of two ways.
  - A pin can be terminated to a logic 1 state by connecting directly to the 1.4-V supply or through a 400-Ω resistor to VCC25.
  - A pin can be terminated to a logic 0 state by connecting directly to the 1.0-V supply or through a 300-Ω resistor to GND.
- Terminate unused inputs to their inactive states by using the termination guide above. Termination rules are also discussed in detail in the MSF pin description section of the *Intel® IXP2800 and Intel® IXP2850 Network Processors Datasheet.*

5.2.4 LVDS Routing Example

Figure 60 illustrates LVDS routing as signal pairs with 15-mil trace spacing and an 11-mil air gap. This stackup yields a 92-ohm differential impedance. Note that the characteristic impedance is a function of the PCB stackup and varies from vendor to vendor. Consult your PCB vendor for additional information.

Figure 60. LVDS Routing as Signal Pairs



5.3 Simulation Results for LVDS Signals on IXDP2800 Advanced Development Platform

Figure 61 illustrates the connections between the IXP28XX network processor and an LVDS load device showing two unique, connected PCBs:

Figure 61. Topology 1 - Two Unique PCBs Connected

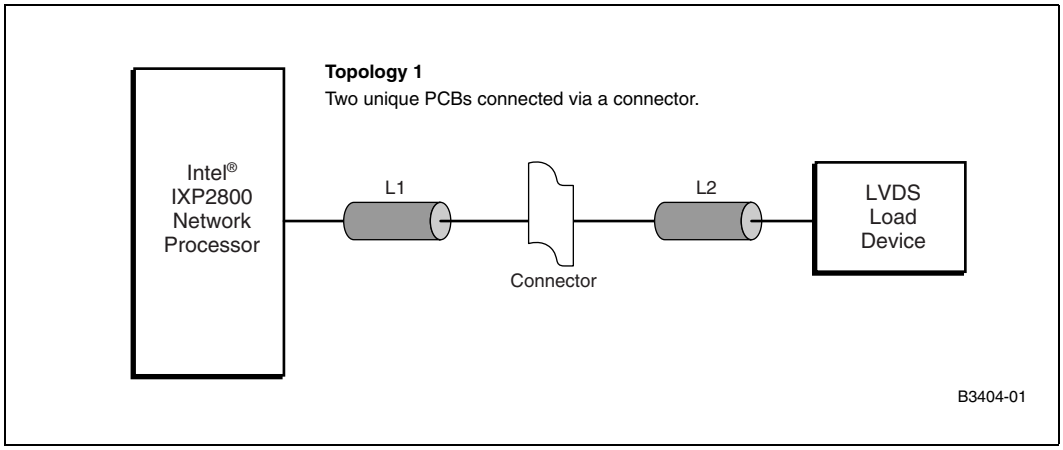


Table 36 provides network length results for Topology 1. The table illustrates the resulting data EYE opening from simulations of the topology shown in Figure 61.

Table 36. Topology 1 Network Length Results

Transfer Net	L1 (inches)	L2 (inches)	EYE Opening (mV)
SPI4_RX	1.5 to 3	3 to 7	210
SPI4_RX_CLK	1.5 to 3	3 to 7	230
SPI4_TX	3 to 7	1.5 to 3	260
SPI4_TX_CLK	3 to 7	1.5 to 3	280

Figure 62 illustrates the connections between the IXP28XX network processor and an LVDS load device showing two unique, connected PCBs with a loopback signal and connectors in each path.

Figure 62. Topology 2 - Two Unique PCBs with Signal Loopback Through Connectors

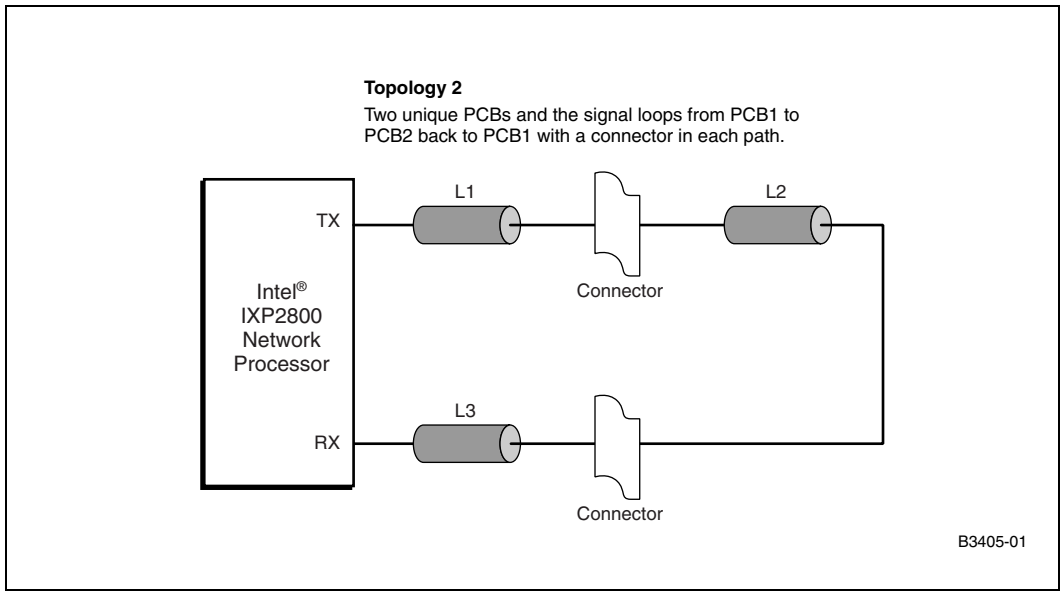


Table 37 provides network length results for Topology 2. The table illustrates the resulting data EYE opening from simulations of the topology shown in Figure 62.

Table 37. Topology 2 Network Length Results

Transfer Net	L1 (inches)	L2 (inches)	L3 (inches)	Maximum Total Etch Length (inches)	EYE Opening (mV)
FLOW_CONTROL	3 to 7	0.4	3 to 7	14.4	200
FLOW_CONTROL_CLK	3 to 7	0.4	3 to 7	14.4	200

5.4 Package Trace Lengths for LVDS_Diff Signals

Table 38 provides package trace lengths for LVDS_Diff signals, listed by decreasing lengths. For designs that implement dynamic deskew via training, matching of trace lengths through the package is not required as the deskew logic will correct this mismatch. For designs that implement static deskew, trace length-matching through the package may be required.

The flight time on the package substrate is 154ps/in which differs from the flight delay of standard FR4, typical 180ps/in. As a result the package routing lengths in Table 38 must be adjusted to compensate for the difference in flight delay between the package and the PCB. For example FC_RXCSRB_L has a package length of 0.597 in, and the target PCB has a flight delay of 180ps/in. In order to adjust the package length to match the PCB flight delay this length must be multiplied by the ratio of 154/180 or the difference between the package and PCB flight delays. Therefore the trace package routing length that must be accounted for on the PCB is 0.597*(154/180) or 0.511 in.

Note: If the flight delay of the target PCB is not 180 ps/in then the ratio, (154/180), must be modified accordingly, i.e., the denominator would be changed to reflect the actual flight delay.

Table 38. Package Trace Lengths for LVDS_Diff Signals (Sheet 1 of 2)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
FC_RXCSRB_L	15.168	0.597	SPI4_TDAT[15]	11.51	0.453	SPI4_TDAT[2]	8.628	0.340
FC_RXCSRB	15.167	0.597	SPI4_RDAT[2]	11.313	0.445	SPI4_TDAT_L[2]	8.623	0.339
SPI4_RDAT[0]	14.548	0.573	SPI4_RDAT_L[2]	11.312	0.445	FC_RXCDAT_L[3]	8.424	0.332
SPI4_RDAT_L[0]	14.546	0.573	SPI4_RDAT_L[10]	11.166	0.440	FC_RXCDAT[3]	8.42	0.331
FC_RXCSOF_L	14.46	0.569	SPI4_RDAT[10]	11.164	0.440	SPI4_TDAT[14]	7.807	0.307
FC_RXCSOF	14.455	0.569	FC_RXCDAT_L[2]	11.135	0.438	SPI4_TDAT_L[14]	7.807	0.307
SPI4_RDAT[4]	14.249	0.561	FC_RXCDAT[2]	11.133	0.438	SPI4_RCLK	7.721	0.304
SPI4_RDAT_L[4]	14.246	0.561	FC_TXCFC	11.018	0.434	SPI4_RCLK_L	7.717	0.304
FC_RXCDAT[0]	14.115	0.556	FC_TXCFC_L	11.013	0.434	SPI4_TDAT[13]	7.684	0.303
FC_RXCDAT_L[0]	14.114	0.556	SPI4_TPAR	10.961	0.432	SPI4_TDAT_L[13]	7.68	0.302
SPI4_RDAT[5]	13.928	0.548	SPI4_TPAR_L	10.953	0.431	SPI4_TDAT_L[5]	7.657	0.301
SPI4_RDAT_L[5]	13.928	0.548	FC_RXCPAR_L	10.769	0.424	SPI4_TDAT[5]	7.654	0.301
FC_RXCCLK_L	13.368	0.526	FC_RXCPAR	10.768	0.424	SPI4_RCTL	7.65	0.301
FC_RXCCLK	13.365	0.526	SPI4_TCLK_L	10.745	0.423	SPI4_RCTL_L	7.649	0.301
SPI4_TDAT_L[11]	12.978	0.511	SPI4_TCLK	10.744	0.423	SPI4_RDAT[11]	7.489	0.295
SPI4_TDAT[11]	12.976	0.511	SPI4_TCTL_L	10.595	0.417	SPI4_RDAT_L[11]	7.486	0.295
SPI4_TDAT_L[3]	12.947	0.510	SPI4_TCTL	10.591	0.417	FC_TXCCLK_L	7.436	0.293
SPI4_TDAT[3]	12.945	0.510	SPI4_TDAT_L[8]	10.226	0.403	FC_TXCCLK	7.435	0.293
FC_RXCFC_L	12.888	0.507	SPI4_TDAT[8]	10.222	0.402	SPI4_RDAT[8]	7.314	0.288
FC_RXCFC	12.883	0.507	SPI4_RDAT[14]	9.97	0.393	SPI4_RDAT_L[8]	7.311	0.288
FC_RXCDAT_L[1]	12.577	0.495	SPI4_RDAT_L[14]	9.968	0.392	FC_TXCDAT[2]	7.195	0.283
FC_RXCDAT[1]	12.573	0.495	SPI4_TDAT_L[10]	9.952	0.392	FC_TXCDAT_L[2]	7.195	0.283

Table 38. Package Trace Lengths for LVDS_Diff Signals (Sheet 2 of 2)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
SPI4_TPROT_L	12.448	0.490	SPI4_TDAT[10]	9.947	0.392	SPI4_TDAT_L[0]	6.571	0.259
SPI4_TPROT	12.447	0.490	SPI4_RDAT[3]	9.848	0.388	SPI4_TDAT[0]	6.563	0.258
SPI4_RDAT[1]	12.257	0.483	SPI4_RDAT_L[3]	9.844	0.388	FC_TXCDAT[3]	6.463	0.254
SPI4_RDAT_L[1]	12.257	0.483	SPI4_TDAT[1]	9.702	0.382	FC_TXCDAT_L[3]	6.463	0.254
SPI4_TDAT[6]	12.207	0.481	SPI4_TDAT_L[1]	9.696	0.382	SPI4_RDAT_L[6]	6.427	0.253
SPI4_TDAT_L[6]	12.206	0.481	FC_TXCPAR_L	9.44	0.372	SPI4_RDAT[6]	6.422	0.253
SPI4_RDAT[7]	12.02	0.473	FC_TXCPAR	9.437	0.372	SPI4_RDAT[13]	6.354	0.250
SPI4_RDAT_L[7]	12.018	0.473	SPI4_RDAT[9]	8.974	0.353	SPI4_RDAT_L[13]	6.346	0.250
SPI4_RDAT[15]	11.864	0.467	SPI4_RDAT_L[9]	8.971	0.353	FC_TXCDAT[0]	6.205	0.244
SPI4_RDAT_L[15]	11.863	0.467	FC_TXCSOF	8.904	0.351	FC_TXCDAT_L[0]	6.202	0.244
SPI4_TDAT_L[15]	11.513	0.453	FC_TXCSOF_L	8.903	0.351	SPI4_TDAT[12]	6.129	0.241
SPI4_TDAT_L[12]	6.129	0.241						
SPI4_RDAT[12]	6.124	0.241						
SPI4_RDAT_L[12]	6.119	0.241						
FC_TXCDAT_L[1]	6.079	0.239						
FC_TXCDAT[1]	6.077	0.239						
SPI4_TDAT_L[7]	6.046	0.238						
SPI4_TDAT[7]	6.041	0.238						
SPI4_TDAT[9]	6.034	0.238						
SPI4_TDAT_L[9]	6.034	0.238						
SPI4_RPROT	6.004	0.236						
SPI4_RPROT_L	6.003	0.236						
FC_TXCSRB	6.003	0.236						
FC_TXCSRB_L	6.003	0.236						
SPI4_RCLK_REF_L	6	0.236						
SPI4_RCLK_REF	5.994	0.236						
SPI4_RPAR	5.923	0.233						
SPI4_RPAR_L	5.92	0.233						
SPI4_TCLK_REF	5.606	0.221						
SPI4_TCLK_REF_L	5.599	0.220						
SPI4_TDAT[4]	5.58	0.220						
SPI4_TDAT_L[4]	5.578	0.220						

PCI 6

6.1 PCI Controller

The PCI Controller provides a 64-bit, 66-MHz-capable *PCI Local Bus Specification, Version 2.2** interface to the Intel® IXP2800 or Intel® IXP2850 Network Processor. It is also compatible to 32-bit and/or 33-MHz PCI devices. The PCI controller provides the following functions:

- Target Access (external Bus Master access to SRAM, DRAM, and CSRs)
- Master Access (Intel XScale® core or Microengine access to PCI target devices)
- Two DMA Channels
- Mailbox and Doorbell Registers for Intel XScale® core to host communication
- PCI Arbiter

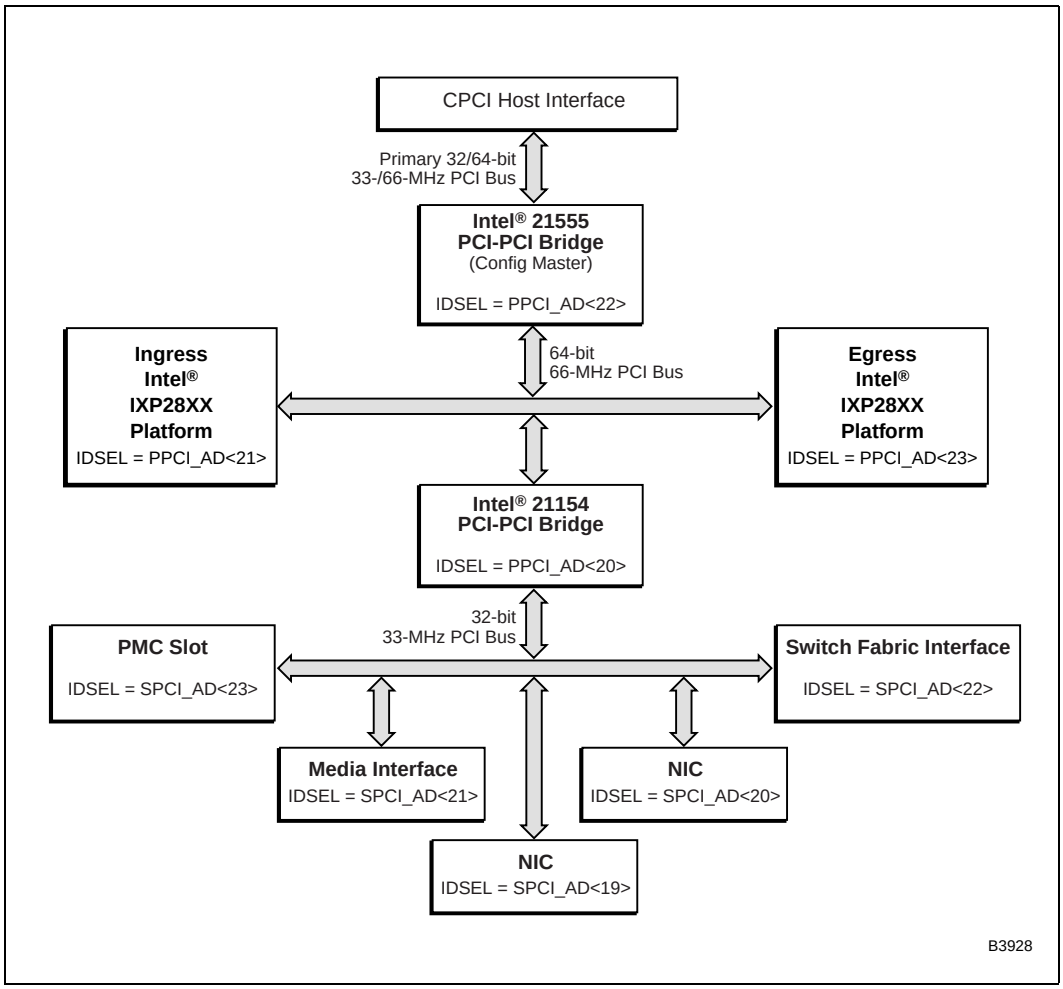
The network processor can be configured to act as a PCI central function (for use in a stand-alone system), where it provides the PCI reset signal, or as an add-in device, where it uses the PCI reset signal as the chip reset input.

6.2 PCI Interface

The IXP28XX network processor has a PCI controller with its own bus arbiter supporting two external masters in addition to the PCI unit's initiator interface. The base card implementation requires more than two external masters; therefore, the arbiter in both the ingress and egress INXP2800 network processor is disabled and the arbiter in the 21555 PCI-PCI bridge is enabled instead. In this implementation, both the ingress and egress network processors provide their PCI request signals as output to the 21555 and use the 21555's grant signals as inputs. The PCI Bus in the IXP28XX network processor is a CMOS bus and is based on reflected wave rather than incident wave signaling.

As shown in Figure 63, the Primary PCI bus is connected to the cPCI back plane through the J1 and J2 connectors. The interface is configurable to be 32-bit or 64-bit and the interface runs at the clock speed of the cPCI backplane. The configuration master PCI-PCI bridge provides reset and arbitration to all devices on its secondary side. The secondary bus is 3.3 V, 64-bit, and 66 MHz.

Figure 63. PCI Subsystem



6.2.1 PPCI Bus Interface

The Primary PCI (PPCI) bus is a 64-bit PCI bus that can operate at 33 or 66 MHz. This bus connects the ingress and egress IXP28XX network processor to the master and slave PCI-PCI bridge chips.

6.2.1.1 PPCI Address/Data Signals

Figure 64 illustrates the topology for PPCI address/data signals.

Figure 64. PPCI Address/Data Signal Topology

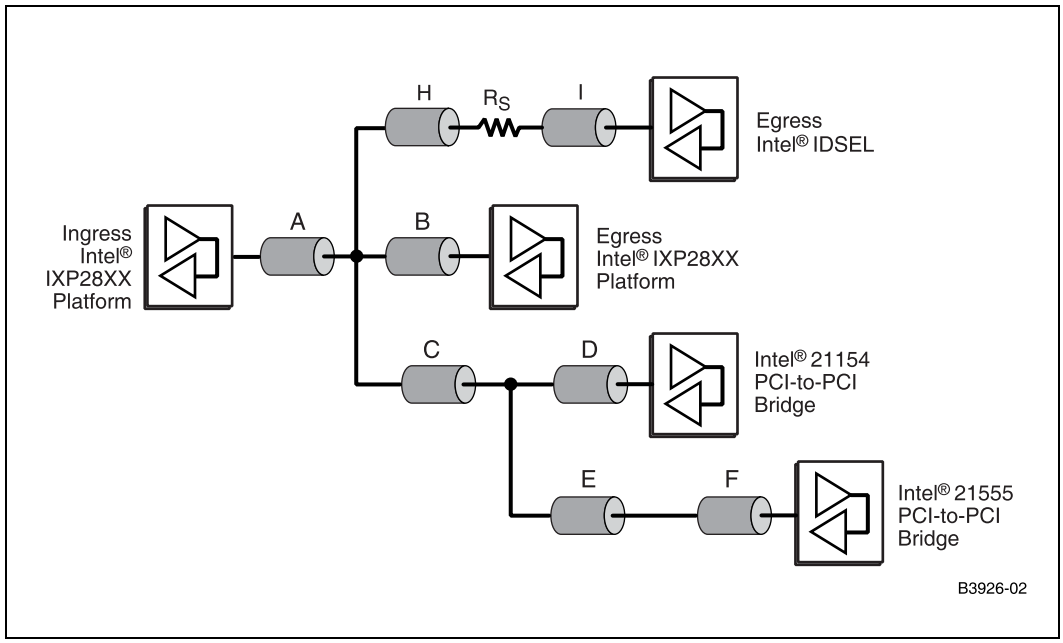


Table 39 provides routing guidelines for the PPCI address/data group parameters.

Table 39. PPCI Address/Data Group Guidelines

Parameter	Routing Guidelines
Signal Group	Address/Data
Topology	Daisy Chain
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9.0 mils
Spacing to Other Groups	20 mils
Trace Length A	Maximum = 50 mils
Trace Length B	Maximum = 4200 mils
Trace Length C	Maximum = 4500 mils
Trace Length D	Maximum = 50 mils
Trace Length E	Maximum = 1200 mils
Trace Length F	Maximum = 2500 mils
Maximum Via Count per Signal	8 Vias

6.2.1.2 PPCI Clock Signals

Figure 65 illustrates the topology for PPCI clock signals. All of the clock signal traces for the PPCI bus should be matched.

Figure 65. PPCI Clock Signals Topology

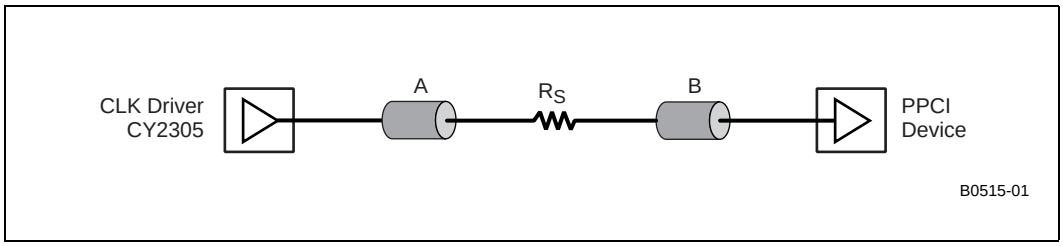


Table 40 provides routing guidelines for the PPCI clock signals group parameters.

Table 40. PPCI Clock Signals Group Guidelines

Parameter	Routing Guidelines
Signal Group	Clock
Topology	Point-to-Point
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace Length A	Maximum = 200 mils
Trace Length B	Maximum = 5800 mils
Resistor R_S	30 Ω ±10%
Maximum Count per Signal	5 vias

6.2.1.3 Address/Data Signals with IDSEL

Figure 66 illustrates the topology for address/data signals with IDSEL (showing only the ingress IXP28XX network processor).

Figure 66. Address/Data Signals with IDSEL Topology (Showing Only the Ingress Intel® IXP28XX Network Processor)

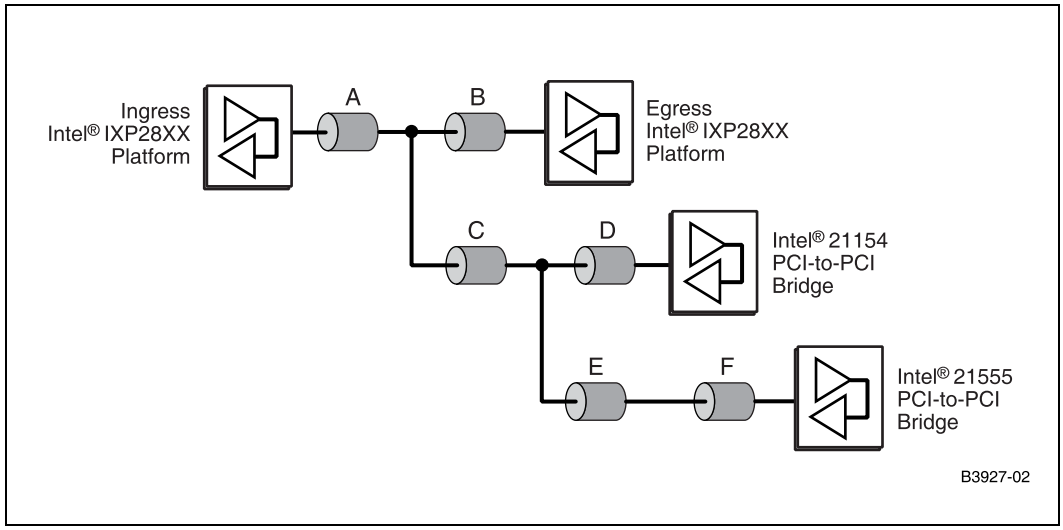


Table 41 provides routing guidelines for the address/data signal with IDSEL group parameters.

Table 41. Address/Data Signal with IDSEL Group Guidelines

Parameter	Routing Guidelines
Signal Group	Address/Data with IDSEL
Topology	Daisy Chain
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace Length A	Maximum = 50 mils
Trace Length B	Maximum = 4200 mils
Trace Length C	Maximum = 4500 mils
Trace Length D	Maximum = 50 mils
Trace Length E	Maximum = 1200 mils
Trace Length F	Maximum = 2500 mils
Trace Length H	Maximum = 100 mils
Trace Length I	Maximum = 2000 mils
Resistor R_S	84 Ω ± 10%
Maximum Via Count per Signal	10 vias

6.2.2 SPCI Bus Interface

The Secondary PCI interface is a 32-bit bus operating at 33 MHz. This bus starts from the 21154 master PCI-PCI bridge chip.

6.2.2.1 SPCI Address/Data Signals

Figure 67 illustrates the topology for SPCI address/data signals.

Figure 67. SPCI Address/Data Signal Topology

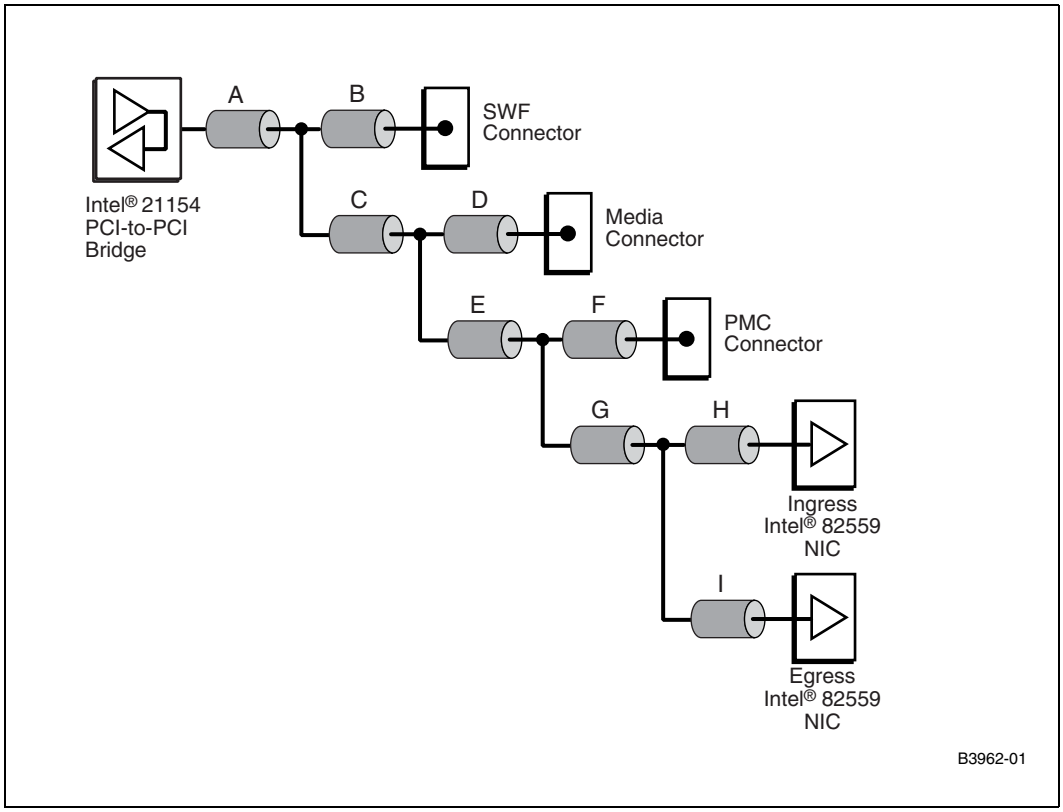


Table 42 provides routing guidelines for the SPCI address/data group parameters.

Table 42. SPCI Address/Data Group Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines
Signal Group	SPCI Address/Data
Topology	Daisy Chain
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ±10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils

Table 42. SPCI Address/Data Group Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines
Trace Length A	Maximum = 4300 mils
Trace Length B	Maximum = 200 mils
Trace Length C	Maximum = 5200 mils
Trace Length D	Maximum = 500 mils
Trace Length E	Maximum = 7000 mils
Trace Length F	Maximum = 200 mils
Trace Length G	Maximum = 4500 mils
Trace Length H	Maximum = 200 mils
Trace Length I	Maximum = 1200 mils
Maximum Via Count per Signal	10 vias

6.2.2.2 SPCI Clock Signals

Figure 68 illustrates the topology for SPCI clock signals.

Figure 68. SPCI Clock Signals Topology

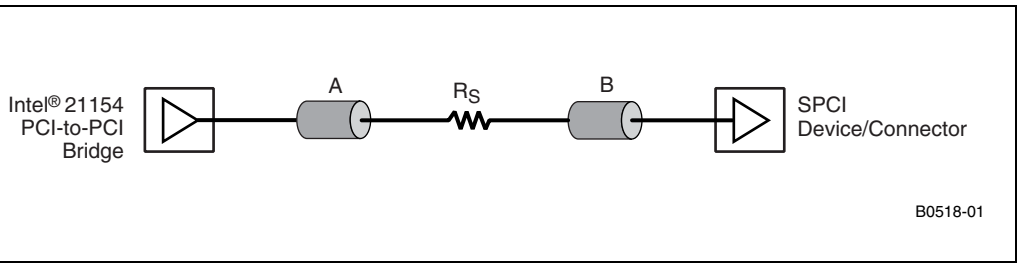


Table 43 provides routing guidelines for the SPCI clock signals group parameters.

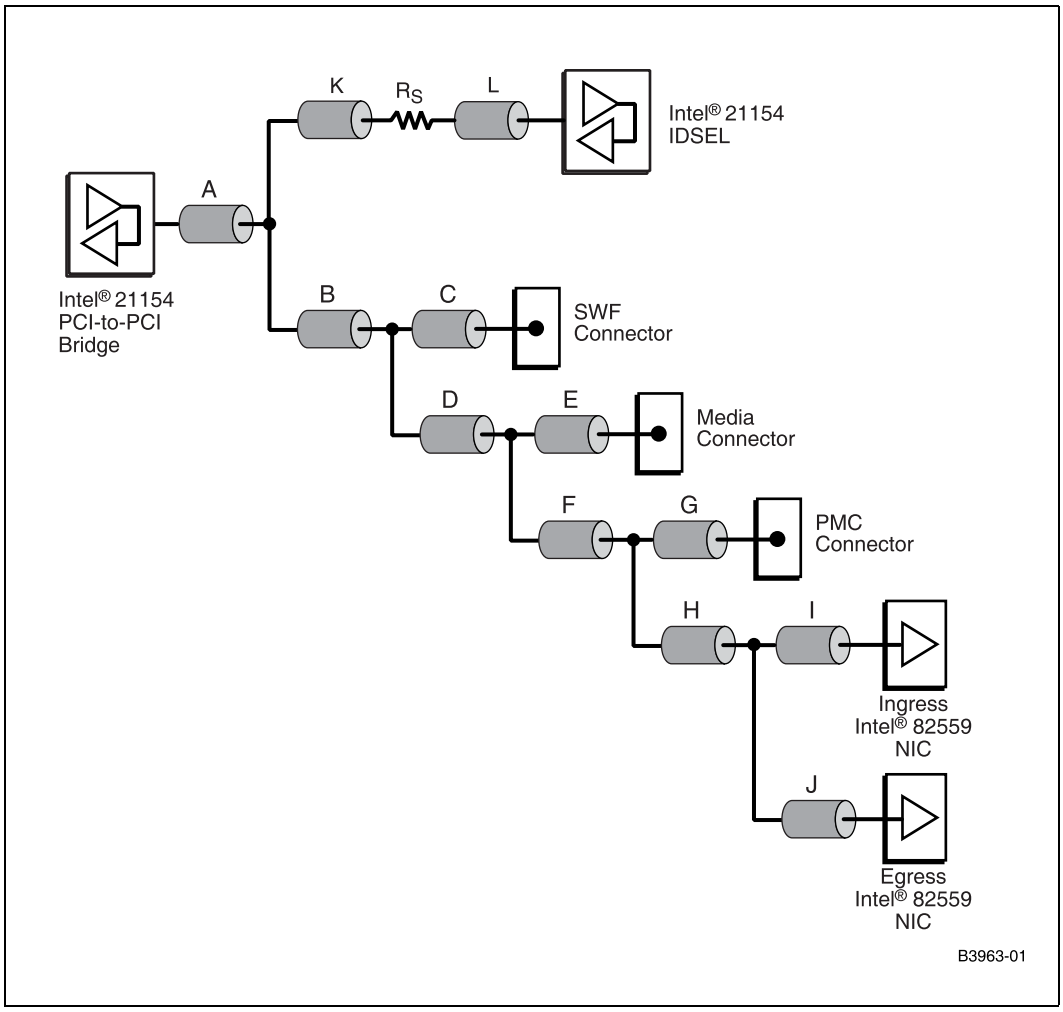
Table 43. SPCI Clock Signals Group Guidelines

Parameter	Routing Guidelines
Signal Group	SPCI Clk
Topology	Point-to-Point
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace Length A	Maximum = 200 mils
Trace Length B	Maximum = 11000 mils
Resistor R_S	30 Ω ± 10%
Maximum Via Count per Signal	4 vias

6.2.2.3 SPCI Address/Data Signals with IDSEL

Figure 69 illustrates the topology for SPCI address/data signals with IDSEL signal.

Figure 69. SPCI Address/Data Signals with IDSEL Signal Topology[1]



1. Only the 211154 PCI-PCI bridge case is shown.

Table 44 provides routing guidelines for the SPCI address/data signals with IDSEL group parameters.

Table 44. SPCI Address/Data Signals with IDSEL Group Guidelines

Parameter	Routing Guidelines
Signal Group	SPCI Address/Data with IDSEL
Topology	Daisy Chain
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace Length A	Maximum = 2500 mils
Trace Length B	Maximum = 1800 mils
Trace Length C	Maximum = 200 mils
Trace Length D	Maximum = 5200 mils
Trace Length E	Maximum = 500 mils
Trace Length F	Maximum = 7000 mils
Trace Length G	Maximum = 200 mils
Trace Length H	Maximum = 4500 mils
Trace Length I	Maximum = 200 mils
Trace Length J	Maximum = 1200 mils
Trace Length K	Maximum = 150 mils
Trace Length L	Maximum = 2000 mils
Resistor R_S	84 Ω ± 10%
Maximum Via Count per Signal	12 vias

6.2.3 cPCI Bus Interface

The compact PCI (cPCI) interface can be a 32- or 64-bit bus, which can operate at either 33 or 66 MHz. When the base card is not connected to a host, V_{IO} for this bus comes from the base card 3.3 V power supply. When there is a host present, resistor R2401 and R2305 need to be removed and V_{IO} is provided by the host.

6.2.3.1 cPCI Signals

Figure 70 illustrates the topology for the cPCI signal.

Figure 70. cPCI Signal Topology

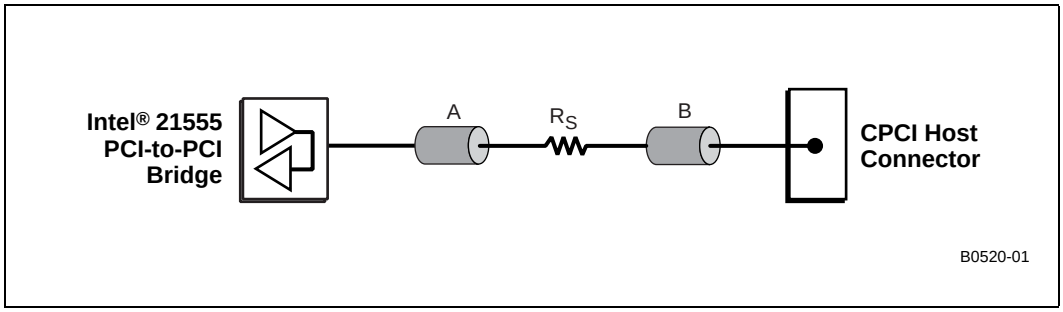


Table 45 provides routing guidelines for the cPCI signal group parameters.

Table 45. cPCI Signal Group Guidelines

Parameter	Routing Guidelines
Signal Group	cPCI Signals
Topology	Point-to-Point
Reference Plane	Dual-referenced, PWR–SIG–GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace Length A	Maximum = 1200 mils
Trace Length B	Maximum = 500 mils
Resistor R_S	10 Ω ± 10%
Maximum Via Count per Signal	3 vias

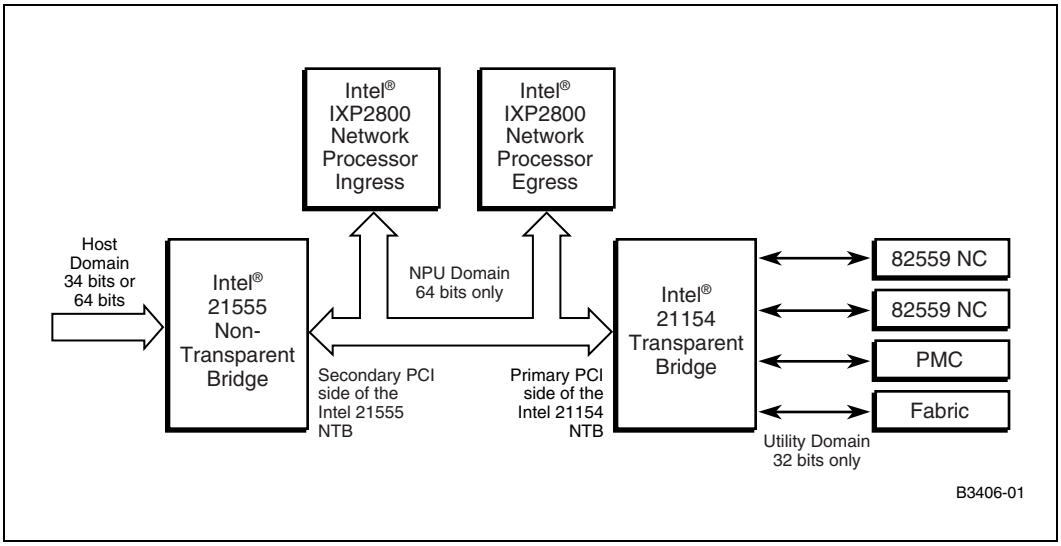
6.3 PCI Design Review Checklist

Use the following list of requirements and recommendations for your PCI design:

- PCI ZQ line termination:
  - — ZQ1 tied to V_{SS} through a 31.6-Ω resistor
  - — ZQ2 tied to V_{CC33} through a 28-Ω resistor
- PCI_M66EN must be terminated accordingly.
- PCI_IDSEL must be terminated to GND if it is a central function.
- Unused AD/Control signals must be terminated per PCI specification.
- For a 64-bit operation, PCI_REQ# must be sampled at assertion on the rising edge of PCI_RST and can also be enabled via the PCI_IXP_PARAM register.
- Loading guidelines:
  - — 66 MHz – four loads
  - — 33 MHz – eight loads

Figure 71 illustrates PCI bus topology for the IXDP2800 Advanced Development Platform.

Figure 71. IXDP2800 PCI Bus Topology Block Diagram



6.4 PCI Routing Examples: IXP2800 Network Processor

Figure 72 illustrates 64-bit PCI bus routing between processors and Figure 73 illustrates 64-bit PCI bus routing from the IXP28XX network processor to a bridge.

Figure 72. 64-Bit PCI Bus Routing Between Processors

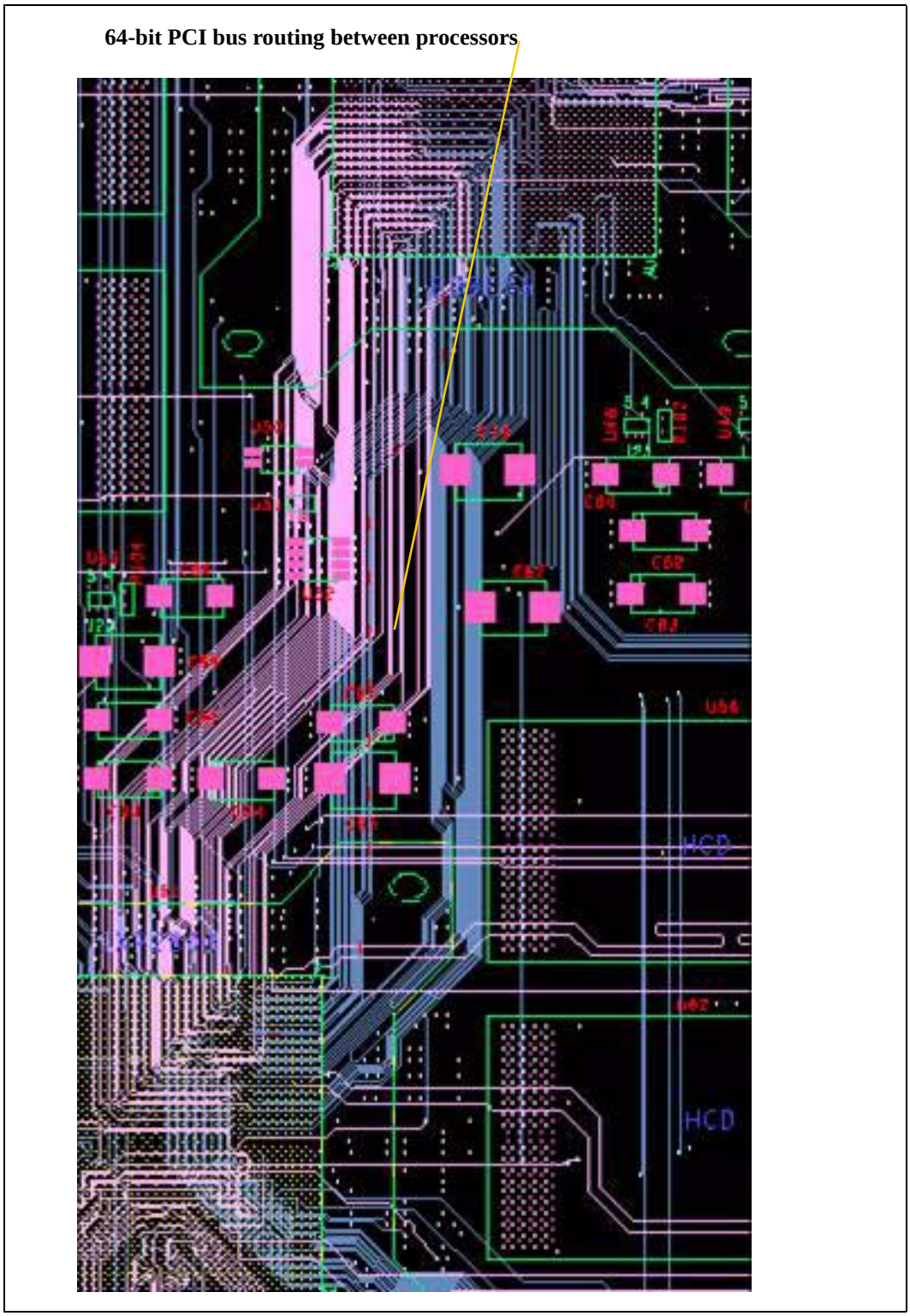
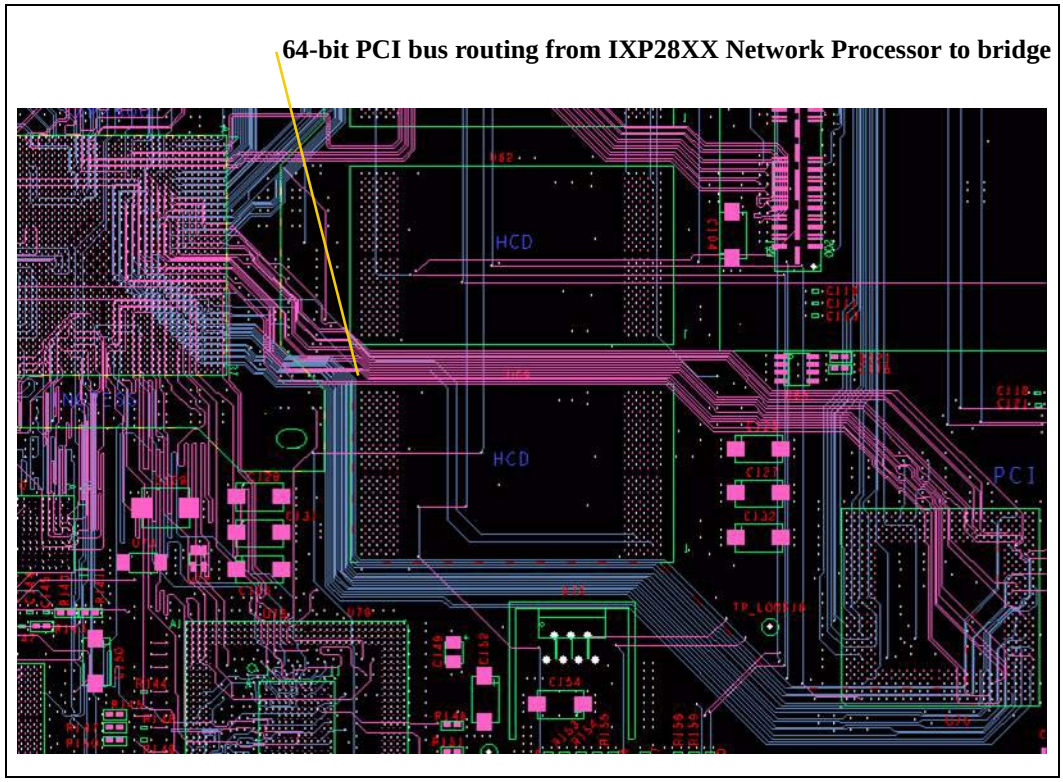


Figure 73 illustrates 64-bit PCI bus routing from the IXP28XX network processor to the bridge.

Figure 73. 64-bit PCI Bus Routing from IXP28XX Network Processor to Bridge



6.5 Package Trace Lengths for PCI Signals

Table 46 provides package trace lengths for PCI signals.

Note: It is typically not required to account for the package trace length for PCI interface signals.

The flight time on the package substrate is 154ps/in which differs from the flight delay of standard FR4, typical 180ps/in. As a result the package routing lengths in Table 46 must be adjusted to compensate for the difference in flight delay between the package and the PCB. For example PCI_ACK64_L has a package length of 0.593 in, and the target PCB has a flight delay of 180ps/in. In order to adjust the package length to match the PCB flight delay this length must be multiplied by the ratio of 154/180 or the difference between the package and PCB flight delays. Therefore the trace package routing length that must be accounted for on the PCB is 0.593*(154/180) or 0.507 in.

Note: If the flight delay of the target PCB is not 180 ps/in then the ratio, (154/180), must be modified accordingly, i.e., the denominator would be changed to reflect the actual flight delay.

Table 46. Package Trace Lengths for PCI Signals (Sheet 1 of 2)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
PCI_ACK64_L	15.052	0.593	PCI_AD[38]	8.43	0.332	PCI_CBE_L[1]	3.597	0.142
PCI_AD[0]	6.118	0.241	PCI_AD[39]	15.183	0.598	PCI_CBE_L[2]	1.571	0.062
PCI_AD[1]	7.934	0.312	PCI_AD[4]	4.626	0.182	PCI_CBE_L[3]	9.587	0.377
PCI_AD[10]	11.996	0.472	PCI_AD[40]	5.386	0.212	PCI_CBE_L[4]	13.866	0.546
PCI_AD[11]	16.187	0.637	PCI_AD[41]	14.329	0.564	PCI_CBE_L[5]	3.349	0.132
PCI_AD[12]	2.379	0.094	PCI_AD[42]	9.768	0.385	PCI_CBE_L[6]	10.543	0.415
PCI_AD[13]	10.843	0.427	PCI_AD[43]	10.39	0.409	PCI_CBE_L[7]	6.818	0.268
PCI_AD[14]	13.881	0.546	PCI_AD[44]	4.96	0.195	PCI_CLK	5.22	0.206
PCI_AD[15]	13.628	0.537	PCI_AD[45]	4.537	0.179	PCI_DEVSEL_L	8.571	0.337
PCI_AD[16]	8.055	0.317	PCI_AD[46]	2.088	0.082	PCI_FRAME_L	4.673	0.184
PCI_AD[17]	11.044	0.435	PCI_AD[47]	12.445	0.490	PCI_GNT_L[0]	14.405	0.567
PCI_AD[18]	3.802	0.150	PCI_AD[48]	5.838	0.230	PCI_GNT_L[1]	13.908	0.548
PCI_AD[19]	7.593	0.299	PCI_AD[49]	11.942	0.470	PCI_IDSEL	11.147	0.439
PCI_AD[2]	14.995	0.590	PCI_AD[5]	9.05	0.356	PCI_INTA_L	12.348	0.486
PCI_AD[20]	12.79	0.504	PCI_AD[50]	10.852	0.427	PCI_INTB_L	7.397	0.291
PCI_AD[21]	10.251	0.404	PCI_AD[51]	10.741	0.423	PCI_IRDY_L	5.826	0.229
PCI_AD[22]	10.299	0.405	PCI_AD[52]	1.893	0.075	PCI_M66EN	1.72	0.068
PCI_AD[23]	5.299	0.209	PCI_AD[53]	11.913	0.469	PCI_PAR	13.373	0.526
PCI_AD[24]	1.845	0.073	PCI_AD[54]	5.843	0.230	PCI_PAR64	5.838	0.230
PCI_AD[25]	17.686	0.696	PCI_AD[55]	7.053	0.278	PCI_PERR_L	2.9	0.114
PCI_AD[26]	7.434	0.293	PCI_AD[56]	7.908	0.311	PCI_REQ_L[0]	3.644	0.143
PCI_AD[27]	2.48	0.098	PCI_AD[57]	10.645	0.419	PCI_REQ_L[1]	9.697	0.382
PCI_AD[28]	12.666	0.499	PCI_AD[58]	2.518	0.099	PCI_REQ64_L	1.72	0.068

Table 46. Package Trace Lengths for PCI Signals (Sheet 2 of 2)

Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)	Signal	Metric Units (mm)	English Units (in)
PCI_AD[29]	15.481	0.609	PCI_AD[59]	15.545	0.612	PCI_RST_L	5.807	0.229
PCI_AD[3]	5.255	0.207	PCI_AD[6]	3.443	0.136	PCI_SERR_L	4.71	0.185
PCI_AD[30]	9.829	0.387	PCI_AD[60]	4.687	0.185	PCI_STOP_L	16.576	0.653
PCI_AD[31]	10.76	0.424	PCI_AD[61]	9.023	0.355	PCI_TRDY_L	9.061	0.357
PCI_AD[32]	2.776	0.109	PCI_AD[62]	3.817	0.150	PCI_ZQ1	5.038	0.198
PCI_AD[33]	5.09	0.200	PCI_AD[63]	13.417	0.528	PCI_ZQ2	1.491	0.059
PCI_AD[34]	4.105	0.162	PCI_AD[7]	5.076	0.200	SP_ACK_L	6.263	0.247
PCI_AD[35]	5.94	0.234	PCI_AD[8]	10.682	0.421	SP_AD[0]	15.47	0.609
PCI_AD[36]	11.244	0.443	PCI_AD[9]	12.02	0.473	SP_AD[1]	9.926	0.391
PCI_AD[37]	1.647	0.065	PCI_CBE_L[0]	11.033	0.434	SP_AD[2]	3.151	0.124
SP_AD[3]	1.572	0.062						
SP_AD[4]	6.606	0.260						
SP_AD[5]	5.044	0.199						
SP_AD[6]	4.375	0.172						
SP_AD[7]	7.962	0.313						
SP_ALE_L	3.457	0.136						
SP_CLK	0.898	0.035						
SP_CP	2.438	0.096						
SP_CS_L[0]	1.193	0.047						
SP_CS_L[1]	14.245	0.561						
SP_DIR	3.299	0.130						
SP_OE_L	1.942	0.076						
SP_RD_L	7.843	0.309						
SP_WR_L	0.89	0.035						

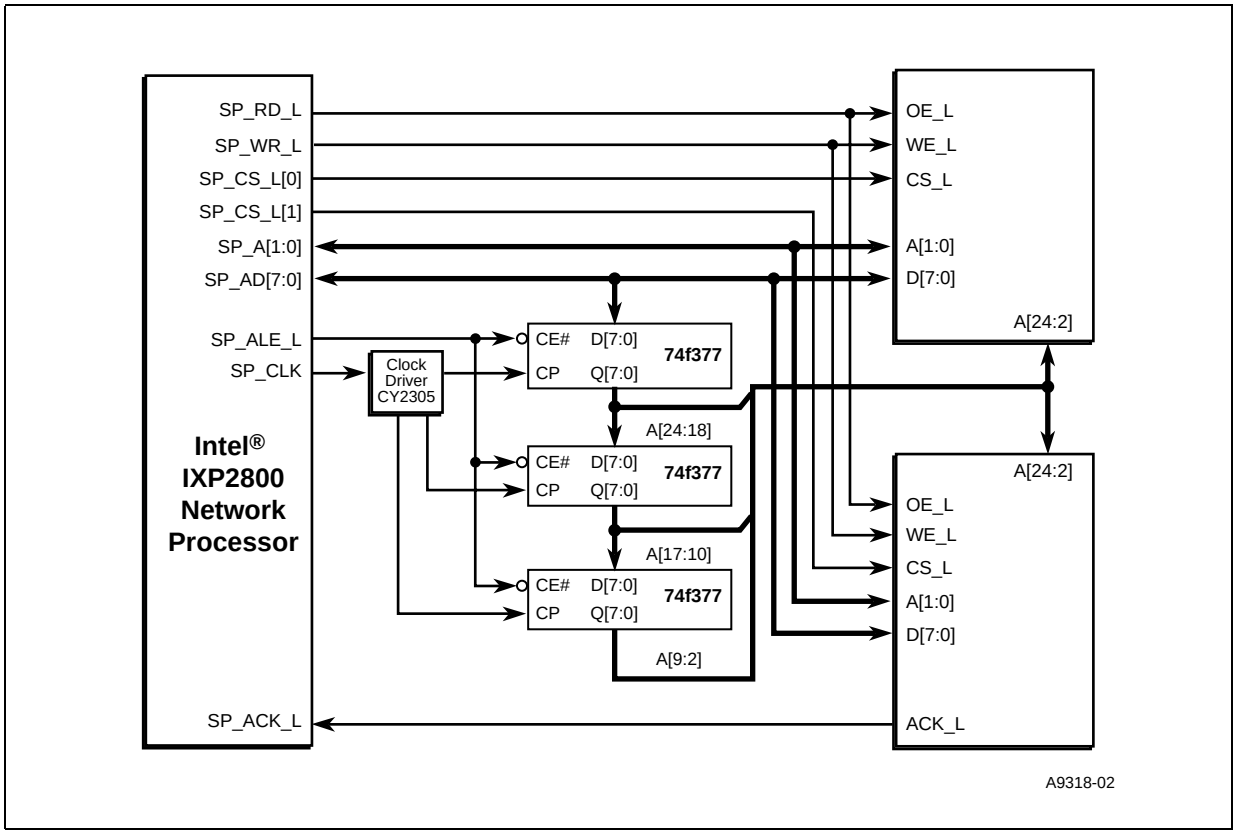
Slowport 7

The Slowport is an external interface to the Intel® IXP2800 or Intel® IXP2850 Network Processor, and is used for 8-bit flash PROM access and 8-, 16-, or 32-bit microprocessor device access. The Slowport allows the Intel XScale® core to perform read/write data transfers to external slave devices. The Slowport supports 4-, 8-, and 16-Mbyte flash sizes.

The address bus and data bus are multiplexed to reduce the pin count and 24 bits of address are shifted out on three clock cycles. Therefore, an external set of buffers is needed to latch the address; two chip selects are provided – see Figure 74 (note that the ACK signal is optional).

Note: To meet interface timing requirements, Intel suggests the external interface logic be implemented in a high speed CPLD (Complex Programmable Logic Device), as shown in Figure 77.

Figure 74. Generic Slowport Connection



7.1 Slowport Interface

The PROM or microprocessor access via the Slowport can be asynchronous. Insertion of delay cycles is possible for both setup and hold data; the Slowport includes a programmable timing control mechanism for this purpose. For Slowport programming and timing setup, refer to the *Intel® IXP2400 and IXP2800 Network Processor Programmer's Reference Manual.*

The Slowport unit contains two types of interface and two ports:

- Flash memory interface with a dedicated port used for the PROM device
- Microprocessor interface used for SONET/SDH Framer Microprocessor access

Access to each of these interfaces is differentiated by two chip selects, SP_CS[n]. External decode logic is required to latch the address and data.

Examples of the Slowport interface configuration on the IXP28XX network processor is shown in Figure 75 for ingress and in Figure 76 for egress.

Figure 75. Example Ingress IXP28XX Network Processor Slowport Configuration

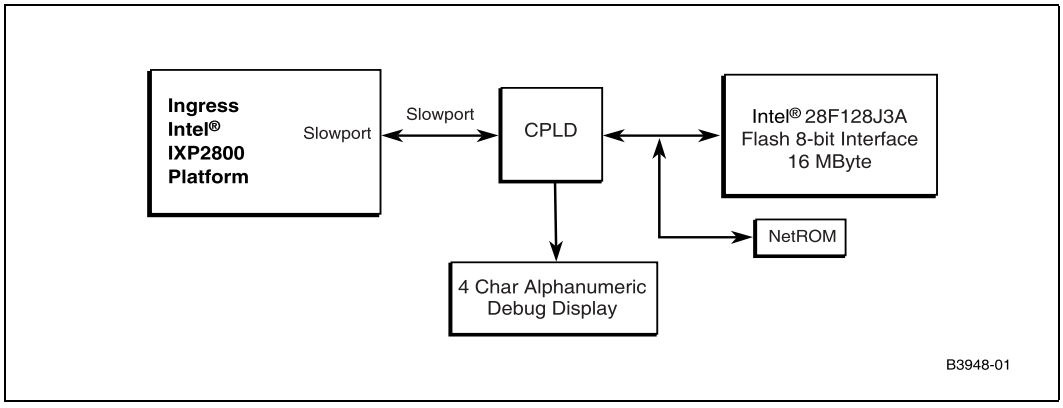


Figure 76. Example Egress IXP28XX Slowport Configuration

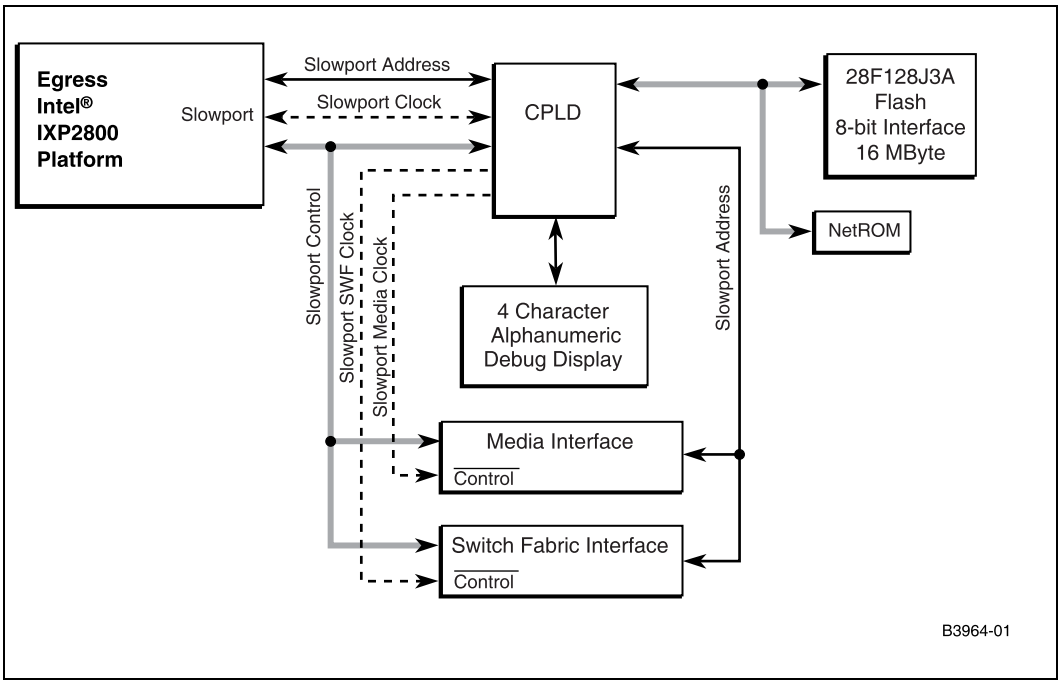
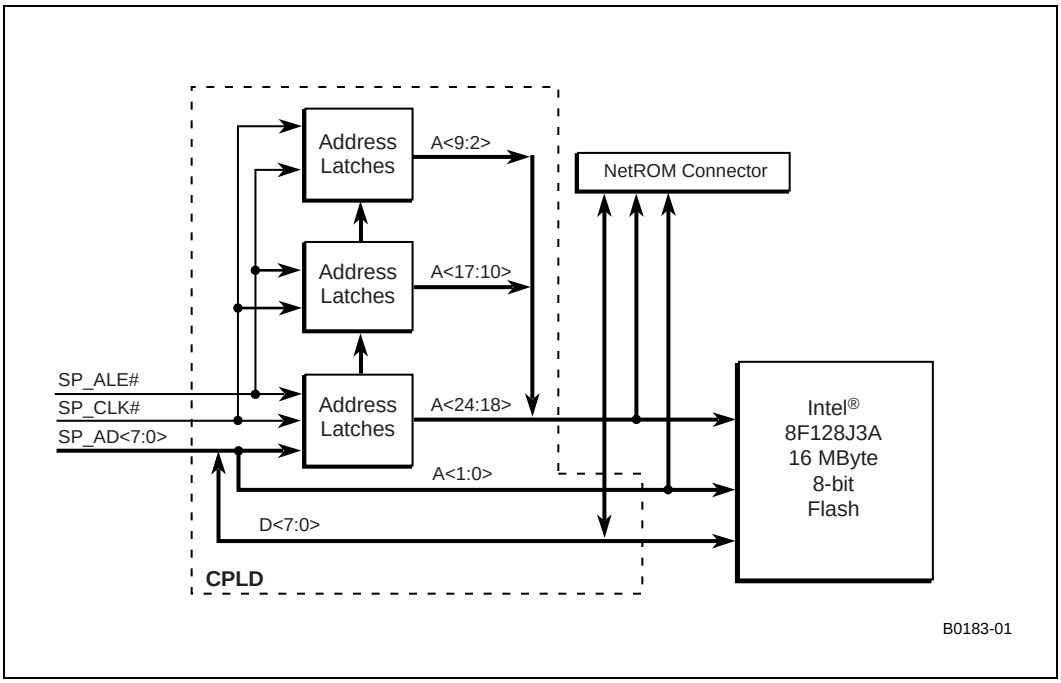


Figure 77 illustrates the CPLD implementation of a Flash EEPROM interface.

Figure 77. CPLD Implementation of a Flash EEPROM Interface



7.1.1 Slowport Signals

The Slowport signals are defined in Table 47; Slowport signals use LVTTL signal levels.

Table 47. Signal Description

Signal Name	Description	I/O
SP_AD[7:0]	Address and Data multiplexed bidirectional tri-state busses	I/O
SP_OE_L	Output enable for external buffer	O
SP_CP/SP_A0	Latch enable for 16- or 32-bit data bus devices. Address [0] for 8-bit devices.	O
SP_DIR/SP_A1	Data transaction direction. Low for read, High for write. Address [1] for 8-bit devices	O
SP_ALE_L	Address latch enable	O
SP_CS[1:0]	Device Selects: SP_CS[0] Lower 32-Mbyte address spaces used for FLASH. SP_CS[1] Upper 32-Mbyte address space used for Microprocessor type devices.	O
SP_RD_L	Read strobe	O
SP_WR_L	Write Strobe	O
SP_ACK	Acknowledge signal	I
SP_CLK	Clock	O

7.1.1.1 Topology and Routing

The following sections describe the topology and routing guidelines for Slowport interface control signals, clocks, and address/data signals.

7.1.1.1.1 Slowport Control Signals

Figure 78 illustrates the Slowport control signals topology.

Figure 78. Slowport Control Signals Topology

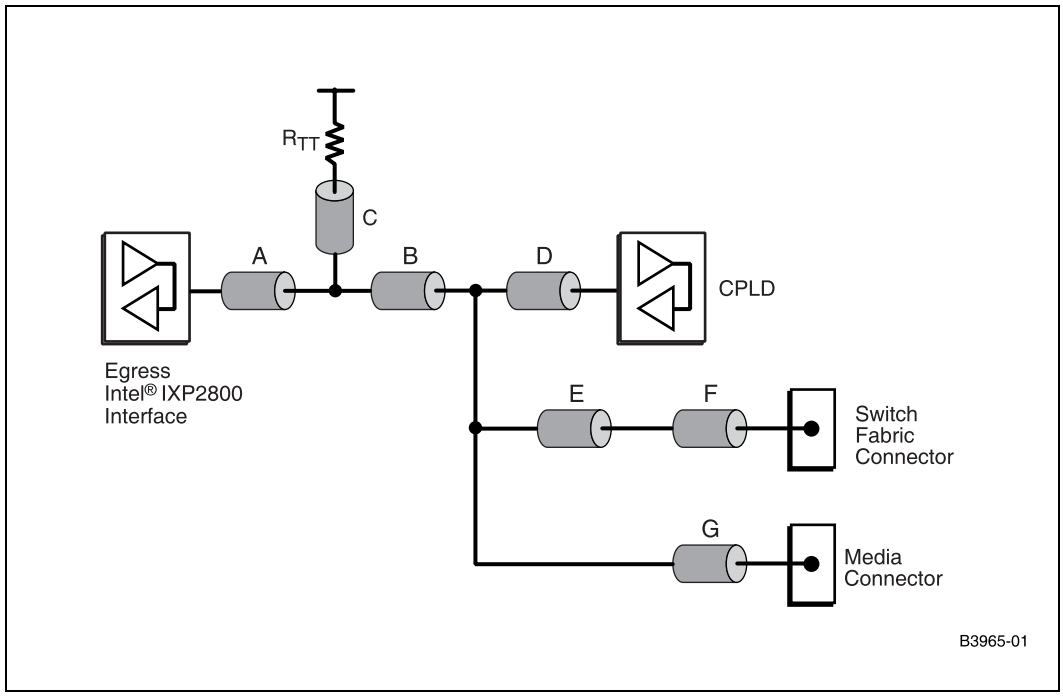


Table 48 provides routing guidelines for the Slowport control signals.

Table 48. Slowport Control Signals Routing Guidelines

Parameter	Routing Guideline
Signal Group	Slowport control
Topology	Daisy Chain
Reference Plane	Dual-Referenced, PWR-SIG-GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Group spacing	Isolation from other signal groups is 20 mils.
IXP28XX breakout guideline	4 mils with 4-mil space for a maximum of 300 mils.
Trace Length A	Maximum = 1500 mils.
Trace Length B	Maximum = 3500 mils.
Trace Length C	Maximum = 150 mils.
Trace Length D	Maximum = 100 mils.
Trace Length E	Maximum = 3000 mils.
Trace Length F	Maximum = 150 mils.
Trace Length G	Maximum = 6000 mils.
Resistor R_{tt}	4.7K Ω ±10%
Maximum via count per signal	8 vias

7.1.1.1.2 Slowport Clock Signals

Figure 79 illustrates the topology for the Slowport clock.

Figure 79. Slowport Clock Topology

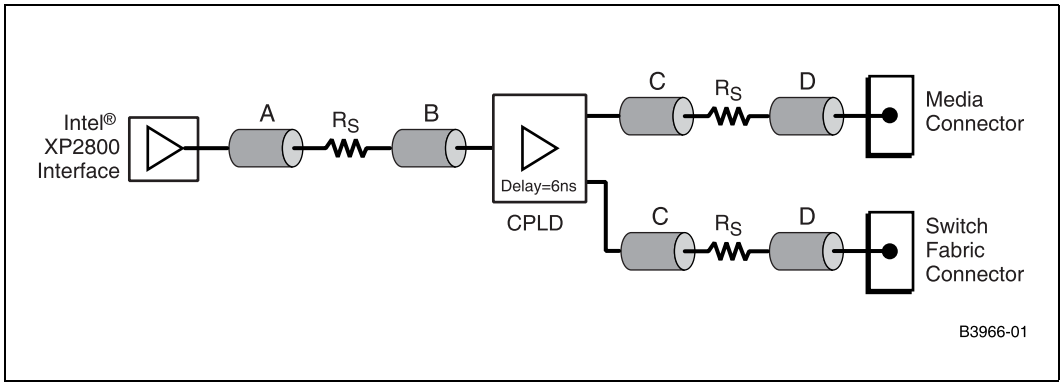


Table 49 provides routing guidelines for the Slowport media interface clock signals.

Table 49. Slowport Clock Signals Guideline

Parameter	Routing Guideline
Signal Group	Slowport Clock
Topology	Point-to-point
Reference Plane	Dual-referenced, PWR-SIG-GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Group spacing	Isolation from other signal groups is 20 mils.
IXP28XX breakout guideline	4 mil with 4-mil space for a maximum of 300 mils
Trace Length A	Maximum = 400 mils.
Trace Length B	Maximum = 5500 mils.
Trace Length C	Maximum = 250 mils.
Trace Length D	Maximum = 7000 mils.
Resistor - R_S	30.1 Ω ± 10%
Maximum Via Count per Signal	8 vias

7.1.1.1.3 Slowport Address/Data Signals

Figure 80 illustrates the topology for Slowport address/data signals.

Figure 80. Slowport Address/Data Topology

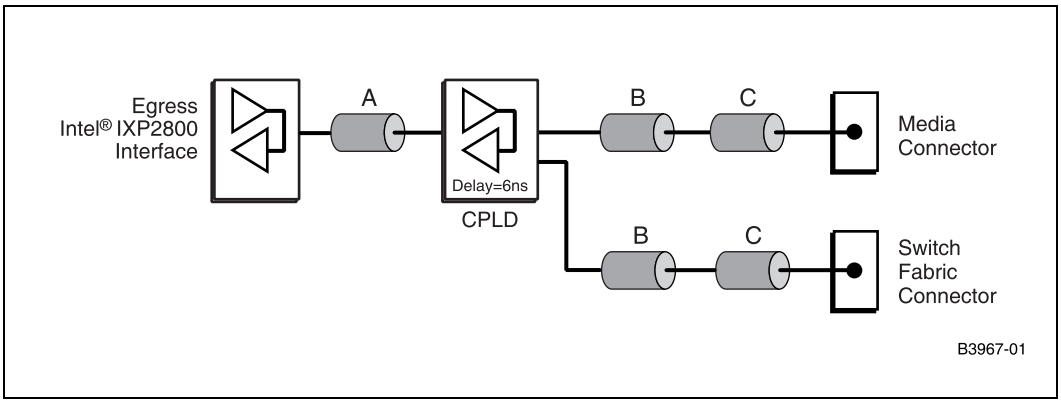


Table 50 provides routing guidelines for the Slowport address/data routing.

Table 50. Slowport Address/Data Routing Guidelines

Parameter	Routing Guideline
Signal Group	Address/Data
Topology	Point-to-point
Reference Plane	Dual-referenced, PWR-SIG-GND
Characteristic Trace Impedance	60 Ω ± 10%
Nominal Trace Width	3.5 mils
Nominal Trace Separation	9 mils
Group spacing	Isolation from non-Slowport-related signals is 20 mils.
IXP2800 breakout guideline	4 mil with 4-mil space for a maximum of 300 mils
Trace Length A	Maximum = 5000 mils.
Trace Length B	Maximum = 4000 mils.
Trace Length C	Maximum = 250 mils.
Maximum via count per signal	8 vias

7.1.2 Flash Memory and Microprocessor Interface Support

The Slowport supports two types of interfaces: the flash memory interface and the microprocessor interface. Two chip-select signals, SP_CS[1:0], differentiate between the two interfaces. The total address window for the Slowport is 64 Mbytes, which is divided into two 32-Mbyte regions, one region for each interface. Access to the lower 32-Mbyte region of address space is decoded with SP_CS[0], while access to the upper 32-Mbyte region of microprocessor space is decoded with SP_CS[1]. Using these two signals, the glue logic distinguishes between accesses to each interface.

Refer to the *Intel® IXP2800 Network Processor Hardware Reference Manual* for additional details about the Slowport unit.

7.1.2.1 Flash PROM Interface Logic

The following sections describe the address latch logic and provide example implementations of this logic.

7.1.2.1.1 Address Latch Logic

The flash memory interface only supports 8-bit devices; therefore, no data packing or unpacking is required. Since the address bus is only eight bits wide, the 24-bit address must be latched by the external logic. The address is shifted out by the network processor, eight bits at a time in three consecutive clock cycles to form the upper 24 bits (A[25:2]) of the address, while the lower two bits (A[1:0]) are provided on dedicated pins.

The external logic monitors the SP_ALE_L signal; when this signal is asserted, the external logic latches the presented address on the SP_AD[7:0] bus on the rising edge of SP_CLK for three consecutive cycles. The least significant byte (LSB) of the address is delivered first and the most significant byte (MSB) is presented last.

Note: Timing diagrams for all supported modes are provided in the Slowport unit section of the *Intel® IXP2800 Network Processor Hardware Reference Manual*. We recommend that you consult the HRM and review *all* of the timing diagrams in that section.

The Verilog* code in Example 1 depicts an example implementation of the logic:

Example 1. PROM Address Latch Logic

```
// implementation of address packing logic
always @(posedge sp_clk) begin
    if (~rst_l) begin
        latched_add    <= 24'h000000;
    end
    else begin
        sp_ale_l_d     <= sp_ale_l;
        if (~sp_ale_l) begin
            latched_add[7:0]   <= sp_ad_in;
            latched_add[15:8]  <= latched_add[7:0];
            latched_add[23:16] <= latched_add[15:8];
        end
    end // else: !if(~rst_l)
end // always @ (posedge sp_clk)
```

This logic is equivalent to the F377 devices shown in Figure 81.

No additional logic is required to interface to the flash. Figure 82 and Figure 83 depict the timing for a single write and read transaction, respectively, to the flash memory interface.

Figure 81. Slowport Application Topology

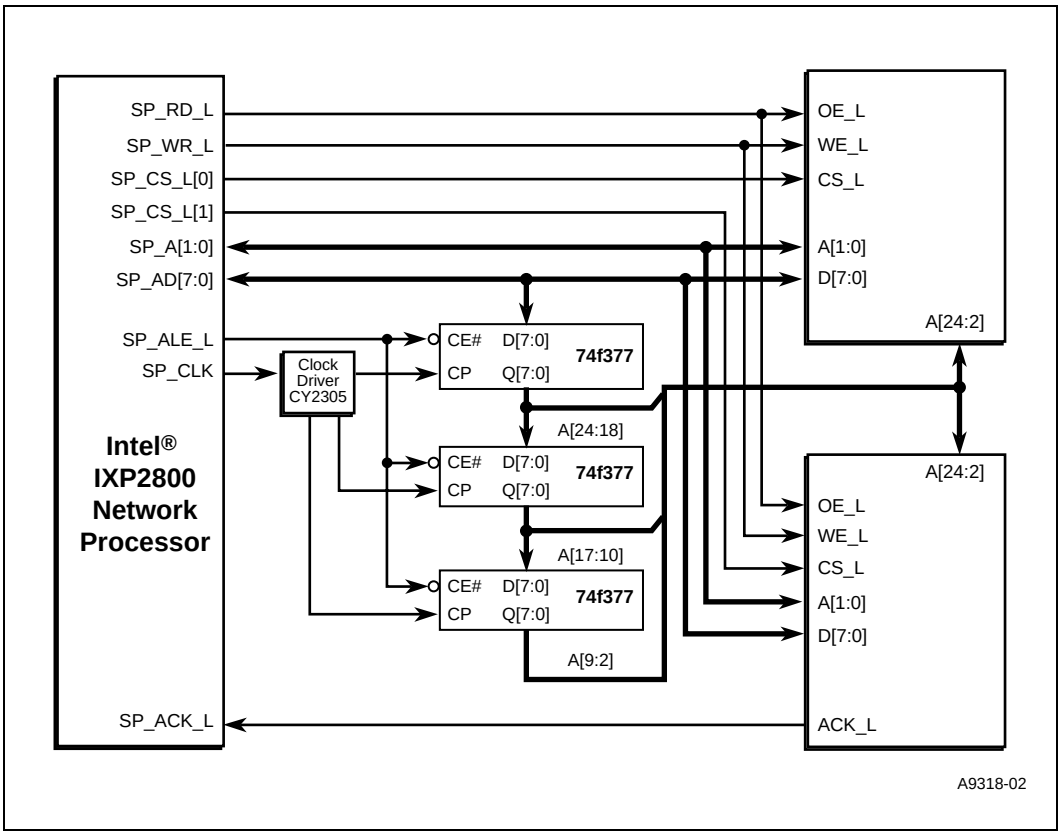


Figure 82. Mode 0 Single Write Transfer for a Fixed-timed Device

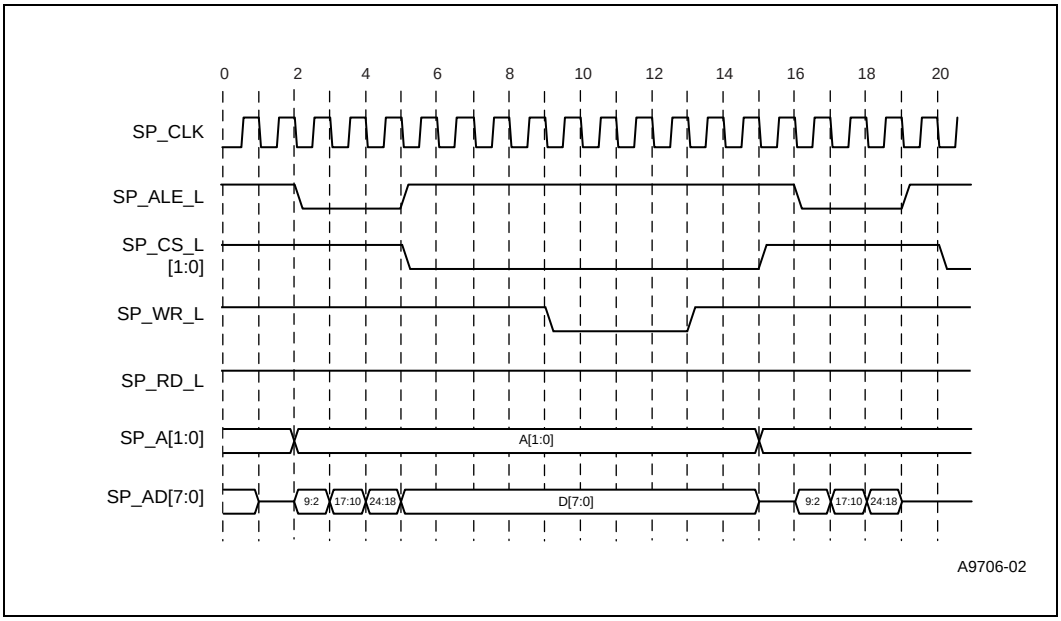
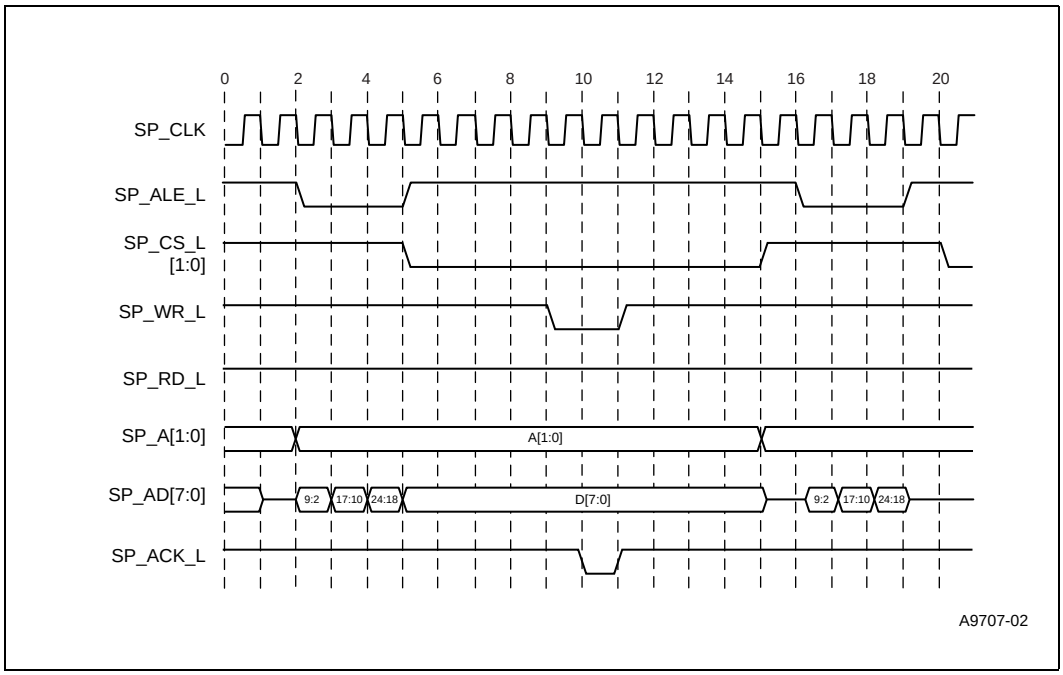


Figure 83. Mode 0 Single Write Transfer for a Self-timing Device



7.1.2.2 Microprocessor Interface Logic

The Slowport microprocessor interface can be configured to support 8-, 16-, and 32-bit devices. Refer to the *Intel® IXP2400 and IXP2800 Network Processor Programmer's Reference Manual* for detailed information about each mode.

As with the flash interface, external logic must be implemented to latch the address. Since this interface can also support 8-, 16-, and 32-bit devices, external logic must also be implemented to perform the packing and unpacking of the read and write data when configured for 16- and 32-bit mode. To control the packing and unpacking of data and steer the direction of the bus, the microprocessor interface provides three additional signals: SP_CP, SP_OE_L, and SP_DIR.

The logic required to latch the address is the same as the logic described in Figure 81 for the flash interface. The following sections describe the differences from the flash interface as they pertain to the address latch logic and data multiplexing and demultiplexing; each section provides example implementations of the appropriate logic.

7.1.2.2.1 Address Latch Logic

The size of the address for the flash interface is fixed, but is programmable in the microprocessor interface. The Slowport address size/data width control register, SP_ADC, configures the size of the address and data bus. Since the address can be 8-, 16-, 24-, or 25-bits wide, the number of clock cycles required to latch the address could be as many as four for the 25-bit case, and as few as one for the 8-bit case. The mechanism for latching the address is the same: on the rising edge of SP_CLK if SP_ALE_L is asserted. The number of clock cycles in which SP_ALE_L is asserted varies and depends on the programmed address size. The address logic implemented for the flash interface could be modified for the microprocessor interface as depicted in Example 2.

Example 2. Microprocessor Address Latch Logic

```
// implementation of 25-bit address packing control logic
always @(posedge sp_clk) begin
    if (~rst_l) begin
        ale_cnt   <= 2'b00;
    end
    else begin
        if (~sp_ale_l)begin
            ale_cnt   <= ale_cnt + 1;
        end
        else if (sp_ale_l) begin
            ale_cnt   <= 2'b00;
        end
    end // else: !if(~rst_l)
end // always @ (posedge sp_clk)
always @(posedge sp_clk) begin
    if (~rst_l) begin
        latched_add    <= 25'h0000000;
    end
    else begin
        if (~sp_ale_l) begin
            case (ale_cnt)   //synopsys full_case parallel_case
            2'b00:   latched_add[7:0]     <= sp_ad_in;
            2'b01:   latched_add[15:8]    <= sp_ad_in;
            2'b10:   latched_add[23:16]   <= sp_ad_in;
            2'b11:   latched_add[24]      <= sp_ad_in[0];//for 25-bit address space
            endcase // case(ale_cnt)
        end
    end // else: !if(~rst_l)
end // always @ (posedge sp_clk)
```

In Example 2, we use a two-bit count, `ale_cnt`, to steer the data into the appropriate byte-lane. Another method would be to define the `latched_add` register to be 32 bits, dropping any unused upper bits; then `ale_cnt` would not be needed. Example 3 shows a coded example of this logic.

Example 3. Microprocessor Address Latch Logic Without `ale_cnt`

```
// implementation of 32-bit address packing logic
always @(posedge sp_clk) begin
    if (~rst_l) begin
        latched_add    <= 32'h00000000;
    end
    else begin
        if (~sp_ale_l) begin
            latched_add[7:0]       <= sp_ad_in;
            latched_add[15:8]      <= latched_add[7:0];
            latched_add[23:16]     <= latched_add[15:8];
            latched_add[31:24]     <= latched_add[23:16];
        end
    end // else: !if(~rst_l)
end // always @ (posedge sp_clk)
```

7.1.2.2.2 Data Multiplexing and Demultiplexing

The microprocessor interface supports 8-, 16-, and 32-bit devices while the flash interface supports only 8-bit devices. This functionality requires that the SP_AD data bus be multiplexed/demultiplexed to support read and write transactions. Additionally, there are four

different operating modes that are implemented to support a variety of microprocessor interfaces, with different address and data widths. For more information on the operating modes, refer to the *Intel® IXP2800 Network Processor Hardware Reference Manual.*

7.1.2.2.3 Write Transactions

During write transactions to 16- and 32-bit devices, the 8-bit data from the IXP28XX SP_AD bus must be packed into 16 bits (WORD) or 32 bits (DWORD). Extra signals, SP_CP, SP_OE_L, and SP_DIR, provide the management of packing and unpacking operations and control which device drives the bus during read and write transactions.

Note: The actual protocol of these control signals varies depending on the interface configuration mode (1, 2, 3, or 4). The remainder of this section concentrates on the Mode 3 protocol, the mode that would be used to interface to the Intel® IXF1010 10-port 100/1000Mbps Ethernet MAC.

Figure 84 shows an example of discrete components and their associated signal connections that could be used to implement the glue logic. Figure 85 shows the timing of the Slowport interface signals presented to the glue logic during a write transaction with the Slowport configured for Mode 3, i.e., SP_PCR = 0x3, and the address and data size set to 32-bit, i.e., SP_ADC = 0x33.

Figure 84. An Interface Topology with Intel / AMCC* SONET/SDH Device

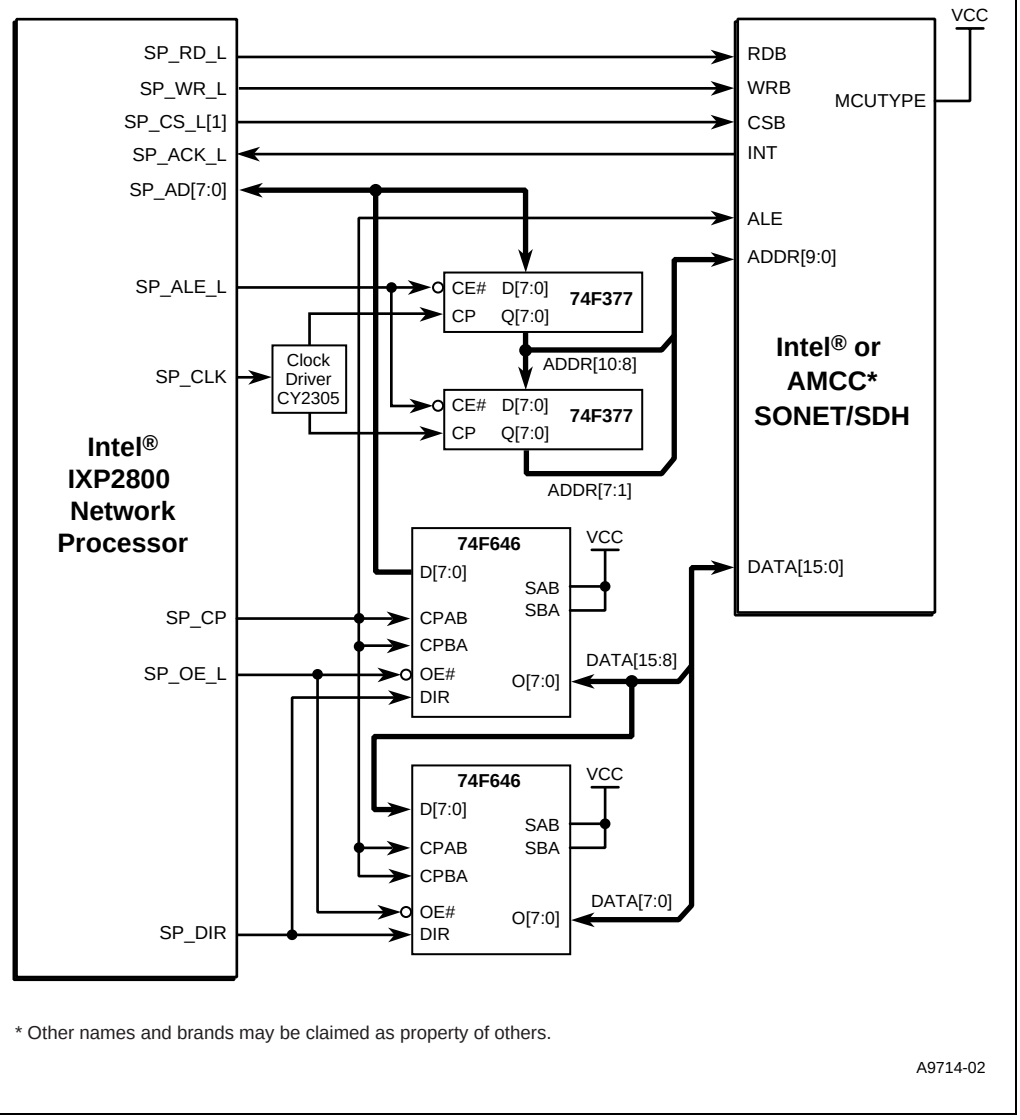
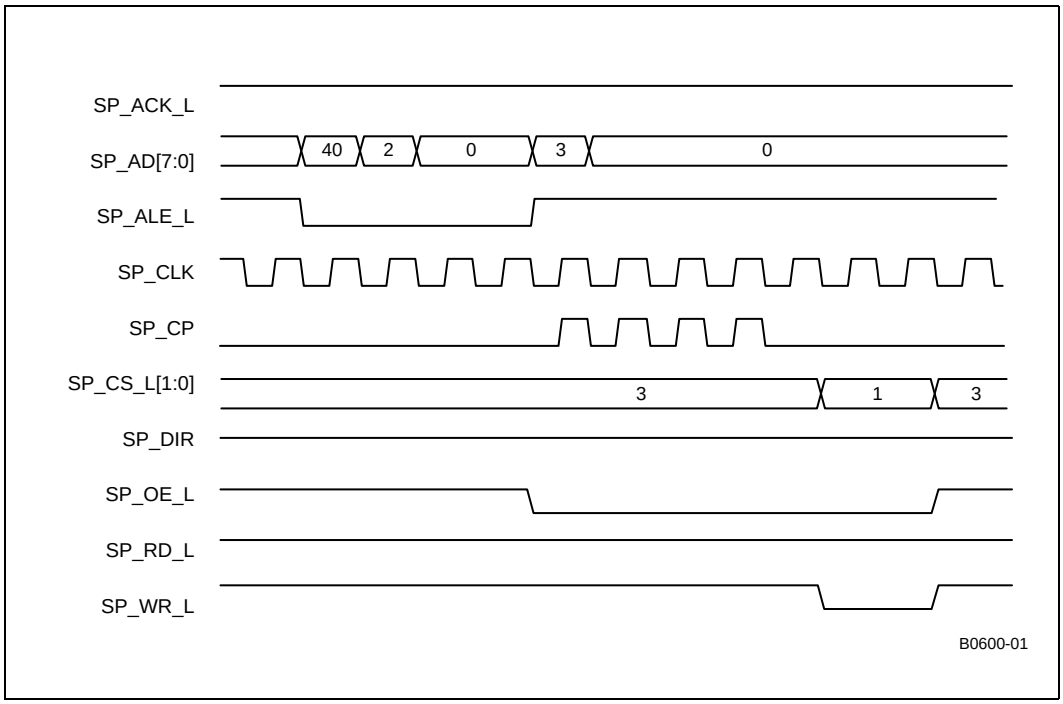


Figure 85. Mode 3 32-Bit Write Transfer

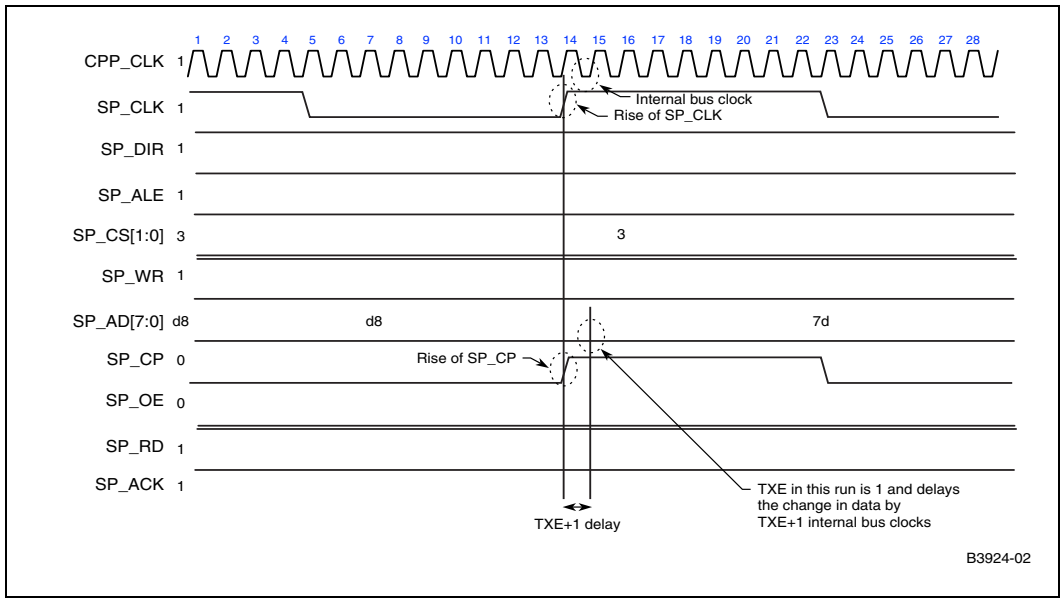


To pack the 32-bit write data, the IXP28XX network processor drives a byte of write data onto the SP_AD bus in four cycles that are qualified with the rising edge of the SP_CP signal, with the SP_OE_L && SP_DIR signal being active, i.e., SP_OE_L = 0 and SP_DIR = 1. On every rising edge of the SP_CP signal with SP_OE_L && SP_DIR asserted, the data is shifted into a register implemented in the glue logic device – from least significant byte (LSB) through most significant byte (MSB).

Note: The IXP28XX CSR Transmit Enable Register (SP_TXE) can be used to delay the data and relevant Slowport signals in relation to the SP_CLK. For programming information, refer to the *Intel® IXP2800 Network Processor Hardware Reference Manual*.

Figure 86 is a Slowport Mode 3 Write example with TXE +1 delay using SP_TXE.

Figure 86. Slowport Mode 3 write example showing TXE +1 delay using SP_TXE



The Verilog* code in Example 4 is an example implementation of the logic.

Example 4. 32-bit Write Data Packing Logic Implementation

```
//implementation of latch control for 32-bit pack/unpacking to/from NP
//to uP port
always @(posedge sp_a[0]) begin
    if (~rst_l) begin
        data[31:0]    <= 32'h0000_0000;
    end
//data is shifted during four cycles
    if (~sp_oe_l && sp_a[1]) begin
        data[31:24]     <= sp_ad_in;
        data[23:16]     <= data[31:24];
        data[15:8]      <= data[23:16];
        data[7:0]       <= data[15:8];
    end
//here we can latch all the read data, the controller will
//pulse SPA[0] multiple times but it's a "don't care"
//as we capture all 32-bits on each edge of SP_CP
    else begin
        if (~sp_rd_l) begin
            data[31:0]    <= uP_rd_data;
        end
    end // else: !if(~sp_oe_l && sp_rd_l)
end // always @ (posedge spa[0])
```

In the Example 4 code, the 32-bit register used for latching the write data is also used for latching the read data, decreasing the number of gates needed for implementing the glue logic. If desired, separate registers for latching the write and read data can be used; in this case, the rising edge of the SP_RD_L signal is used to capture the read data and the SP_CP signal is not used.

7.1.2.2.4 Read Transactions

As with the write operations, the read transactions to 16- and 32-bit devices will need to be unpacked: eight bits per cycle prior to the data being sent back to the IXP28XX network processor via the SP_AD bus. Again, the SP_CP, SP_OE_L, and SP_DIR signals implement the control logic needed to perform the unpacking of the read data. This example also highlights the logic required for Mode 3.

The glue logic is responsible for latching the 32-bit read data coming from the downstream device on the rising edge of the read signal or as specified by the device. Figure 87 shows the timing of the Slowport interface signals presented to the glue logic during a read transaction.

Note: The IXP28XX CSR Receive Enable Register (SP_RXE) can be used to advance the data sampled internally before the rising edge of the SP_CLK. For programming SP_RXE, refer to the *Intel® IXP2400 and IXP2800 Network Processor Programmer's Reference Manual*. Figure 88 is an example of a Slowport Mode 3 Read with RXE = 2.

Figure 87. Mode 32-Bit Read Transfer

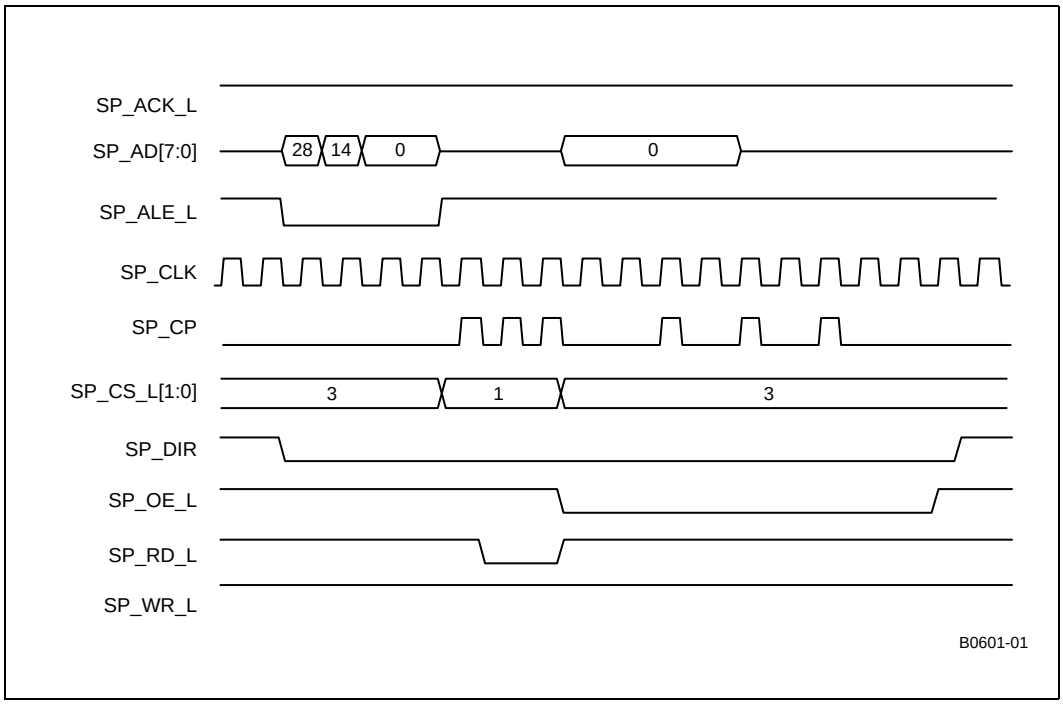
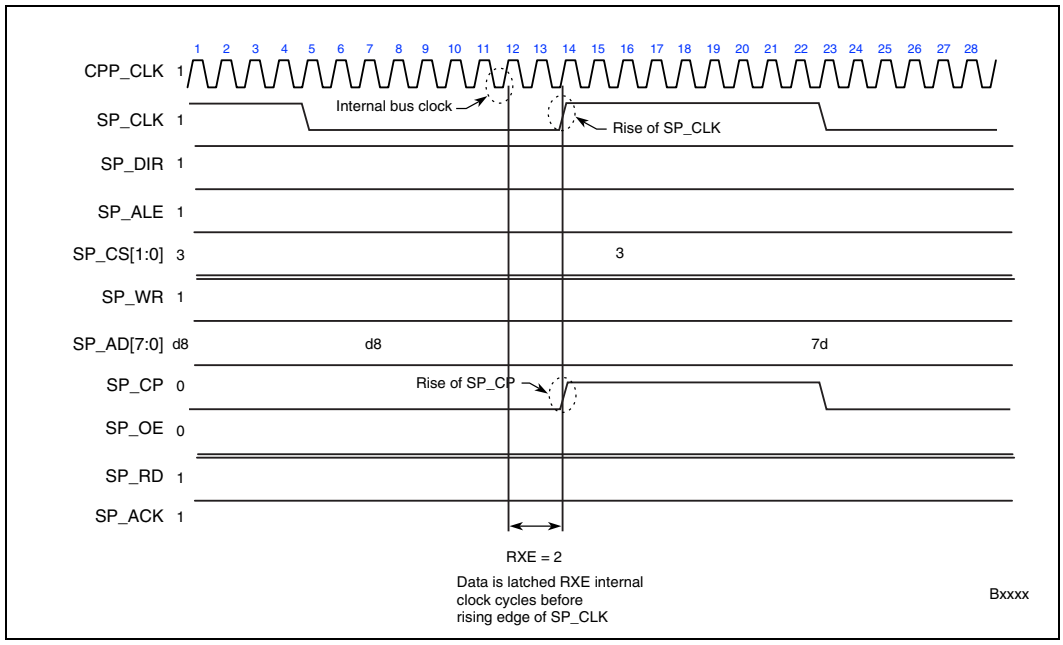


Figure 88. Slowport Mode 3 read example showing RXE = 2



The glue logic latches all 32 bits of read data on the rising edge of SP_CP if SP_RD_L is asserted. The logic latches all the data on each rising edge and will always get the last 32 bits of data presented on the data bus, and is therefore unaffected by multiple pulses of the bus. Alternately, the rising edge of the SP_RD_L signal could be used in place of SP_CP to latch the read data; however this procedure requires separate registers for the read and write data, as explained in Section 7.1.2.2.4.

The read-latching logic, shown in Example 4, is combined with the data-packing logic and shares the same 32-bit register. After the data is captured, the logic must also unpack the data back to the IXP28XX network processor at eight bits per transfer (MSB to LSB) onto the SP_AD. This is accomplished by the glue logic driving the first byte of the read data back to the network processor on the SP_RD_OUT bus when the signal SHIFT_EN is asserted.

Note: The SHIFT_EN signal is used in combination with a two-bit counter, PACK_CNT, which is used to steer the appropriate byte, based on the count, onto the SP_RD_OUT bus. The PACK_CNT counter is incremented on every rising edge of SP_CP if the SHIFT_EN control signal is asserted; PACK_CNT is cleared if SHIFT_EN is de-asserted. This procedure ensures that PACK_CNT will be zero at the beginning of each read cycle. As the count increments, the appropriate byte is driven onto the SP_RD_OUT bus as SP_CP is pulsed to complete the 32-bit transfer.

The SHIFT_EN control signal detects if the SP_OE_L signal is asserted, the SP_RD_L signal is de-asserted, and the SP_DIR signal is de-asserted; these conditions indicate this is a read cycle and that the glue logic owns the bus. Ultimately, the SP_RD_OUT bus connects to the output port of a bidirectional buffer, which will connect to the SP_AD bus. The output enable for this buffer can be controlled by SP_DIR or the SHIFT_EN control signal. The Verilog* code in Example 5 depicts an example implementation of the SHIFT_EN control signal and the data unpacking logic.

Note: The SP_CP signal may pulse after the SP_RD_L signal has been deasserted; therefore, only the SP_OE_L, SP_DIR, and SP_CP signals should be used to control the unpacking of the data.

On the clock cycle after the read signal is de-asserted from the downstream device, the glue logic will drive the first byte of data onto the SP_AD bus since the IXP28XX network processor does not pulse the SP_CP signal to promote the first read. The remaining three bytes of data are shifted out on the rising edge of the SP_CP signal to complete the 32-bit transfer.

Example 5. 32-bit Read Unpacking Logic Implementation

```
// control logic for shifting the 32-bit read data back to IXP, 8-bits
// per cycle
assign shift_en = (~sp_oe_l && ~sp_a[1]);
```

The following Verilog* code depicts an example implementation of the data unpacking logic:

```
// implementation of pack_cnt control logic, the count is incremented on each
// rising edge of sp_a[0] if shift_en is active
always @(posedge sp_a[0]) begin
    if (~rst_l) begin
        pack_cnt   <= 2'b00;
    end
    else begin
        if (shift_en)begin
            pack_cnt   <= pack_cnt + 1;
        end
        else if (~shift_en) begin
            pack_cnt   <= 2'b00;
        end
    end // else: !if(~rst_l)
end // always @ (posedge sp_clk)


// Implementation of read data mux, pack_cnt is used to determine which byte
// should be driven onto the sp_rd_out bus
always @ (pack_cnt) begin
    //data is shifted during four consecutive cycles
    case (pack_cnt)    //synopsis full_case parallel_case
        2'b00:   sp_rd_out     <= #1 data[31:24];
        2'b01:   sp_rd_out     <= #1 data[23:16];
        2'b10:   sp_rd_out     <= #1 data[15:8];
        2'b11:   sp_rd_out     <= #1 data[7:0];
    endcase // case(pack_cnt)
end
```

7.2 Summary

The address latching control logic for the PROM and microprocessor ports is essentially the same; the only difference is the PROM port constant fixed size (24 bits) and the latching of the PROM port during three consecutive clock cycles.

For the microprocessor port, the size of the address is programmable via the SP_ADC register. Depending on the programmed size of the address, this could be 8 to 25 bits, which will require one to four cycles to latch. In our example, we used the 25-bit case because this is a complete implementation and can be easily modified to support the other three values.

The data packing/unpacking logic examples were chosen to provide an interface to an Intel/AMCC* device. While the other modes have subtle protocol and interface signal differences, the logic used for address latching and data packing/unpacking should be essentially the same. Again, the example uses the 32-bit case because this is a complete implementation and can be easily modified to support 8- or 16-bit devices.

Some minor changes may be required for the control logic; however the general concept remains unchanged as it uses the same combination of F377 flip-flops and F646 Octal registers for the glue logic in all modes.

Mechanical/Packaging 8

8.1 Package Marking

The Intel® IXP2800 Network Processor package marking is shown in Figure 89, and the Intel® IXP2850 Network Processor package marking is shown in Figure 90.

Product Name	Stepping	QDF Number	Marketing Part Number	Version
RPIXP2800BA	B0	Q668	MM# 857259	1.0 GHz
RPIXP2800BB	B0	Q669	MM# 857266	1.4 GHz
RPIXP2800BC	B1	Q853	MM# 862906	650 MHz
RPIXP2800BA	B1	Q808	MM# 861093	1.0 GHz
RPIXP2800BB	B1	Q809	MM# 861099	1.4 GHz
RPIXP2800BC	B1	NA[1]	MM# 862907	650 MHz
RPIXP2800BA	B1	NA[1]	MM# 862117	1.0 GHz
RPIXP2800BB	B1	NA[1]	MM# 855650	1.4 GHz
RPIXP2850BA	B0	Q670	MM# 858140	1.0 GHz
RPIXP2850BB	B0	Q671	MM# 858141	1.4 GHz
RPIXP2850BC	B1	Q854	MM# 862908	650 MHz
RPIXP2850BA	B1	Q810	MM# 861102	1.0 GHz
RPIXP2850BB	B1	Q811	MM# 861132	1.4 GHz
RPIXP2850BC	B1	NA[1]	MM# 862910	650 MHz
RPIXP2850BA	B1	NA[1]	MM# 862113	1.0 GHz
RPIXP2850BB	B1	NA[1]	MM# 862114	1.4 GHz

1. Not applicable — production-qualified devices are not marked with a QDF number.

Figure 89. Intel® IXP2800 Network Processor Package Marking

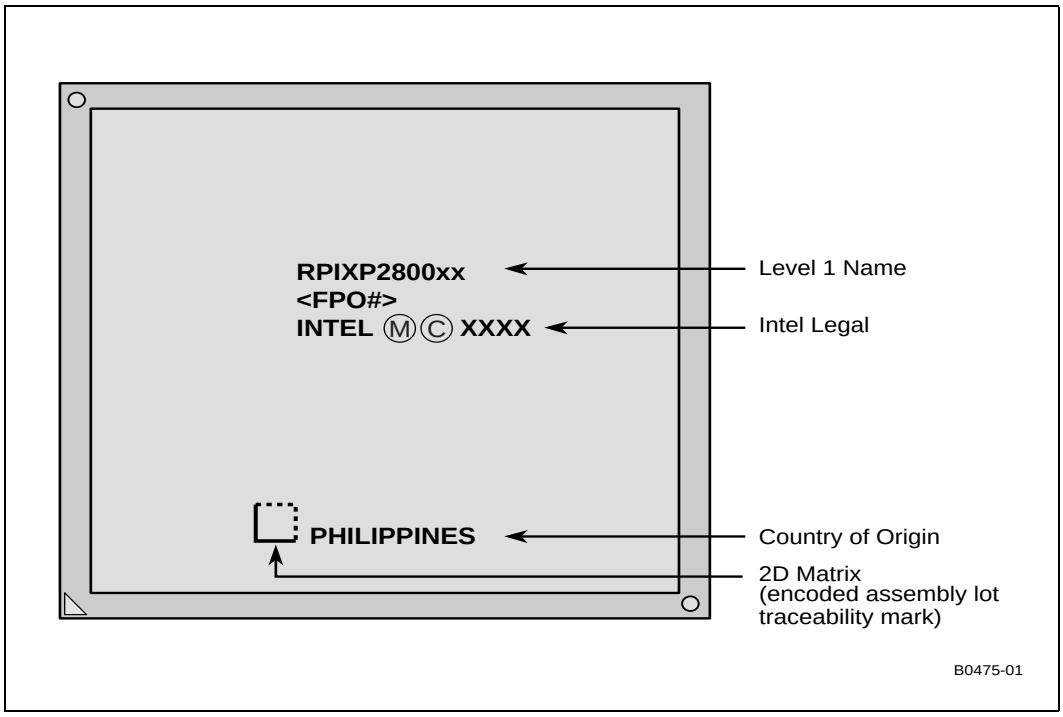
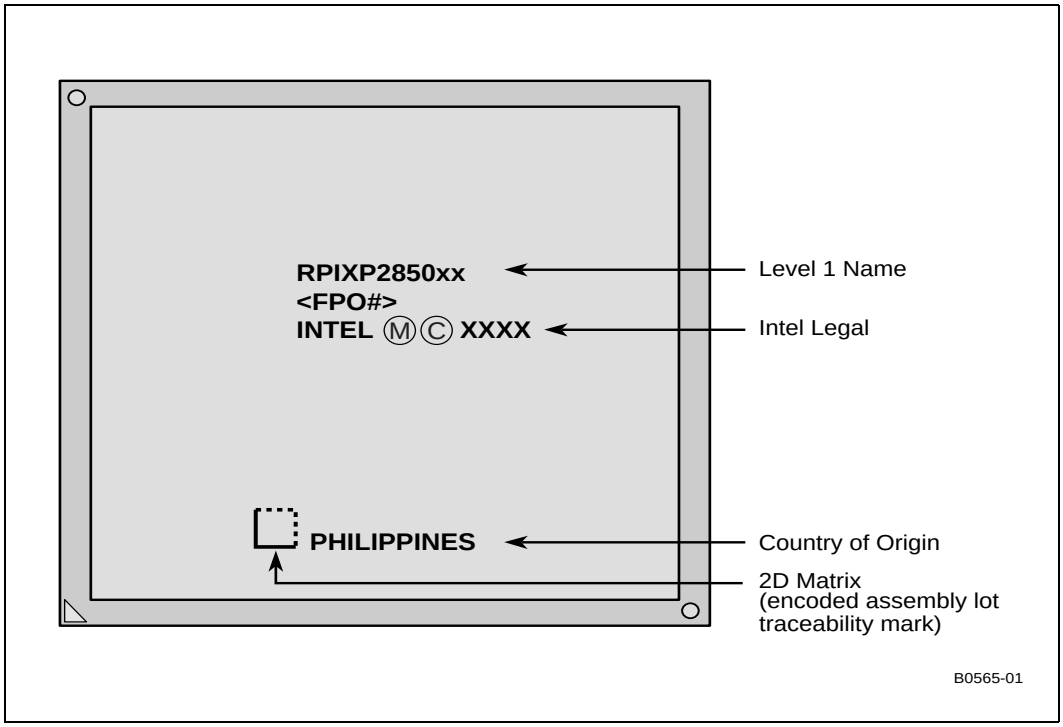


Figure 90. Intel® IXP2850 Network Processor Package Marking



8.2 Package Dimensions

The network processor package dimensions are shown in Figure 91, Figure 92, and Figure 93and detailed in Table 51.

Figure 91. Intel® IXP2800 or Intel® IXP2850 Network Processor Package Ball Grid Array

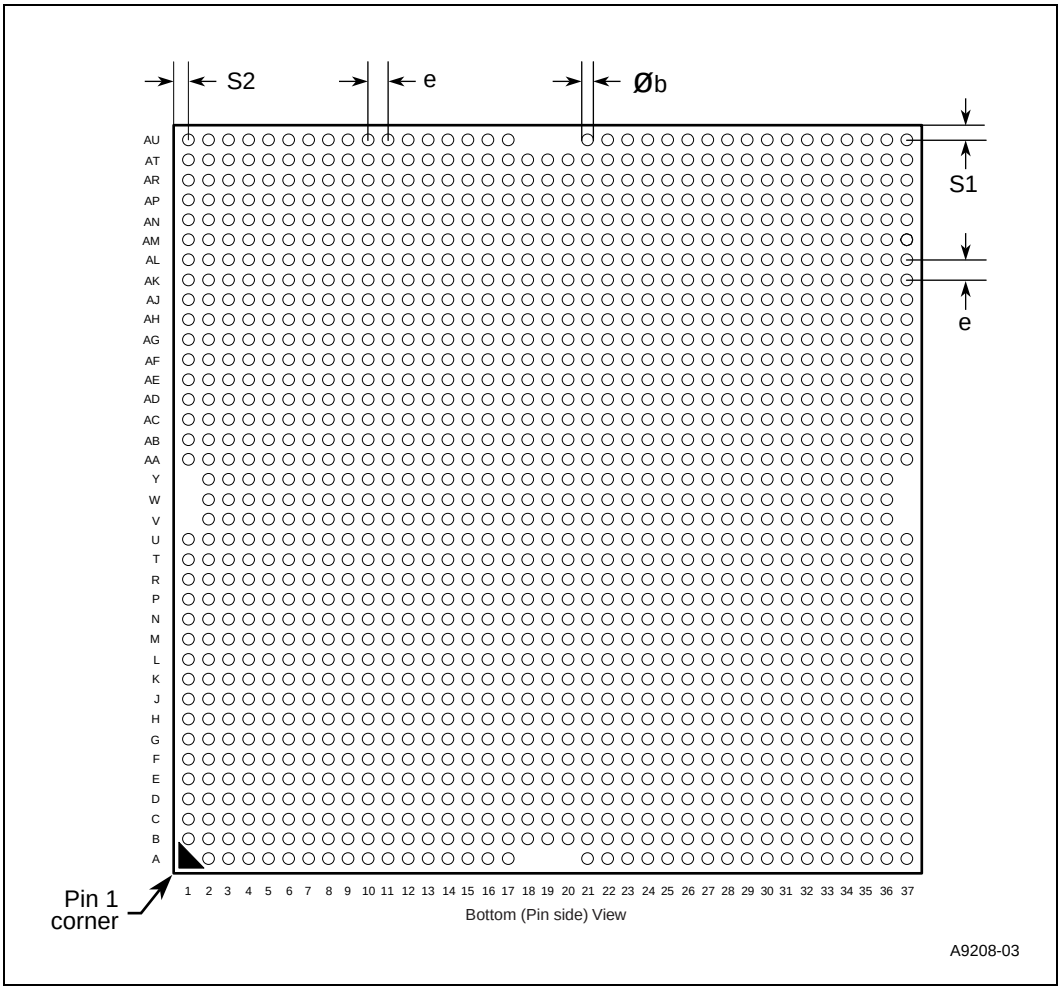


Figure 92. Intel® IXP2800 or Intel® IXP2850 Network Processor Package Side View

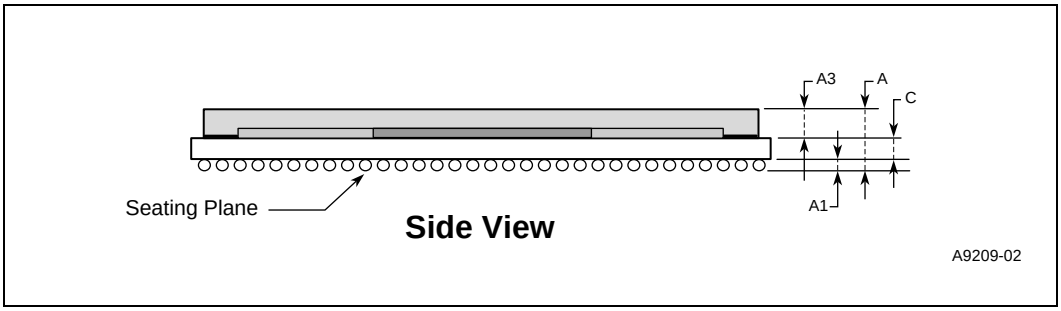


Figure 93. Intel® IXP2800 or Intel® IXP2850 Network Processor Package Top View

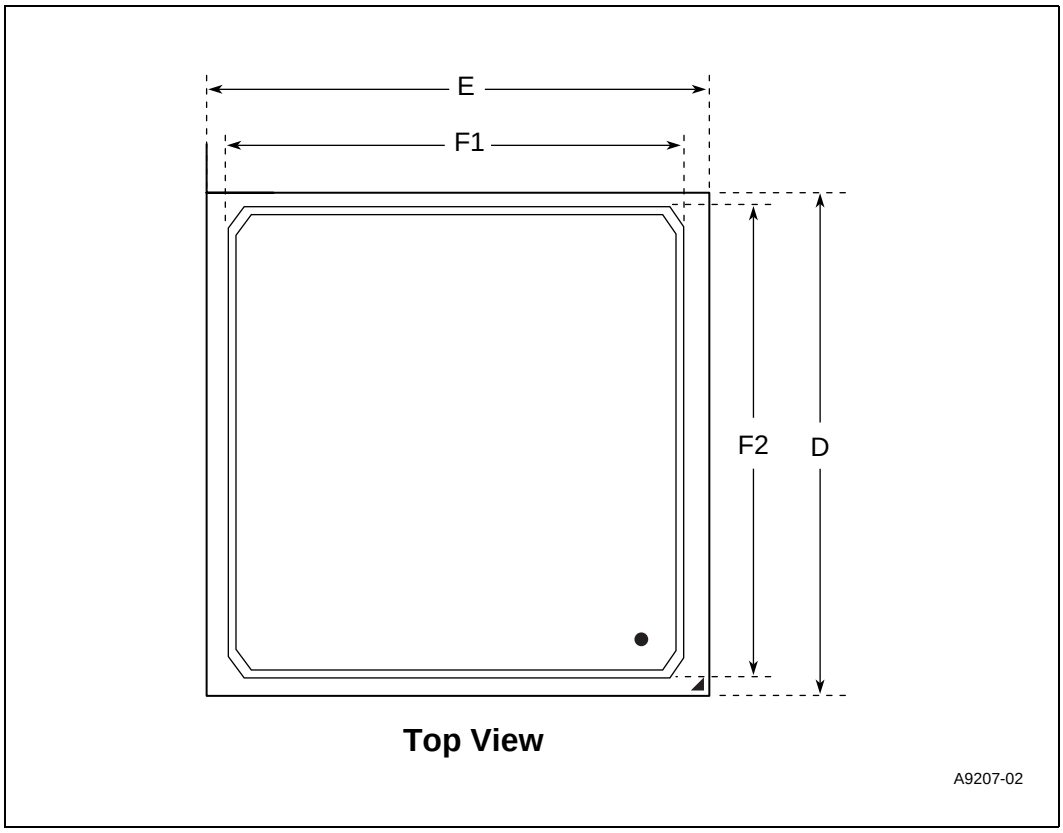


Table 51. Intel® IXP2800 or IXP2850 Network Processor Package Dimensions

Symbol	Minimum	Maximum
A	3.891	4.565
A1	0.40	0.60
A3	2.266	2.49
b	0.61	
C	1.225	1.475
D	37.45	37.55
E	37.45	37.55
F1	33.4	33.6
F2	33.4	33.6
e	1.00	
S1	0.750	
S2	0.750	
Note: All dimensions are in millimeters (mm).		

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