



# Intel® IXP1250 Network Processor

## Datasheet

### Product Features

The Intel® IXP1250 Network Processor delivers high-performance processing power and flexibility to a wide variety of LAN and telecommunications products. Distinguishing features of the IXP1250 are the performance of ASIC hardware along with programmability of a microprocessor.

- **Applications**
  - Multi-layer LAN Switches
  - Multi-protocol Telecommunications Products
  - Broadband Cable Products
  - Remote Access Devices
  - Intelligent PCI adapters
- **Integrated StrongARM® Core**
  - High-performance, low-power, 32-bit Embedded RISC processor
  - 16 Kbyte instruction cache
  - 8 Kbyte data cache
  - 512 byte mini-cache for data that is used once and then discarded
  - Write buffer
  - Memory management unit
  - Access to IXP1250 FBI Unit, PCI Unit and SDRAM Unit via the ARM® AMBA Bus
- **Six Integrated Programmable Microengines**
  - Operating frequency of up to 232 MHz
  - Multi-thread support of four threads per microengine
  - Single-cycle ALU and shift operations
  - Zero context swap overhead
  - Large Register Set: 128 General-Purpose and 128 Transfer Registers
  - 2 K x 32-bit Instruction Control Store
  - Access to the IXP1250 FBI Unit, PCI DMA channels, SRAM, and SDRAM
- **High Bandwidth I/O Bus (IX Bus)**
  - 64-bit, up to 104 MHz operation
  - 6.6 Gbps peak bandwidth
  - 64-bit or dual 32-bit bus options
- **Integrated 32-bit, 66 MHz PCI Interface**
  - Supports *PCI Local Bus Specification Revision 2.2* as a Bus Master
  - 264 Mbytes/sec peak burst mode operation
  - I<sup>2</sup>O\* support for StrongARM Core
  - Dual DMA channels
- **Industry Standard 64-bit SDRAM Interface**
  - Peak bandwidth of up to 928 Mbytes/sec
  - Address up to 256 Mbytes of SDRAM
  - Memory bandwidth improvement through bank switching
  - Read-modify-write support
  - Byte aligner/merger
  - Cyclic Redundancy Check (CRC)
  - Error Correction Code (ECC)
- **Industry Standard 32-bit SRAM Interface**
  - Peak bandwidth of up to 464 Mbytes/sec
  - Address up to 8 Mbytes of SRAM
  - Up to 8 Mbytes FlashROM for booting StrongARM Core
  - Supports atomic push/pop operations
  - Supports atomic bit set and bit clear operations
  - Memory bandwidth improvement by reduced read/write turnaround bus cycles
- **Other Integrated Features**
  - Hardware Hash Unit for generation of 48- or 64-bit adaptive polynomial hash keys
  - Serial UART port
  - Real Time Clock
  - Four general-purpose I/O pins
  - Four 24-bit timers with CPU watchdog support
  - Limited JTAG Support
  - 4 Kbyte Scratchpad Memory
- **520-pin, HL-PBGA package**
- **2 V CMOS device**
  - 3.3 V tolerant I/O

**Notice:** This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 278371-006  
December 2001

## Revision History

---

Date	Revision	Description
February 2001	001	Advance Information release.
March 2001	002	Preliminary release.
May 11, 2001	003	First external release.
June 1, 2001	004	Revised Extended Temperature maximum power.
August 10, 2001	005	Updates for the V2.0 SDK. Changes to the SRAM Bus and SDRAM Bus signal timing parameters.
December 10, 2001	006	Updates for the V2.01 SDK.

Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The IXP1250 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Copyright © Intel Corporation, 2001

Intel is a registered trademark of Intel Corporation or its subsidiaries in the United States and other countries

\*Other names and brands may be claimed as the property of others.

# Contents

1.0	Product Description .....	9
2.0	Functional Units.....	11
2.1	Conventions .....	11
2.2	StrongARM* Core Microprocessor .....	11
2.3	Microengines .....	11
2.4	FBI Unit and the IX Bus.....	12
2.4.1	IX Bus Access Behavior .....	12
2.4.1.1	Reset and Idle Bus Considerations .....	14
2.5	SDRAM and SRAM Units.....	15
2.5.1	SDRAM Unit .....	15
2.5.2	SDRAM Bus Access Behavior .....	16
2.5.3	SDRAM Cyclic Redundancy Checking (CRC) .....	17
2.5.4	SDRAM Error Correction Code (ECC) .....	17
2.5.5	SDRAM Configurations .....	18
2.5.6	SRAM Unit.....	18
2.5.6.1	SRAM Types Supported.....	20
2.5.6.2	SRAM Configurations.....	20
2.5.6.3	BootROM Configurations .....	21
2.5.6.4	SRAM Bus Access Behavior .....	21
2.6	PCI Unit.....	22
2.6.1	PCI Arbitration and Central Function Support .....	22
2.7	Device Reset.....	23
2.7.1	Hardware Initiated Reset.....	25
2.7.2	Software Initiated Reset .....	25
2.7.3	PCI Initiated Reset .....	25
2.7.4	Watchdog Timer Initiated Reset .....	25
3.0	Signal Description .....	26
3.1	Pinout Diagram.....	26
3.2	Pin Type Legend .....	27
3.3	Pin Description, Grouped by Function.....	28
3.3.1	Processor Support Pins.....	28
3.3.2	SRAM Interface Pins .....	29
3.3.3	SDRAM Interface Pins .....	31
3.3.4	IX Bus Interface Pins.....	33
3.3.5	General Purpose I/Os.....	37
3.3.6	Serial Port (UART) Pins .....	37
3.3.7	PCI Interface Pins .....	38
3.3.8	Power Supply Pins .....	41
3.3.9	IEEE 1149.1 Interface Pins .....	42
3.3.10	Miscellaneous Test Pins.....	42
3.3.11	Pin Usage Summary .....	43
3.4	Pin/Signal List.....	44
3.5	Signals Listed in Alphabetical Order .....	49
3.6	IX Bus Pins Function Listed by Operating Mode .....	53
3.7	IX Bus Decode Table Listed by Operating Mode Type .....	63

3.8	Pin State During Reset.....	65
3.9	Pullup/Pulldown and Unused Pin Guidelines.....	67
4.0	Electrical Specifications.....	68
4.1	Absolute Maximum Ratings.....	68
4.2	DC Specifications.....	71
4.2.1	Type 1 Driver DC Specifications.....	71
4.2.2	Type 2 Driver DC Specifications.....	72
4.2.3	Overshoot/Undershoot Specifications.....	72
4.3	AC Specifications.....	73
4.3.1	Clock Timing Specifications.....	73
4.3.2	PXTAL Clock Input.....	73
4.3.3	PXTAL Clock Oscillator Specifications.....	74
4.3.4	PCI.....	74
4.3.4.1	PCI Electrical Specification Conformance.....	74
4.3.4.2	PCI Clock Signal AC Parameter Measurements.....	74
4.3.4.3	PCI Bus Signals Timing.....	76
4.3.5	Reset.....	77
4.3.5.1	Reset Timings Specification.....	77
4.3.6	IEEE 1149.1.....	78
4.3.6.1	IEEE 1149.1 Timing Specifications.....	79
4.3.7	IX Bus.....	81
4.3.7.1	FCLK Signal AC Parameter Measurements.....	81
4.3.7.2	IX Bus Signals Timing.....	82
4.3.7.3	IX Bus Protocol.....	84
4.3.7.4	RDYBus.....	118
4.3.7.5	TK_IN/TK_OUT.....	120
4.3.8	SRAM Interface.....	121
4.3.8.1	SRAM SCLK Signal AC Parameter Measurements.....	121
4.3.8.2	SRAM Bus Signal Timing.....	122
4.3.8.3	SRAM Bus - SRAM Signal Protocol and Timing.....	124
4.3.8.4	SRAM Bus - BootROM and SlowPort Timings.....	129
4.3.8.5	SRAM Bus - BootRom Signal Protocol and Timing.....	129
4.3.8.6	SRAM Bus - Slow-Port Device Signal Protocol and Timing....	132
4.3.9	SDRAM Interface.....	136
4.3.9.1	SDCLK AC Parameter Measurements.....	136
4.3.9.2	SDRAM Bus Signal Timing.....	137
4.3.9.3	SDRAM Signal Protocol.....	138
4.4	Asynchronous Signal Timing Descriptions.....	143
5.0	Mechanical Specifications.....	144
5.1	Package Dimensions.....	144
5.2	IXP1250 Package Dimensions (mm).....	147

## Figures

1	Silicon Block Diagram.....	9
2	System Block Diagram.....	10
3	SDRAM Unit Block Diagram.....	16
4	SRAM Unit Block Diagram.....	19
5	Reset Logic.....	24

6	Pinout Diagram.....	26
7	64-Bit Bidirectional IX Bus, 1-2 MAC Mode.....	53
8	64-Bit Bidirectional IX Bus, 1-2 MAC Mode, FastPort Device .....	54
9	64-Bit Bidirectional IX Bus, 3+ MAC Mode.....	56
10	32-Bit Unidirectional IX Bus, 1-2 MAC Mode .....	59
11	32-bit Unidirectional IX Bus, 3+ MAC Mode (3-4 MACs Supported).....	61
12	Typical IXP1250 Heatsink Application.....	70
13	PXTAL Clock Input .....	73
14	PCI Clock Signal AC Parameter Measurements .....	74
15	PCI Bus Signals .....	75
16	RESET_IN_L Timing Diagram .....	77
17	IEEE 1149.1/Boundary-Scan General Timing.....	79
18	IEEE 1149.1/Boundary-Scan Tri-State Timing.....	80
19	FCLK Signal AC Parameter Measurements.....	81
20	IX Bus Signals Timing .....	82
21	64-Bit Bidirectional IX Bus Timing, 1-2 MAC Mode, Consecutive Receive and Transmit, No EOP .....	84
22	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, No EOP .....	85
23	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 8th Data Return with Status .....	86
24	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 7th Data Return with Status .....	87
25	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 6th Data Return with Status .....	88
26	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 5th Data Return with Status .....	89
27	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 4th Data Return with Status .....	90
28	64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 1st through 3rd Data Return with Status (3rd Data Return Shown) .....	91
29	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 1st Data Return, No Status.....	92
30	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, No EOP .....	93
31	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 8th Data Return with Status .....	94
32	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 7th Data Return with Status .....	95
33	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 6th Data Return with Status .....	96
34	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP, Two Element Transfer with Status .....	97
35	64-Bit Bidirectional IX Bus Timing - Consecutive Receives, Fetch-9, No EOP... ..	98
36	64-Bit Bidirectional IX Bus Timing - Consecutive Transmits, EOP.....	99
37	64-Bit Bidirectional IX Bus Timing - Consecutive Transmits with Prepend, EOP .....	100
38	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, No EOP.....	101
39	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 16th Data Return with Status .....	102
40	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 15th Data Return with Status .....	103

41	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 14th Data Return with Status .....	104
42	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 1st Through 13th Data Return with Status (13th Data Return Shown) .....	105
43	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP, 64-Bit Status .....	106
44	32-Bit Unidirectional IX Bus Timing - Consecutive Receives, Two Element Transfers with 32-Bit Status .....	107
45	32-Bit Unidirectional IX Bus Timing - Consecutive Transmits, EOP .....	108
46	32-Bit Unidirectional IX Bus Timing - Consecutive Transmits with Prepend, EOP .....	109
47	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP_READY_WAIT=0 .....	110
48	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP_READY_WAIT=5 .....	111
49	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, with Status, FP_READY_WAIT=0 .....	112
50	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP_READY_WAIT=5 .....	113
51	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP_READY_WAIT=0, Cancelled Request .....	114
52	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, No EOP, FP_READY_WAIT=Don't Care .....	115
53	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Different Ports, EOP, No Status, FP_READY_WAIT=0 .....	116
54	64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Different Ports, EOP, No Status, FP_READY_WAIT=0, Cancelled Request .....	117
55	Consecutive Fetch Ready Flags, 1-2 MAC Mode (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=1 .....	118
56	Consecutive Fetch Ready Flags, 3+ MAC Mode (with External Decoder) - RDYBUS_TEMPLATE_CTL[10]=0 .....	118
57	Fetch Ready Flags, Get/Send Commands, 3+ MAC Mode (with External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=0 .....	119
58	Ready Bus Control Timing, Fetch Ready Flags - Flow Control - Fetch Ready Flags, 1-2 MAC Mode (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=1 .....	119
59	Ready Bus Control Timing, Fetch Ready Flags - Flow Control - Fetch Ready Flags, 3+ MAC Mode (with External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=0 .....	120
60	IX Bus Ownership Passing .....	121
61	SRAM SCLK Signal AC Parameter Measurements .....	121
62	SRAM Bus Signal Timing .....	122
63	Pipelined SRAM Read Burst of Eight Longwords .....	124
64	Pipelined SRAM Write Burst of Eight Longwords .....	125
65	Pipelined SRAM Read Burst of Four From Bank 0 Followed by Write Burst of Four From Bank 8 .....	126
66	Pipelined SRAM Longword Write Followed by 2 Longword Burst Read Followed by 4 Longword Burst Write .....	127
67	Flowthrough SRAM Read Burst of Eight Longwords .....	128
68	BootROM Read .....	129
69	BootROM Write .....	130
70	Pipelined SRAM Two Longword Burst Read Followed by BootROM Write .....	131
71	SRAM SlowPort Read .....	132

72	SRAM SlowPort Write .....	133
73	SRAM SlowPort RDY_L .....	134
74	Pipelined SRAM Two Longword Burst Read Followed By SlowPort Write .....	135
75	SDCLK AC Timing Diagram .....	136
76	SDRAM Bus Signal Timing .....	137
77	SDRAM Initialization Sequence .....	140
78	SDRAM Read Cycle .....	141
79	SDRAM Write Cycle .....	142
80	SDRAM Read-Modify-Write Cycle .....	143
81	IXP1250 Part Marking .....	144
82	520-HL-PBGA Package - Bottom View .....	145
83	IXP1250 Side View .....	145
84	IXP1250 A-A Section View .....	146

## Tables

1	64-bit IX Bus Receive Remainder Cycles, No Status Transfer .....	13
2	64-bit IX Bus Receive Remainder Cycles, with Status Transfer .....	13
3	32-bit IX Bus Receive Remainder Cycles, No Status Transfer .....	13
4	32-bit IX Bus Receive Remainder Cycles, with Status Transfer .....	14
5	SDRAM CRC Types .....	17
6	SDRAM Configurations .....	18
7	SRAM Configurations .....	20
8	BootROM x32 Sample Configurations .....	21
9	BootROM x16 Sample Configurations .....	21
10	PCI Configuration Options .....	23
11	Signal Type Abbreviations .....	27
12	Processor Support Pins .....	28
13	SRAM Interface Pins .....	29
14	SDRAM Interface Pins .....	31
15	IX Bus Interface Pins .....	33
16	General Purpose I/Os .....	37
17	Serial Port (UART) Pins .....	37
18	PCI Interface Pins .....	38
19	Power Supply Pins .....	41
20	IEEE 1149.1 Interface Pins .....	42
21	Miscellaneous Test Pins .....	42
22	Pin Usage Summary .....	43
23	Pin Table in Pin Order .....	44
24	Pin Table in Alphabetical Order .....	49
25	64-Bit Bidirectional IX Bus, 1-2 MAC Mode .....	55
26	64-Bit Bidirectional IX Bus, 3+ MAC Mode (Shared IX Bus Operation Only in This Mode) .....	57
27	32-Bit Unidirectional IX Bus, 1-2 MAC Mode .....	60
28	32-bit Unidirectional IX Bus, 3+ MAC Mode .....	62
29	IX Bus Decode Table Listed by Operating Mode Type .....	63
30	Pin State During Reset .....	65
31	Absolute Maximum Ratings .....	68
32	Functional Operating Range .....	69
33	Typical and Maximum Power .....	69

34	Maximum and Typical Bus Loading Used for the Power Calculations .....	70
35	I1, I3, O1, O3, O4, and O5 Pin Types .....	71
36	I2 and O2 Pin Types .....	72
37	Overshoot/Undershoot Specifications .....	72
38	PXTAL Clock Inputs .....	73
39	66 MHz PCI Clock Signal AC Parameters .....	74
40	33 MHz PCI Clock Signal AC Parameters .....	75
40	33 MHz PCI Signal Timing .....	76
41	66 MHz PCI Signal Timing .....	76
42	Reset Timings Specification .....	77
43	IEEE 1149.1/Boundary-Scan Interface Timing .....	80
44	FCLK Signal AC Parameter Measurements .....	81
45	IX Bus Signals Timing .....	82
46	Signal Delay Derating .....	83
47	SRAM SCLK Signal AC Parameter Measurements .....	122
48	SRAM Bus Signal Timing .....	123
49	Signal Delay Deratings for $T_{val}$ and $T_{ctl}$ .....	123
50	SDCLK AC Parameter Measurements .....	136
51	SDRAM Bus Signal Timing Parameters .....	137
52	Signal Delay Deratings for $T_{val}$ and $T_{ctl}$ .....	138
53	IXP1250 Package Dimensions (mm) .....	147

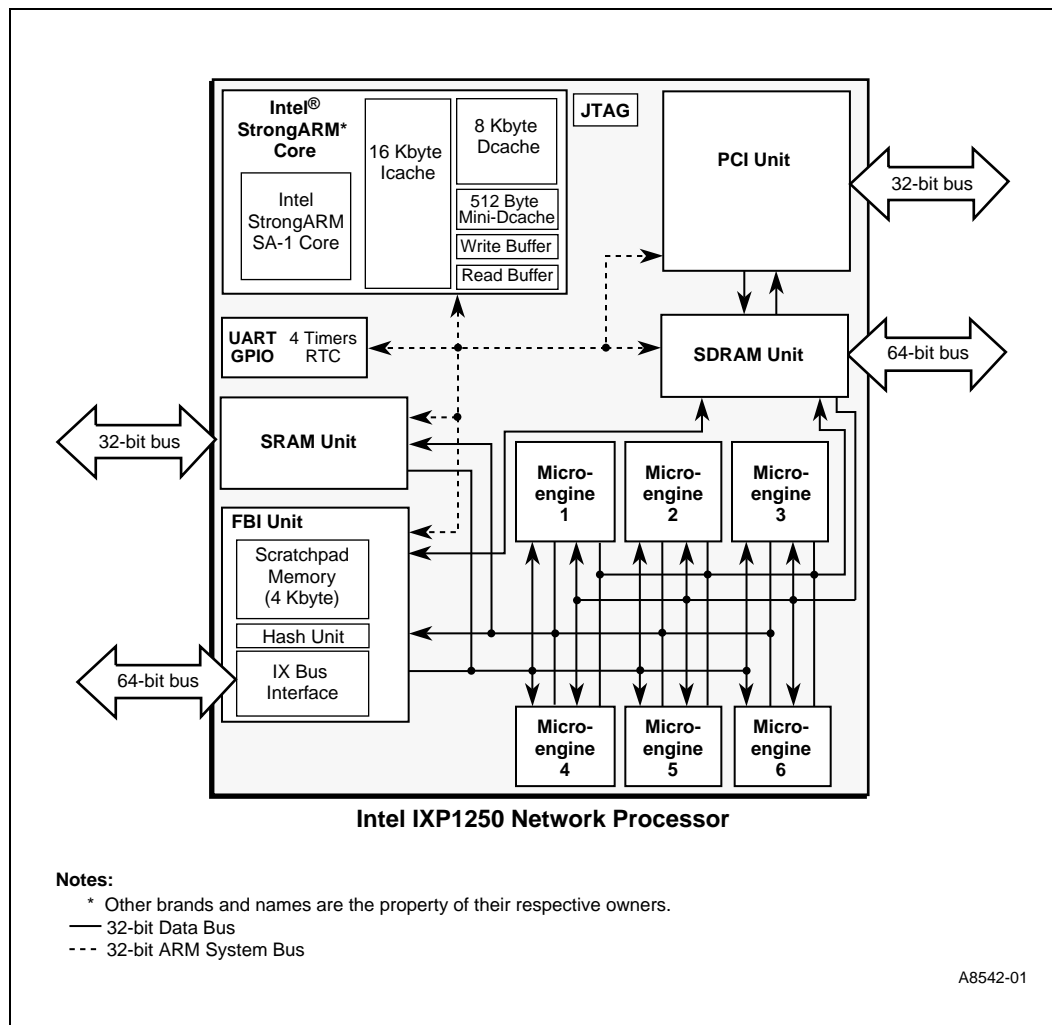


## 1.0 Product Description

The Intel® IXP1250 Network Processor is a highly integrated, hybrid data processor that delivers high-performance parallel processing power and flexibility to a wide variety of networking, communications, and other data-intensive products. The IXP1250 is designed specifically as a data control element for applications that require access to a fast memory subsystem, a fast interface to I/O devices such as network MAC devices, and processing power to perform efficient manipulation on bits, bytes, words, and longword data.

The IXP1250 combines the popular StrongARM® microprocessor with six independent 32-bit RISC data engines with hardware multithread support that combined, provide over 1 giga-operations per second. The Microengines contain the processing power to perform tasks typically reserved for high speed ASICs. In LAN switching applications, the six Microengines are capable of packet forwarding of over 3 million Ethernet packets per second at Layer 3. The StrongARM® processor can then be used for more complex tasks such as address learning, building and maintaining forwarding tables, and network management.

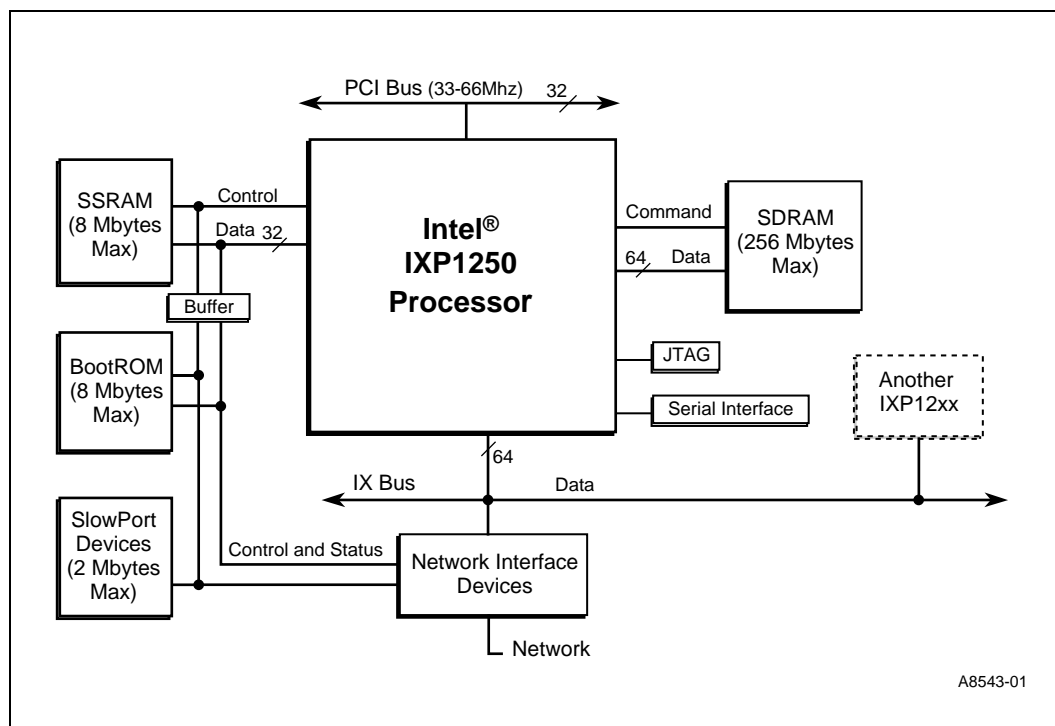
Figure 1. Silicon Block Diagram



As shown in [Figure 2](#),

- The IXP1250 interfaces to a maximum of 256 Mbytes of SDRAM over a 64-bit data bus.
- A separate 32-bit SRAM bus supports up to 8 Mbytes of SSRAM and 8 Mbytes of BootROM. The SRAM Bus also supports memory-mapped I/O devices within a 2 Mbyte memory space.
- A 32-bit PCI interface supports interfacing with industry-standard PCI devices.
- The IX Bus, a flexible 64-bit or dual 32-bit interface, supports attachment of MACs, framers, custom logic devices, and an additional IXP1250.
- An asynchronous serial interface is supported for a debugger console over an RS-232 link.
- An IEEE 1149.1 interface is supported for Boundary Scan testing.

**Figure 2. System Block Diagram**



## 2.0 Functional Units

---

### 2.1 Conventions

- In all signal descriptions, an active low signal is indicated by `_L` in the signal name.
- In this and related IXP1250 documents, a word is equal to 16 bits, a longword is equal to 32 bits, and a quadword is equal to 64 bits. StrongARM® documents and the ARM® V4.0 Architecture Reference typically refer to a word as being equal to 32 bits, and a halfword as being equal to 16 bits.

### 2.2 StrongARM® Core Microprocessor

The StrongARM® core is the same industry standard 32-bit RISC processor as used in the Intel® StrongARM® SA-1100. It is compatible with the StrongARM® processor family currently used in applications such as network computers, PDAs, palmtop computers and portable telephones. The differentiating feature of the StrongARM® processor is that it provides very high performance in a low-power, compact design. This makes it feasible to combine it with a collection of other dedicated execution units on the same silicon die.

The StrongARM® core processor and six RISC Microengines provide the processing power required to forward greater than 3 million Ethernet packets per second through the IXP1250. A multi-IXP1250 system scales linearly so that a system comprised of eight IXP1250s can process over 24 million packets per second.

The designer can partition his/her application by allocating Microengines, threads, and StrongARM® tasks. If necessary, multiple IXP1250 devices can be used to aggregate CPU MIPs, increase data bandwidth, increase port fanout and density, or some combination of all three metrics.

The StrongARM® core operates at a frequency determined by programming the Phase-Locked Loop Configuration register (PLL\_CFG) and the maximum rated operating frequency of the IXP1250 device selected. The IXP1250 is currently available with an  $F_{\text{core}}$  operating frequency of 166, 200, or 232 MHz.

### 2.3 Microengines

Six 32-bit, multithreaded RISC Microengines perform data movement and processing without assistance from the StrongARM® core. Each Microengine has four independent program counters, zero overhead context switching and hardware semaphores from other hardware units to ensure that each Microengine can be fully utilized. A Microengine's powerful ALU and shifter perform both ALU and shift operations in a single cycle. The instruction set was specifically designed for networking and communications applications that require bit, byte, word and longword operations to forward data quickly and efficiently. Each Microengine contains a large amount of local memory and registers: 8 Kbytes organized as 2048 by 32 bits of high-speed RAM Control Store for program execution, 128 32-bit General Purpose Registers, and 128 32-bit transfer registers to service the SRAM and SDRAM Units.

The Microengines operate at the Core clock frequency ( $F_{\text{core}}$ ).

## 2.4 FBI Unit and the IX Bus

The FBI Unit is responsible for servicing fast peripherals, such as MAC-layer devices, on the IX Bus. This includes moving data to and from the IXP1250 Receive and Transmit FIFOs.

The IX Bus provides a 4.4 Gbps interface to peripheral devices. The IX Bus was specifically designed to provide a simple and efficient interface. The IX Bus can be configured as either a 64-bit bidirectional bus or as two 32-bit unidirectional buses. The maximum operating frequency of the IX Bus is 104 MHz.

Two IXP1250 devices can be placed on a single IX Bus in shared IX Bus mode. This option is supported only in 64-bit bidirectional mode.

The FBI Unit contains the Transmit and Receive FIFO elements, control and status registers (CSRs), a 4 Kbyte Scratchpad RAM, and a Hash Unit for generating 48- and 64-bit hash keys. It also contains the drivers and receivers for the IX Bus.

The IX Bus consists of 64 data pins, 23 control pins, and a clock input pin. A sideband bus operating in parallel to the IX Bus, called the Ready Bus, consists of eight additional data pins and five control pins.

The Ready Bus is synchronous to the IX Bus clock, but operation is controlled by a programmable hardware sequencer. Ready Bus cycles are separate and distinct from IX Bus cycles. Up to twelve sequencer commands are loaded at chip initialization time, and run in a continuous loop. The commands can consist of sampling FIFO status for the IX Bus devices, sending Flow Control messages to MAC devices, and reads/writes to other IXP1250 devices as required by the application design. Refer to the *IXP1250 Network Processor Hardware Reference Manual* for specific details on using the Ready Bus.

### 2.4.1 IX Bus Access Behavior

There are two basic modes of IX Bus operation. This is a configuration option only and is not intended to be used “on the fly” to switch between modes.

- **64-Bit Bidirectional Mode**  
The entire 64-bit data path FDAT[63:0] is used for reads or writes to IX Bus devices. The IXP1250 always drives and receives all 64 bits of the IX Bus in this mode. Valid bytes are indicated on the FBE\_L[7:0] signals driven by the IXP1250 during writes and by the IX Bus slave device on reads.
- **32-Bit Unidirectional Mode**  
The IX Bus is split into independent 32-bit transmit and 32-bit receive data paths. Transmit data is driven on FDAT[63:32] and receive data is input on FDAT[31:0]. In this mode, the transmit path is always driven. The receive path is an input during receive cycles and driven by the IXP1250 during device reset cycles or during prolonged idle time on the bus. Valid bytes are identified for the transmit path by the FBE\_L[7:4] signals. Valid bytes are identified for the receive path by the FBE\_L[3:0] signals.

Each basic mode has two additional modes depending on the number of IX Bus devices and ports being used: 1-2 MAC mode for one or two slave devices, and 3+ MAC mode when using three to seven slave devices. Bus timing and the functions of the IX Bus signals are slightly different in each mode. These functional definitions per IX Bus mode are listed in [Section 3.6](#) and [Section 3.7](#).

In addition, a shared IX Bus mode is supported in 64-bit bidirectional mode. Refer to the list at the bottom of [Table 26](#) for the signals that the IX Bus masters must drive and IX Bus slaves must tri-state.

The IX Bus and Intel devices using the IX Bus, such as the IXF440 and IXF1002, observe a pipelined bus protocol. When receive transfers are terminated early, the pipeline continues to cause several extra bus cycles depending on when the EOP signal was asserted. Data is a “don’t care” for these trailing bus cycles, except in the case of a status transfer where the IX Bus burst includes a possible status transfer if the device were programmed to support it. Slave devices must drive valid logic levels on the FDAT data pins during these cycles.

The tables below show the number of total IX Bus data cycles that will occur for a burst with EOP asserted at specific clocks for 64-bit and 32-bit IX Bus modes. In each case, the tables show IX Bus cycles with and without the optional status transfer cycle. Refer to the IX Bus Protocol Timing diagrams ([Figure 21](#) through [Figure 54](#)) when interpreting these tables.

**Table 1. 64-bit IX Bus Receive Remainder Cycles, No Status Transfer**

EOP signaled on this cycle:	1	2	3	4	5	6	7	8
Number of bus cycles in burst:	5	6	7	8	8	8	8	8
Number of Don't Care cycles:	4	4	4	4	3	2	1	0

**Table 2. 64-bit IX Bus Receive Remainder Cycles, with Status Transfer**

EOP signaled on this cycle:	1	2	3	4	5	6	7	8
Number of bus cycles in burst:	5	6	7	8	8	8	8	8
Status transfer	1	1	1	1	1	1	1	Note 1
Number of Don't Care cycles:	3	3	3	3	2	1	0	0

**NOTE:**

1. Status transfer occurs on a subsequent IX Bus status cycle.

**Table 3. 32-bit IX Bus Receive Remainder Cycles, No Status Transfer**

EOP signaled on this cycle:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Number of bus cycles in burst:	5	6	7	8	9	10	11	12	13	14	15	16	16	16	16	16
Number of Don't Care cycles:	4	4	4	4	4	4	4	4	4	4	4	4	3	2	1	0

**Table 4. 32-bit IX Bus Receive Remainder Cycles, with Status Transfer**

EOP signaled on this cycle:		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Number of bus cycles in burst:		5	6	7	8	9	10	11	12	13	14	15	16	16	16	16	16
Status transfer	32-bit status	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	N o t e 1
	64-bit status	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
Number of Don't Care cycles:		3	3	3	3	3	3	3	3	3	3	3	3	2	1	0	0

**NOTE:**

- Status transfer occurs on one or two subsequent IX Bus cycles.

In both 32-bit and 64-bit modes, all of the associated FBE\_L signals (FBE\_L[7:4] in 32-bit mode and FBE\_L[7:0] for 64-bit mode) are driven low on a transmit. The last bus transfer, identified by the assertion of EOP in 64-bit mode or by EOP32 in 32-bit mode, indicates the number of valid bytes of this last transfer by driving only the valid FBE\_L signals.

Similarly for receive cycles, in both 32-bit and 64-bit modes, all associated FBE\_L signals must be driven low by the peripheral or MAC device. The FBE\_L signals must identify the number of valid bytes on the last transfer driven with EOP. The IXP1250 uses this information to update the RCV\_CTL register's Valid Bytes field. Driving fewer than the four or eight FBE\_Ls, except for the last transfer with EOP, may cause undefined behavior.

### 2.4.1.1 Reset and Idle Bus Considerations

While the IXP1250 is in reset, or when the IX Bus is idle for at least 4 FCLK cycles and no IX Bus requests are pending, the IXP1250 drives the pins listed below. This is done so that the bus is not left in a high-Z state for a prolonged period of time. This allows the designer to avoid the use of keeper resistors on the pins to maintain valid levels.

FDAT[63:0]  
 FBE\_L[7:0]  
 FPS[2:0]  
 TXAXIS  
 RDYBUS[7:0]  
 RDYCTL\_L[3:0]  
 RDYCTL\_L[4]  
 EOP  
 SOP  
 EOP32  
 SOP32  
 RXFAIL

In shared IX Bus mode, pullups should be used on PORTCTL\_L[3:0], FPS[2:0], and TXAXIS to maintain valid logic levels during bus exchanges.

In configurations where two IXP1250s are in Shared IX Bus Mode, the IXP1250s must be reset synchronously, preferably with the same signal driving RESET\_IN\_L. During reset, the IXP1250s drive the pins listed above to identical logic states thereby avoiding logic state contention. If the

two devices are not reset synchronously, bus contention could result if one of the devices is held in reset while the alternate device assumes the role of initial IX Bus owner and begins driving transactions. This would result in obvious bus malfunction, and over time could affect device reliability due to resulting high current conditions in the device.

## 2.5 SDRAM and SRAM Units

The IXP1250 supports two high performance memory units. The SRAM Unit provides fast memory that can be used to store look-up tables. The SDRAM Unit provides lower cost memory for forwarding information and transmit queues. Both units contain features that improve memory bandwidth utilization.

### 2.5.1 SDRAM Unit

The IXP1250 provides an SDRAM Unit to access low cost, high bandwidth memory for mass data storage. The StrongARM\* core address space allows up to 256 Mbytes of SDRAM to be addressed. The SDRAM interface operates at half the Core frequency ( $0.5 * F_{core}$ ), providing a peak bandwidth of 800 Mbytes per second at 232 MHz.

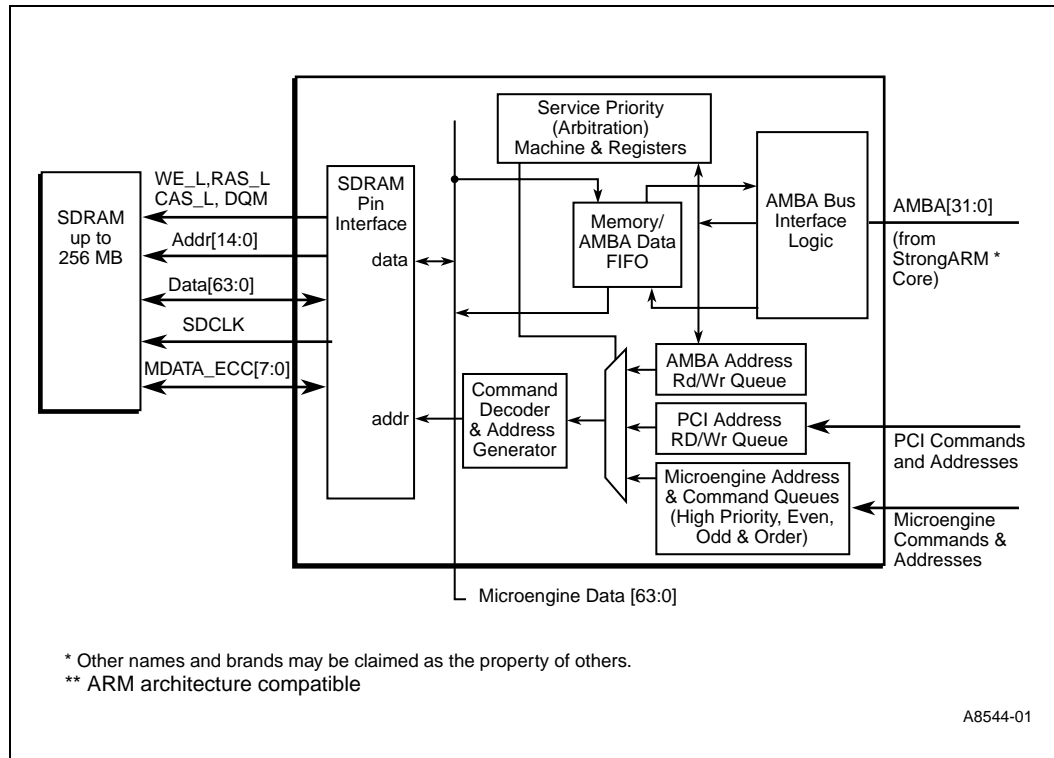
Bus cycles are generated by requests from the PCI Unit including PCI DMA cycles, the StrongARM\* core, and the Microengines.

The SDRAM is operated by commands that are loaded into command queues within the unit. The SDRAM Unit decodes the command, reads or writes the data, then deletes the command from the head of the queue. The read and write sources may be SDRAM memory locations, transfer registers, or the Transmit and Receive FIFOs in the FBI Unit. Refer to the *IXP1200 Network Processor Family Hardware Reference Manual* for details on how these requests are queued, prioritized, and serviced by the SDRAM Unit.

SDRAM should have an access time ( $t_{ac}$ ) of 6 ns or less (CAS latency = 2), PC100 compatible.

Figure 3 details the major components of the SDRAM Unit.

**Figure 3. SDRAM Unit Block Diagram**



The SDRAM Bus consists of 15 row/column address bits, 64 data bits, RAS\_L, CAS\_L, write enable, DQM control, and a synchronous output clock running at one-half the IXP1250 Core frequency ( $0.5 * F_{core}$ ).

The PCI, Microengines, and StrongARM\* core require single byte, word, and longword write capabilities. The SDRAM Unit supports this using a read-modify-write technique. As data is written from the PCI or StrongARM\* core to SDRAM, a quadword is read from SDRAM. The IXP1250 then updates only the bytes that were enabled and writes the entire quadword of data back to SDRAM memory. (Note that the bytes do not have to be consecutive.) These three steps are performed automatically.

## 2.5.2 SDRAM Bus Access Behavior

- The number of quadwords transferred by the SDRAM Unit is determined by the requesting interface (StrongARM\* core, Microengine, or PCI). The SDRAM Unit may reorder SDRAM accesses for best performance.
- Accesses are always quadword (64-bit) cycles on the SDRAM Bus.
- Accesses from the StrongARM\* core.
  - Byte, word, and longword accesses generated from the StrongARM\* core result in Read-Modify-Write cycles to SDRAM space.
  - Consecutive longword writes over the AMBA Bus to the same quadword address are buffered and aggregated into quadword writes to SDRAM.



- Read accesses using the Prefetch Memory address space allow the SDRAM Unit to prefetch quadword data to be supplied to the AMBA Bus using 32-bit burst cycles.
- Accesses from the Microengines.
  - The **sdram** microinstruction defines the number of 64-bit accesses to make, with up to 16 quadwords with one instruction.
  - Only quadword accesses are supported. Less than 8 bytes can be written when using the byte mask within an instruction, but result in Read-Modify-Write cycles.

### 2.5.3 SDRAM Cyclic Redundancy Checking (CRC)

SDRAM Cyclic Redundancy Checking (CRC) is used to protect blocks of data called Frames. Using this technique, the transmitter appends an extra n-bit sequence (called a Frame Check Sequence or FCS) to every frame. The FCS holds redundant information about the frame that helps the transmitter detect errors in the frame.

The CRC is one of the most used techniques for error detection in data communications. The technique combines three advantages:

- Extreme error detection capabilities
- Minimal overhead
- Ease of implementation

All CRC processing and checking is performed in software (microcode) and is only accessible from microcode instructions.

The CRC types supported are described in [Table 5](#).

**Table 5. SDRAM CRC Types**

CRC Type	Polynomial	Application	Bit Order
CRC-32	$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$	ATM AAL5 Ethernet	MSB first LSB first
CRC-16	$X^{16} + X^{12} + X^5 + 1$	HDLC Frame Relay	LSB first LSB first
CRC-10	$X^{10} + X^9 + X^5 + X^4 + X + 1$	ATM OAM	MSB first, LW (or LW +1)

### 2.5.4 SDRAM Error Correction Code (ECC)

SDRAM Error Correction Code (ECC) allows data that is being read or transmitted to the SDRAM to be checked for errors and, when necessary, corrected “on the fly.” It differs from standard parity-checking because errors are not only detected but also corrected.

When a unit of data (or “word”) is stored in SDRAM, a code that describes the bit sequence in the word is calculated and stored along with that unit of data. For each 64-bit word, an extra 8 bits are needed to store this code.

When the unit of data is requested for reading, a code for the stored and about-to-be-read word is again calculated using the original algorithm. The newly generated code is compared with the code generated when the word was stored.

If the codes match, the data is free of errors and is sent.

If the codes don't match, the missing or erroneous bits are determined through the code comparison and the bit or bits are supplied or corrected.

ECC only corrects single bit errors. Multiple bit errors are detected, but not corrected.

No hardware attempt is made to correct the data that is still in storage. Eventually, it will be overlaid by new data and, assuming the errors were transient, the incorrect bits will "go away."

There are no timing penalties associated with ECC operation.

## 2.5.5 SDRAM Configurations

**Table 6. SDRAM Configurations**

Total Memory	Number of Chips	Size DRAM	Configuration (per bank)	Internal Banks	Bank Bits	RAS Bits	CAS Bits
8 Mbytes	4	16 Mbit	512 K x 16-bit	2	1	11	8
16 Mbytes	8	16 Mbit	1 M x 8-bit	2	1	11	9
32 Mbytes	4	64 Mbit	2 M x 16-bit	2	1	13	8
64 Mbytes	8	64 Mbit	4 M x 8-bit	2	1	13	9
32 Mbytes	4	64 Mbit	1 M x 16-bit	4	2	12	8
64 Mbytes	8	64 Mbit	2 M x 8-bit	4	2	12	9
64 Mbytes	4	128 Mbit	2 M x 16-bit	4	2	12	9
128 Mbytes	8	128 Mbit	4 M x 8-bit	4	2	12	10
128 Mbytes	4	256 Mbit	4 M x 16-bit	4	2	13	9
256 Mbytes	8	256 Mbit	8 M x 8-bit	4	2	13	10

## 2.5.6 SRAM Unit

The IXP1250 provides an SRAM Unit for very high bandwidth memory for storage of lookup tables and other data for the packet processing Microengines. The SRAM Unit controls the SRAM (up to 8 Mbytes), BootROM (up to 8 Mbytes) for booting, and 2 Mbytes of SlowPort address space for peripheral device access. The I/O signal timing is determined by internal address decodes and configuration registers for the BootROM and SlowPort address regions. The SRAM Unit includes an 8 entry Push/Pop register list for fast queue operations, bit test, set and clear instructions for atomic bit operations, and an 8 entry CAM for Read Locks.

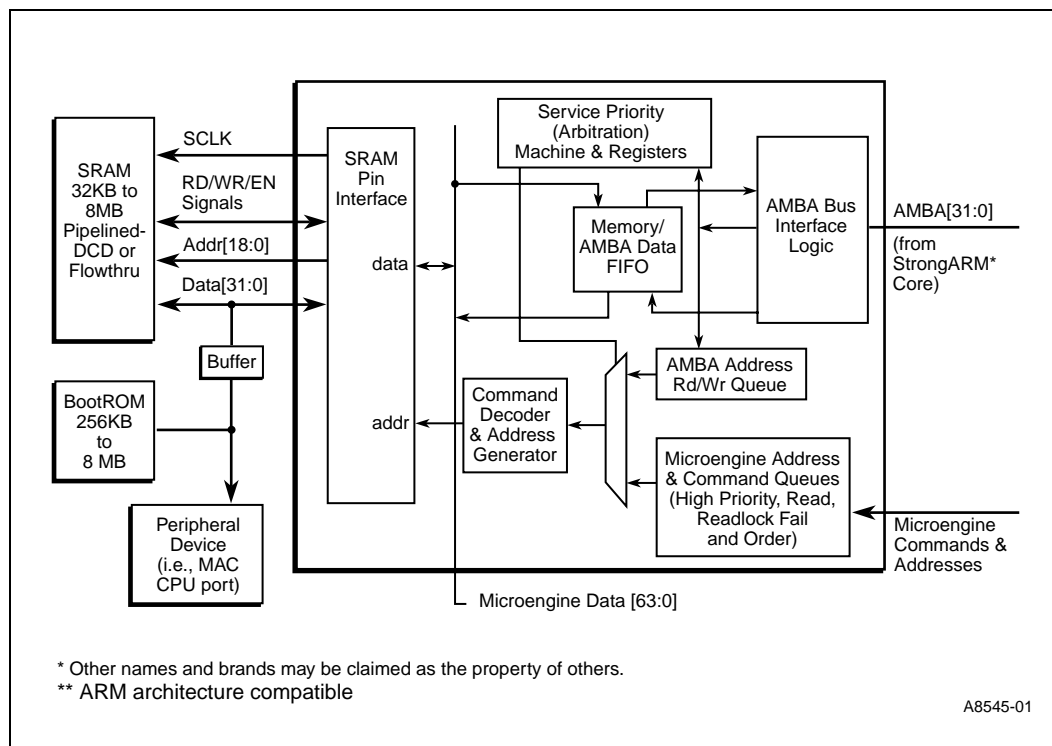
The SRAM interface operates at one-half the IXP1250 Core frequency ( $0.5 * F_{core}$ ).

The SRAM Unit supports both Pipelined Burst Double Cycle Deselect (DCD) and Flowthru SRAM types. Other SSRAM devices, including single cycle deselect, are not supported. The bus is also used to attach BootROM and can be used to interface other peripheral devices such as custom interface logic or MAC management ports. The SRAM interface provides three separate timing domains for the three device types: SRAM, BootROM, and Peripheral (also referred to as SlowPort access).

BootROM devices may be either 32 bits or 16 bits in width. This is determined by GPIO[3] during reset. When 16-bit BootROM devices are used, the maximum BootROM address space is reduced from 8 Mbytes to 4 Mbytes.

Figure 4 details the major components of the SRAM Unit.

Figure 4. SRAM Unit Block Diagram



The SRAM Bus consists of 19 address bits, 32 data bits, 4 chip enable bits, 8 buffer and read/write control signals, a synchronous output clock (SCLK) running at one-half the IXP1250 Core frequency, and a synchronous input clock (NA/SACLK). When using Flowthru SRAM types, it is recommended to route the SCLK signal from the SRAMs back to the NA/SACLK input. Routing this trace identically to the DQ data signals will skew the NA/SACLK slightly to track the return data trace propagation delay. When using Pipelined/DCD SRAMs, the NA/SACLK input is not used and may be held inactive with a pulldown to GND to save power.

The SRAM Unit receives memory requests from seven sources: the StrongARM\* core and each of the six Microengines. Refer to the IXP1250 Hardware Reference Manual for details on the prioritization and queues provided for servicing these requests.

The IXP1250 supports the use of an optional asynchronous ready input for flexibility in interfacing memory-mapped I/O devices to the SRAM Slowport region. This will allow the I/O device to add wait-states to IXP1250 I/O accesses. This function is supported on the HIGH\_EN\_L pin. An I/O device must drive HIGH\_EN\_L with a wired-OR open drain buffer configuration, and only drive the pin when the I/O device is selected.

To use the RDY\_L pin function, it must be enabled by setting SRAM\_CSR[19]=1. The RDY\_L Pause State Value field located in register SRAM\_SLOW\_CONFIG[23:16] must be programmed with the state value at which you choose to pause the internal wait-state logic. This pause state relates to the other timing parameters programmed into the SRAM\_SLOW\_CONFIG and

SRAM\_SLOWPORT\_CONFIG register fields. See [Figure 73](#) which illustrates this example. The SCC value is the total number of Core clocks for the I/O cycle, and the SRWA, SCEA, SRWD, and SCED values specify the RD/WR and Chip Enable signal assert and deassert times. When the I/O cycles begins, the SCC value is loaded into the internal state counter and is decremented on each Core clock tick (twice the SCLK frequency). When the state counter reaches the RDY\_L Pause State Value, it will remain in that state until the HIGH\_EN\_L pin is sampled LOW, allowing the state counter to resume its decrement operation. The HIGH\_EN\_L must be driven for at least two SCLK periods to be sampled properly by the IXP1250.

The RDY\_L Pause State must also occur at a minimum of 5 Core clock periods prior to the SRWD state to be recognized. A RDY\_L Pause State value of SRWD+5 (Decimal 10, Hexidecimal A) is used in this example.

In this example, 6 additional Core clock “wait-states” are inserted. If the RDY\_L input is synchronous to SCLK and it meets the specified setup and hold times, the resulting number of wait states will be predictable. However, if the RDY\_L input is asynchronous to SCLK, the number of wait-states the IXP1250 inserts could vary by +/- 2 Core clock periods.

### 2.5.6.1 SRAM Types Supported

Pipeline Burst DCD (double cycle deselect) type: tKQmax=4.2 ns, 3.3 V.

Flowthru type: tKQmax= 9 ns, 3.3 V.

*Note:* Other SSRAM devices, including single cycle deselect, are not supported.

### 2.5.6.2 SRAM Configurations

**Table 7. SRAM Configurations**

Total Memory	Number of Chips (Maximum of 8)	Size of SRAM	Device Organization
1 Mbytes	8	1 Mbit	32 K x 32-bit
2 Mbytes	8	2 Mbit	64 K x 32-bit
2 Mbytes	8	2 Mbit	128 K x 16-bit
4 Mbytes	8	4 Mbit	128 K x 32-bit
4 Mbytes	8	4 Mbit	256 K x 16-bit
8 Mbytes (maximum)	8	8 Mbit	256 K x 32-bit

### 2.5.6.3 BootROM Configurations

**Table 8. BootROM x32 Sample Configurations**

Total Memory	Number of Chips (Maximum of 8)	Size of Boot ROM	Device Organization
512 Kbytes	2	2 Mbit	128 K x 16-bit
2 Mbytes	8	2 Mbit	128 K x 16-bit
4 Mbytes	8	4 Mbit	256 K x 16-bit
6 Mbytes	6	8 Mbit	512 K x 16-bit
8 Mbytes	8	8 Mbit	512 K x 16-bit

**Table 9. BootROM x16 Sample Configurations**

Total Memory	Number of Chips (Maximum of 8)	Size of Boot ROM	Device Organization
256 Kbytes	1	2 Mbit	128 K x 16-bit
512 Kbytes - 4 Mbytes	2 - 8	2 Mbit	128 K x 16-bit
512 Kbytes	1	4 Mbit	256 K x 16-bit
1 Mbytes - 4 Mbytes	2 - 8	4 Mbit	256 K x 16-bit
1 Mbytes	1	8 Mbit	512 K x 16-bit
2Mbytes - 4 Mbytes	2 - 4	8 Mbit	512 K x 16-bit

### 2.5.6.4 SRAM Bus Access Behavior

- The SRAM controller within the IXP1250 will never initiate automatic bursting. Bursting is controlled by the requestor (StrongARM\* core or Microengine) depending on the type and number of SRAM accesses needed.
- Accesses are always longword 32-bit cycles on the SRAM Bus.
- The IXP1250 always drives the address for each data cycle. No external address generation or address advance control to SRAM devices is required.
- Accesses from the StrongARM\* core:
  - Byte, word, and longword accesses generated from the StrongARM\* core are supported.
  - Bit operations are supported via StrongARM\* core accesses to the SRAM Alias Address Space to perform the same operations as a Microengine can accomplish implicitly in a microinstruction (Push, Pop, Bit Test and Set, CAM operations, Lock/Unlock, etc.).
  - Bit, byte, and word writes result in Read-Modify-Write cycles.
  - Declare memory-mapped I/O as non-cacheable to prevent line fill burst cycles, and disable caching and write buffering to ensure I/O device coherency.
  - For best performance, use longword accesses to avoid Read-Modify-Write cycles on the SRAM Bus that occur with byte and word accesses.
- Accesses from the Microengines:

- The **sram** microinstruction defines the number of 32-bit accesses to make, up to 8 longwords with one Microengine command.
- Only bit and longword accesses are supported.
- Bit write accesses result in Read-Modify-Write cycles.
- Unlike the StrongARM\* core, the Microengine microinstruction allows you to perform bit operations within the instruction (Push, Pop, Bit Test and Set, CAM operations, Lock/Unlock, etc.).

## 2.6 PCI Unit

The PCI Unit provides an industry standard 32-bit PCI Bus to interface to PCI peripheral devices such as host processors and MAC devices. The PCI Unit supports operating speeds from DC up to 66 MHz, and supports *PCI Local Bus Specification, Revision 2.2*. This unit contains:

- Arbitration logic to support up to three PCI Bus masters,
- PCI Intelligent I/O (I<sub>2</sub>O),
- Two DMA channels, and
- Four 24-bit timers.

Refer to the *IXP1200 Network Processor Family Hardware Reference Manual* for details on PCI Bus behavior for Target (Slave) and Initiator (Master) modes, configuration and register definitions.

The PCI interface is specified to operate from DC up to 66 MHz. Above 33 MHz operation, two PCI devices are supported only, the IXP1250 and a second PCI device. To increase the number of PCI devices supported or to add connectors to the bus at the higher PCI Bus speeds, a PCI-to-PCI bridge device, such the Intel 21150, 21152, or 21153 is required.

Both PCI Initiator and Target cycles are supported. As a target device, the IXP1250 responds as a Medium Speed device asserting DEVSEL\_L two PCI\_CLK cycles after FRAME\_L is asserted.

### 2.6.1 PCI Arbitration and Central Function Support

The IXP1250 contains an optional arbiter to support up to three PCI Bus masters. This includes the IXP1250 plus two external PCI Bus master devices. The external masters are supported by two request signals, REQ\_L[1:0], and two grant signals GNT\_L[1:0].

The IXP1250 can also provide PCI Central Function support. In this configuration, the IXP1250:

- Drives the PCI Reset signal, PCI\_RST\_L, as an output,
- Monitors the PCI System Error input signal, SERR\_L, and
- Provides Bus Parking where the IXP1250 is the default PCI Bus master, and it drives valid logic levels on the PCI A/D, C/BE, and PAR pins during reset and idle PCI Bus conditions.

Two configuration pins, PCI\_CFN[1:0], are sampled at the rising edge of RESET\_IN\_L to determine the PCI configuration (see [Table 10](#))

**Table 10. PCI Configuration Options**

PCI_CFN[1:0]	PCI FUNCTION
00	Central Function and Arbitration disabled.
10	Reserved for future use.
01	Reserved for future use.
11	Central Function and Arbitration enabled.

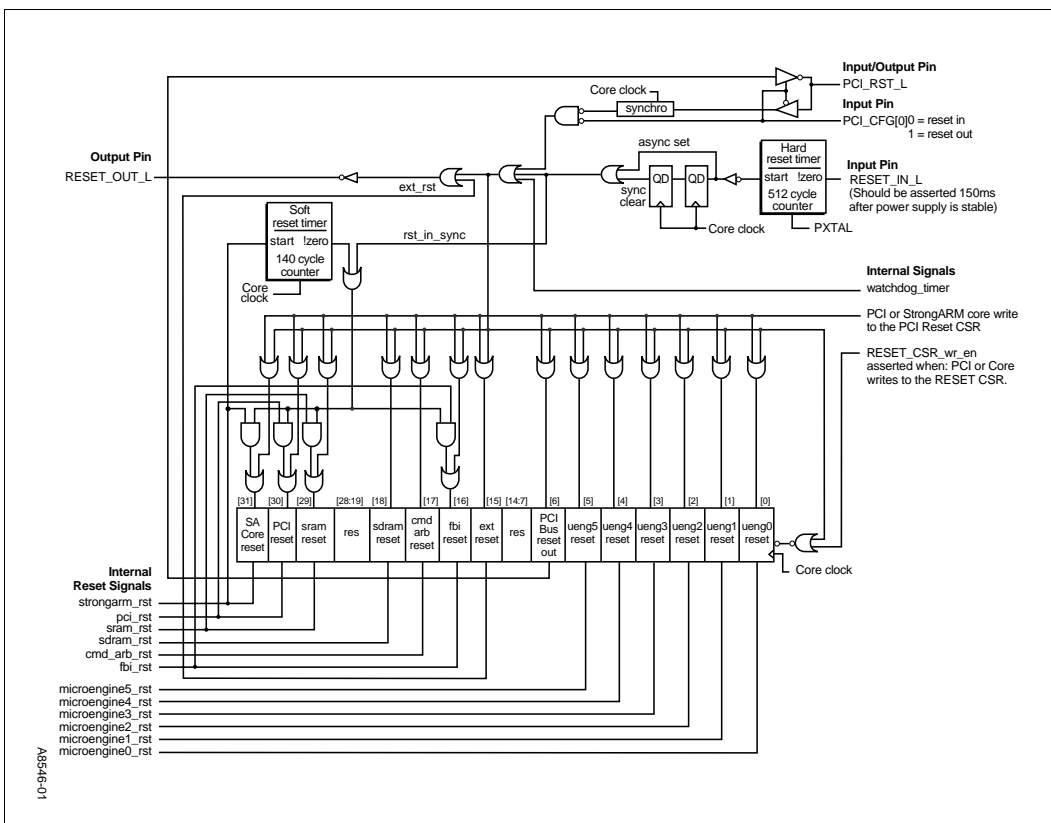
## 2.7 Device Reset

The IXP1250 can be reset by the following:

- Hardware Reset via RESET\_IN\_L pin
- Software Reset by StrongARM\* core or by PCI device write to the IXP1250\_RESET register
- PCI Reset via the PCI\_RST\_L pin
- Watchdog Timer expiration

Figure 5 illustrates details of the internal reset function logic.

Figure 5. Reset Logic



A8546-01



### 2.7.1 Hardware Initiated Reset

The IXP1250 provides the RESET\_IN\_L pin so that an external device can reset the IXP1250. Asserting this pin resets the internal functions and generates an external reset via the RESET\_OUT\_L pin.

Upon power-up, RESET\_IN\_L must remain asserted for 150 ms after VDD and VDDX are stable to properly reset the IXP1250 and ensure that the PXTAL clock input and PLL Clock generator are stable.

While RESET\_IN\_L is asserted, the processor is held reset. When RESET\_IN\_L is released, the StrongARM® processor begins execution from SRAM address 0 after 512 PXTAL cycles. If RESET\_IN\_L is asserted while the StrongARM® core is executing, the current instruction terminated abnormally and the on-chip caches, MMU, and write buffer are disabled.

The RESET\_OUT\_L signal remains asserted until deasserted by the StrongARM® core. The StrongARM® core deasserts the signal by writing bit 15 of the IXP1250\_RESET register.

### 2.7.2 Software Initiated Reset

The StrongARM® core or an external PCI Bus master can reset specific functions in the IXP1250 by writing to the IXP1250\_RESET register. In most cases, only the individual Microengines are reset and the external RESET\_OUT\_L pin will be asserted via this register. The ability to reset the other functions is provided for debugging. The SRAM Unit is always reset when the StrongARM® Core is reset. To ensure a proper reset, the StrongARM® core and the SRAM Unit are held in reset for 140 system clock cycles after RESET\_IN\_L is deasserted. The other functions that can be reset via the IXP1250\_RESET register are properly reset when consecutive writes are performed to assert and deassert the reset.

### 2.7.3 PCI Initiated Reset

The IXP1250 can be reset by an external PCI Bus master when the IXP1250 is not the PCI Central Function and arbiter device (PCI\_CFG[1:0] = 00) and PCI\_RST\_L is an input. The entire IXP1250 is reset during a PCI Initiated Reset. When the IXP1250 is assigned as the PCI Central Function and arbiter device (PCI\_CFG[1:0] = 11), the IXP1250 drives PCI\_RST\_L as an output to the other devices on the PCI Bus.

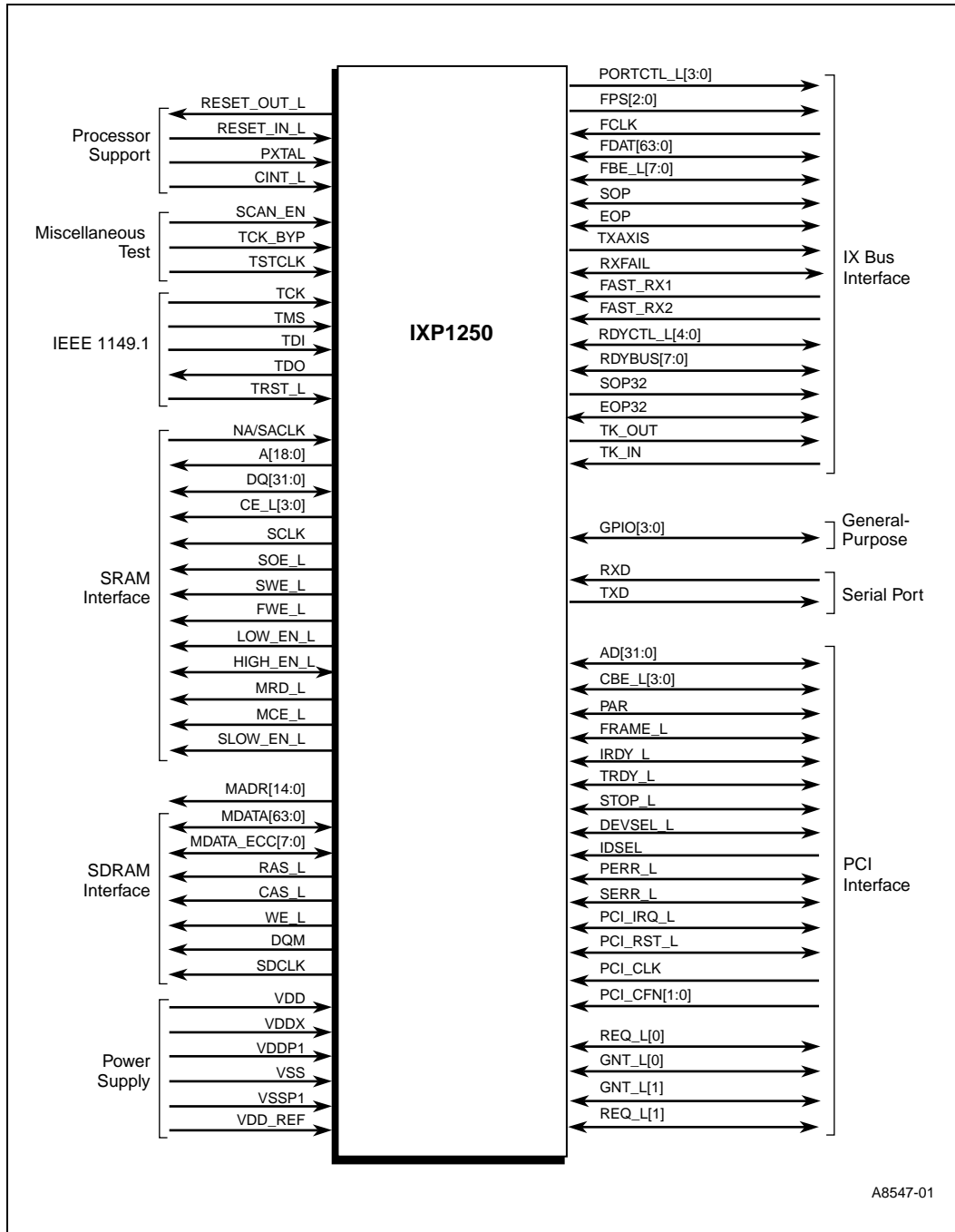
### 2.7.4 Watchdog Timer Initiated Reset

The IXP1250 provides a watchdog timer that can reset the StrongARM® core. The StrongARM® core should be programmed to reset the watchdog timer periodically to ensure that the timer does not expire. If the watchdog timer expires, it is assumed the StrongARM® core has ceased executing instructions properly. The reset generated by the Watchdog Timer will reset each of the functions in the IXP1250.

### 3.0 Signal Description

#### 3.1 Pinout Diagram

Figure 6. Pinout Diagram



A8547-01

## 3.2 Pin Type Legend

The IXP1250 signals are categorized into one of several groups: Processor Support, Miscellaneous/Test, IEEE 1149.1, SRAM Interface, SDRAM Interface, IX Bus Interface, General Purpose, Serial Port, and PCI Interface.

Table 11 defines the signal type abbreviations used in the Pin Description section.

**Table 11. Signal Type Abbreviations**

Signal Type	Description
I	Standard input only. There are three types of inputs (I1,I2, and I3) for the IXP1250. Refer to <a href="#">Table 35</a> and <a href="#">Table 36</a> for more information.
O	Standard output only. There are 5 types of outputs (O1,O2,O3,O4, O5) for the IXP1250. Refer to <a href="#">Table 35</a> and <a href="#">Table 36</a> for more information.
TS	Tri-state output.
STS	Sustained tri-state. Active low signal owned and driven by one and only one agent at a time. The agent that drives this pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving this signal any sooner than one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it, and it must be provided by the central resource (that is, on a PC board).
P	Power supply.
OD	Standard open drain allows multiple devices to share as a wire-OR. A pullup is required to sustain the inactive state until another agent drives it, and it must be provided by the central resource.

### 3.3 Pin Description, Grouped by Function

#### 3.3.1 Processor Support Pins

Table 12. Processor Support Pins

Processor Support Signal Names	Pin Number	Type	Total	Pin Descriptions
PXTAL	E7	I1	1	Input connection for system oscillator. Typically 3.6864 MHz. Drives internal PLL clock generator.
CINT_L	AA30	I1	1	Level-sensitive interrupt input to the StrongARM* core.
RESET_OUT_L	E8	O4	1	IXP1250 System Reset Output. Asserted when: <ul style="list-style-type: none"> <li>• RESET_IN_L is asserted.</li> <li>• PCI Central Function and arbiter disabled (PCI_CFN[1:0]=00) and PCI_RST_L is asserted.</li> <li>• A soft reset is initiated.</li> <li>• The Watchdog Timer expires.</li> </ul> To deassert, write register IXP1250_RESET bit 15.
RESET_IN_L	D8	I1	1	IXP1250 System Reset Input. If asserted, the IXP1250 will reset and will assert RESET_OUT_L. If PCI Central Function and arbiter enabled (PCI_CFN[1:0]=11), PCI_RST_L output will also be asserted.
Totals:			4	

### 3.3.2 SRAM Interface Pins

**Table 13. SRAM Interface Pins**

SRAM Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
A[18:0]	[18] E25 [17] C26 [16] A27 [15] E30 [14] F28 [13] E31 [12] F29 [11] G27 [10] F30 [9] G28 [8] G29 [7] G30 [6] H27 [5] G31 [4] H28 [3] H29 [2] H30 [1] J27 [0] H31	O4	19	Address outputs
DQ[31:0]	[31] J29 [30] J31 [29] K28 [28] K29 [27] K31 [26] L28 [25] L29 [24] L30 [23] M27 [22] M28 [21] M29 [20] M30 [19] M31 [18] N27 [17] N28 [16] N29 [15] N30 [14] N31 [13] P27 [12] P28 [11] P29 [10] P30 [9] P31 [8] R27 [7] R28 [6] R29 [5] R30 [4] U31 [3] V30 [2] V29 [1] V28 [0] V27		32	32 Bidirectional data signals

Table 13. SRAM Interface Pins (Continued)

SRAM Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
CE_L[3:0] [3] [2] [1] [0]	D24 A25 E24 B25	O4	4	SRAM Bus chip enable outputs. Internally decoded from SRAM address. Valid during SRAM and BootROM accesses.
SCLK	W30	O3	1	SRAM clock output - Frequency is one half the speed of the Core clock ( $\frac{1}{2} * F_{core}$ ).
SOE_L	W29	O4	1	SRAM output enable.
SWE_L	Y31	O4	1	SRAM write enable.
LOW_EN_L	D25	O4	1	Low order SRAM bank enable and buffer direction select for slow interface.
HIGH_EN_L	B26	I1/O4	1	High-order SRAM bank enable output and Flash PROM/BootROM read enable or asynchronous Ready input from I/O devices. The pin function is determined by programming SRAM_CSR[19] = 1, which enables RDY_L or SRAM_CSR[19] = 0, which enables the HIGH_EN_L function.
SLOW_EN_L	Y29	O4	1	Slow device enable: 0 = Slow device (BootROM or SlowPort), 1=SRAM.
NA/SACLK	B23	I1	1	SRAM clock input, used to compensate for skew in data path when using Flowthru SRAMs. Must be connected to SCLK output when using Flowthru devices. Not used with Pipelined devices and should be pulled low.
FWE_L	Y30	O4	1	Asynchronous interface write enable (BootROM or MAC devices).
MRD_L	W27	O4	1	Slow asynchronous interface read enable output.
MCE_L	W28	O4	1	Slow asynchronous interface chip enable output.
Totals:			65	

### 3.3.3 SDRAM Interface Pins

**Table 14. SDRAM Interface Pins**

SDRAM Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
MADR[14:0] [14] [13] [12] [11] [10] [9] [8] [7] [6] [5] [4] [3] [2] [1] [0]	AK7 AC3 AC2 AB5 AC1 AB4 AB3 AB1 AA4 AA3 Y4 Y3 Y2 Y1 W5	O4	15	Multiplexed Row/Column address outputs.
MDATA[63:0] [63] [62] [61] [60] [59] [58] [57] [56] [55] [54] [53] [52] [51] [50] [49] [48] [47] [46] [45] [44] [43] [42] [41] [40] [39] [38] [37] [36] [35] [34] [33] [32] [31] [30] [29] [28] [27] [26]	AH7 AK6 AG7 AJ6 AL5 AG2 AF4 AG1 AF3 AE5 AF2 AE4 AE3 AE2 AD5 AE1 AD4 AD3 V4 V3 R3 R4 R5 P1 P2 P3 P4 P5 N1 N2 N3 N4 N5 M1 M2 M3 M4 M5	I1/O1	64	64 Bidirectional data signals.

Table 14. SDRAM Interface Pins (Continued)

SDRAM Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
[25] [24] [23] [22] [21] [20] [19] [18] [17] [16] [15] [14] [13] [12] [11] [10] [9] [8] [7] [6] [5] [4] [3] [2] [1] [0]	L2 L3 L4 K2 K3 K5 J2 J3 J4 H1 H5 H2 H3 H4 G1 H5 G2 G3 G4 F2 G5 F3 E1 F4 E2 F5			
MDATA_ECC [7:0] [7] [6] [5] [4] [3] [2] [1] [0]	V2 V1 U5 U4 U3 U2 R1 R2	I1/O1	8	64 Bidirectional data signals.
RAS_L	W3	O4	1	Row Address Select output. Precharge cycle indicated if asserted with WE_L.
CAS_L	W4	O4	1	Column Address Select output.
WE_L	W2	O4	1	Write Enable output.
DQM	W1	O4	1	SDRAM data control output. SDRAMs use this signal to enable their data buffers to drive MDATA[63:0] on reads, or enable the SDRAM to accept input data from MDATA[63:0] for writes.
SDCLK	AD1	O3	1	SDRAM Clock output. Frequency is one half the speed of the Core clock ( $\frac{1}{2} * F_{core}$ ).
Totals:			92	



### 3.3.4 IX Bus Interface Pins

**Table 15. IX Bus Interface Pins**

IX Bus Signal Names	Pin Number	Type	Total	Pin Descriptions
FCLK	AB30	I3	1	IX Bus Clock input. All IX Bus transfers are synchronized to this clock. Typical operating frequency 33 MHz - 104 MHz.
PORTCTL_L[3:0]	AC30 AB27 AC31 AB28	O1/TS	4	Port Control outputs. Used to select the transmit and/or receive mode for IX Bus devices, typically MAC devices. In 64-bit bidirectional IX Bus mode, this is a 4-bit bus used to indicate transmit or receive commands and device selects. In 32-bit unidirectional IX Bus mode, bits [1:0] are used to select the receive device and bits [3:2] are used to select the transmit device. In a shared IX Bus system, these pins will be tri-stated when passing ownership of the IX Bus.
FPS[2:0]	AC29 AC28 AD31	O4/TS	3	MAC Port Select outputs. In 32-bit and 64-bit modes, these pins select one of eight MAC receive ports from the selected MAC device. See IX Bus control signal decode tables. In a shared IX Bus system, these pins will be tri-stated when passing ownership of the IX Bus.
FDAT[63:0]	AC27 AD30 AD29 AD28 AE30 AE29 AE28 AF30 AE27 AF29 AG31 AF28 AG30 AJ26 AG25 AK26 AH25 AJ25 AK25 AG24 AL25 AH24 AJ24 AK24 AG23 AL24 AH23 AJ23 AK23 AG22 AL23 AH22 AJ22	I2/O5/ TS	64	IX Bus Data. One 64-bit bus in bidirectional IX Bus mode. Two 32-bit buses in unidirectional IX Bus mode where bits [63:32] are used for Transmit Data output and [31:0] are used for Receive Data input. In a shared IX Bus system, these pins will be tri-stated when passing ownership of the IX Bus.

Table 15. IX Bus Interface Pins (Continued)

IX Bus Signal Names	Pin Number	Type	Total	Pin Descriptions
[30] AK22 [29] AH21 [28] AJ21 [27] AK21 [26] AG20 [25] AH20 [24] AJ20 [23] AK20 [22] AL20 [21] AG19 [20] AH19 [19] AJ19 [18] AK19 [17] AL19 [16] AG18 [15] AH18 [14] AJ18 [13] AK18 [12] AL18 [11] AG17 [10] AH17 [9] AJ17 [8] AK17 [7] AL15 [6] AK15 [5] AJ15 [4] AH15 [3] AG15 [2] AL14 [1] AK14 [0] AJ14				
FBE_L[7:0]	[7] AH14 [6] AG14 [5] AL13 [4] AK13 [3] AJ13 [2] AH13 [1] AG13 [0] AL12	I2/O5/ TS	8	<p>Bidirectional Byte Enables.</p> <p>64-bit bidirectional IX Bus mode. Bits [7:0] indicate transmit and receive valid bytes on FDAT[63:0].</p> <p>32-bit unidirectional IX Bus mode. Bits [7:4] are used to indicate valid transmit bytes on FDAT[63:32] and bits [3:0] are used to indicate valid receive bytes on FDAT[31:0].</p> <p>In a shared IX Bus system, these pins will be tri-stated when passing ownership of the IX Bus.</p>
TXASIS	AH12	O4/TS	1	<p>Transmit As Is.</p> <p>TXASIS states are output according to values programmed in the TFIFO control field. TXASIS value driven coincident with SOP/SOP_TX signal.</p> <p>In a shared IX Bus system, this pin will be tri-stated when passing ownership of the IX Bus.</p>
RXFAL	AG12	I1/O1/ TS	1	<p>Receive Packet Failure. As input, asserted by a MAC device if a packet was received with errors. Mimics the behavior of EOP to terminate an IX Bus cycle.</p> <p>As output, driven when no receive cycle in-progress.</p> <p>In a shared IX Bus system, these pins will be tri-stated when passing ownership of the IX Bus.</p>
FAST_RX1	AK11	I1	1	Ready Input from Fast Port 0 (i.e., Gigabit port). Pulldown through 10 KOhms to VSS if not used.
FAST_RX2	AJ11	I1	1	Ready Input from Fast Port 1 (i.e., Gigabit port). Pulldown through 10 KOhms to VSS if not used.

Table 15. IX Bus Interface Pins (Continued)

IX Bus Signal Names	Pin Number	Type	Total	Pin Descriptions
RDYCTL_L[4]	AJ8	I1	1	<p>In 64-bit Bidirectional IX Bus Mode:</p> <ul style="list-style-type: none"> <li>1-2 MAC mode: Used as an active low flow control enable for MAC 1 (GPIO[0] is used as a flow control enable for MAC 0).</li> <li>3+ MAC mode: Used in conjunction with RDYCTL_L[3:0].</li> <li>In a shared IX Bus system the IXP1250 Ready Bus Master drives this pin. IXP1250 Ready Bus slave devices snoop this pin.</li> </ul> <p>In 32-bit Unidirectional Mode:</p> <ul style="list-style-type: none"> <li>1-2 MAC mode: Used as an active low flow control enable for MAC 1. GPIO[0] is used as a flow control enable for MAC 0.</li> <li>3+ MAC mode: Used as an active low enable for an external decoder for the PORTCTL[1:0] signals.</li> </ul>
RDYCTL_L[3:0] [3] AK8 [2] AG9 [1] AL8 [0] AH9		I1/O4/ TS	4	<p>Bidirectional Ready Control signals.</p> <p>In 64-bit Bidirectional IX Bus Mode:</p> <ul style="list-style-type: none"> <li>1-2 MAC mode: Bits [3:0] are used to enable the transmit or receive FIFO Ready Flags.</li> <li>3+ MAC mode: The transmit and receive FIFO Ready, the flow control, and inter-processor communication enables are decoded from RDYCTL_L[4:0].</li> <li>In a shared IX Bus system the IXP1250 Ready Bus Master drives this bus. IXP1250 Ready Bus slave devices snoop these pins as inputs.</li> </ul> <p>In 32-bit Unidirectional Mode:</p> <ul style="list-style-type: none"> <li>1-2 MAC mode: Bits [3:0] are used to enable the transmit or receive FIFO Ready Flags.</li> <li>3+ MAC mode: The transmit and receive FIFO ready and flow control enables are decoded from RDYCTL_L[3:0].</li> </ul>
RDYBUS[7:0] [7] AH11 [6] AK10 [5] AJ10 [4] AH10 [3] AL9 [2] AG10 [1] AK9 [0] AJ9		I1/O4	8	<p>8-Bit Bidirectional Ready Bus data.</p> <ul style="list-style-type: none"> <li>Inputs the Transmit and Receive Ready Flags from IX Bus devices.</li> <li>Outputs flow control data to IX Bus devices.</li> <li>Data bus for interprocessor communications.</li> </ul>
SOP	AK12	I1/TS	1	<p>Start of Packet indication.</p> <ul style="list-style-type: none"> <li>Receive Start of Packet Input in 32-bit unidirectional IX Bus mode.</li> <li>Input/Output in 64-bit bidirectional IX Bus mode. SOP is Transmit Start of Packet output according to values programmed in the TFIFO control field. Is Receive Start of Packet input during receive cycles.</li> <li>In a shared IX Bus system, this pin will be tri-stated when passing ownership of the IX Bus.</li> </ul>

Table 15. IX Bus Interface Pins (Continued)

IX Bus Signal Names	Pin Number	Type	Total	Pin Descriptions
EOP	AJ12	I1/TS	1	<p>End of Packet Indication.</p> <ul style="list-style-type: none"> <li>Receive End of Packet Input in 32-bit unidirectional IX Bus mode.</li> <li>Input/Output in 64-bit bidirectional IX Bus mode. EOP is Transmit End of Packet output according to values programmed in the TFIFO control field. Is Receive End of Packet input during receive cycles.</li> <li>In a shared IX Bus system, this pin will be tri-stated when passing ownership of the IX Bus.</li> </ul>
EOP32	AL7	O4	1	<p>Transmit End Of Packet</p> <p>32-bit unidirectional IX Bus modes EOP32 is Transmit End of Packet output according to values programmed in the TFIFO control field.</p>
SOP32	AH8	O4	1	<p>Transmit Start Of Packet Indication</p> <ul style="list-style-type: none"> <li>Output in 32-bit unidirectional IX Bus modes. SOP32 is Transmit Start of Packet output during transmit according to values programmed in the TFIFO control field.</li> </ul>
TK_OUT	AA29	O1	1	<p>Token Output.</p> <p>Used to pass ownership of the IX Bus in a shared IX Bus system in 64-bit bidirectional IX Bus mode.</p> <p>In 32-bit unidirectional mode this bit is unused and should be left unconnected.</p>
TK_IN	AA28	I1	1	<p>Token Input.</p> <p>64-bit bidirectional IX Bus Mode: A high-to-low transition indicates that this device has been given ownership of the IX Bus in a shared IX Bus system.</p> <p>In 32-bit unidirectional mode, this input is not used and should be pulled high.</p> <p>During Reset, used to configure the device as initial IX Bus owner. 1= device is initial owner, 0= device does not own the IX Bus. TK_IN is sampled from the rising edge of RESET_IN_L.</p>
Totals:			103	

### 3.3.5 General Purpose I/Os

Table 16. General Purpose I/Os

General Purpose I/O Signal Names	Pin Number	Type	Total	Pin Descriptions
GPIO[3:1] [3] [2] [1]	A24 E23 B24	I1/O4	3	Bidirectional General Purpose pins. 64-bit Bidirectional IX Bus mode: Accessible by StrongARM* core. Configurable as Input or Output. 32-bit Unidirectional IX Bus mode: Transmit Port Select [2:0] outputs. GPIO[3] is sampled during reset to determine if a 32-bit or 16-bit BootROM device is used. If low, enable 32-bit BootROM. If high, Enable 16-bit BootROM.
GPIO[0]	C24	I1/O4	1	Bidirectional General Purpose I/O pin. 1-2 MAC mode (Uni or Bidirectional mode): Active low Flow Control Enable output for MAC 0. 3+ MAC 64-bit Bidirectional IX Bus mode: Accessible to the StrongARM* core. Configurable as input or output. 3+ MAC 32-bit Unidirectional IX Bus mode: Active high Transmit Port Enable for an external PORTCTL_L[3:2] decoder.
Totals:			4	

### 3.3.6 Serial Port (UART) Pins

Table 17. Serial Port (UART) Pins

Serial Port (UART) Signal Names	Pin Number	Type	Total	Pin Descriptions
RXD	C23	I1	1	UART Receive data.
TXD	D23	O1	1	UART Transmit data.
Totals:			2	

### 3.3.7 PCI Interface Pins

Table 18. PCI Interface Pins

PCI Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
AD[31:0] [31] D19 [30] C19 [29] B19 [28] D18 [27] C18 [26] B18 [25] A18 [24] E17 [23] B17 [22] A17 [21] B15 [20] C15 [19] D15 [18] E15 [17] A14 [16] B14 [15] C12 [14] D12 [13] E12 [12] B11 [11] C11 [10] D11 [9] A10 [8] C10 [7] A9 [6] E10 [5] B9 [4] C9 [3] D9 [2] A8 [1] E9 [0] B8		I2/O2/ TS	32	Address/data. These signals are multiplexed address and data bus. The IXP1250 receives addresses as target and drives addresses as master. It receives write data and drives read data as target. It drives write data and receives read data as master.
CBE_L[3:0] [3] D17 [2] C14 [1] B12 [0] D10		I2/O2/ TS	4	Command byte enables. These signals are multiplexed command and byte enable signals. The IXP1250 receives commands as target and drives commands as master. It receives byte enables as target and drives byte enables as master.
PAR	A12	I2/O2/ TS	1	Parity. This signal carries even parity for AD and CBE_L pins. It has the same receive and drive characteristics as the address and data bus, except that it occurs on the next PCI clock cycle.
FRAME_L	D14	I2/O2/ STS	1	FRAME_L indicates the beginning and duration of an access. The IXP1250 receives as target and drives as master.
IRDY_L	E14	I2/O2/ STS	1	Initiator ready. Indicates the master's ability to complete the current data phase of the transaction. The IXP1250 receives as target and drives as master.
TRDY_L	A13	I2/O2/ STS	1	Target ready. Indicates the target's ability to complete the current data phase of the transaction. The IXP1250 drives as target and receives as master.

Table 18. PCI Interface Pins (Continued)

PCI Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
STOP_L	C13	I2/O2/STS	1	Stop. Indicates that the target is requesting the master to stop the current transaction. The IXP1250 drives as target and receives as master.
DEVSEL_L	B13	I2/O2/STS	1	Device Select. Indicates that the target has decoded its address as the target of the current access. The IXP1250 drives as target and receives as initiator.
IDSEL	C17	I2	1	Initialization Device Select. Used as Chip Select during PCI Configuration Space read and write transactions.
PERR_L	D13	I2/O2/STS	1	Parity error. Used to report data parity errors. The IXP1250 asserts this when it receives bad data parity as target of a write or master of a read.
SERR_L	E13	I2/O2/OD	1	System Error. As an input, it can cause an interrupt to the StrongARM* core if the IXP1250 is selected for PCI Central Function and arbitration support (PCI_CFN[1:0]=11). As an output it can be asserted by the IXP1250 by writing the SERR bit in the PCI control register, or in response to a PCI address parity error when not providing PCI Central Function and arbitration support (PCI_CFN[1:0]=00).
PCI_IRQ_L	B21	I2/O2/OD	1	PCI Interrupt Request. As output, used to interrupt the PCI Host Processor. It is asserted when there is a doorbell set or there are messages on the I <sub>2</sub> O outbound post list. This is usually connected to INTA_L on the PCI Bus. As Input, It is asserted when there is a doorbell set or there are messages on the I <sub>2</sub> O outbound post list.
PCI_RST_L	E20	I2/O2/TS	1	PCI Reset. <ul style="list-style-type: none"> <li>When providing PCI Central Function and arbitration support (PCI_CFN[1:0]=11), PCI_RST_L is an output controlled by the StrongARM* core. Used to reset the PCI Bus.</li> <li>When not providing PCI Central Function and arbitration (PCI_CFN[1:0]=00), PCI_RST_L is an input, and when asserted resets the IXP1250 StrongARM* core, all registers, all transaction queues, and all PCI related state.</li> </ul>
PCI_CLK	D20	I2	1	PCI Clock input. Reference for PCI signals and internal operations. PCI clock is typically 33 to 66 MHz.

Table 18. PCI Interface Pins (Continued)

PCI Interface Signal Names	Pin Number	Type	Total	Pin Descriptions
PCI_CFN [1] [0]	A23 E22	I2	2	<p>PCI Central Function and arbitration select inputs. Sampled on the rising edge of RESET_IN_L.</p> <p>When = 11, the IXP1250 provides the PCI Central Function and arbitration support and:</p> <ul style="list-style-type: none"> <li>• PCI_RST_L is an output asserted by the PCI Unit when initiated by the StrongARM* core.</li> <li>• IXP1250 provides bus parking during reset.</li> <li>• SERR_L is an input that can generate an interrupt to the StrongARM* core.</li> </ul> <p>When = 00, PCI Central Function and arbitration is disabled and:</p> <ul style="list-style-type: none"> <li>• PCI_RST_L is an input asserted by the Host processor.</li> <li>• The IXP1250 does not provide bus parking during reset.</li> </ul> <p>Values of 10 and 01 are reserved for future use.</p>
GNT_L[0]	C20	I2/O2	1	<p>PCI Bus Master Grant 1.</p> <p>Internal PCI arbiter is enabled (PCI_CFN[1:0] = 11): Pin is an output to grant a PCI device 1 control of the PCI Bus. (The IXP1250 is PCI device 0 in this case)</p> <p>Internal PCI arbiter is disabled (PCI_CFN[1:0] = 00): Pin is an input that indicates that the IXP1250 can assert FRAME_L and become the bus master. If the IXP1250 is idle when GNT_L[0] is asserted, it parks the PCI Bus.</p>
REQ_L[0]	B20	I2/O2	1	<p>PCI Bus Master Request 1.</p> <p>Internal PCI arbiter is enabled (PCI_CFN[1:0] = 11): Pin is an input indicating an external PCI device is requesting use of the PCI Bus.</p> <p>Internal PCI arbiter is disabled (PCI_CFN[1:0] = 00): Pin is an output indicating that the IXP1250 is requesting use of the PCI Bus.</p>
GNT_L[1]	A20	I2/O2	1	<p>PCI Bus Master Grant 2.</p> <p>Internal PCI arbiter is enabled (PCI_CFN[1:0] = 11): Pin is an output to grant a PCI device 2 control of the PCI Bus (The IXP1250 is PCI device 0 in this case).</p> <p>When Internal PCI arbiter is disabled (PCI_CFN[1:0]=00, GNT_L[1] should be connected to VDDX through a pullup resistor of 10 KOhms.</p>
REQ_L[1]	E19	I2/O2	1	<p>PCI Bus Master Request 2.</p> <p>Internal PCI arbiter is enabled (PCI_CFN[1:0] = 11): This input indicates that PCI device 2 is requesting to take control of the PCI Bus.</p> <p>Is driven to an output high level when internal PCI arbiter is disabled (PCI_CFN[1:0] = 00).</p>
Totals:			54	



### 3.3.8 Power Supply Pins

**Table 19. Power Supply Pins**

Supply Signal Names	Pin Number	Type	Total	Pin Descriptions
VDD		P		IXP1250 Core supply (2V).
	A19, C25, E18, J1, J30, K4, K27, Y5, Y27, Y28, AA2, AC5, AD2, AD27, AE31, AF5, AF27			
Total VDD pins			17	
VDDX		P		IXP1250 I/O supply (3.3V).
	A15, A22, B4, B10, B28, C3, C4, C16, C28, C29, D2 - D5, D16, D27 - D30, E4, E5, E11, E16, E21, E27, E28, K1, K30, L5, L27, R31, T3 - T5, T27 - T29, U1, AA5, AA27, AB2, AB31, AG4, AG5, AG11, AG16, AG21, AG27, AG28, AH2 - AH5, AH16, AH27-AH30, AJ3, AJ4, AJ16, AJ28, AJ29, AK4, AK28, AL10, AL17, AL22			
Total VDDX pins			68	
VDD_REF	E3	P	1	IXP1250 3.3V reference - used to bias the ESD circuitry Can be tied directly to VDDX external to chip.
VSSP1	B6	P	1	IXP1250 PLL ground.
VDDP1	C6	P	1	IXP1250 2V PLL supply. Use decoupling capacitor between VDDP1 and VSSP1.
Total			3	
VSS		P		IXP1250 ground.
	A1-A4, A6, A7, A11, A16, A21, A26, A28 - A31, B1-B3, B16, B29 - B31, C1, C2, C8, C30, C31, D1, D31, F1, F31, J28, L1, L31, T1, T2, T30, T31, V5, W31, AA1, AA31, AB29, AC4, AF1, AF31, AG8, AH1, AH31, AJ1, AJ2, AJ7, AK16, AJ30, AJ31, AL1- AL4, AL6, AL11, AL16, AL21, AL26, AL28 - AL31, AK1 - AK3, AK29 - AK31			
Total VSS pins			73	
Total Power Supply Pins			168	

### 3.3.9 IEEE 1149.1 Interface Pins

Table 20. IEEE 1149.1 Interface Pins

IEEE 1149.1 Interface Pin Name	Pin Number	Type	Total	Pin Description
TCK	C22	I1	1	Test Interface reference clock. This clock times all the transfers on the IEEE 1149.1 test interface.
TMS	B22	I1	1	Test Interface mode select. Causes state transitions on the test access port (TAP) controller.
TDI	C21	I1	1	Test Interface data input. The serial input through which IEEE 1149.1 instructions and test data enter the IEEE 1149.1 interface.
TDO	D21	O1	1	Test Interface data output. The serial output through which test instruction and data from the test logic leave the IXP1250.
TRST_L	D22	I1	1	Test Interface RESET. When asserted low, the TAP controller is asynchronously forced to enter a reset state, and disables the IEEE 1149.1 port. This pin must be driven or held low to achieve normal device operation.
Totals:			5	

### 3.3.10 Miscellaneous Test Pins

Table 21. Miscellaneous Test Pins

Processor Support Signal Names	Pin Number	Type	Total	Pin Descriptions
SCAN_EN	D7	I1	1	Used for Intel test purposes only. Enables internal scan chains for chip testing. This pin should be connected to VSS through a pulldown resistor.
TCK_BYP	C7	I1	1	Used for Intel test purposes only. When high, bypasses PLL for Test/debug. Must be low for normal system operation.
TSTCLK	B7	I1	1	Used for Intel test purposes only. Used as clock input when bypassing the internal PLL clock generator. For Normal operation, this pin should not be allowed to float. It should be pulled up or pulled down through the proper value resistor.
Totals:			3	

### 3.3.11 Pin Usage Summary

Table 22. Pin Usage Summary

Type	Quantity
Inputs	21
Outputs	68
Bidirectional	235
Total Signal	324
Power	168
Overall Totals:	520

## 3.4 Pin/Signal List

Table 23. Pin Table in Pin Order

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
A1	VSS	B4	VDDX	C7	TCK_BYP
A2	VSS	B5	UNUSED24	C8	VSS
A3	VSS	B6	VSSP1	C9	AD[4]
A4	VSS	B7	TSTCLK	C10	AD[8]
A5	UNUSED22	B8	AD[0]	C11	AD[11]
A6	VSS	B9	AD[5]	C12	AD[15]
A7	VSS	B10	VDDX	C13	STOP_L
A8	AD[2]	B11	AD[12]	C14	CBE_L[2]
A9	AD[7]	B12	CBE_L[1]	C15	AD[20]
A10	AD[9]	B13	DEVSEL_L	C16	VDDX
A11	VSS	B14	AD[16]	C17	IDSEL
A12	PAR	B15	AD[21]	C18	AD[27]
A13	TRDY_L	B16	VSS	C19	AD[30]
A14	AD[17]	B17	AD[23]	C20	GNT_L[0]
A15	VDDX	B18	AD[26]	C21	TDI
A16	VSS	B19	AD[29]	C22	TCK
A17	AD[22]	B20	REQ_L[0]	C23	RXD
A18	AD[25]	B21	PCI_IRQ_L	C24	GPIO[0]
A19	VDD	B22	TMS	C25	VDD
A20	GNT_L[1]	B23	NC/SACLK	C26	A[17]
A21	VSS	B24	GPIO[1]	C27	UNUSED18
A22	VDDX	B25	CE_L[0]	C28	VDDX
A23	PCI_CFN[1]	B26	HIGH_EN_L	C29	VDDX
A24	GPIO[3]	B27	UNUSED20	C30	VSS
A25	CE_L[2]	B28	VDDX	C31	VSS
A26	VSS	B29	VSS	D1	VSS
A27	A[16]	B30	VSS	D2	VDDX
A28	VSS	B31	VSS	D3	VDDX
A29	VSS	C1	VSS	D4	VDDX
A30	VSS	C2	VSS	D5	VDDX
A31	VSS	C3	VDDX	D6	UNUSED23
B1	VSS	C4	VDDX	D7	SCAN_EN
B2	VSS	C5	UNUSED26	D8	RESET_IN_L
B3	VSS	C6	VDDP1	D9	AD[3]

Table 23. Pin Table in Pin Order (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
D10	CBE_L[0]	E14	IRDY_L	G29	A[8]
D11	AD[10]	E15	AD[18]	G30	A[7]
D12	AD[14]	E16	VDDX	G31	A[5]
D13	PERR_L	E17	AD[24]	H1	MDATA[16]
D14	FRAME_L	E18	VDD	H2	MDATA[14]
D15	AD[19]	E19	REQ_L[1]	H3	MDATA[13]
D16	VDDX	E20	PCI_RST_L	H4	MDATA[12]
D17	CBE_L[3]	E21	VDDX	H5	MDATA[10]
D18	AD[28]	E22	PCI_CFN{0}	H27	A[6]
D19	AD[31]	E23	GPIO[2]	H28	A[4]
D20	PCI_CLK	E24	CE_L[1]	H29	A[3]
D21	TDO	E25	A[18]	H30	A[2]
D22	TRST_L	E26	UNUSED19	H31	A[0]
D23	TXD	E27	VDDX	J1	VDD
D24	CE_L[3]	E28	VDDX	J2	MDATA[19]
D25	LOW_EN_L	E29	UNUSED17	J3	MDATA[18]
D26	UNUSED21	E30	A[15]	J4	MDATA[17]
D27	VDDX	E31	A[13]	J5	MDATA[15]
D28	VDDX	F1	VSS	J27	A[1]
D29	VDDX	F2	MDATA[6]	J28	VSS
D30	VDDX	F3	MDATA[4]	J29	DQ[31]
D31	VSS	F4	MDATA[2]	J30	VDD
E1	MDATA[3]	F5	MDATA[0]	J31	DQ[30]
E2	MDATA[1]	F27	UNUSED16	K1	VDDX
E3	VDD_REF	F28	A[14]	K2	MDATA[22]
E4	VDDX	F29	A[12]	K3	MDATA[21]
E5	VDDX	F30	A[10]	K4	VDD
E6	UNUSED25	F31	VSS	K5	MDATA[20]
E7	PXTAL	G1	MDATA[11]	K27	VDD
E8	RESET_OUT_L	G2	MDATA[9]	K28	DQ[29]
E9	AD[1]	G3	MDATA[8]	K29	DQ[28]
E10	AD[6]	G4	MDATA[7]	K30	VDDX
E11	VDDX	G5	MDATA[5]	K31	DQ[27]
E12	AD[13]	G27	A[11]	L1	VSS
E13	SERR_L	G28	A[9]	L2	MDATA[25]

Table 23. Pin Table in Pin Order (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
L3	MDATA[24]	P29	DQ[11]	V3	MDATA[44]
L4	MDATA[23]	P30	DQ[10]	V4	MDATA[45]
L5	VDDX	P31	DQ[9]	V5	VSS
L27	VDDX	R1	MDATA_ECC1	V27	DQ[0]
L28	DQ[26]	R2	MDATA_ECC0	V28	DQ[1]
L29	DQ[25]	R3	MDATA[43]	V29	DQ[2]
L30	DQ[24]	R4	MDATA[42]	V30	DQ[3]
L31	VSS	R5	MDATA[41]	V31	UNUSED11
M1	MDATA[30]	R27	DQ[8]	W1	DQM
M2	MDATA[29]	R28	DQ[7]	W2	WE_L
M3	MDATA[28]	R29	DQ[6]	W3	RAS_L
M4	MDATA[27]	R30	DQ[5]	W4	CAS_L
M5	MDATA[26]	R31	VDDX	W5	MADR[0]
M27	DQ[23]	T1	VSS	W27	MRD_L
M28	DQ[22]	T2	VSS	W28	MCE_L
M29	DQ[21]	T3	VDDX	W29	SOE_L
M30	DQ[20]	T4	VDDX	W30	SCLK
M31	DQ[19]	T5	VDDX	W31	VSS
N1	MDATA[35]	T27	VDDX	Y1	MADR[1]
N2	MDATA[34]	T28	VDDX	Y2	MADR[2]
N3	MDATA[33]	T29	VDDX	Y3	MADR[3]
N4	MDATA[32]	T30	VSS	Y4	MADR[4]
N5	MDATA[31]	T31	VSS	Y5	VDD
N27	DQ[18]	U1	VDDX	Y27	VDD
N28	DQ[17]	U2	MDATA_ECC2	Y28	VDD
N29	DQ[16]	U3	MDATA_ECC3	Y29	SLOW_EN_L
N30	DQ[15]	U4	MDATA_ECC4	Y30	FWE_L
N31	DQ[14]	U5	MDATA_ECC5	Y31	SWE_L
P1	MDATA[40]	U27	UNUSED12	AA1	VSS
P2	MDATA[39]	U28	UNUSED13	AA2	VDD
P3	MDATA[38]	U29	UNUSED14	AA3	MADR[5]
P4	MDATA[37]	U30	UNUSED15	AA4	MADR[6]
P5	MDATA[36]	U31	DQ[4]	AA5	VDDX
P27	DQ[13]	V1	MDATA_ECC6	AA27	VDDX
P28	DQ[12]	V2	MDATA_ECC7	AA28	TK_IN

Table 23. Pin Table in Pin Order (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
AA29	TK_OUT	AE3	MDATA[51]	AG18	FDAT[16]
AA30	CINT_L	AE4	MDATA[52]	AG19	FDAT[21]
AA31	VSS	AE5	MDATA[54]	AG20	FDAT[26]
AB1	MADR[7]	AE27	FDAT[55]	AG21	VDDX
AB2	VDDX	AE28	FDAT[57]	AG22	FDAT[34]
AB3	MADR[8]	AE29	FDAT[58]	AG23	FDAT[39]
AB4	MADR[9]	AE30	FDAT[59]	AG24	FDAT[44]
AB5	MADR[11]	AE31	VDD	AG25	FDAT[49]
AB27	PORTCTL_L[2]	AF1	VSS	AG26	UNUSED8
AB28	PORTCTL_L[0]	AF2	MDATA[53]	AG27	VDDX
AB29	VSS	AF3	MDATA[55]	AG28	VDDX
AB30	FCLK	AF4	MDATA[57]	AG29	UNUSED10
AB31	VDDX	AF5	VDD	AG30	FDAT[51]
AC1	MADR[10]	AF27	VDD	AG31	FDAT[53]
AC2	MADR[12]	AF28	FDAT[52]	AH1	VSS
AC3	MADR[13]	AF29	FDAT[54]	AH2	VDDX
AC4	VSS	AF30	FDAT[56]	AH3	VDDX
AC5	VDD	AF31	VSS	AH4	VDDX
AC27	FDAT[63]	AG1	MDATA[56]	AH5	VDDX
AC28	FPS[1]	AG2	MDATA[58]	AH6	UNUSED4
AC29	FPS[2]	AG3	UNUSED0	AH7	MDATA[63]
AC30	PORTCTL_L[3]	AG4	VDDX	AH8	SOP32_OUT
AC31	PORTCTL_L[1]	AG5	VDDX	AH9	RDYCTL_L[0]
AD1	SDCLK	AG6	UNUSED2	AH10	RDYBUS[4]
AD2	VDD	AG7	MDATA[61]	AH11	RDYBUS[7]
AD3	MDATA[46]	AG8	VSS	AH12	TXAXIS
AD4	MDATA[47]	AG9	RDYCTL_L[2]	AH13	FBE_L[2]
AD5	MDATA[49]	AG10	RDYBUS[2]	AH14	FBE_L[7]
AD27	VDD	AG11	VDDX	AH15	FDAT[4]
AD28	FDAT[60]	AG12	RXFAIL	AH16	VDDX
AD29	FDAT[61]	AG13	FBE_L[1]	AH17	FDAT[10]
AD30	FDAT[62]	AG14	FBE_L[6]	AH18	FDAT[15]
AD31	FPS[0]	AG15	FDAT[3]	AH19	FDAT[20]
AE1	MDATA[48]	AG16	VDDX	AH20	FDAT[25]
AE2	MDATA[50]	AG17	FDAT[11]	AH21	FDAT[29]

Table 23. Pin Table in Pin Order (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
AH22	FDAT[32]	AJ27	UNUSED9	AL1	VSS
AH23	FDAT[37]	AJ28	VDDX	AL2	VSS
AH24	FDAT[42]	AJ29	VDDX	AL3	VSS
AH25	FDAT[47]	AJ30	VSS	AL4	VSS
AH26	UNUSED6	AJ31	VSS	AL5	MDAT[59]
AH27	VDDX	AK1	VSS	AL6	VSS
AH28	VDDX	AK2	VSS	AL7	EOP32_OUT
AH29	VDDX	AK3	VSS	AL8	RDYCTL_L[1]
AH30	VDDX	AK4	VDDX	AL9	RDYBUS[3]
AH31	VSS	AK5	UNUSED3	AL10	VDDX
AJ1	VSS	AK6	MDATA[62]	AL11	VSS
AJ2	VSS	AK7	MADR[14]	AL12	FBE_L[0]
AJ3	VDDX	AK8	RDYCTL_L[3]	AL13	FBE_L[5]
AJ4	VDDX	AK9	RDYBUS[1]	AL14	FDAT[2]
AJ5	UNUSED1	AK10	RDYBUS[6]	AL15	FDAT[7]
AJ6	MDATA[60]	AK11	FAST_RX1	AL16	VSS
AJ7	VSS	AK12	SOP	AL17	VDDX
AJ8	RDYCTL_L[4]	AK13	FBE_L[4]	AL18	FDAT[12]
AJ9	RDYBUS[0]	AK14	FDAT[1]	AL19	FDAT[17]
AJ10	RDYBUS[5]	AK15	FDAT[6]	AL20	FDAT[22]
AJ11	FAST_RX2	AK16	VSS	AL21	VSS
AJ12	EOP	AK17	FDAT[8]	AL22	VDDX
AJ13	FBE_L[3]	AK18	FDAT[13]	AL23	FDAT[33]
AJ14	FDAT[0]	AK19	FDAT[18]	AL24	FDAT[38]
AJ15	FDAT[5]	AK20	FDAT[23]	AL25	FDAT[43]
AJ16	VDDX	AK21	FDAT[27]	AL26	VSS
AJ17	FDAT[9]	AK22	FDAT[30]	AL27	UNUSED5
AJ18	FDAT[14]	AK23	FDAT[35]	AL28	VSS
AJ19	FDAT[19]	AK24	FDAT[40]	AL29	VSS
AJ20	FDAT[24]	AK25	FDAT[45]	AL30	VSS
AJ21	FDAT[28]	AK26	FDAT[48]	AL31	VSS
AJ22	FDAT[31]	AK27	UNUSED7		
AJ23	FDAT[36]	AK28	VDDX		
AJ24	FDAT[41]	AK29	VSS		
AJ25	FDAT[46]	AK30	VSS		
AJ26	FDAT[50]	AK31	VSS		



### 3.5 Signals Listed in Alphabetical Order

Table 24. Pin Table in Alphabetical Order

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
A[0]	H31	AD[22]	A17	DQ[14]	N31
A[1]	J27	AD[23]	B17	DQ[15]	N30
A[10]	F30	AD[24]	E17	DQ[16]	N29
A[11]	G27	AD[25]	A18	DQ[17]	N28
A[12]	F29	AD[26]	B18	DQ[18]	N27
A[13]	E31	AD[27]	C18	DQ[19]	M31
A[14]	F28	AD[28]	D18	DQ[2]	V29
A[15]	E30	AD[29]	B19	DQ[20]	M30
A[16]	A27	AD[3]	D9	DQ[21]	M29
A[17]	C26	AD[30]	C19	DQ[22]	M28
A[18]	E25	AD[31]	D19	DQ[23]	M27
A[2]	H30	AD[4]	C9	DQ[24]	L30
A[3]	H29	AD[5]	B9	DQ[25]	L29
A[4]	H28	AD[6]	E10	DQ[26]	L28
A[5]	G31	AD[7]	A9	DQ[27]	K31
A[6]	H27	AD[8]	C10	DQ[28]	K29
A[7]	G30	AD[9]	A10	DQ[29]	K28
A[8]	G29	CAS_L	W4	DQ[3]	V30
A[9]	G28	CBE_L[0]	D10	DQ[30]	J31
AD[0]	B8	CBE_L[1]	B12	DQ[31]	J29
AD[1]	E9	CBE_L[2]	C14	DQ[4]	U31
AD[10]	D11	CBE_L[3]	D17	DQ[5]	R30
AD[11]	C11	CE_L[0]	B25	DQ[6]	R29
AD[12]	B11	CE_L[1]	E24	DQ[7]	R28
AD[13]	E12	CE_L[2]	A25	DQ[8]	R27
AD[14]	D12	CE_L[3]	D24	DQ[9]	P31
AD[15]	C12	CINT_L	AA30	DQM	W1
AD[16]	B14	DEVSEL_L	B13	EOP	AJ12
AD[17]	A14	DQ[0]	V27	<b>EOP32</b>	<b>AL7</b>
AD[18]	E15	DQ[1]	V28	FAST_RX1	AK11
AD[19]	D15	DQ[10]	P30	FAST_RX2	AJ11
AD[2]	A8	DQ[11]	P29	FBE_L[0]	AL12
AD[20]	C15	DQ[12]	P28	FBE_L[1]	AG13
AD[21]	B15	DQ[13]	P27	FBE_L[2]	AH13

Table 24. Pin Table in Alphabetical Order (Continued)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
FBE_L[3]	AJ13	FDAT[37]	AH23	FWE_L	Y30
FBE_L[4]	AK13	FDAT[38]	AL24	GNT_L[0]	C20
FBE_L[5]	AL13	FDAT[39]	AG23	GNT_L[1]	A20
FBE_L[6]	AG14	FDAT[4]	AH15	GPIO[0]	C24
FBE_L[7]	AH14	FDAT[40]	AK24	GPIO[1]	B24
FCLK	AB30	FDAT[41]	AJ24	GPIO[2]	E23
FDAT[0]	AJ14	FDAT[42]	AH24	GPIO[3]	A24
FDAT[1]	AK14	FDAT[43]	AL25	HIGH_EN_L	B26
FDAT[10]	AH17	FDAT[44]	AG24	IDSEL	C17
FDAT[11]	AG17	FDAT[45]	AK25	IRDY_L	E14
FDAT[12]	AL18	FDAT[46]	AJ25	LOW_EN_L	D25
FDAT[13]	AK18	FDAT[47]	AH25	MADR[0]	W5
FDAT[14]	AJ18	FDAT[48]	AK26	MADR[1]	Y1
FDAT[15]	AH18	FDAT[49]	AG25	MADR[10]	AC1
FDAT[16]	AG18	FDAT[5]	AJ15	MADR[11]	AB5
FDAT[17]	AL19	FDAT[50]	AJ26	MADR[12]	AC2
FDAT[18]	AK19	FDAT[51]	AG30	MADR[13]	AC3
FDAT[19]	AJ19	FDAT[52]	AF28	MADR[14]	AK7
FDAT[2]	AL14	FDAT[53]	AG31	MADR[2]	Y2
FDAT[20]	AH19	FDAT[54]	AF29	MADR[3]	Y3
FDAT[21]	AG19	FDAT[55]	AE27	MADR[4]	Y4
FDAT[22]	AL20	FDAT[56]	AF30	MADR[5]	AA3
FDAT[23]	AK20	FDAT[57]	AE28	MADR[6]	AA4
FDAT[24]	AJ20	FDAT[58]	AE29	MADR[7]	AB1
FDAT[25]	AH20	FDAT[59]	AE30	MADR[8]	AB3
FDAT[26]	AG20	FDAT[6]	AK15	MADR[9]	AB4
FDAT[27]	AK21	FDAT[60]	AD28	MCE_L	W28
FDAT[28]	AJ21	FDAT[61]	AD29	MDATA[0]	F5
FDAT[29]	AH21	FDAT[62]	AD30	MDATA[1]	E2
FDAT[3]	AG15	FDAT[63]	AC27	MDATA[10]	H5
FDAT[30]	AK22	FDAT[7]	AL15	MDATA[11]	G1
FDAT[31]	AJ22	FDAT[8]	AK17	MDATA[12]	H4
FDAT[32]	AH22	FDAT[9]	AJ17	MDATA[13]	H3
FDAT[33]	AL23	FPS[0]	AD31	MDATA[14]	H2
FDAT[34]	AG22	FPS[1]	AC28	MDATA[15]	J5
FDAT[35]	AK23	FPS[2]	AC29	MDATA[16]	H1
FDAT[36]	AJ23	FRAME_L	D14	MDATA[17]	J4

Table 24. Pin Table in Alphabetical Order (Continued)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
MDATA[18]	J3	MDATA[51]	AE3	PORTCTL_L[3]	AC30
MDATA[19]	J2	MDATA[52]	AE4	PXTAL	E7
MDATA[2]	F4	MDATA[53]	AF2	RAS_L	W3
MDATA[20]	K5	MDATA[54]	AE5	RDYBUS[0]	AJ9
MDATA[21]	K3	MDATA[55]	AF3	RDYBUS[1]	AK9
MDATA[22]	K2	MDATA[56]	AG1	RDYBUS[2]	AG10
MDATA[23]	L4	MDATA[57]	AF4	RDYBUS[3]	AL9
MDATA[24]	L3	MDATA[58]	AG2	RDYBUS[4]	AH10
MDATA[25]	L2	MDATA[59]	AL5	RDYBUS[5]	AJ10
MDATA[26]	M5	MDATA[6]	F2	RDYBUS[6]	AK10
MDATA[27]	M4	MDATA[60]	AJ6	RDYBUS[7]	AH11
MDATA[28]	M3	MDATA[61]	AG7	RDYCTL_L[0]	AH9
MDATA[29]	M2	MDATA[62]	AK6	RDYCTL_L[1]	AL8
MDATA[3]	E1	MDATA[63]	AH7	RDYCTL_L[2]	AG9
MDATA[30]	M1	MDATA[7]	G4	RDYCTL_L[3]	AK8
MDATA[31]	N5	MDATA[8]	G3	RDYCTL_L[4]	AJ8
MDATA[32]	N4	MDATA[9]	G2	REQ_L[0]	B20
MDATA[33]	N3	MDATA_ECC[0]	R2	REQ_L[1]	E19
MDATA[34]	N2	MDATA_ECC[1]	R1	RESET_IN_L	D8
MDATA[35]	N1	MDATA_ECC[2]	U2	RESET_OUT_L	E8
MDATA[36]	P5	MDATA_ECC[3]	U3	RXD	C23
MDATA[37]	P4	MDATA_ECC[4]	U4	RXFAIL	AG12
MDATA[38]	P3	MDATA_ECC[5]	U5	SCAN_EN	D7
MDATA[39]	P2	MDATA_ECC[6]	V1	SCLK	W30
MDATA[4]	F3	MDATA_ECC[7]	V2	SDCLK	AD1
MDATA[40]	P1	MRD_L	W27	SERR_L	E13
MDATA[41]	R5	NC/SACLK	B23	SLOW_EN_L	Y29
MDATA[42]	R4	PAR	A12	SOE_L	W29
MDATA[43]	R3	PCI_CFN[0]	E22	SOP	AK12
MDATA[44]	V3	PCI_CFN[1]	A23	SOP32	AH8
MDATA[45]	V4	PCI_CLK	D20	STOP_L	C13
MDATA[46]	AD3	PCI_IRQ_L	B21	SWE_L	Y31
MDATA[47]	AD4	PCI_RST_L	E20	TCK	C22
MDATA[48]	AE1	PERR_L	D13	TCK_BYP	C7
MDATA[49]	AD5	PORTCTL_L[0]	AB28	TDI	C21
MDATA[5]	G5	PORTCTL_L[1]	AC31	TDO	D21
MDATA[50]	AE2	PORTCTL_L[2]	AB27	TK_IN	AA28

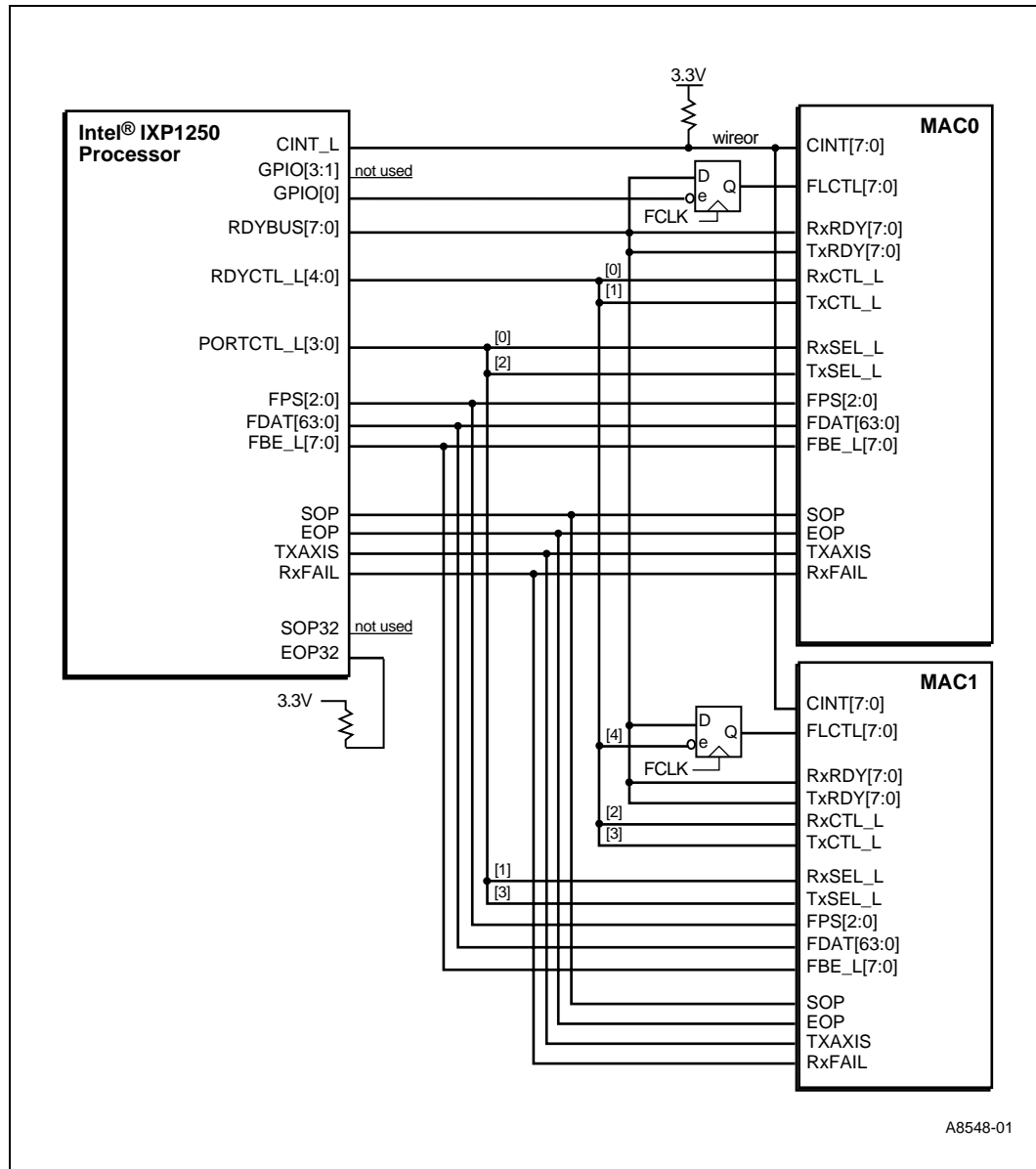
Table 24. Pin Table in Alphabetical Order (Continued)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
TK_OUT	AA29				
TMS	B22				
TRDY_L	A13				
TRST_L	D22				
TSTCLK	B7				
TXASIS	AH12				
TXD	D23				
WE_L	W2				
VDD	A19, C25, E18, J1, J30, K4, K27, Y5, Y27, Y28, AA2, AC5, AD2, AD27, AE31, AF5, AF27				
VDDX	A15, A22, B4, B10, B28, C3, C4, C16, C28, C29, D2 - D5, D16, D27 - D30, E4, E5, E11, E16, E21, E27, E28, K1, K30, L5, L27, R31, T3 - T5, T27 - T29, U1, AA5, AA27, AB2, AB31, AG4, AG5, AG11, AG16, AG21, AG27, AG28, AH2 - AH5, AH16, AH27-AH30, AJ3, AJ4, AJ16, AJ28, AJ29, AK4, AK28, AL10, AL17, AL22				
VDD_REF	E3				
VDD_P1	C6				
VSS	A1-A4, A6, A7, A11, A16, A21, A26, A28 - A31, AL28 - AL31, B1 - B3, B16, B29 - B31, C1, C2, C8, C30, C31, D1, D31, F1, F31, J28, L1, L31, T1, T2, T30, T31, V5, W31, AA1, AA31, AB29, AC4, AF1, AF31, AG8, AH1, AH31, AJ1, AJ2, AJ7, AK16, AJ30, AJ31, AL1 - AL4, AL6, AL11, AL16, AL21, AL26, AL28 - AL31, AK1 - AK3, AK29 - AK31				
VSSP1	B6				
UNUSED0 - UNUSED26 (not listed in order)	AG3, AG26, AG29, AH6, AH26, AJ5, AJ27, AK27, AL27, V31, U27, U28, U29, U30, F27, E29, C27, E26, AG6, B27, D26, A5, D6, B5, E6, C5, AK5				

### 3.6 IX Bus Pins Function Listed by Operating Mode

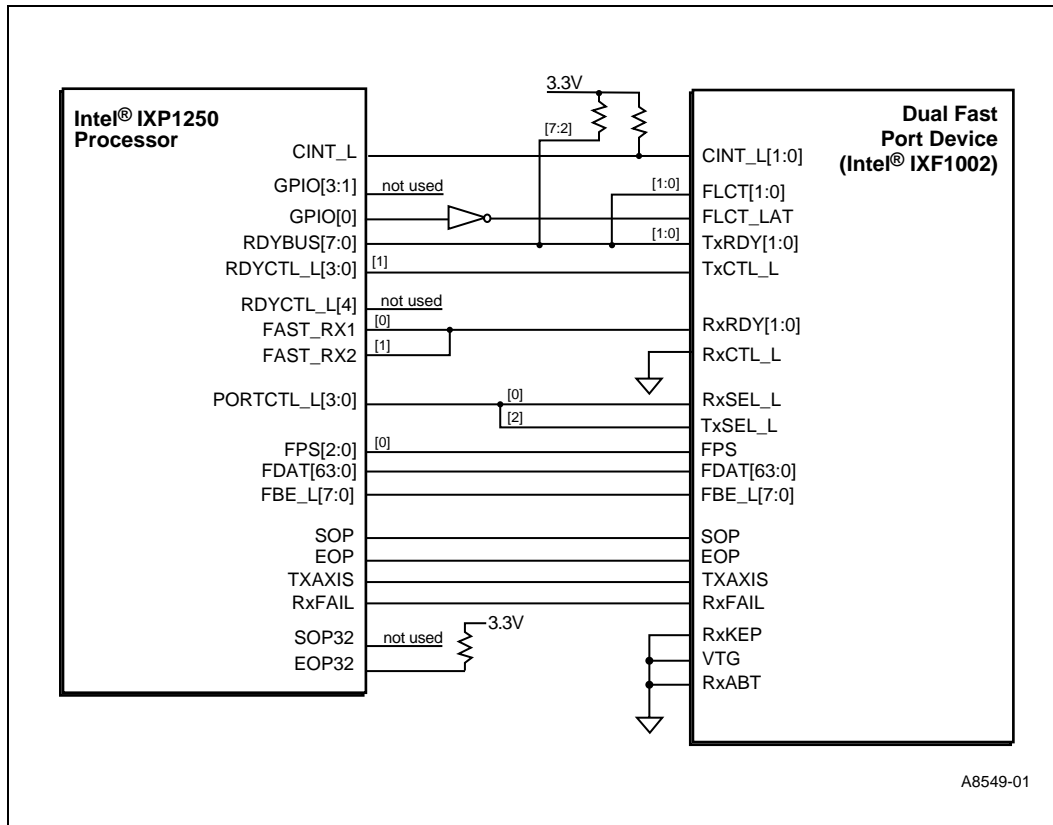
Figure 7 through Figure 11 illustrate the four IX Bus modes. Each figure shows the logic interface to one or more MAC devices and is accompanied by a pin description for the IX Bus in that mode.

Figure 7. 64-Bit Bidirectional IX Bus, 1-2 MAC Mode



A8548-01

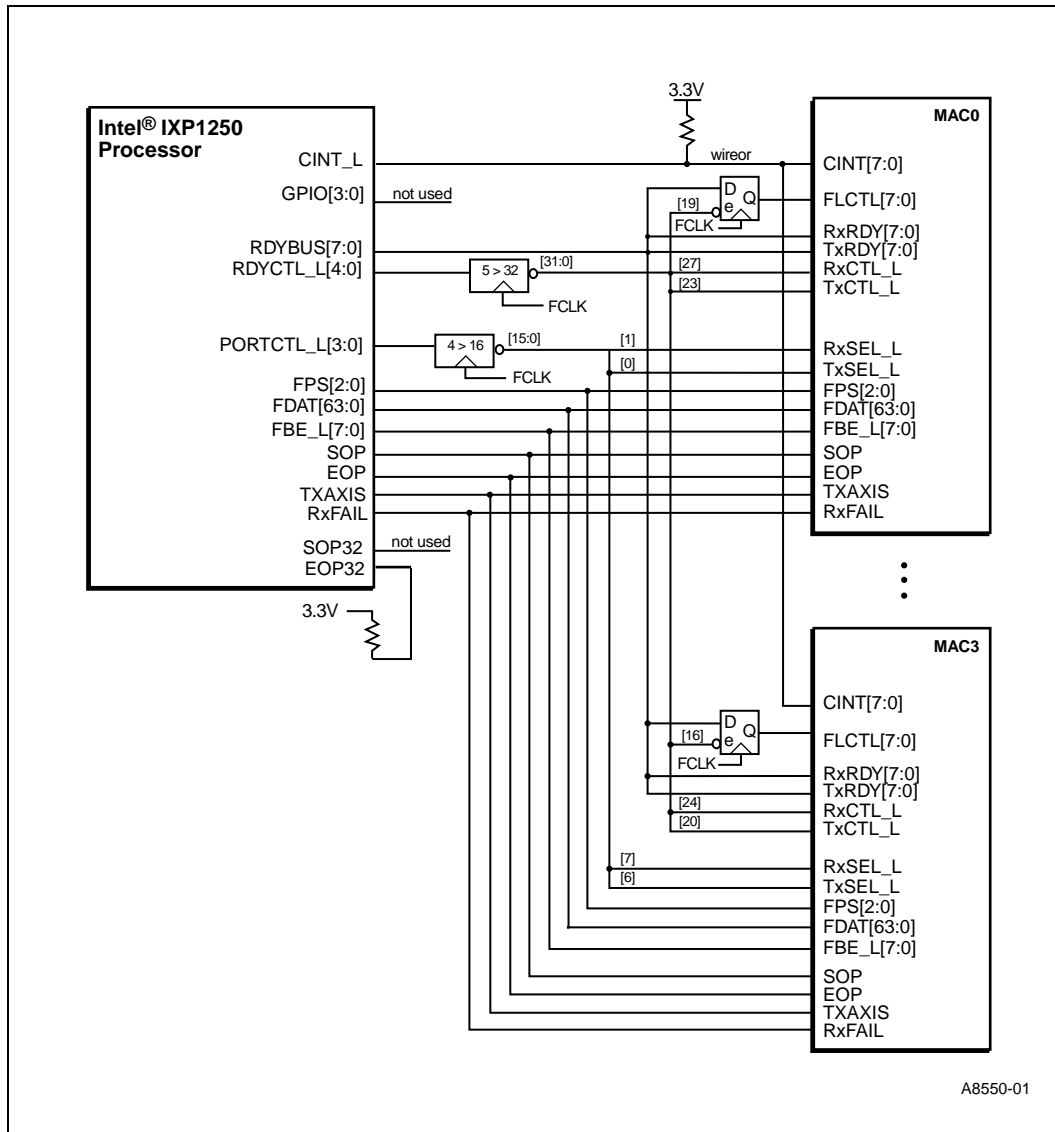
Figure 8. 64-Bit Bidirectional IX Bus, 1-2 MAC Mode, FastPort Device



**Table 25. 64-Bit Bidirectional IX Bus, 1-2 MAC Mode**

Signal	Description
GPIO[3:1]	Active High, input/output assigned to StrongARM* core not used for MAC interface.
GPIO[0]	Active Low, output flow-control enable for MAC 0.
RDYCTL_L[3:0]	Active Low, output, enables for Transmit or Receive Ready flags.
RDYCTL_L[4]	Active Low, output, flow-control enable for MAC 1.
RDYBUS[7:0]	Active High, input/output, Transmit or Receive Ready flags, and flow control mask data.
PORTCTL_L[3:0]	Active Low, output, transmit and receive device selects.
FPS[2:0]	Active High, output, port select.
SOP	Active High, input/output, Start of Packet indication. SOP is an output during transmit according to values programmed in the TFIFO control field. Is an input during receives indicating Receive Start of Packet from MAC.
EOP	Active High, input/output, End of Packet indication. EOP is an output during transmit according to values programmed in the TFIFO control field. Is an input during receives indicating Receive End of Packet from MAC.
TK_IN	Input, not used, must be pulled High in this mode.
TK_OUT	Output, not used, no connect.
RXFAIL	Active High, input/output. Input - Receive Error input. Output - driven low during transmit and when bus maintains a No-Select state.
TXAXIS	Active High, output. TXAXIS states are output according to values programmed in the TFIFO Control field. TXAXIS state is output coincident with SOP signal, TXERR state is output coincident with EOP signal.
FBE_L[7:0]	Active Low, byte enables for FDAT [64:0].
FDAT[63:0]	Active High, read and write data.
FAST_RX1	Active High ready input from FastPort 0, pulldown 10 KOHms to GND if not used.
FAST_RX2	Active High ready input from FastPort 1, pulldown 10 KOHms to GND if not used.

Figure 9. 64-Bit Bidirectional IX Bus, 3+ MAC Mode





**Table 26. 64-Bit Bidirectional IX Bus, 3+ MAC Mode  
(Shared IX Bus Operation Only in This Mode)**

Signal	Description
GPIO[3:1]	Active High input/output assigned to StrongARM* core not used for MAC interface.
GPIO[0]	Active High, output assigned to StrongARM* core not used for MAC interface.
RDYCTL_L[4:0]	Output, 5 bits encoded for Transmit/Receive ready flags, flow-control, and inter-chip communication in shared IX Bus mode. Shared IX Bus mode, Initial Ready Bus master drives RDYCTL_L[4:0] and Ready Bus slave snoops.
RDYBUS[7:0]	Active High, input/output, Transmit or Receive Ready flags, flow control mask data, and inter-processor communication in shared IX Bus mode.
PORTCTL_L[3:0]	Active Low, output, 4 bits encoded for transmit and receive commands and device selects. Shared IX Bus mode - Tri-stated when the IXP1250 does not own the IX Bus.
FPS[2:0]	Active High, output, port select. Shared IX Bus mode - Tri-stated when the IXP1250 does not own the IX Bus.
SOP	Active High, input/output, Start of Packet indication. SOP is an output during transmit according to values programmed in the TFIFO control field. Shared IX Bus mode - Tri-stated when the IXP1250 does not own the IX Bus.
TK_REQ_OUT/	Active High, output. Single chip mode - not used, no connect. Shared IX Bus mode - IX Bus Request.
EOP/	Active High, input/output, End of Packet indication. EOP is an output during transmit according to values programmed in the TFIFO control field. Is an input during receives indicating Receive End of Packet from MAC. Shared IX Bus mode - Tri-stated when the IXP1250 does not own the IX Bus.
TK_IN	Input in Shared IX Bus mode. Single chip mode - pullup through 10 KOHms to VDDX. Shared IX Bus mode - Token_Input, enables IX Bus ownership when a high-to-low transition is detected. At reset, pull down through 10 KOHms to GND to tell the IXP1250 that it does not own the IX Bus, pull up through 10 KOHms to VDDX to set as initial IX Bus owner.
TK_OUT	Active High, output. Single chip mode - output, not used, no connect. Shared IX Bus mode - Token_Output. When high, indicates this IXP1250 owns the IX Bus.
RXFAIL	Active High, input/output. Input - Receive Error input. Output - driven low during transmit and when bus maintains a No-Select state. Shared IX Bus mode - Tri-stated when the IXP1250 does not own the IX Bus.
TXASIS	Active High, output. TXASIS states are output according to values programmed in the TFIFO Control field. TXASIS state is output coincident with SOP signal. Shared IX Bus mode - Tri-stated when the IXP1250 does not own the IX Bus.
FBE_L[7:0]	Active Low, byte enables for FDAT [64:0]. Tri-stated in shared IX Bus Mode when the IXP1250 does not own the IX Bus.
FDAT[63:0]	Active High, read and write data. Tri-stated in shared IX Bus mode when the IXP1250 does not own the IX Bus.

**Table 26. 64-Bit Bidirectional IX Bus, 3+ MAC Mode  
(Shared IX Bus Operation Only in This Mode) (Continued)**

Signal	Description
FAST_RX1	Active High ready input from FastPort 0, pulldown 10 KOhms to GND if not used.
FAST_RX2	Active High ready input from FastPort 1, pulldown 10 KOhms to GND if not used.
<b>Shared IX Bus Operation Signals</b> These signals are driven by the IXP1250 IX Bus owner, and are tri-stated when the IXP1250 does not own the IX Bus: PORTCTL_L[3:0] FPS[2:0] FDAT[63:0] FBE_L[7:0] TXASIS RXFAIL SOP EOP	

Figure 10. 32-Bit Unidirectional IX Bus, 1-2 MAC Mode

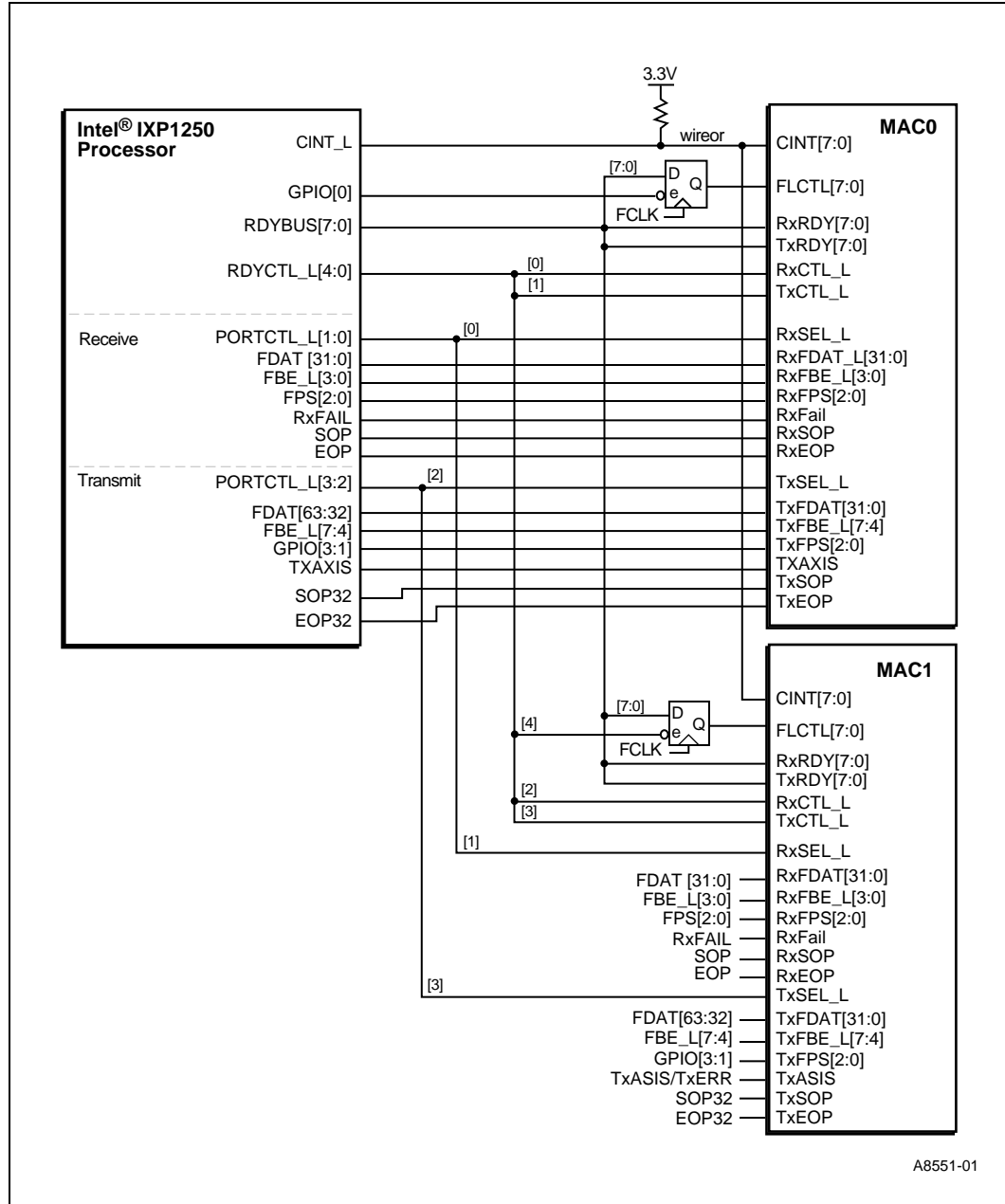
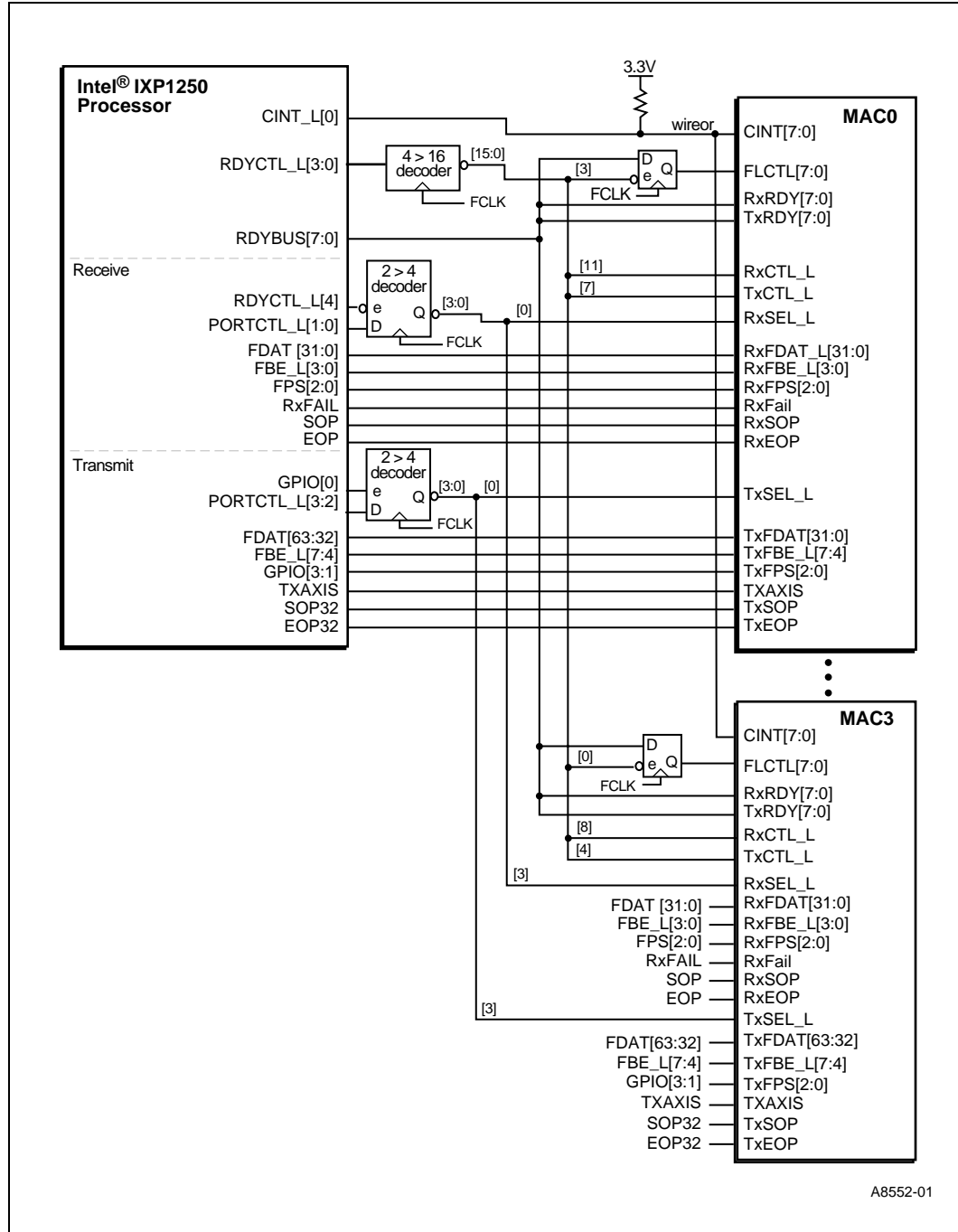


Table 27. 32-Bit Unidirectional IX Bus, 1-2 MAC Mode

Transmit Path Signals	Description
GPIO[3:1]	Active high outputs, Transmit Port Select [2:0].
PORTCTL_L[3:2]	Active Low, output. Transmit Device Selects [1:0].
TXASIS	Active High, output. TXASIS states are output according to values programmed in the TFIFO Control field. TXASIS state is output coincident with SOP32 signal.
FBE_L[7:4]	Active Low, output, byte enables for FDAT [63:31].
FDAT[63:31]	Active High, output, 32-bit transmit data.
<b>Receive Path Signals</b>	
FPS[2:0]	Active High, output. Receive Port Selects [2:0].
PORTCTL_L[1:0]	Active Low, output. Receive Device Selects [1:0].
SOP	Active High, input/output. Driven as output when bus remains in No-Select state.
EOP	Active High, input/output. Driven as output when bus remains in No-Select state.
RXFAIL	Active High, input/output, input Receive Error indication from the MAC. Driven as output when bus remains in No-Select state.
FBE_L[3:0]	Active Low, input/output, input byte enables for FDAT [31:0] from the MAC. Driven as output when bus remains in No-Select state.
FDAT[31:0]	Active High, input/output, input 32-bit receive data from the MAC. Driven as output when bus remains in No-Select state.
<b>Control Signals Common to both Transmit/Receive Paths</b>	
GPIO[0]	Active Low, output, flow-control for MAC 0.
RDYCTL_L[4]	Active Low, output, flow-control for MAC 1.
RDYCTL_L[3:0]	Active Low enable outputs for Transmit or Receive Ready flags.
RDYBUS[7:0]	Active High, input/output, Transmit or Receive Ready flags, and flow control mask data.
TK_IN	Input, not used, must be pulled High in this mode.
TK_OUT	Output, not used, no connect.
FAST_RX1	Active High, ready input from Fast Port 0, pulldown 10 KOhms if not used.
FAST_RX2	Active High, ready input from Fast Port 1, pulldown 10 KOhms if not used.

Figure 11. 32-bit Unidirectional IX Bus, 3+ MAC Mode (3-4 MACs Supported)



A8552-01

Table 28. 32-bit Unidirectional IX Bus, 3+ MAC Mode

Transmit Path Signals	Description
GPIO[3:1]	Active high outputs, Transmit Port Selects [2:0].
PORTCTL_L[3:2]	Active Low, outputs. Used with GPIO[0] for transmit device select via external 2-to-4 decoder.
GPIO[0]	Active High, output, transmit enable. Used with PORTCTL_L[3:2] for transmit device select via external 2-to-4 decoder.
TXAXIS	Active High, output. TXAXIS states are output according to values programmed in the TFIFO Control field. TXASIS state is output coincident with SOP32 signal, TXERR state is output coincident with EOP32EOP32 signal.
FBE_L[7:4]	Active Low, output, byte enables for FDAT [63:31].
FDAT[63:31]	Active High, output, 32-bit transmit data.
<b>Receive Path Signals</b>	
FPS[2:0]	Active High, output. Receive Port Selects [2:0].
PORTCTL_L[1:0]	Active Low, output. Used with RDYCTL_L[4] for receive device select via external 2-to-4 decoder.
RDYCTL_L[4]	Active Low, output, receive enable. Used to enable an external 2-to-4 decoder. Used with PORTCTL_L[1:0].
SOP	Active High, input/output, input receive Start of Packet from the MAC. Driven as output when bus remains in No-Select state.
EOP	Active High, input/output, input receive End of Packet from the MAC. Driven as output when bus remains in No-Select state.
RXFAIL	Active Low, input/output, input Receive Error indication from the MAC. Driven as output when bus remains in No-Select state.
FBE_L[3:0]	Active High, input/output, input byte enables for FDAT [31:0] from the MAC. Driven as output when bus remains in No-Select state.
FDAT[31:0]	Active High, input/output, input 32-bit receive data from the MAC. Driven as output when bus remains in No-Select state.
<b>Control Signals Common to both Transmit/Receive Paths</b>	
RDYCTL_L[3:0]	Output, 4 bits encoded for Transmit/Receive Ready flags, flow-control, and inter-chip communication. Decode with external 4-to-16 decoder.
RDYBUS[7:0]	Active High, input/output, Transmit or Receive Ready flags, and flow control mask data.
TK_IN	Input, not used, must be pulled High in this mode.
TK_OUT	Output, not used, no connect.
FAST_RX1	Active High, ready input from Fast Port 0, pulldown 10 KOhms if not used.
FAST_RX2	Active High, ready input from Fast Port 1, pulldown 10 KOhms if not used.

### 3.7 IX Bus Decode Table Listed by Operating Mode Type

**Table 29. IX Bus Decode Table Listed by Operating Mode Type**

PIN NAME	64-bit Bidirectional 1-2 MAC mode	64-bit Bidirectional 3+ MAC mode	32-bit Unidirectional 1-2 MAC mode	32-bit Unidirectional 3+ MAC mode
PORTCTL_L[3:0]	1110 MAC0 RxSEL 1101 MAC1 RxSEL 1011 MAC0 TxSEL 0111 MAC1 TxSEL 1111 No Select	0000 MAC0 TxSEL 0001 MAC0 RxSEL 0010 MAC1 TxSEL 0011 MAC1 RxSEL 0100 MAC2 TxSEL 0101 MAC2 RxSEL 0110 MAC3 TxSEL 0111 MAC3 RxSEL 1000 MAC4 TxSEL 1001 MAC4 RxSEL 1010 MAC5 TxSEL 1011 MAC5 RxSEL 1100 MAC6 TxSEL 1101 MAC6 RxSEL 1110/1111 No Select	1110 MAC0 RxSel 1101 MAC1 RxSel 1011 MAC0 TxSel 0111 MAC1 TxSel 1010 MAC0 TxSel/ MAC0 RxSel 0110 MAC1 TxSel/ MAC0 RxSel 1001 MAC0 TxSel/ MAC1 RxSel 0101 MAC1 TxSel/ MAC1 RxSel	If RDYCTL_L[4] = 0 XX00 MAC0 RxSEL XX01 MAC1 RxSEL XX10 MAC2 RxSEL XX11 MAC3 RxSEL <hr/> If RDYCTL_L[4] = 1 No Select <hr/> If GPIO[0]/ FC_EN0_L/ TXPEN = 1 00XX MAC0 TxSEL 01XX MAC1 TxSEL 10XX MAC2 TxSEL 11XX MAC3 TxSEL <hr/> If GPIO[0]/ FC_EN0_L/ TXPEN = 0 No Select
FPS[2:0]	Rx/Tx Port Select	Rx/Tx Port Select	Rx Port Select	Rx Port Select
GPIO[3:1]	Not used	Not used	Tx Port Select	Tx Port Select
GPIO[0]/ FC_EN0_L/ TXPEN	MAC0 Flw Ctl enable when low	Not used	MAC0 Flw Ctl enable when low	PORTCTL_L[3:2] Tx enable (see above)
FDAT[63:32]	Rx/Tx Data	Rx/Tx Data	Tx Data	Tx Data
FDAT[31:0]	Rx/Tx Data	Rx/Tx Data	Rx Data	Rx Data
FBE_L[7:4]	Rx/Tx Byte Enables	Rx/Tx Byte Enables	Tx Byte Enables	Tx Byte Enables
FBE_L[3:0]	Rx/Tx Byte Enables	Rx/Tx Byte Enables	Rx Byte Enables	Rx Byte Enables
SOP	Rx/Tx SOP	Rx/Tx SOP	Rx SOP	Rx SOP
EOP	Rx/Tx EOP	Rx/Tx EOP	Rx EOP	Rx EOP
TK_REQ_OUT/ SOP_TX	Not used	Not used	Tx SOP	Tx SOP

Table 29. IX Bus Decode Table Listed by Operating Mode Type (Continued)

PIN NAME	64-bit Bidirectional 1-2 MAC mode	64-bit Bidirectional 3+ MAC mode	32-bit Unidirectional 1-2 MAC mode	32-bit Unidirectional 3+ MAC mode
EOP/EOP_TX	Not used	Not used	Tx EOP	Tx EOP
RDYCTL_L[4]	MAC1 Flw Ctl enable when low	Ready Control (see below)	MAC1 Flw Ctl enable when low	PORTCTL_L[1:0] Rx enable (see above)
RDYCTL_L[4:0]	x1111 NOP x1110 MAC0 Rx x1101 MAC0 Tx x1011 MAC1 Rx x0111 MAC1 Tx	11111 NOP 11110 GET 1 11100 autopush  11011 MAC0 Rx 11010 MAC1 Rx 11001 MAC2 Rx 11000 MAC3 Rx  10111 MAC0 Tx 10110 MAC1 Tx 10101 MAC2 Tx 10100 MAC3 Tx  10011 MAC0 Flw Ctl enable 10010 MAC1 Flw Ctl enable 10001 MAC2 Flw Ctl enable 10000 MAC3 Flw Ctl enable  01110 GET 2 01101 SEND  01011 MAC4 Rx 01010 MAC5 Rx 01001 MAC6 Rx 00111 MAC4 Tx 00110 MAC5 Tx 00101 MAC6 Tx  00011 MAC4 Flw Ctl enable 00010 MAC5 Flw Ctl enable 00001 MAC6 Flw Ctl enable	x1111 NOP x1110 MAC0 Rx x1101 MAC0 Tx x1011 MAC1 Rx x0111 MAC1 Tx	x1111 NOP x1110 GET 1 x1101 SEND x1100 autopush  x1011 MAC0 Rx x1010 MAC1 Rx x1001 MAC2 Rx x1000 MAC3 Rx  x0111 MAC0 Tx x0110 MAC1 Tx x0101 MAC2 Tx x0100 MAC3 Tx  x0011 MAC0 Flw Ctl enable x0010 MAC1 Flw Ctl enable x0001 MAC2 Flw Ctl enable x0000 MAC3 Flw Ctl enable



## 3.8 Pin State During Reset

Table 30 summarizes IXP1250 pin states during reset.

**Table 30. Pin State During Reset**

Function	Pin Name	Pin Reset State	Comment
SRAM	SCLK	output, low	
SRAM	A[17:0]	output, low	
SRAM	DQ[31:0]	output, low	
SRAM	CE_L[3:0]	output, high	
SRAM	SLOW_EN_L	output, high	
SRAM	SOE_L	output, high	
SRAM	SWE_L	output, high	
SRAM	HIGH_EN_L	output, high	
SRAM	LOW_EN_L/DIRW_L	output, high	
SRAM	MRD_L	output, high	
SRAM	MCE_L	output, high	
SRAM	FWE_L	output, high	
SRAM	NA/SACLK	input	
SDRAM	SDCLK	active clock output	
SDRAM	MADR[14:0]	output, low	
SDRAM	MDATA[63:0]	output, low	
SDRAM	MDATA_ECC[7:0]	output, low	
SDRAM	CAS_L	output, high	
SDRAM	DQM	output, high	
SDRAM	RAS_L	output, high	
SDRAM	WE_L	output, high	
PCI	PCI_CLK	input	
PCI	AD[31:0]	PCI_CFN[1:0]=00, AD[31:0]=Hi-Z PCI_CFN[1:0]=11 AD[31:0]=output, low	
PCI	CBE_L[3:0]	PCI_CFN[1:0]=00, CBE_L[3:0]=Hi-Z PCI_CFN[1:0]=11 CBE_L[3:0]=output, low	
PCI	FRAME_L	Hi-Z	
PCI	IRDY_L	Hi-Z	
PCI	PAR	PCI_CFN[1:0]=00, PAR=Hi-Z PCI_CFN[1:0]=11 PAR=output, low	
PCI	IDSEL	Hi-Z	

Table 30. Pin State During Reset (Continued)

Function	Pin Name	Pin Reset State	Comment
PCI	PCI_CFN[0]	input	
PCI	PCI_CFN[1]	input	
PCI	PCI_IRQ_L	Hi-Z	
PCI	PCI_RST_L	PCI_CFN[1:0]=00, PCI_RST=Hi-Z PCI_CFN[1:0]=11, PCI_RST=output, low	
PCI	PERR_L	Hi-Z	
PCI	SERR_L	Hi-Z	
PCI	STOP_L	Hi-Z	
PCI	DEVSEL_L	Hi-Z	
PCI	TRDY_L	Hi-Z	
PCI	GNT_L[1:0]	PCI_CFN[1:0]=00, GNT_L[1:0]=Hi-Z PCI_CFN[1:0]=11, GNT_L[1:0]=output, high	
PCI	REQ_L[1:0]	Hi-Z	
IX Bus	FCLK	input	
IX Bus	FDAT[63:0]	output, high	
IX Bus	FBE_L[7:4]	output, high	
IX Bus	FBE_L[3:0]	output, high	
IX Bus	FPS[2:0]	output, high	
IX Bus	TXASIS	output, high	
IX Bus	PORTCTL_L[3:0]	output, high	
IX Bus	FAST_RX1	input	
IX Bus	FAST_RX2	input	
IX Bus	RDYBUS[7:0]	output, high	
IX Bus	RDYCTL_L[3:0]	output, high	
IX Bus	RDYCTL_L[4]	output, high	
IX Bus	EOP	output, high	
IX Bus	SOP	output, high	
IX Bus	RXFAIL	output, high	
IX Bus	TK_IN	input	drive or pullup high to select initial owner
IX Bus	TK_OUT	Hi-Z	
IX Bus	GPIO[3]	input	
IX Bus	GPIO[2]	input	
IX Bus	GPIO[1]	input	
IX Bus	GPIO[0]	input	
Misc Test	TCK_BYP	input	

**Table 30. Pin State During Reset (Continued)**

Function	Pin Name	Pin Reset State	Comment
Misc Test	TSTCLK	input	
Misc Test	SCAN_EN	input	
Processor Support	PXTAL	input	
Processor Support	CINT_L	input	
Processor Support	RESET_IN_L	input	
Processor Support	RESET_OUT_L	output, low	
Serial	RXD	input	
Serial	TXD	output, high	
IEEE 1149.1	TCK	input	
IEEE 1149.1	TDI	input	
IEEE 1149.1	TDO	output, undefined	
IEEE 1149.1	TMS	input	
IEEE 1149.1	TRST_L	input	

### 3.9 Pullup/Pulldown and Unused Pin Guidelines

For normal (i.e., non-test mode) operation, terminate signals as follows:

- Pullup these signals to VDDX: TMS, TDI.
- TCK may be pulled up to VDDX or down to VSSX at the system designer's option.
- Pulldown these signals to VSS: SCAN\_EN, TCK\_BYP, TRST\_L.
- Pullup this signal to VDDX or pulldown to VSS; do not allow it to float: TSTCLK.
- GPIO[3:1] and GPIO[0] are tri-stated during reset. If these signals are used to drive external logic, pullup or pulldown as appropriate to ensure valid logic levels during reset.

Terminate unused signals as follows:

- Pullup these signals to VDDX: GNT\_L[1], TK\_IN, EOP32.
- Pulldown these signals to VSS: NA/SACLK, FAST\_RX1, FAST\_RX2.

For shared IX Bus operation, it is recommended to pullup PORTCTL\_L[3:0] and, additionally, FPS[2:0] and TXAXIS at the designer's discretion.

Typical pullup/pulldown resistor values are in the range of 5-10 KOhms.

## 4.0 Electrical Specifications

This chapter specifies the following electrical behavior of the IXP1250:

- Absolute maximum ratings.
- DC specifications.
- AC timing specifications for the following signal interfaces:
  - PXTAL Clock input.
  - PCI Bus Interface.
  - IX Bus Interface.
  - Ready Bus Interface.
  - TK\_OUT/TK\_IN signals.
  - SRAM interface.
  - SDRAM Interface.
  - Reset signals.
  - GPIO signals.
  - IEEE 1149.1 Interface.
  - Serial Port signals.

### 4.1 Absolute Maximum Ratings

The IXP1250 is specified to operate at a maximum Core frequency ( $F_{\text{core}}$ ) of 232 MHz at a junction temperature ( $T_j$ ) not to exceed 100°C for commercial temperature, and at a maximum Core frequency ( $F_{\text{core}}$ ) of 166 MHz and 105°C for extended temperature. [Table 31](#) lists the absolute maximum ratings for the IXP1250. These are stress ratings only; stressing the device beyond the absolute maximum ratings may cause permanent damage. Operating beyond the functional operating range ([Table 32](#)) is not recommended and extended exposure beyond the functional operating range may affect reliability.

Under all operating conditions, the 3.3 V to 2.0 V supply voltage difference ( $V_{\text{delta}}$ ) must not be exceeded or permanent damage to the device may result.

**Table 31. Absolute Maximum Ratings**

Parameter	Minimum	Maximum	Comment
Junction temperature (Commercial), $T_j$	---	100°C	166 MHz, 200 MHz, and 232 MHz
Junction temperature (Extended Temperature), $T_j$	---	105°C	166 MHz only
Maximum voltage applied to signal pins		3.6 V	
Supply voltage (Core and PLL), VDD, VDDP1	1.9 V	2.1 V	2 V supply

**Table 31. Absolute Maximum Ratings**

Parameter	Minimum	Maximum	Comment
Supply voltage (I/O), VDDX, VDDREF	3.0 V	3.6 V	3.3 V supply
Storage temperature range	-55°C	125°C	
V <sub>delta</sub>	0.0 V	1.8 V	(VDDX - VDD) or (VDDX - VDDP1)

The power specifications listed below are based on the following assumption:

- PCI Bus Frequency (PCI\_CLK) = 66 MHz.

**Table 32. Functional Operating Range**

Parameter	Minimum	Maximum	Comment
Commercial temperature operating range (166 MHz, 200 MHz, and 232 MHz)	0°C	70°C	Tjmax to be managed to stay below 100°C. (see the Heatsink application in <a href="#">Figure 12</a> ).
Extended temperature operating range (166 MHz only)	-40°C	85°C	Tjmax to be managed to stay below 105°C. (see the Heatsink application in <a href="#">Figure 12</a> ).
Supply voltage (Core and PLL), VDD, VDDP1	1.9 V	2.1 V	2.0 V +/- 5%
Supply voltage (I/O), VDDX, VDDREF (Commercial temperature)	3.0 V	3.6 V	3.3 V +/- 10%
Supply voltage (I/O), VDDX, VDDREF (Extended temperature)	3.15 V	3.45 V	3.3 V +/- 5%

**Table 33. Typical and Maximum Power**

Parameter	Commercial Temperature Core Freq/IX Bus Freq 166 MHz/66 MHz		Extended Temperature Core Freq/IX Bus Freq 166 MHz/66 MHz		Commercial Temperature Core Freq/IX Bus Freq 200 MHz/85 MHz		Commercial Temperature Core Freq/IX Bus Freq 232 MHz/104 MHz	
	Typical <sup>1,2</sup>	Maximum <sup>1</sup>	Typical <sup>1,2</sup>	Maximum <sup>1</sup>	Typical <sup>1,2</sup>	Maximum <sup>1</sup>	Typical <sup>1,2</sup>	Maximum <sup>1</sup>
2.0 V supply	3.3 W	4.8 W	3.2 W	3.7 W	3.9 W	5.4 W	4.5 W	5.9 W
3.3 V supply	0.5 W	1.2 W	0.6 W	0.9 W	0.58 W	1.2 W	0.69 W	0.8 W
Total Power	3.80 W	6.0 W	3.80 W	4.6 W	4.48 W	6.6 W	5.19 W	6.7 W

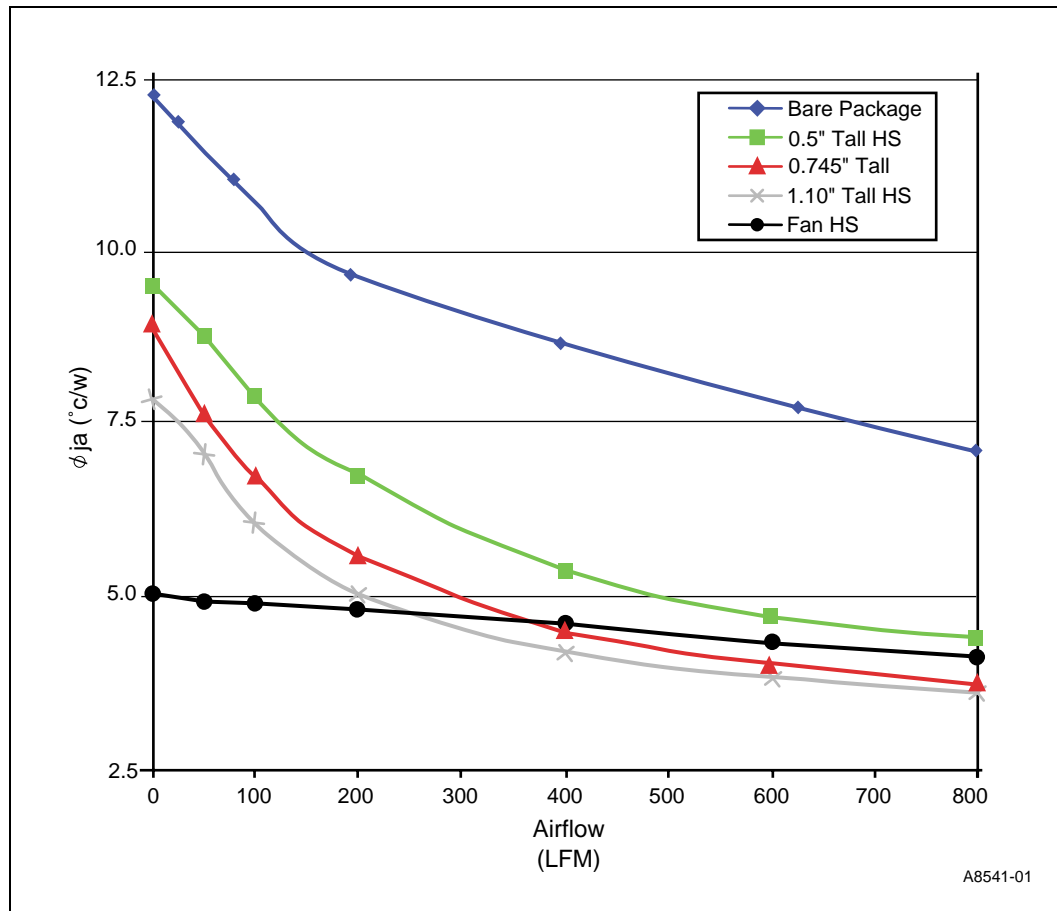
1. Typical and maximum power specifications are based upon the bus loading shown in [Table 34](#).
2. Typical power measured at nominal supply voltages.

**Table 34. Maximum and Typical Bus Loading Used for the Power Calculations<sup>1</sup>**

	Maximum Power Load for Core Freq/ IX Bus Freq 166 MHz/66 MHz (Commercial Temperature)	Maximum Power Load for Core Freq/ IX Bus Freq 166 MHz/66 MHz (Extended Temperature)	Maximum Power Load for Core Freq/ IX Bus Freq 200 MHz/85 MHz (Commercial Temperature)	Maximum Power Load for Core Freq/ IX Bus Freq 232 MHz/104 MHz (Commercial Temperature)	Typical Power Load for IX Bus Frequency $\leq 85$ MHz (Commercial Temperature)
SDRAM Bus	8	5	8	5	5
SRAM Bus	8	5	8	5	5
IX Bus	7	4	4	1	2

1. A load is defined as input capacitance equivalent to a CMOS gate + minimal trace length capacitance, typically 8 pF. The customer is responsible for managing the signal integrity and external power issues that occur with increased IXP1200 Bus loading in their application to ensure reliable system operation.

**Figure 12. Typical IXP1250 Heatsink Application**



**Note:** The heat sink comparison shown in Figure 12 was tested on an IXP1250 Network Processor package mounted on a 4 inch-by-4 inch test board.

**Note:** Refer to the IXP1250 Network Processor Heatsinks:  $\theta_{ja}$  and Airflow - Application Note for additional information on heatsinks and thermal management.

## 4.2 DC Specifications

The IXP1250 supports two fundamental I/O buffer Types: Type 1 and Type 2. The Pin Description section defines which pins use which I/O buffer type. The driver characteristics are described in the following sections. Please note that IXP1250 input pins are not 5 V tolerant. Devices driving the IXP1250 must provide 3.3 V signal levels or use level shifting buffers to provide 3.3 V compatible levels, otherwise damage to the device will result.

The Type 1 pins are 3.3 V Low Voltage TTL compatible I/O buffers. There are three versions of the Type 1 driver that differ by the maximum available driver current.

The Type 2 pins are 3.3 V I/O buffers (supporting *PCI Local Bus Specification, Revision 2.2*).

### 4.2.1 Type 1 Driver DC Specifications

Table 35 refers to pin types: I1, O1, O3, O4, O5.

**Table 35. I1, I3, O1, O3, O4, and O5 Pin Types**

Symbol	Parameter	Condition	Minimum	Maximum
V <sub>ih</sub>	Input High Voltage		2.0 V	---
V <sub>il</sub>	Input Low Voltage		---	0.8 V
V <sub>oh</sub>	Output High Voltage	O1: I <sub>oh</sub> = -2 mA O3: I <sub>oh</sub> = -8 mA O4: I <sub>oh</sub> = -4 mA O5: I <sub>oh</sub> = -4 mA	2.4 V	-
V <sub>ol</sub>	Output Low Voltage	O1: I <sub>ol</sub> = 2 mA O3: I <sub>ol</sub> = 8 mA O4: I <sub>ol</sub> = 4 mA O5: I <sub>ol</sub> = 4 mA	---	0.4 V
I <sub>i</sub>	Input Leakage Current <sup>1</sup>	0 ≤ V <sub>in</sub> ≤ VDDX	-10 μA	10 μA
C <sub>in</sub>	Pin Capacitance	-	4 pF	10 pF

1. Input leakage currents include high impedance output leakage for all bidirectional buffers with tri-state outputs.

## 4.2.2 Type 2 Driver DC Specifications

Table 36 refers to pin types: I2, O2.

**Table 36. I2 and O2 Pin Types**

Symbol	Parameter	Condition	Minimum	Maximum
$V_{ih}$	Input High Voltage		$0.5 \times VDDX$	$VDD\_REF + 0.5 \text{ V}$
$V_{il}$	Input Low Voltage		---	$0.3 \times VDDX$
$V_{oh}$	Output High Voltage	$I_{oh} = -500 \text{ uA}$	$0.9 \times VDDX$	---
$V_{ol}$	Output Low Voltage	$I_{ol} = 1500 \text{ uA}$	---	$0.1 \times VDDX$
$I_i$	Input Leakage Current <sup>1</sup>	$0 \leq V_{in} \leq VDDX$	$-10 \text{ }\mu\text{A}$	$10 \text{ }\mu\text{A}$
$C_{in}$	Pin Capacitance		$5 \text{ pF}$	$10 \text{ pF}$

1. Input leakage currents include high impedance output leakage for all bidirectional buffers with tri-state outputs.

**Note:** In Table 35 and Table 36, currents into the chip (chip sinking) are denoted as positive(+) current. Currents from the chip (chip sourcing) are denoted as negative(-) current. Input leakage currents include high-Z output leakage for all bidirectional buffers with tri-state outputs. The electrical specifications are preliminary and subject to change.

## 4.2.3 Overshoot/Undershoot Specifications

The IXP1250 has been designed to be tolerant of overshoot and undershoot associated with normal I/O switching. However, excessive overshoot or undershoot of I/O signals can cause the device to latchup. Table 37 specifies limits on I/O overshoot and undershoot that should never be exceeded.

**Table 37. Overshoot/Undershoot Specifications**

Pin Type	Undershoot	Overshoot	Maximum Duration
I1/O1	-0.75 V	$VDDX + 0.7 \text{ V}$	4 ns
I2/O2	-0.7 V	$VDDX + 0.65 \text{ V}$	4 ns
O3	-0.7 V	$VDDX + 0.6 \text{ V}$	4 ns
O4	-0.75 V	$VDDX + 1.0 \text{ V}$	4 ns
O5	-0.7 V	$VDDX + 0.65 \text{ V}$	4 ns



## 4.3 AC Specifications

### 4.3.1 Clock Timing Specifications

The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain within the IXP1250.

For example, Figure 14 shows the ac parameter measurements for the PCI\_CLK signal, and Table 39 and Table 40 specify parameter values for clock signal ac timing. See also Figure 15 for a further illustration of signal timing. Unless otherwise noted, all ac parameters are guaranteed when tested within the functional operating range of Table 32.

Unless otherwise indicated, all ac output delays are measured with a 5 pF load. Capacitive deratings are provided for all output buffers.

### 4.3.2 PXTAL Clock Input

Figure 13. PXTAL Clock Input

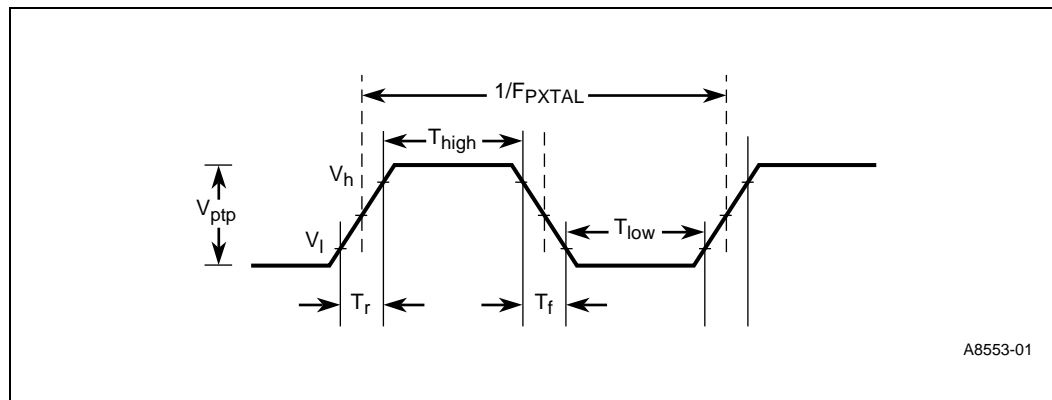


Table 38. PXTAL Clock Inputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$F_{pxtal}$	Clock frequency	3.5795	3.6864	3.7878	MHz
$V_{ptp}$	Clock peak to peak	$0.6 \cdot V_{DDX}$		---	V
$V_{high}$	Clock high threshold	2.0		---	V
$V_{low}$	Clock low threshold	---		0.8	V
	Clock slew rate <sup>1</sup>	1		4	V/ns
$F_{core}$	Core frequency <sup>2,3,4</sup>		165.89		MHz

1. Not tested. Guaranteed by design.
2. Core frequency ( $F_{core}$ ) of 165.89 MHz when register PLL\_CFG[4:0] = 10000b.
3. Core frequency ( $F_{core}$ ) of 166.67 MHz when register PLL\_CFG[4:0] = 01111b and  $F_{pxtal}$  = 3.7878 MHz. Refer to the *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* for a complete list of programmable frequencies.
4. Core frequency ( $F_{core}$ ) of 199.0656 MHz when register PLL\_CFG[4:0] = 10011b and  $F_{pxtal}$  = 3.6864 MHz. Refer to the *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* for a complete list of programmable frequencies..

### 4.3.3 PXTAL Clock Oscillator Specifications

Frequency:	$F_{\text{pxtal}} \pm 0.01\%$
Stability:	100 ppm
Voltage signal level:	3.3 Volts
Rise/fall time:	< 4 ns
Duty cycle:	40%-60%

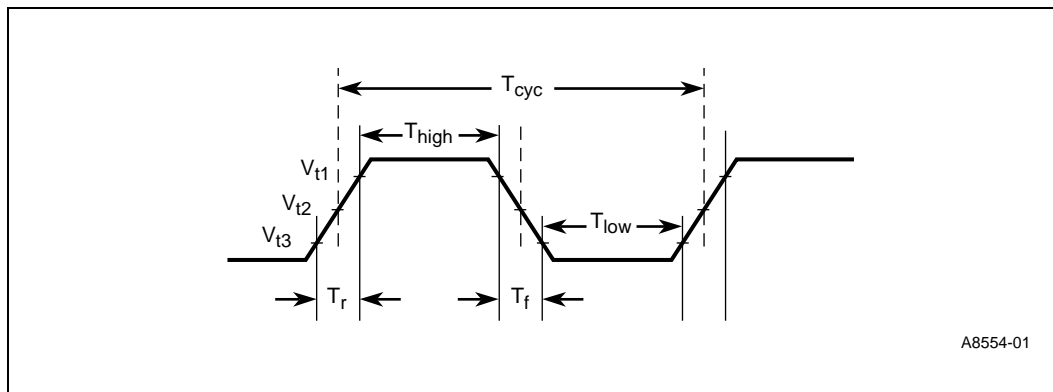
### 4.3.4 PCI

#### 4.3.4.1 PCI Electrical Specification Conformance

The IXP1250 PCI pins support the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.2*. See that document for a complete description of the PCI I/O protocol and pin ac specifications.

#### 4.3.4.2 PCI Clock Signal AC Parameter Measurements

Figure 14. PCI Clock Signal AC Parameter Measurements



$V_{t1} = 0.5 * V_{DDX}$   
 $V_{t2} = 0.4 * V_{DDX}$   
 $V_{t3} = 0.3 * V_{DDX}$

Table 39. 66 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
$T_{\text{cyc}}$	PCI_CLK cycle time	15	$\infty$	ns
$T_{\text{high}}$	PCI_CLK high time	6	---	ns
$T_{\text{low}}$	PCI_CLK low time	6	---	ns
	PCI_CLK slew rate <sup>1, 2</sup>	1.5	4	V/ns
	$F_{\text{core}}/\text{PCI Clock Ratio}$	2:1		

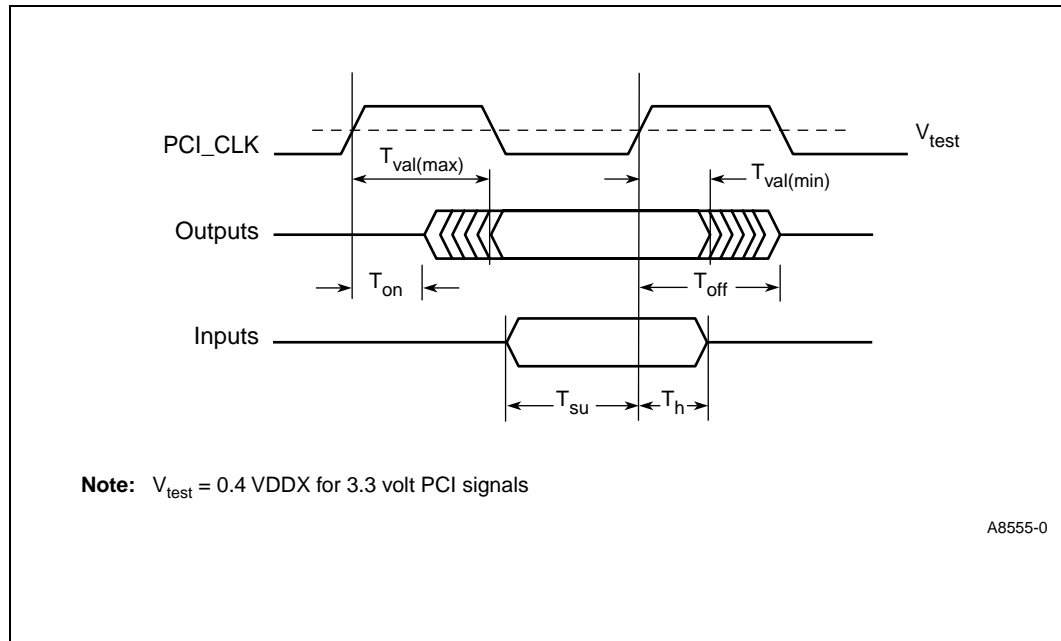
- 0.2 VDDX to 0.6 VDDX.
- Not tested. Guaranteed by design.

**Table 40. 33 MHz PCI Clock Signal AC Parameters**

Symbol	Parameter	Minimum	Maximum	Unit
$T_{cyc}$	PCI_CLK cycle time	30	$\infty$	ns
$T_{high}$	PCI_CLK high time	11	---	ns
$T_{low}$	PCI_CLK low time	11	---	ns
	PCI_CLK slew rate <sup>1 2</sup>	1	4	V/ns
	$F_{core}$ /PCI Clock Ratio	2:1		

- 1. 0.2 VDDX to 0.6 VDDX.
- 2. Not tested. Guaranteed by design.

**Figure 15. PCI Bus Signals**



### 4.3.4.3 PCI Bus Signals Timing

**Table 40. 33 MHz PCI Signal Timing**

Symbol	Parameter	Minimum	Maximum	Unit
$T_{val}^1$	CLK to signal valid delay, bused signals	1.5	11	ns
$T_{val}^1$ (point-to-point)	CLK to signal valid delay, point-to-point signals <sup>2</sup>	1.5	12	ns
$T_{on}^3$	Float to active delay	2	---	
$T_{off}^3$	Active to float delay	---	28	ns
$T_{su}$	Input setup time to CLK, bused signals <sup>2</sup>	7	---	ns
$T_{su}$ (point-to-point)	Input setup time to CLK, point-to-point signals <sup>4</sup>	10	---	ns
$T_h^1$	Input signal hold time from CLK	1	---	ns

1. These parameters are at variance with those in the *PCI Local Bus Specification, Revision 2.2*.

2. Point-to-point signals are REQ\_L, GNT\_L.

3. Not tested. Guaranteed by design.

4. Bused signals are AD, CBE\_L, PAR, PERR\_L, SERR\_L, FRAME\_L, IRDY\_L, TRDY\_L, DEVSEL\_L, STOP\_L.

**Table 41. 66 MHz PCI Signal Timing**

Symbol	Parameter	Minimum	Maximum	Unit
$T_{val}^1$	CLK to signal valid delay, bused signals	1.5	7	ns
$T_{val}^1$ (point-to-point)	CLK to signal valid delay, point-to-point signals <sup>2</sup>	1.5	7	ns
$T_{on}^3$	Float to active delay	2	---	
$T_{off}^3$	Active to float delay	---	6	ns
$T_{su}$	Input setup time to CLK, bused signals <sup>4</sup>	3	---	ns
$T_{su}$ (point-to-point)	Input setup time to CLK, point-to-point signals <sup>2</sup>	5	---	ns
$T_h^1$	Input signal hold time from CLK	1	---	ns

1. These parameters are at variance with those in the *PCI Local Bus Specification, Revision 2.2*.

2. Point-to-point signals are REQ\_L, GNT\_L.

3. Not tested. Guaranteed by design.

4. Bused signals are AD, CBE\_L, PAR, PERR\_L, SERR\_L, FRAME\_L, IRDY\_L, TRDY\_L, DEVSEL\_L, STOP\_L.

### 4.3.5 Reset

#### 4.3.5.1 Reset Timings Specification

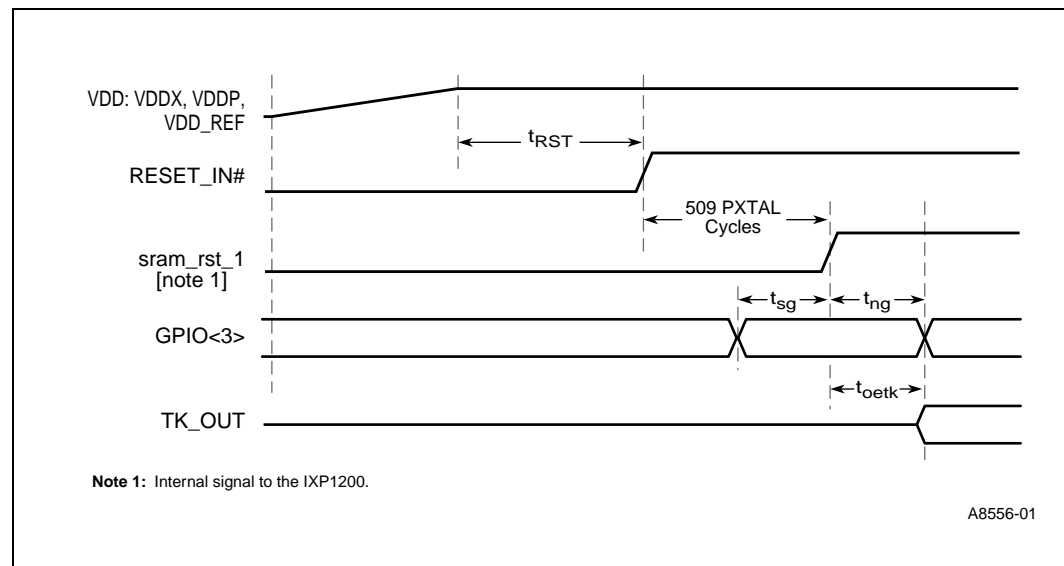
Table 42 shows the reset timing specifications for RESET\_IN\_L and RESET\_OUT\_L.

**Table 42. Reset Timings Specification**

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RST}$	RESET_IN_L asserted after power stable.	150	--	ms
$t_{SG}$	GPIO[3] setup to reset sample edge.	2		core_clk cycles <sup>1</sup>
$t_{HG}$	GPIO[3] hold from reset sample edge.	9		core_clk cycles <sup>1</sup>
$t_{OETK}$	TK_OUT hi-z to valid output.	4	7	core_clk cycles <sup>1</sup>

1. core\_clk is nominally running at 29.491 MHz after a hard reset when PXTAL is 3.6864 MHz.

**Figure 16. RESET\_IN\_L Timing Diagram**



### 4.3.6 IEEE 1149.1

The following pins are considered IEEE 1149.1 compliance pins:

RESET\_IN\_L  
PCI\_CLK  
SCAN\_EN  
TCK\_BYP  
TSTCLK

The following pins are not connected to the Boundary Scan ring:

RESET\_IN\_L  
PCI\_CLK  
SCAN\_EN  
TCK\_BYP  
TSTCLK  
TCK  
TMS  
TDI  
TDO  
TRST\_L

**Caution:** A clock signal must be applied to the core of the IXP1250 when using IEEE 1149.1 functions. The PXTAL clock input should be active, or, if using bypass mode, (TCK\_BYP = 1) TSTCLK should be active. Failure to observe this rule may cause device damage.

4.3.6.1 IEEE 1149.1 Timing Specifications

Figure 17. IEEE 1149.1/Boundary-Scan General Timing

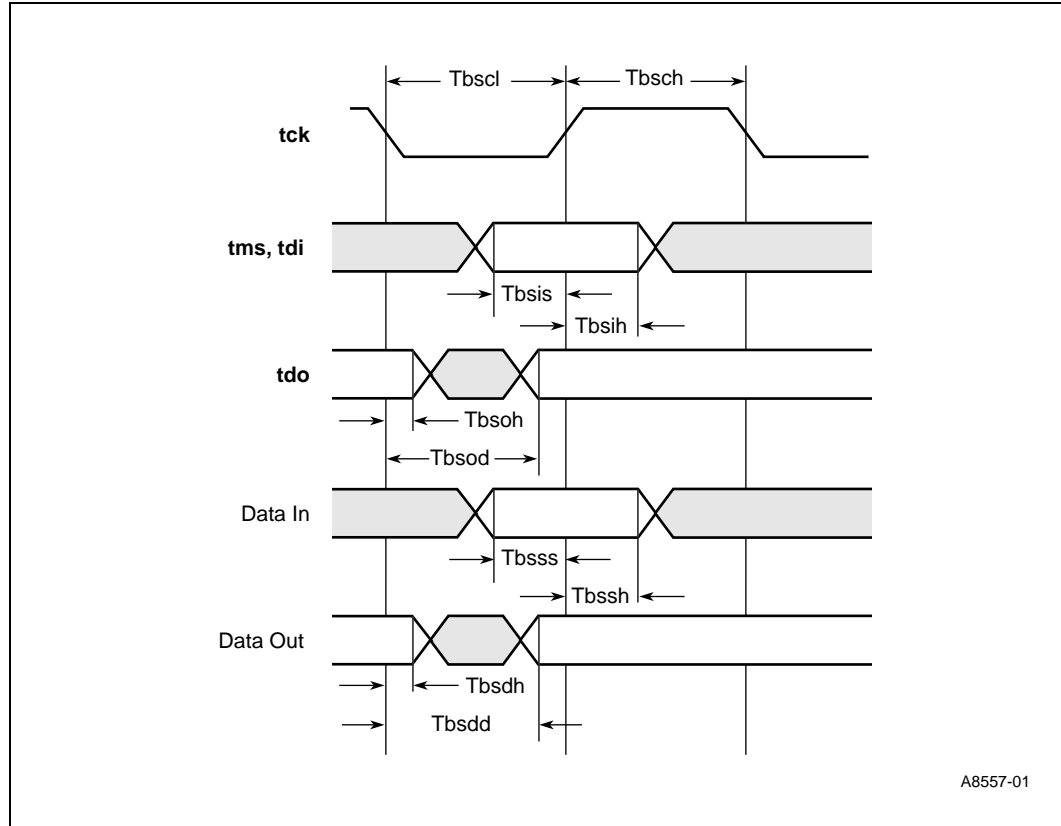


Figure 18. IEEE 1149.1/Boundary-Scan Tri-State Timing

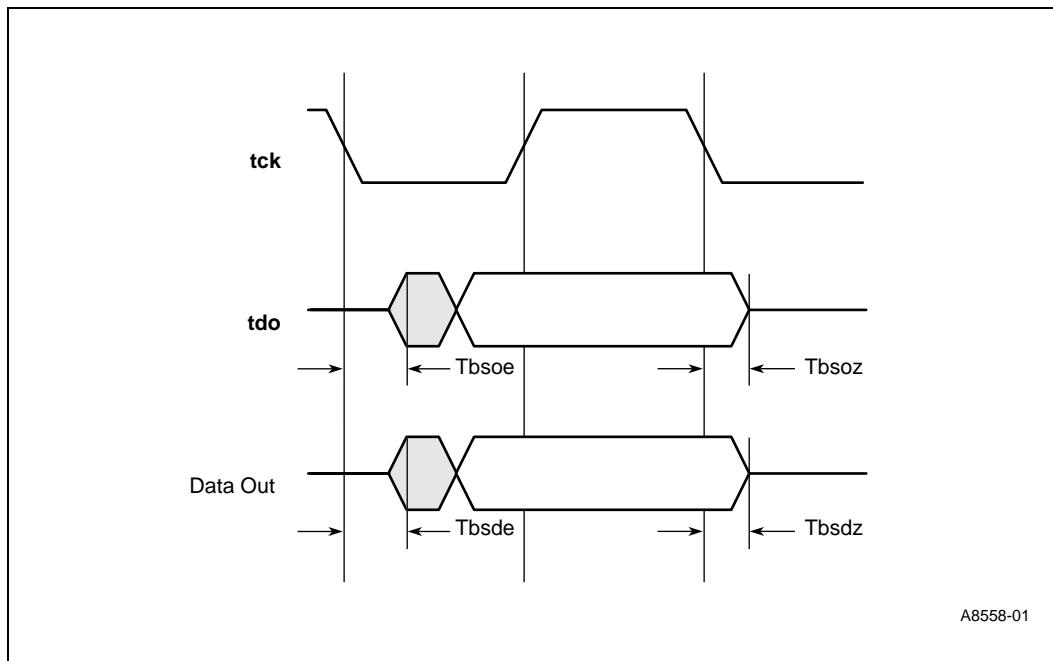


Table 43 shows the IEEE 1149.1/boundary-scan interface timing specifications.

Table 43. IEEE 1149.1/Boundary-Scan Interface Timing

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
Freq	TCK frequency		10		MHz	
$T_{bscl}$	TCK low period	–	50	–	ns	1
$T_{bsch}$	TCK high period	–	50	–	ns	1
$T_{bsis}$	TDI, TMS setup time	40	–	–	ns	–
$T_{bsih}$	TDI, TMS hold time	40	–	–	ns	–
$T_{bsod}$	TDO valid delay	20	–	30	ns	–
$T_{bsss}$	I/O signal setup time	40	–	–	ns	–
$T_{bssh}$	I/O signal hold time	40	–	–	ns	–
$T_{bsdd}$	Data output valid	20	–	30	ns	–
$T_{bsoe}^1, T_{bsoz}^1$	TDO float delay	5	–	40	ns	–
$T_{bsde}^1, T_{bsdz}^1$	Data output float delay	5	–	40	ns	–
$T_{bsr}$	Reset period	40	–	–	ns	–

**NOTES:**

1. TCK may be stopped indefinitely in either the low or high phase.

1. Not tested. Guaranteed by design.



### 4.3.7 IX Bus

#### 4.3.7.1 FCLK Signal AC Parameter Measurements

Figure 19. FCLK Signal AC Parameter Measurements

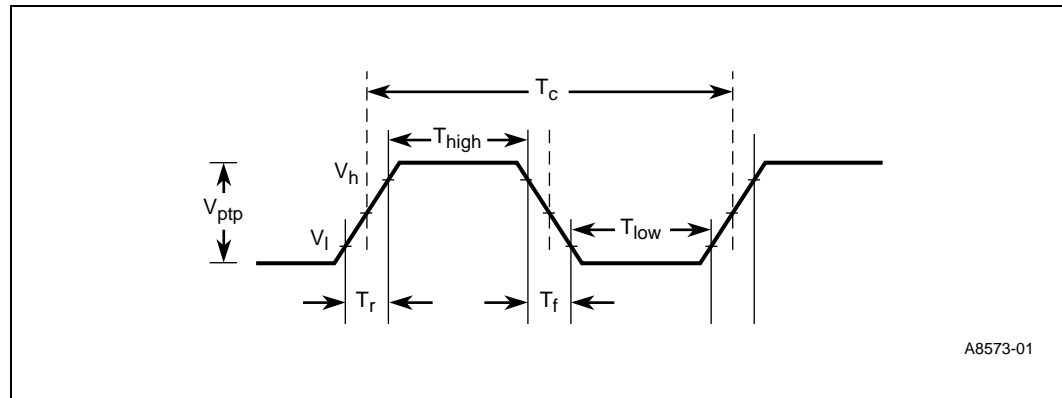


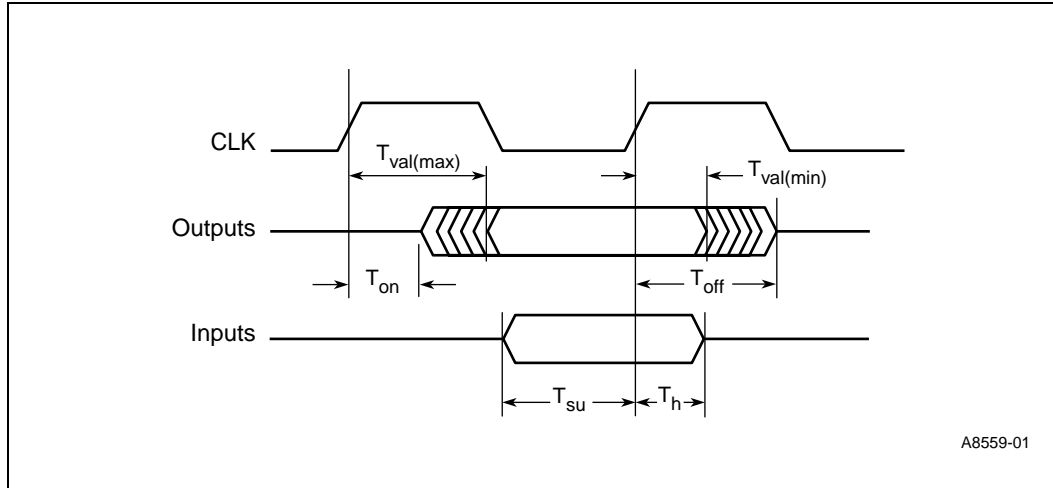
Table 44. FCLK Signal AC Parameter Measurements

Symbol	Parameter	Minimum	Maximum	Unit
$F_{CLK}$	Clock frequency	10	104 <sup>1</sup>	MHz
$T_c$	Cycle time	9.62 <sup>1</sup>	100	ns
$T_{high}^2$	Clock high time	3.8	---	ns
$T_{low}^2$	Clock low time	3.8	---	ns
$V_{ptp}$	Clock peak to peak <sup>2</sup>	0.6*VDDX	---	V
$T_r, T_f$	Clock rise/fall time <sup>3</sup>	1	4	ns
	$F_{core}/F_{CLK}$ Clock Ratio	1.5:1		

1. Maximum FCLK frequency for 232 MHz rated parts is 104 MHz. Maximum FCLK frequency for 200 MHz rated parts is 85 MHz. Maximum FCLK frequency for 166 MHz rated parts is 66 MHz.
2.  $T_{high}$  and  $T_{low}$  are based on a 50% duty cycle and can vary (worst case) 45-55%.
3. Nominal  $V_{ptp} = 0.12*VDDX$  to  $0.75*VDDX$ .

### 4.3.7.2 IX Bus Signals Timing

Figure 20. IX Bus Signals Timing



A8559-01

Table 45. IX Bus Signals Timing

Symbol	Parameter	Minimum (IX Bus Speed)			Maximum (IX Bus Speed)			Unit	Condition
		66 MHz	85 MHz	104 MHz	66 MHz	85 MHz	104 MHz		
$T_{val}$	Clock to output delay	1.0	1.0	0.5	7.0	7.0	5.75	ns	0 pF load <sup>1</sup>
$T_{su}$	Data input setup time before clock	4.0	4.0	3.25	---	---	---	ns	
$T_h$	Data input hold time from clock	1.0	1.0	0.25	---	---	---	ns	
$T_{on}$	Float to FDAT[63:0] and FBE_L[7:0] data driven delay from clock <sup>2</sup>	1.5	1.5	1.5	--	--	--	ns	
$T_{onxf}$	Float to data driven from clock, excluding FDAT[63:0] and FBE_L[7:0] <sup>2</sup>	2.5	2.5	2.5	--	--	--	ns	
$T_{off}$	FDAT[63:0] and FBE_L[7:0] driven to float delay from clock <sup>2</sup>	---	---	---	7.5	7.5	7.5	ns	
$T_{offxf}$	Data driven to float delay, excluding FDAT[63:0] and FBE_L[7:0] <sup>2</sup>	---	---	---	7.0	7.0	7.0	ns	

1. Capacitive loading effects on signal lines are shown in Table 46.  
 2. The parameter specified is guaranteed by design in a minimally configured system environment.

**Table 46. Signal Delay Derating**

Signal	Maximum Derating (ns/pF)			Minimum Derating (ns/pF)		
	66 MHz	85 MHz	104 MHz	66 MHz	85 MHz	104 MHz
FDATA[63:0]	0.055	0.05	0.031	0.03	0.025	0.015
FBE_L[7:0]	0.055	0.05	0.031	0.03	0.025	0.015
FPS[2:0]	0.065	0.06	0.031	0.03	0.025	0.015
EOP32	0.065	0.06	0.031	0.03	0.025	0.015
SOP32	0.065	0.06	0.031	0.03	0.025	0.015
RDYCTL_L[4:0]	0.065	0.06	0.031	0.03	0.025	0.015
RDYBUS[7:0]	0.065	0.06	0.031	0.03	0.025	0.015
TXAXIS	0.065	0.06	0.031	0.03	0.025	0.015
EOP	0.065	0.06	0.031	0.03	0.025	0.015
SOP	0.065	0.06	0.031	0.03	0.025	0.015
GPIO[3:0]	0.065	0.06	0.031	0.03	0.025	0.015
PORTCTL_L[3:0]	0.095	0.09	0.035	0.03	0.025	0.015
TK_OUT	0.095	0.09	0.035	0.03	0.025	0.015
RXFAIL	0.095	0.09	0.035	0.03	0.025	0.015

4.3.7.3 IX Bus Protocol

The following timing diagrams show the IX Bus signal protocol for both 64-bit Bidirectional and 32-bit Unidirectional modes of operation.

Figure 21. 64-Bit Bidirectional IX Bus Timing, 1-2 MAC Mode, Consecutive Receive and Transmit, No EOP

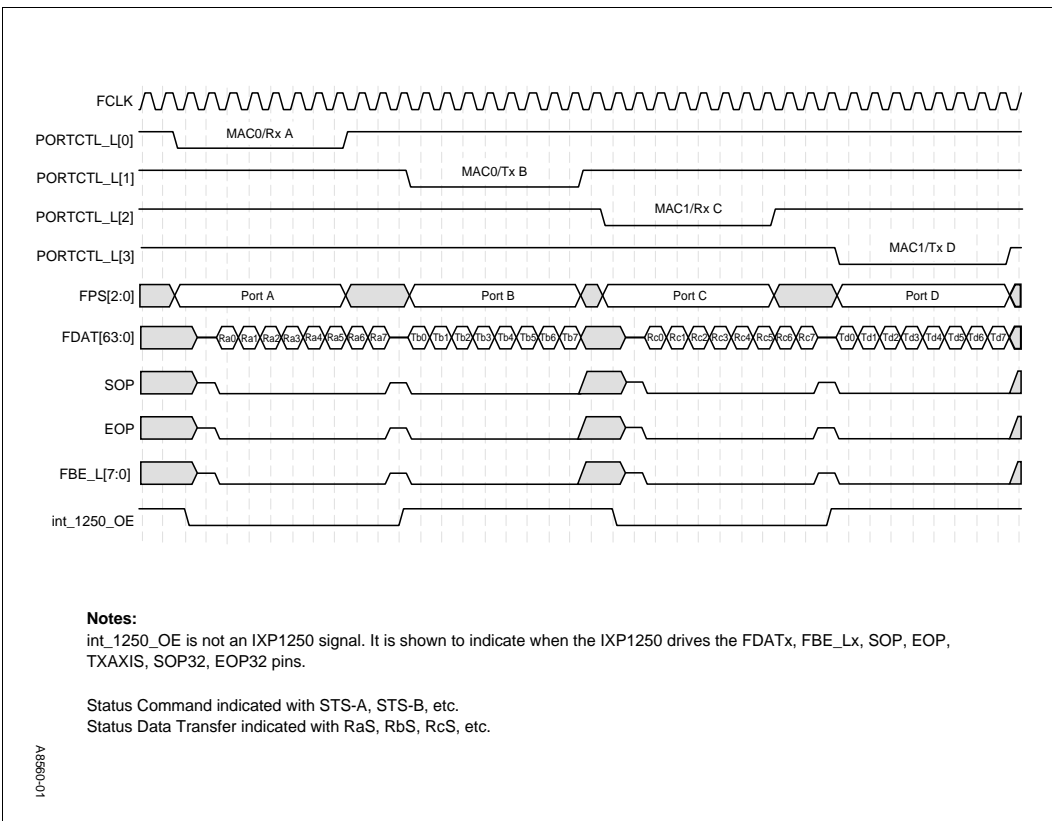


Figure 22. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, No EOP

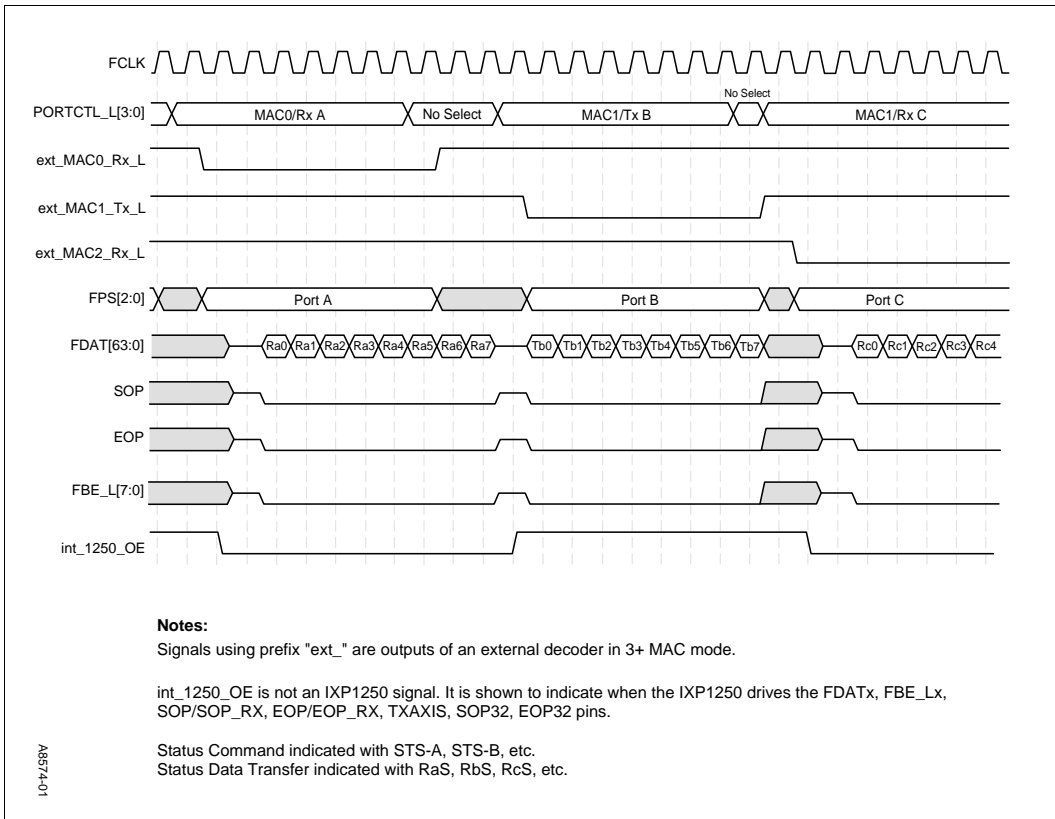
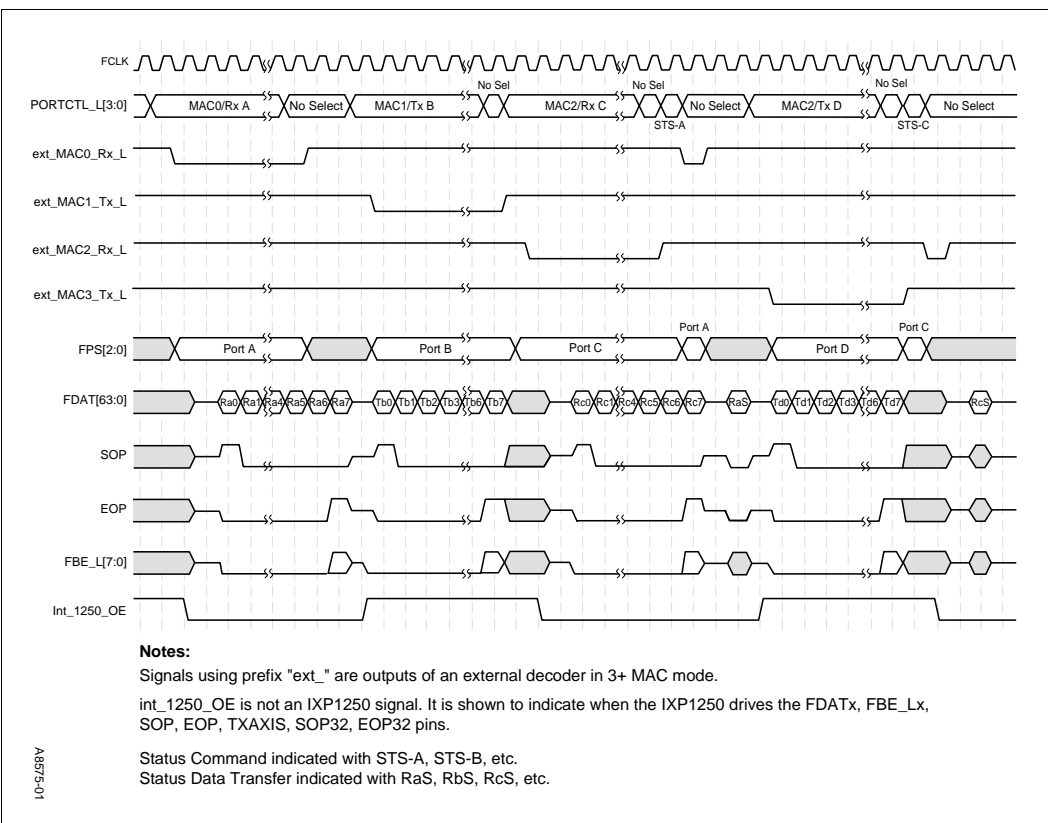


Figure 23. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 8th Data Return with Status



**Figure 24. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 7th Data Return with Status**

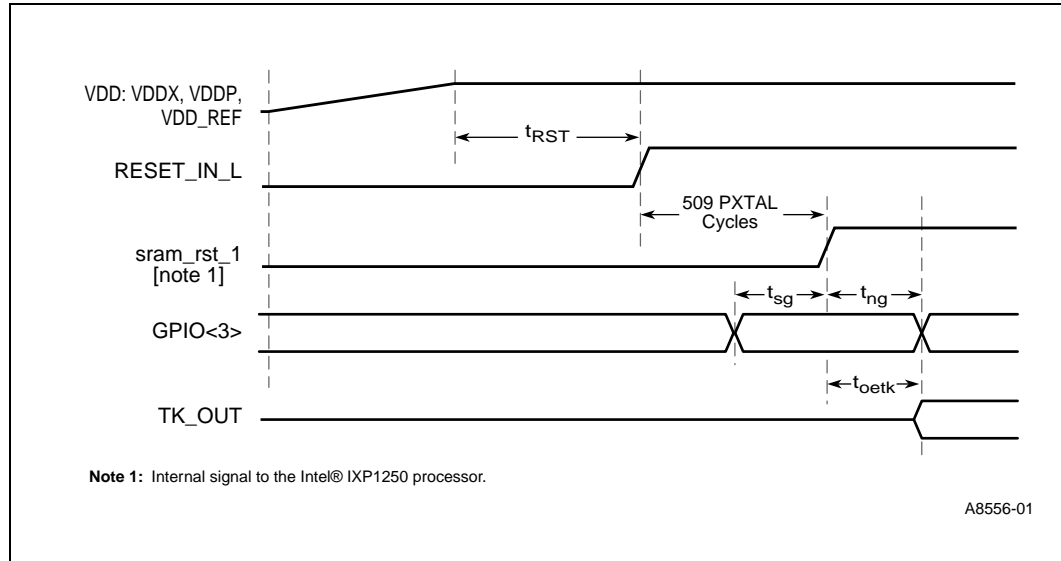


Figure 25. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 6th Data Return with Status

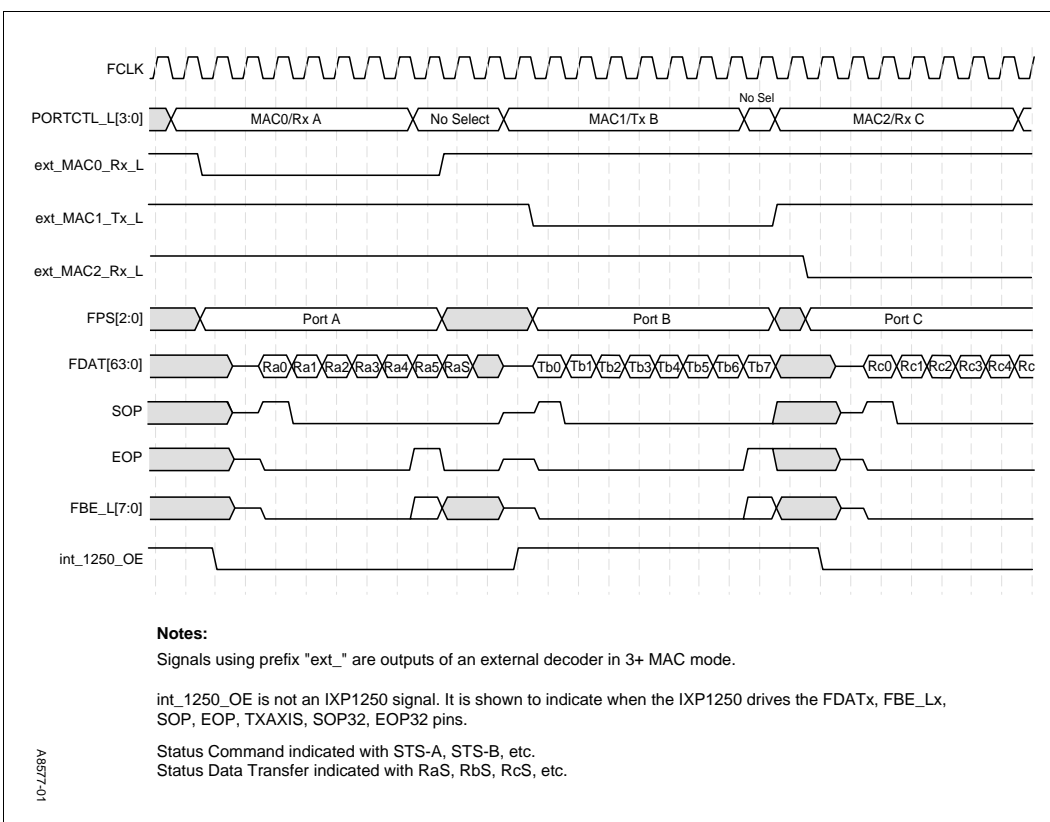




Figure 26. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 5th Data Return with Status

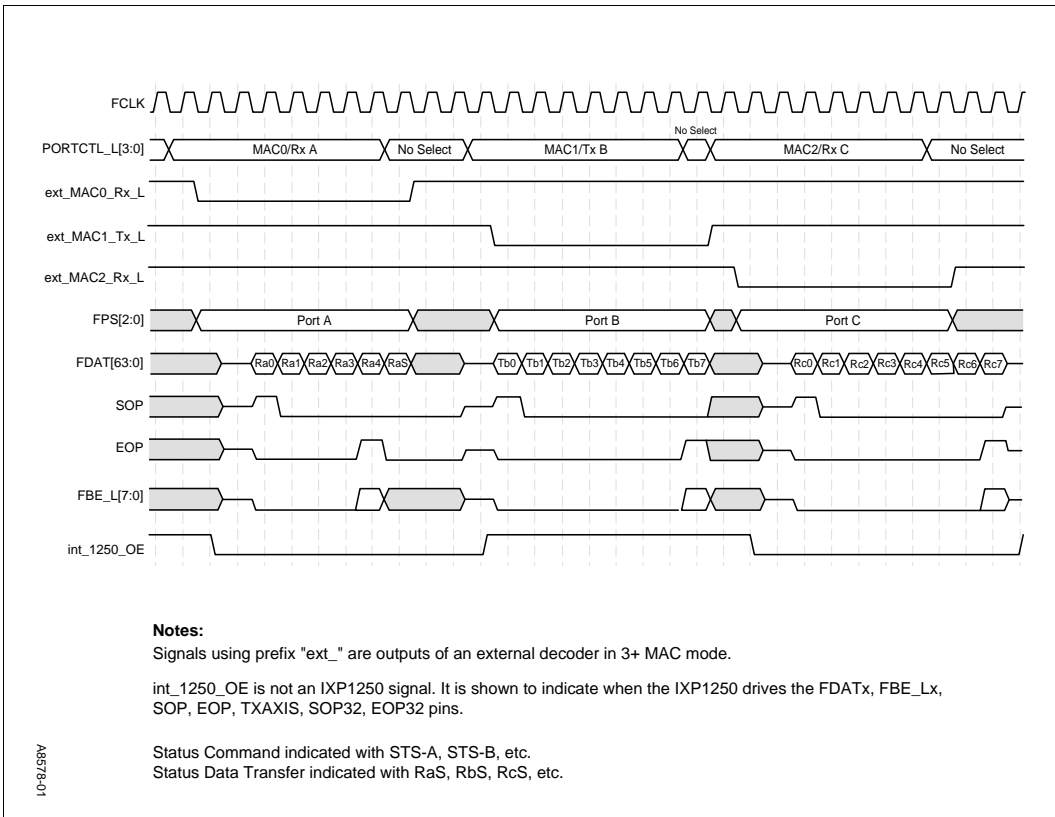


Figure 27. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 4th Data Return with Status

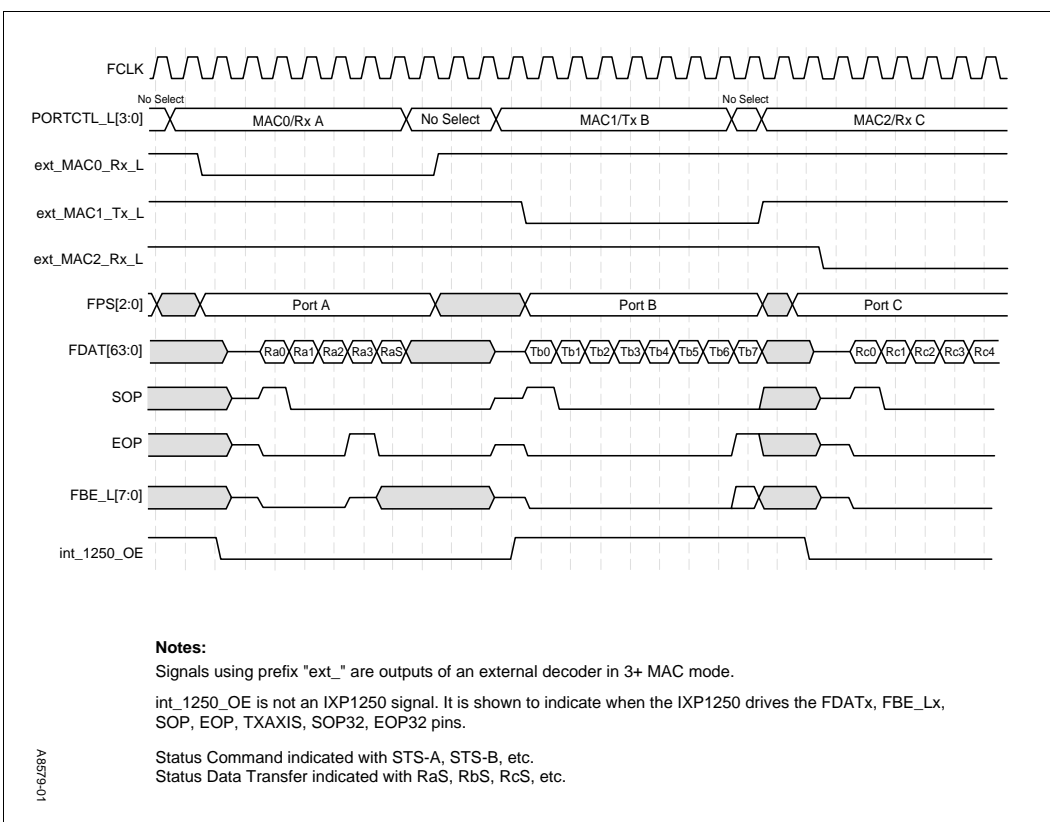
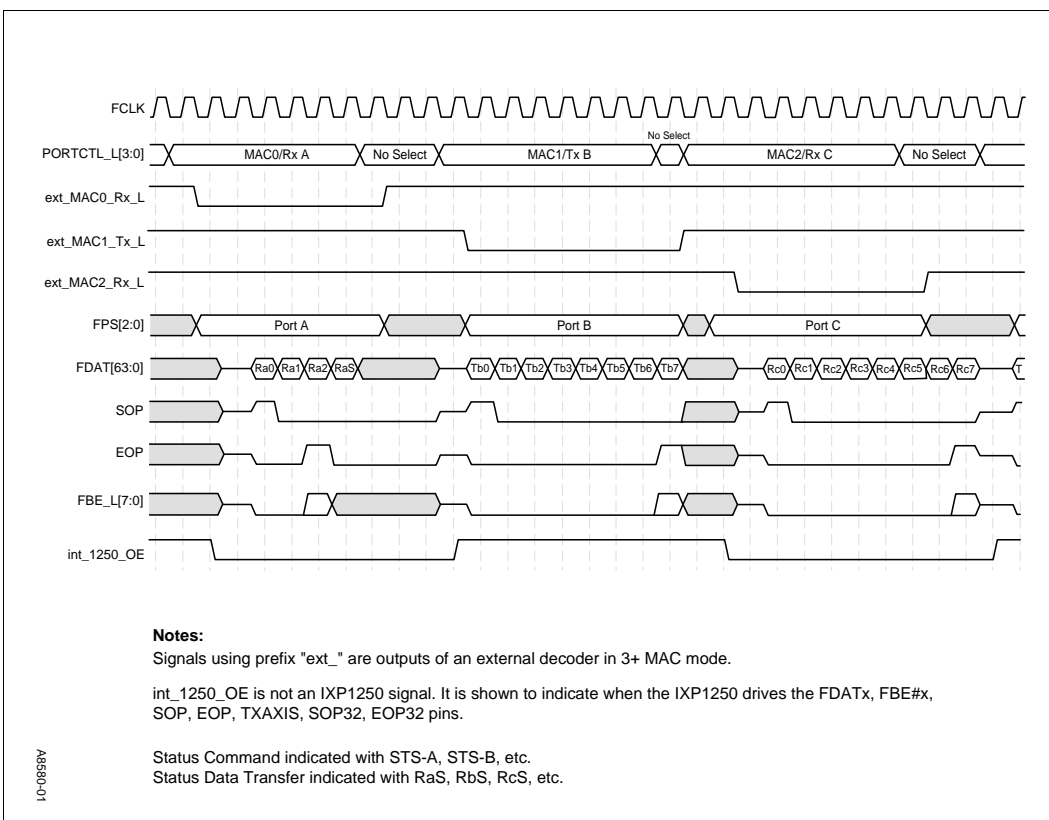


Figure 28. 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit, EOP on 1st through 3rd Data Return with Status (3rd Data Return Shown)



A8580-01

Figure 29. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 1st Data Return, No Status

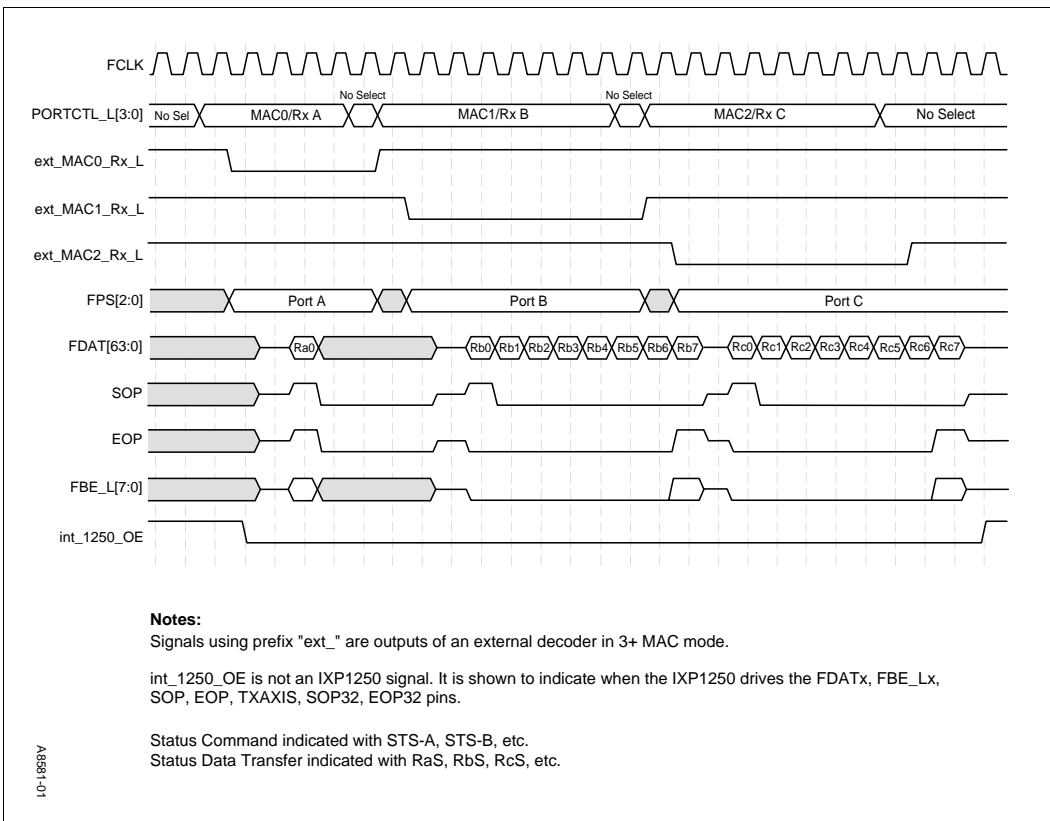


Figure 30. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, No EOP

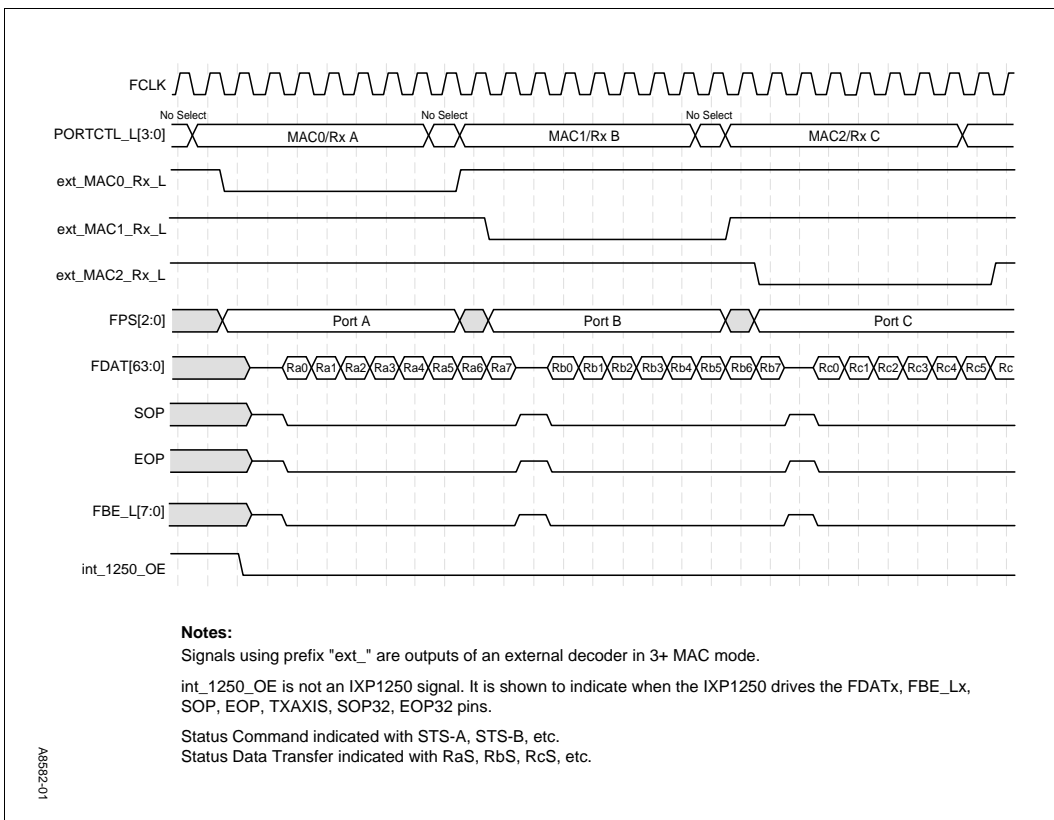


Figure 31. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 8th Data Return with Status

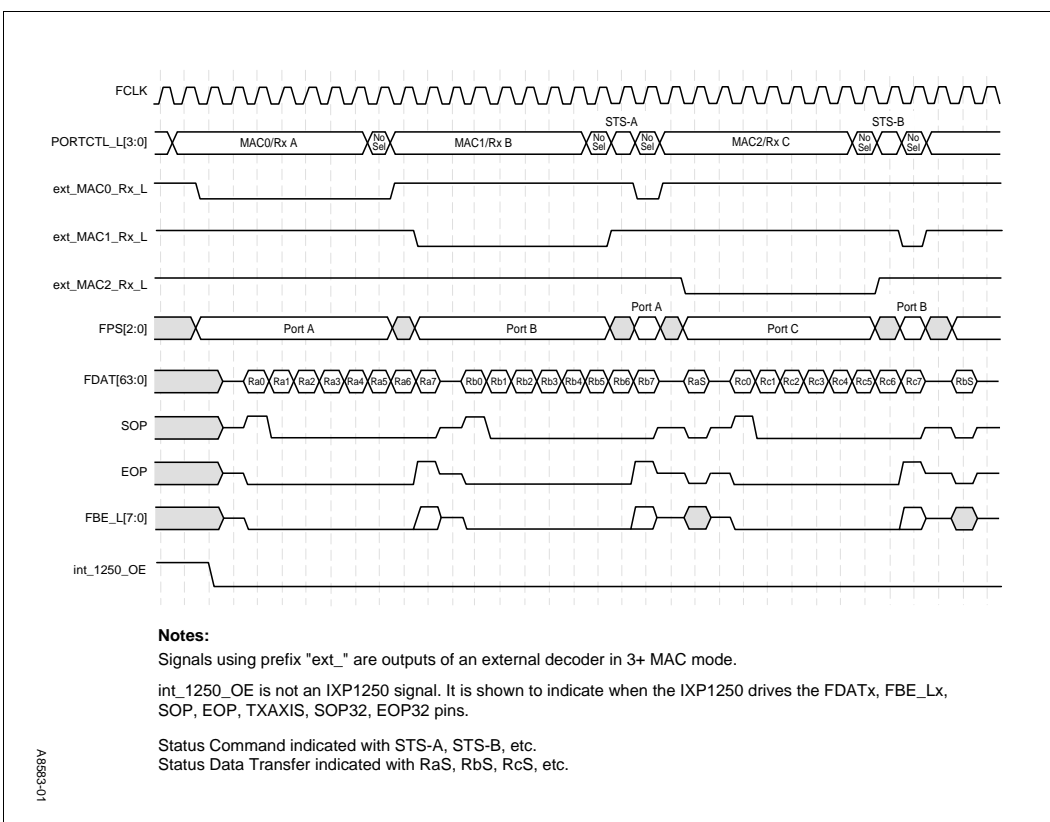


Figure 32. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 7th Data Return with Status

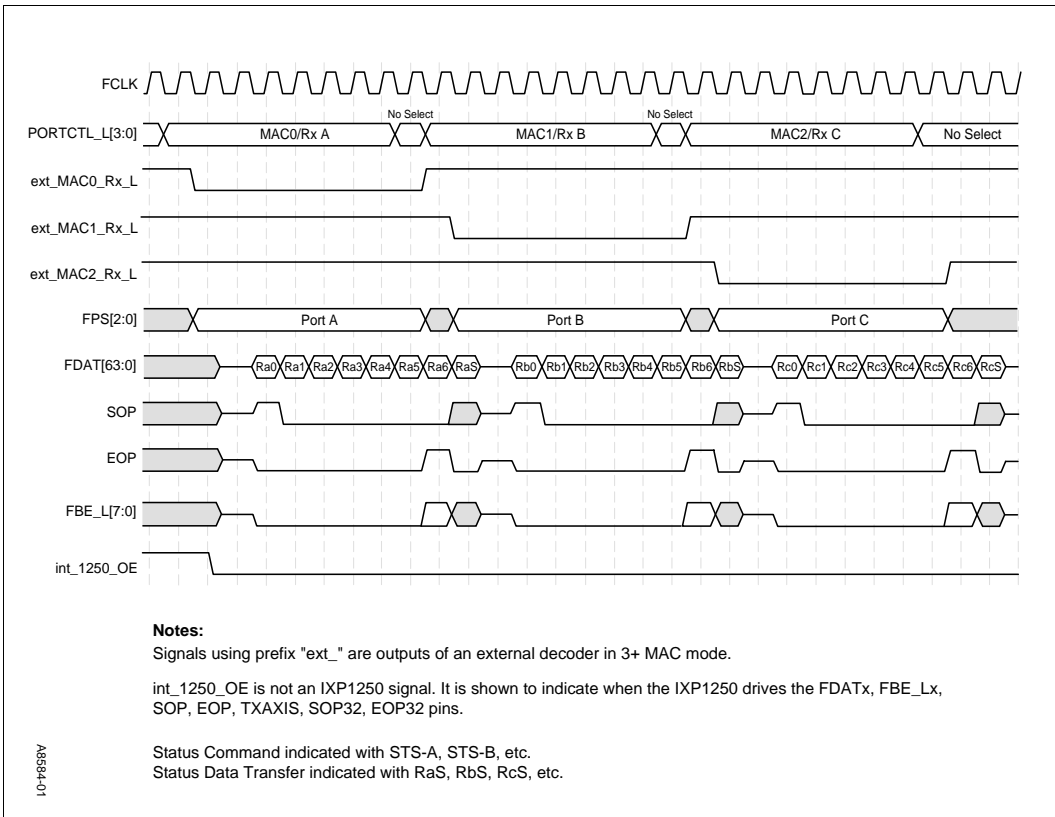


Figure 33. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP on 6th Data Return with Status

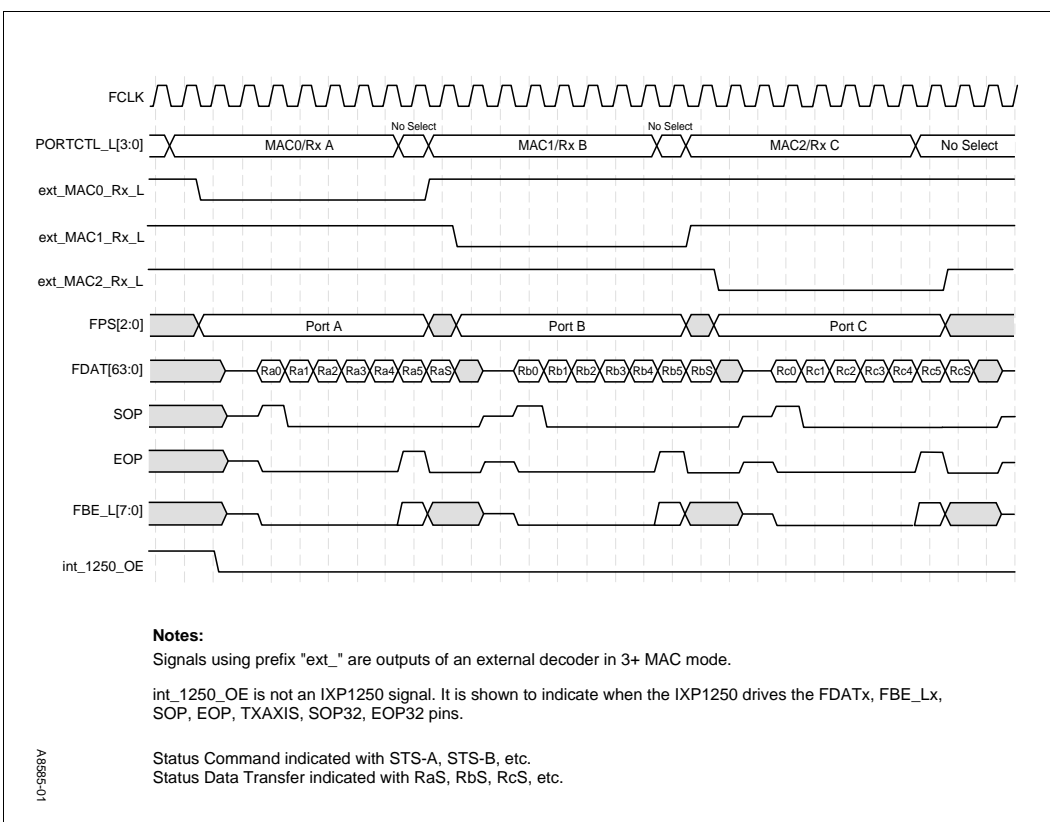




Figure 34. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, EOP, Two Element Transfer with Status

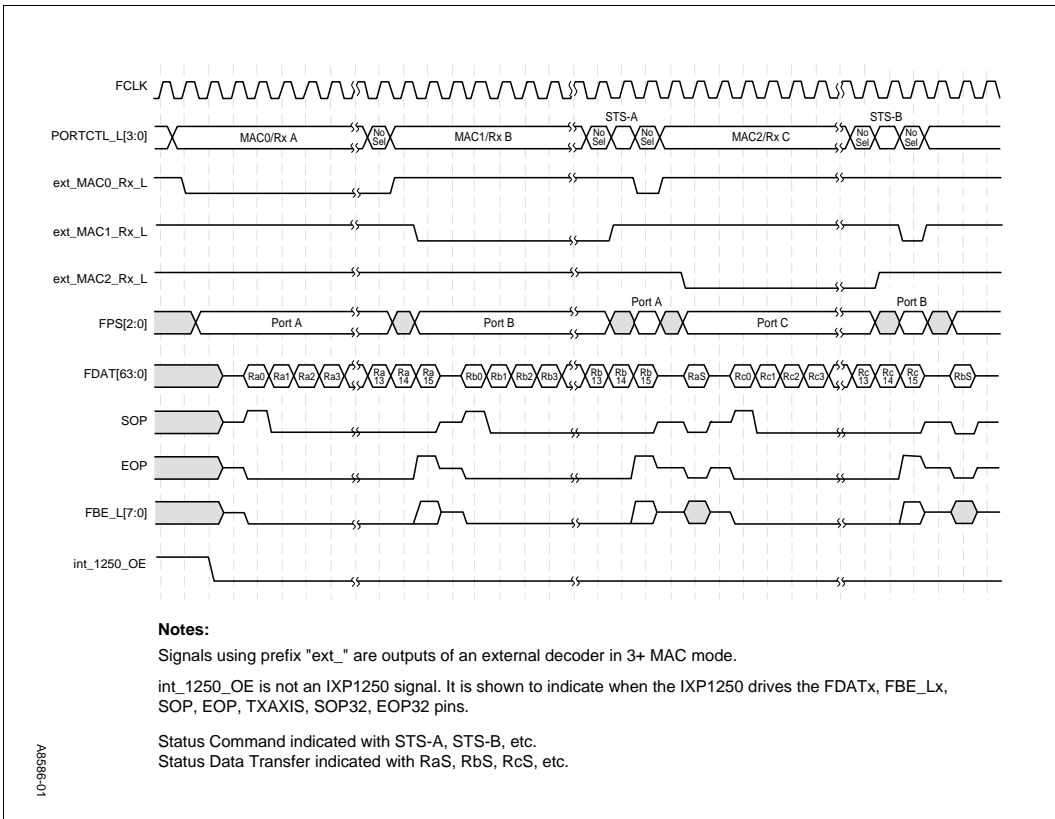


Figure 35. 64-Bit Bidirectional IX Bus Timing - Consecutive Receives, Fetch-9, No EOP

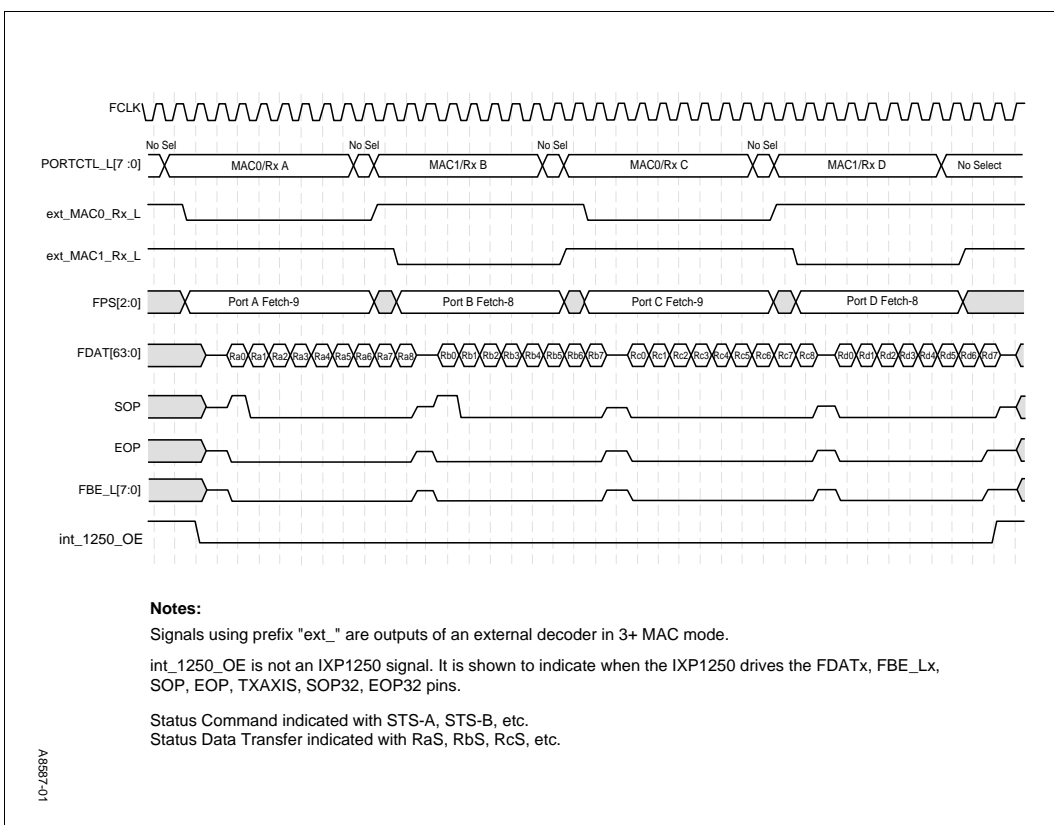


Figure 36. 64-Bit Bidirectional IX Bus Timing - Consecutive Transmits, EOP

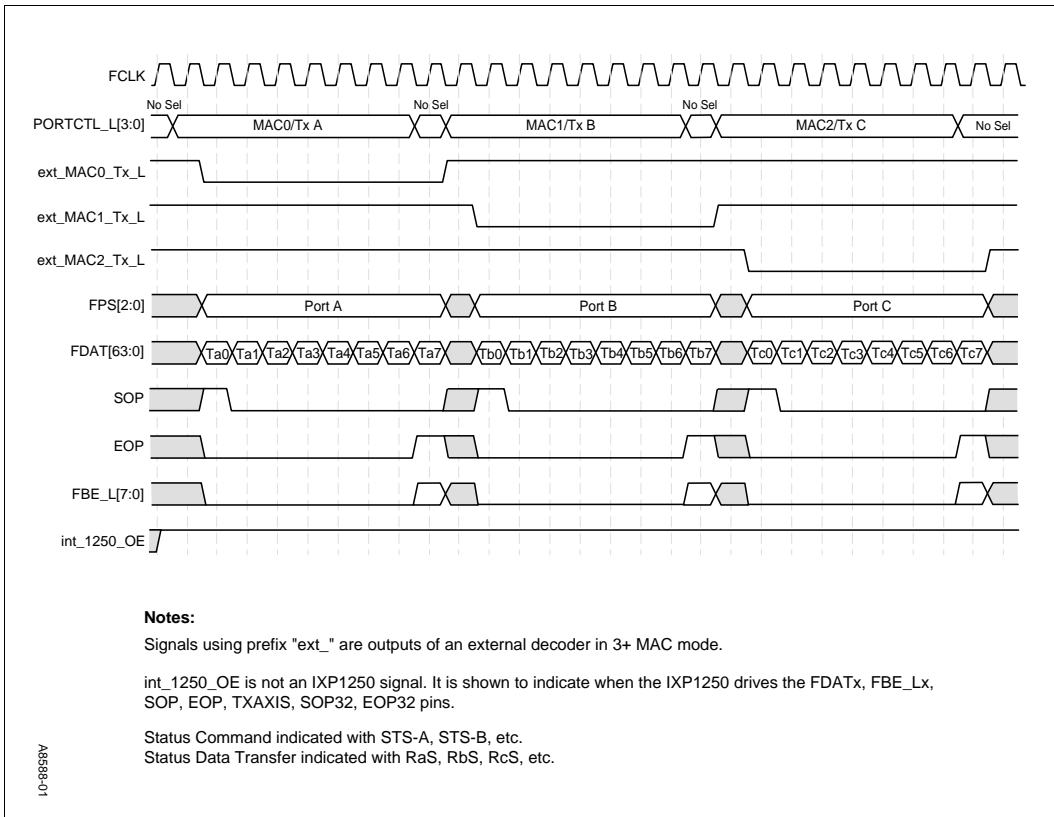


Figure 37. 64-Bit Bidirectional IX Bus Timing - Consecutive Transmits with Prepend, EOP

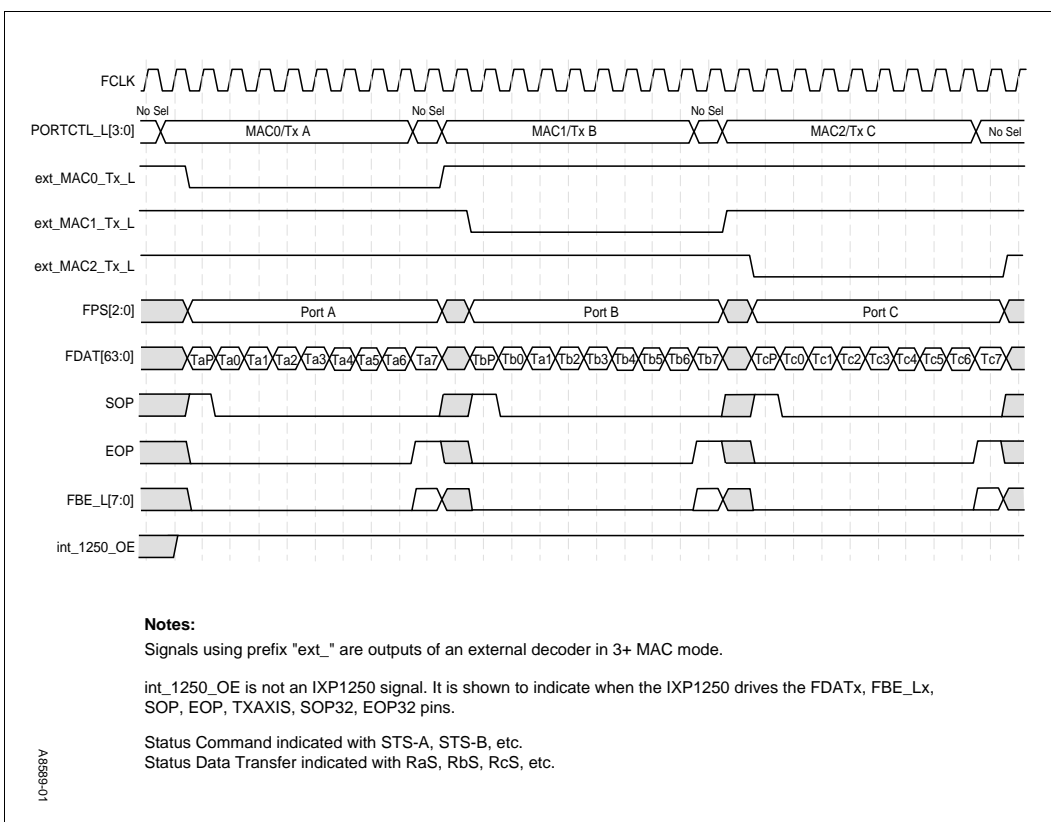


Figure 38. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, No EOP

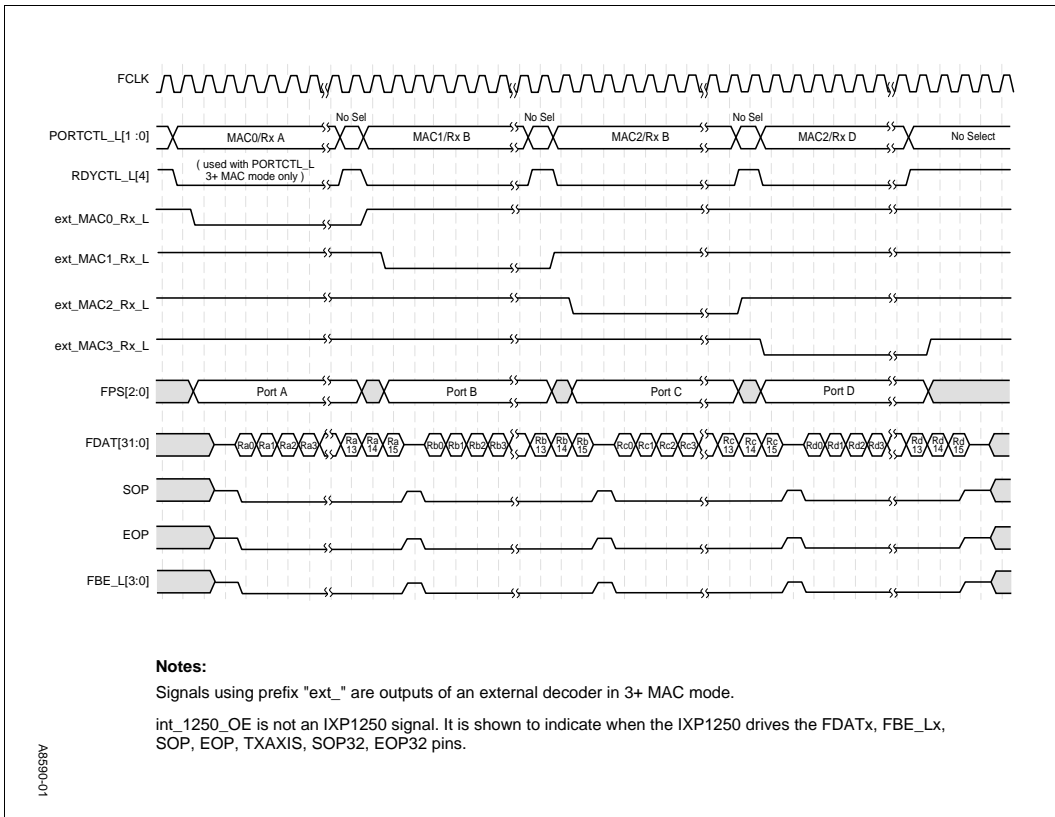


Figure 39. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 16th Data  
Return with Status

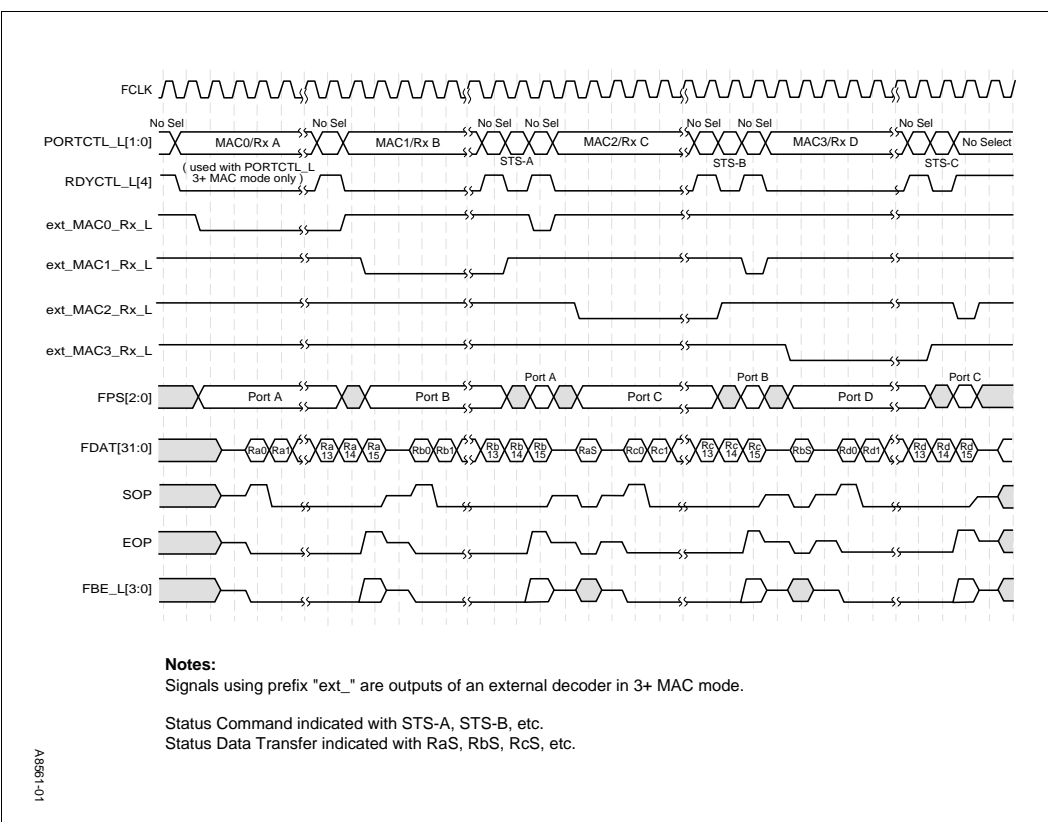


Figure 40. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 15th Data Return with Status

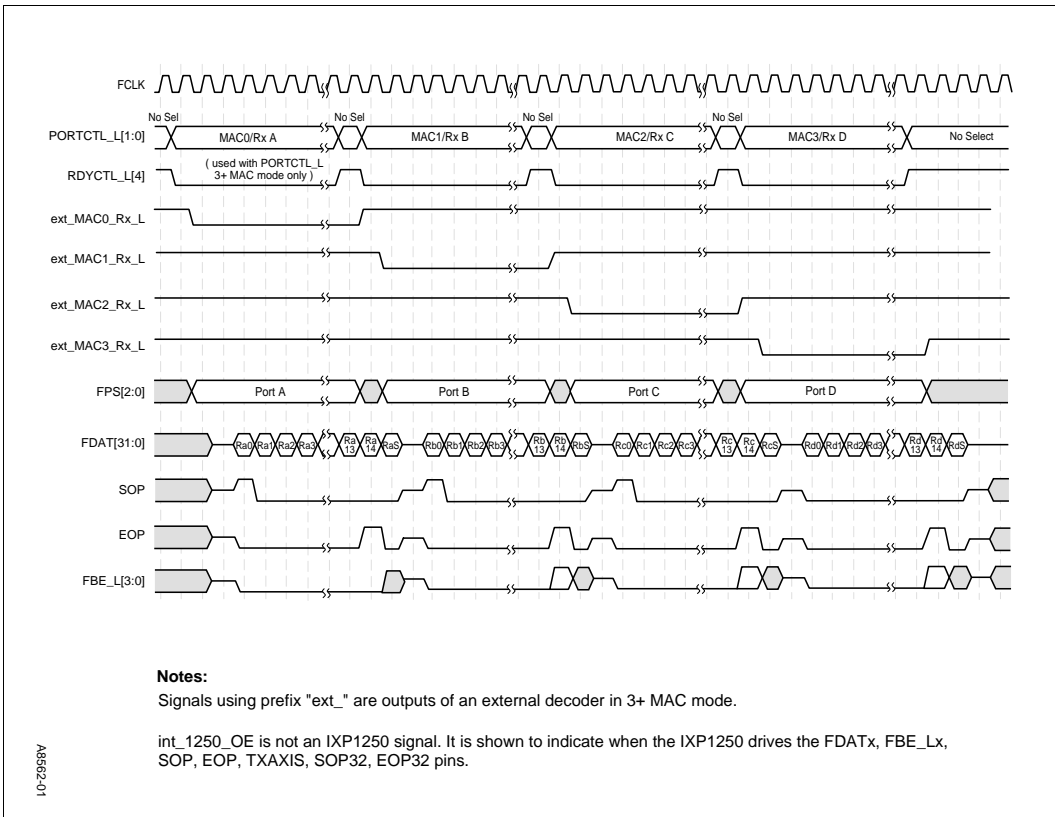


Figure 41. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 14th Data Return with Status

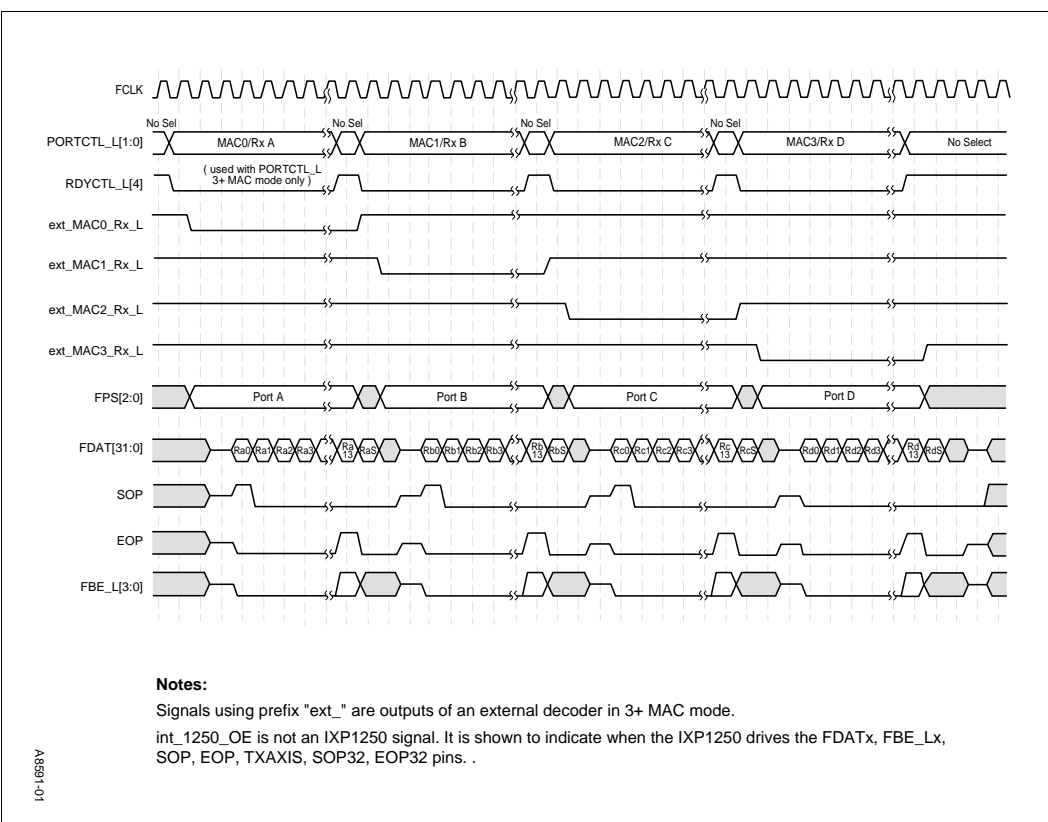




Figure 42. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP on 1st Through 13th Data Return with Status (13th Data Return Shown)

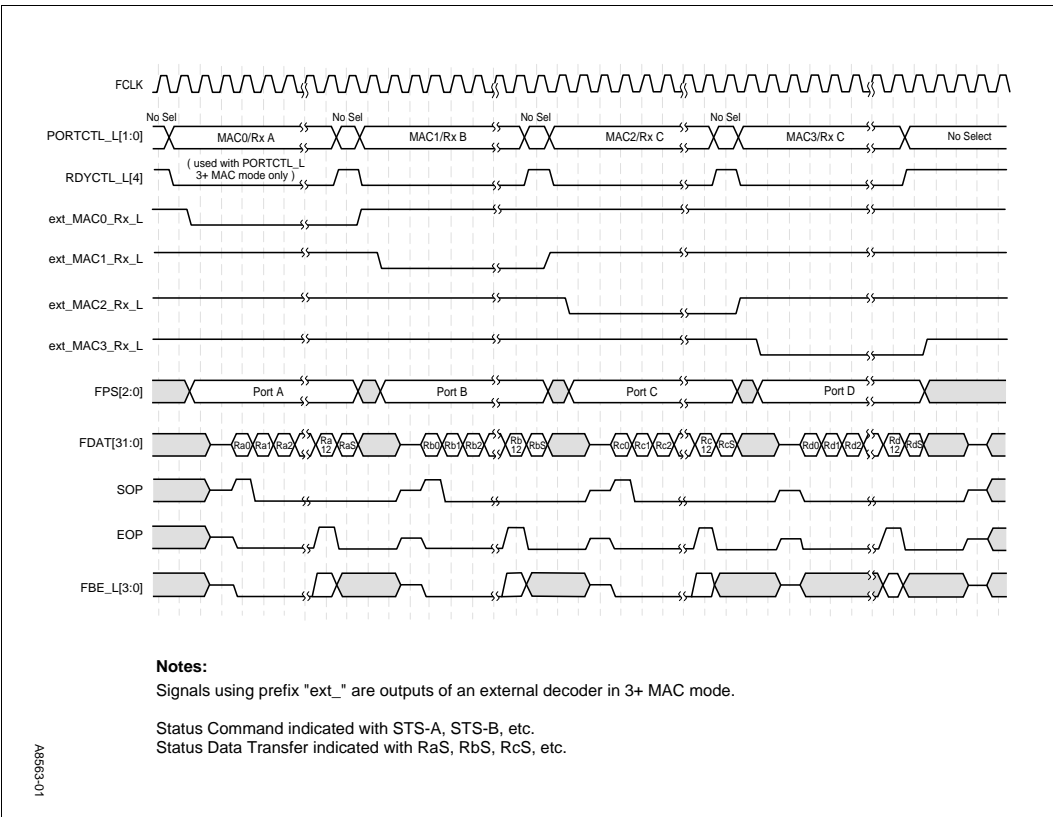


Figure 43. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, EOP, 64-Bit Status

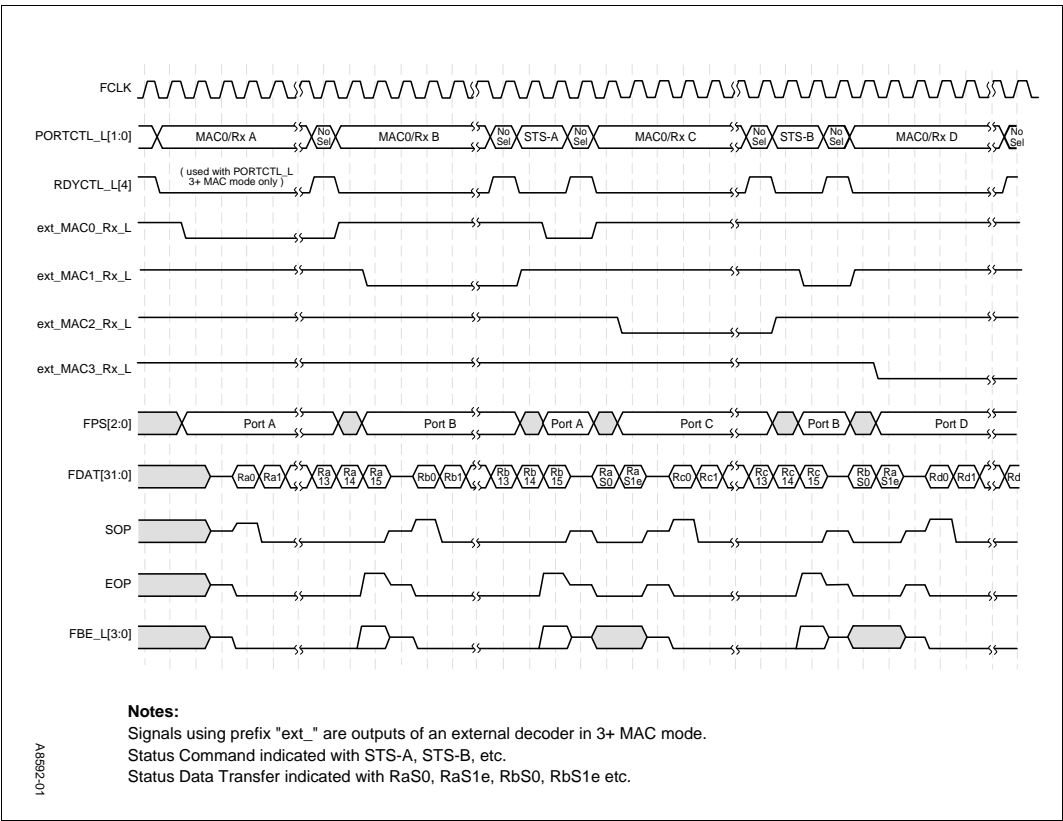


Figure 44. 32-Bit Unidirectional IX Bus Timing - Consecutive Receives, Two Element Transfers with 32-Bit Status

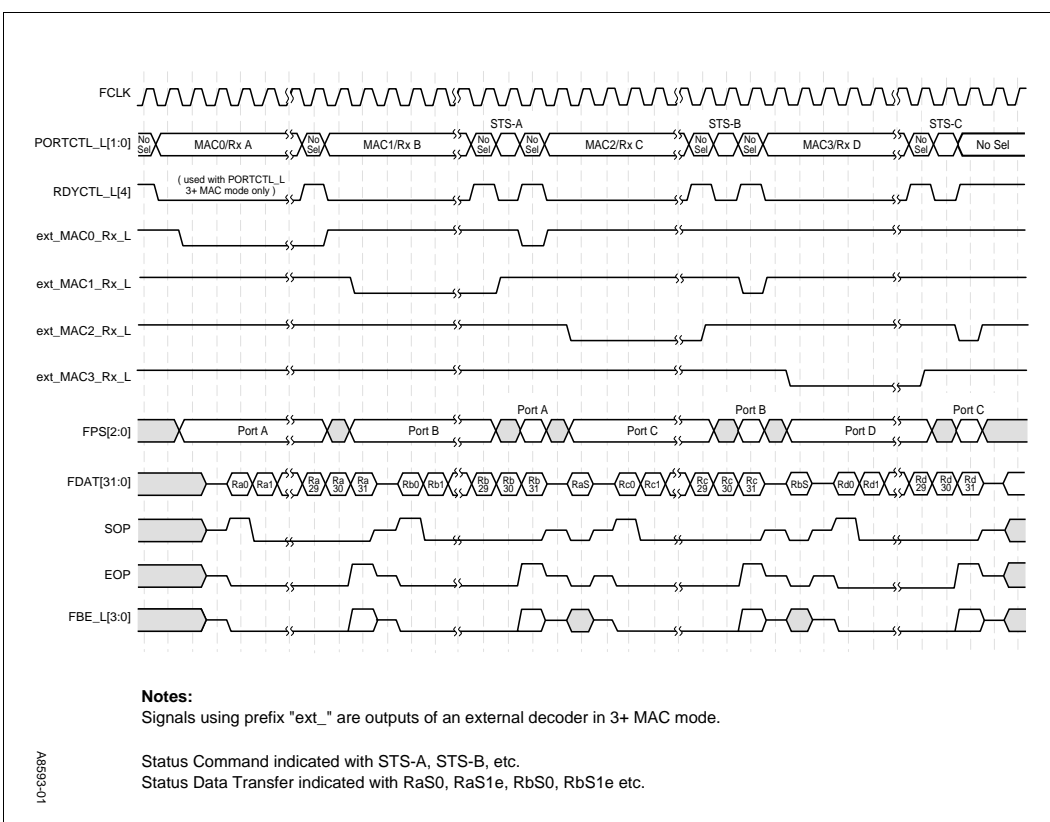


Figure 45. 32-Bit Unidirectional IX Bus Timing - Consecutive Transmits, EOP

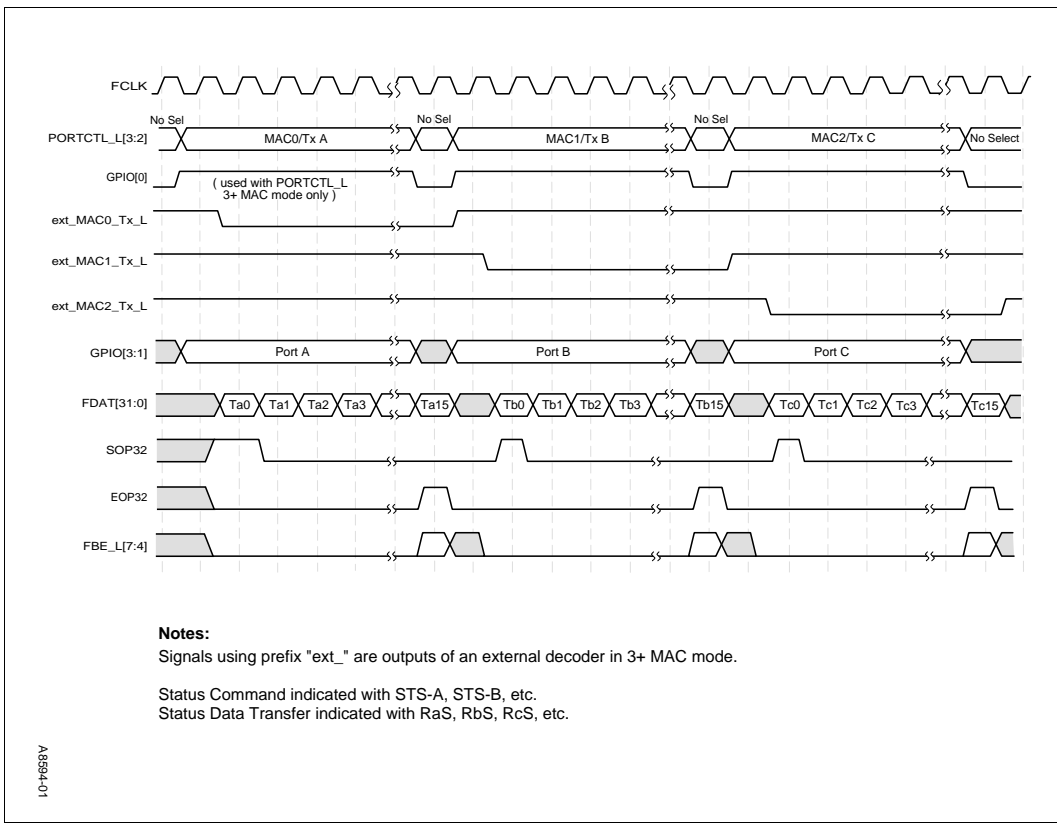


Figure 46. 32-Bit Unidirectional IX Bus Timing - Consecutive Transmits with Prepend, EOP

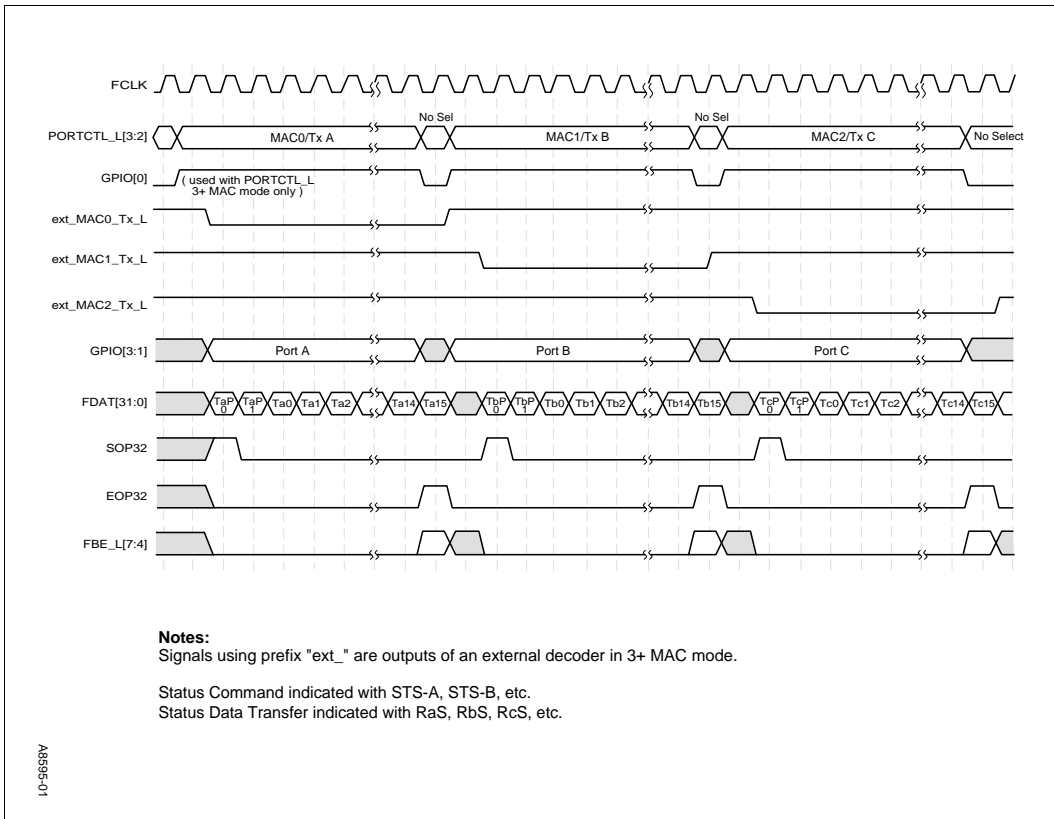
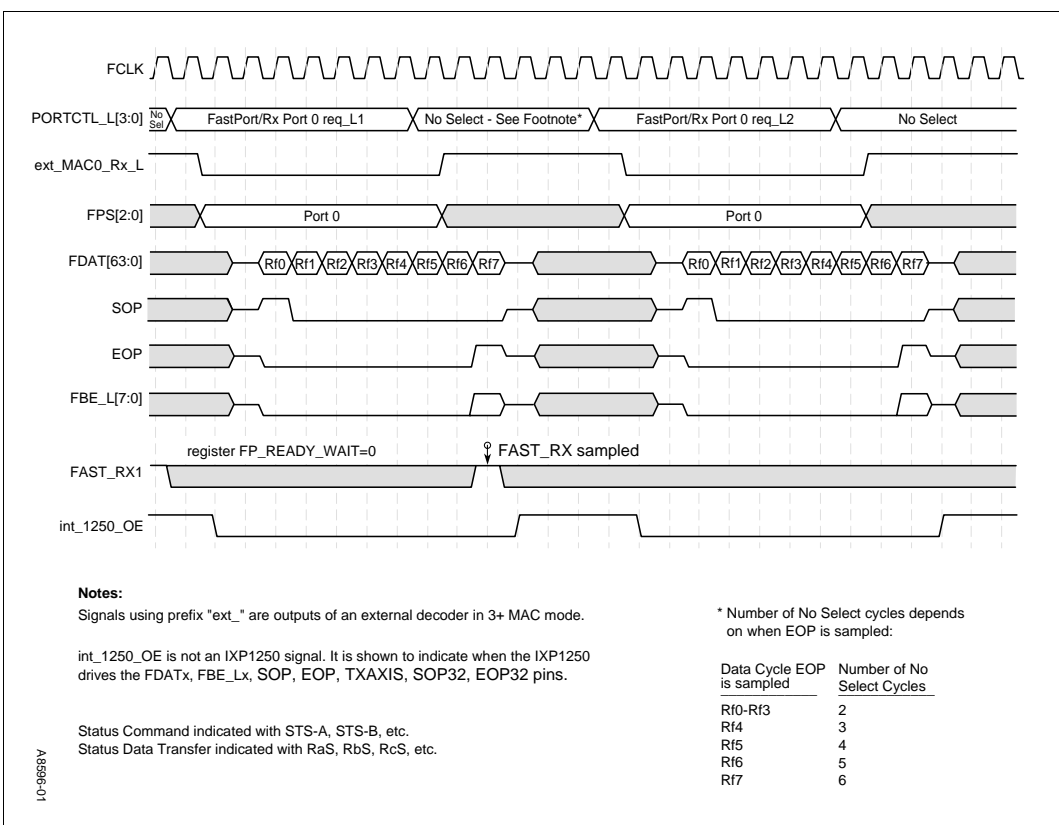


Figure 47. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP\_READY\_WAIT=0



A8596-01

Figure 48. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP\_READY\_WAIT=5

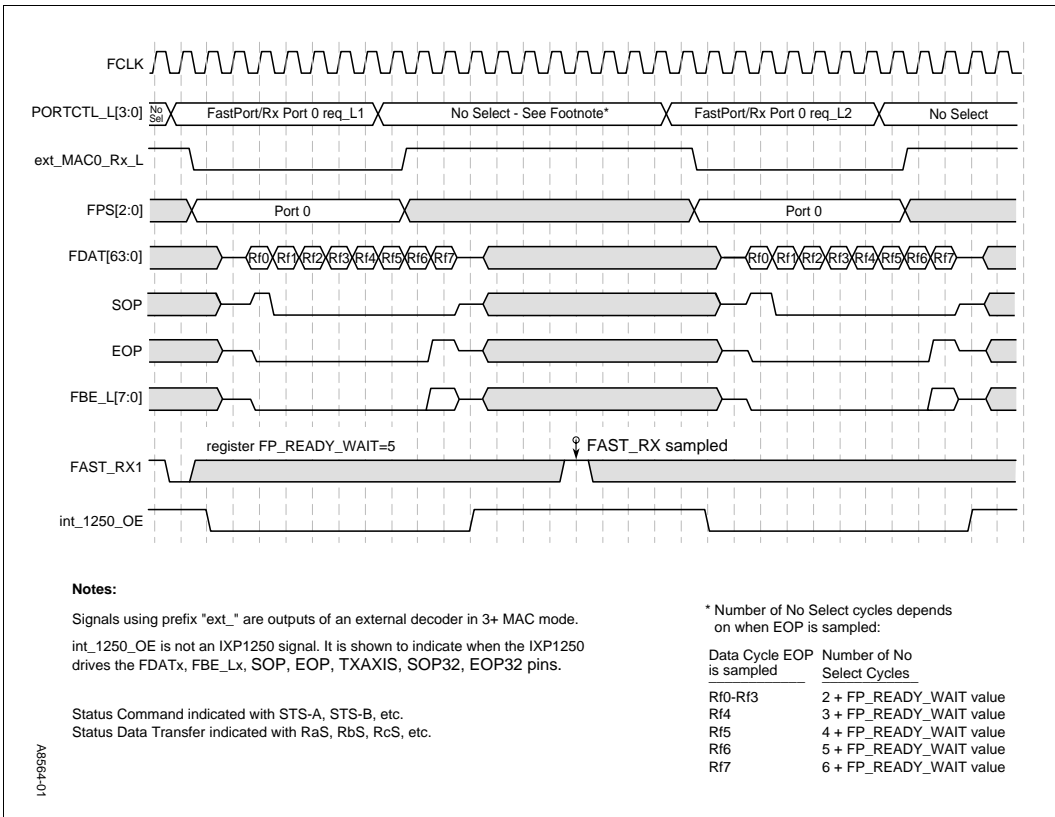


Figure 49. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, with Status, FP\_READY\_WAIT=0

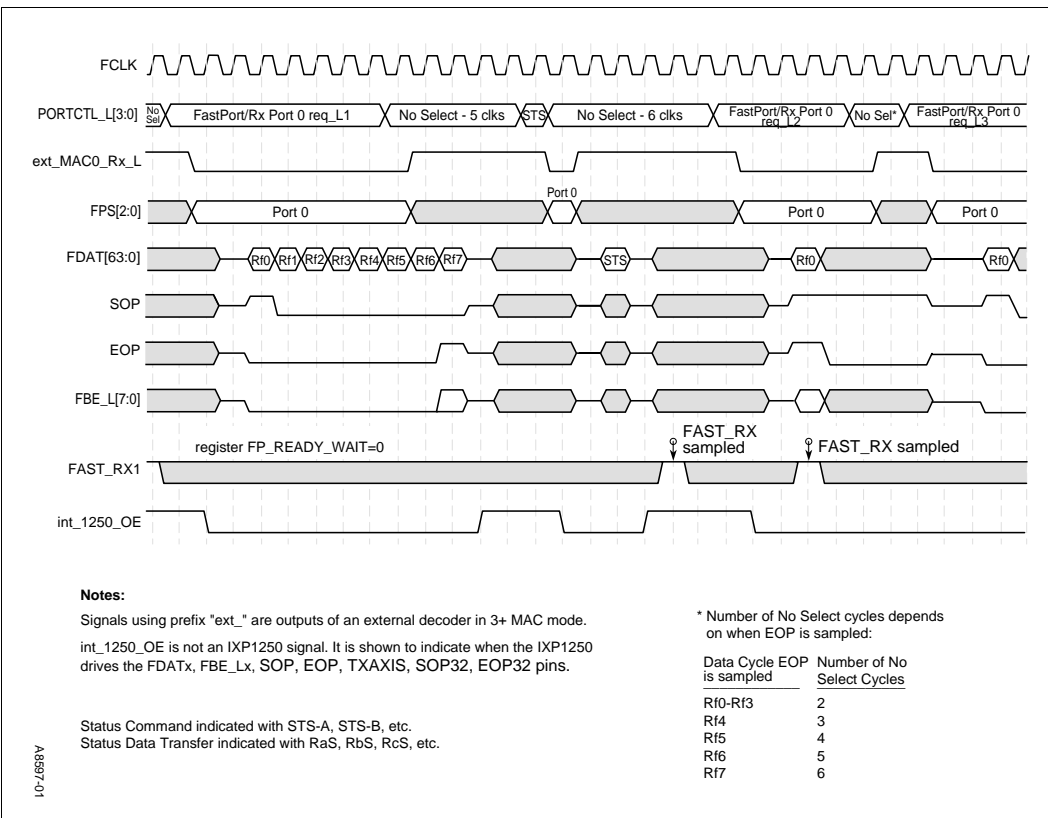




Figure 50. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP\_READY\_WAIT=5

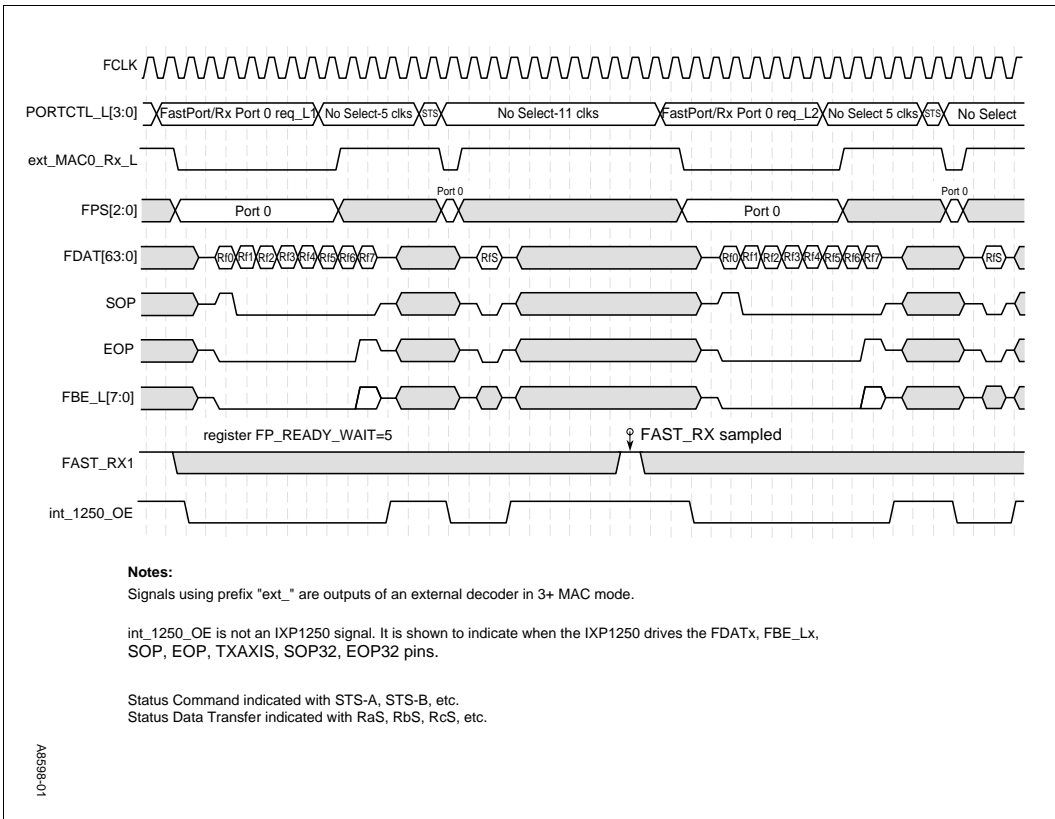


Figure 51. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, EOP, No Status, FP\_READY\_WAIT=0, Cancelled Request

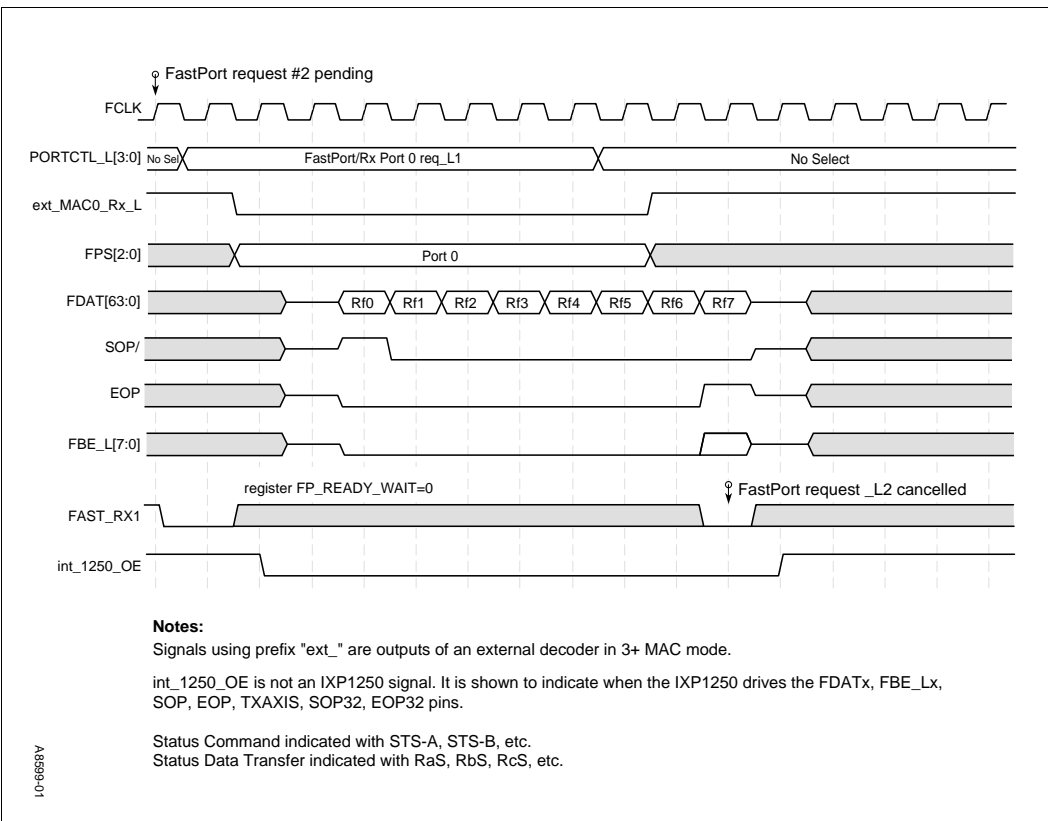


Figure 52. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Same Port, No EOP, FP\_READY\_WAIT=Don't Care

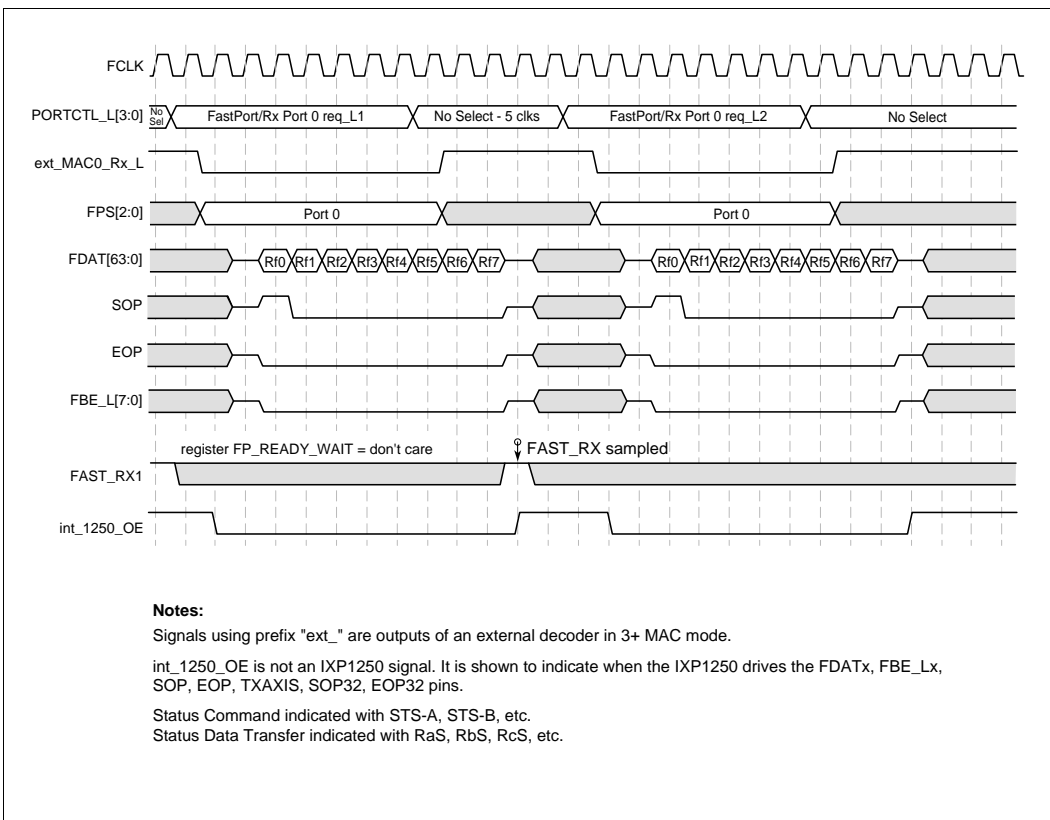


Figure 53. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Different Ports, EOP, No Status, FP\_READY\_WAIT=0

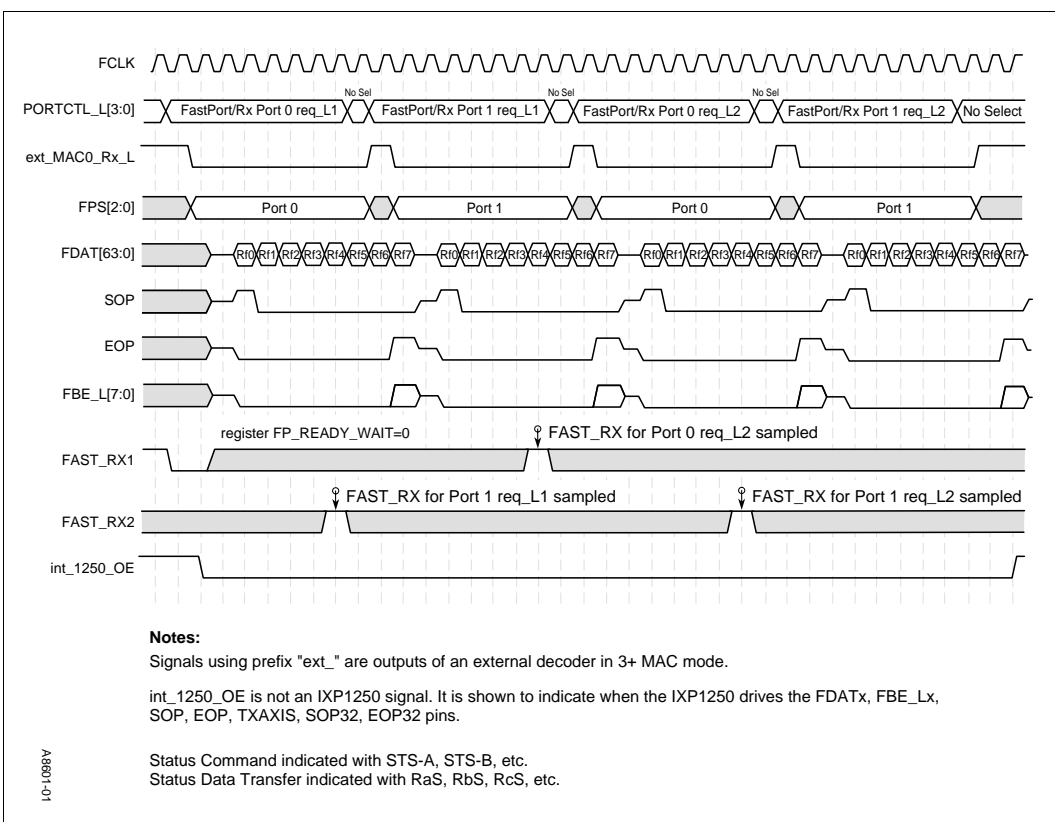
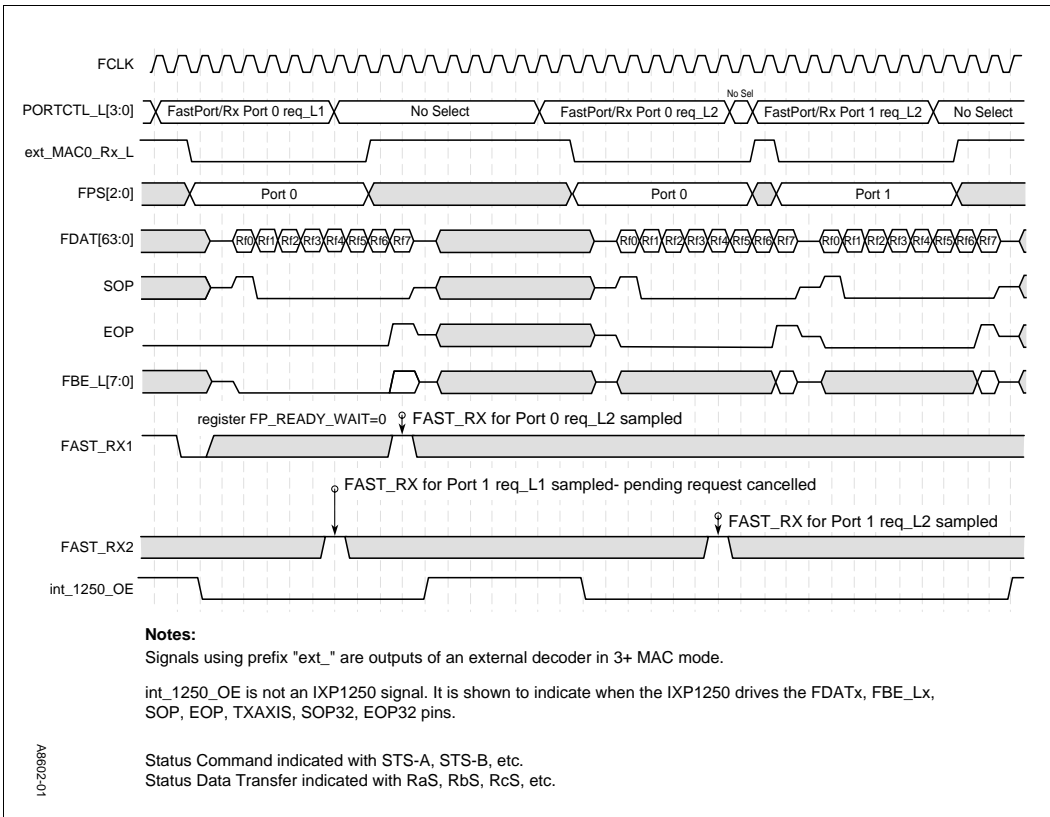


Figure 54. 64-Bit Bidirectional IX Bus Timing - Consecutive FastPort Receives, Different Ports, EOP, No Status, FP\_READY\_WAIT=0, Cancelled Request



### 4.3.7.4 RDYBus

Figure 55. Consecutive Fetch Ready Flags, 1-2 MAC Mode (with No External Registered Decoder) - RDYBUS\_TEMPLATE\_CTL[10]=1

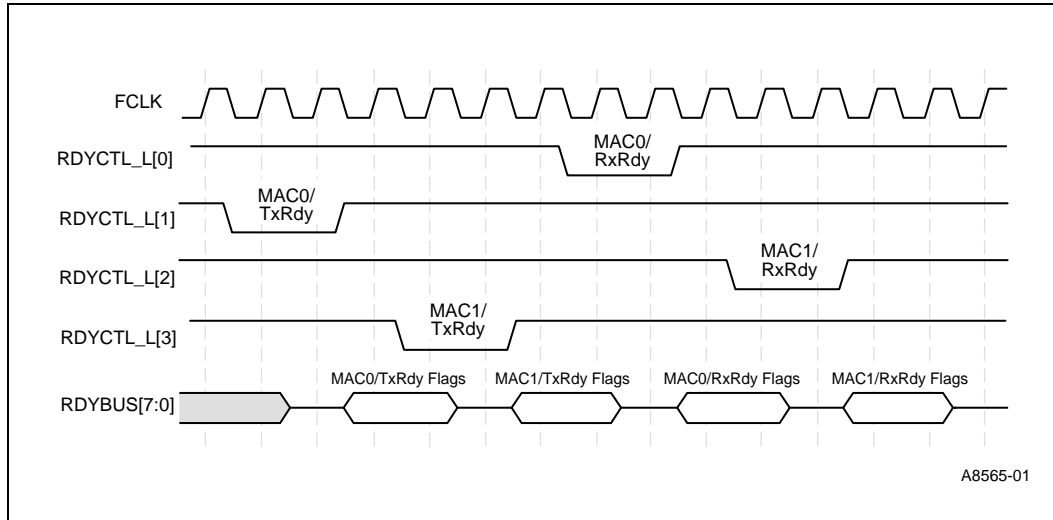
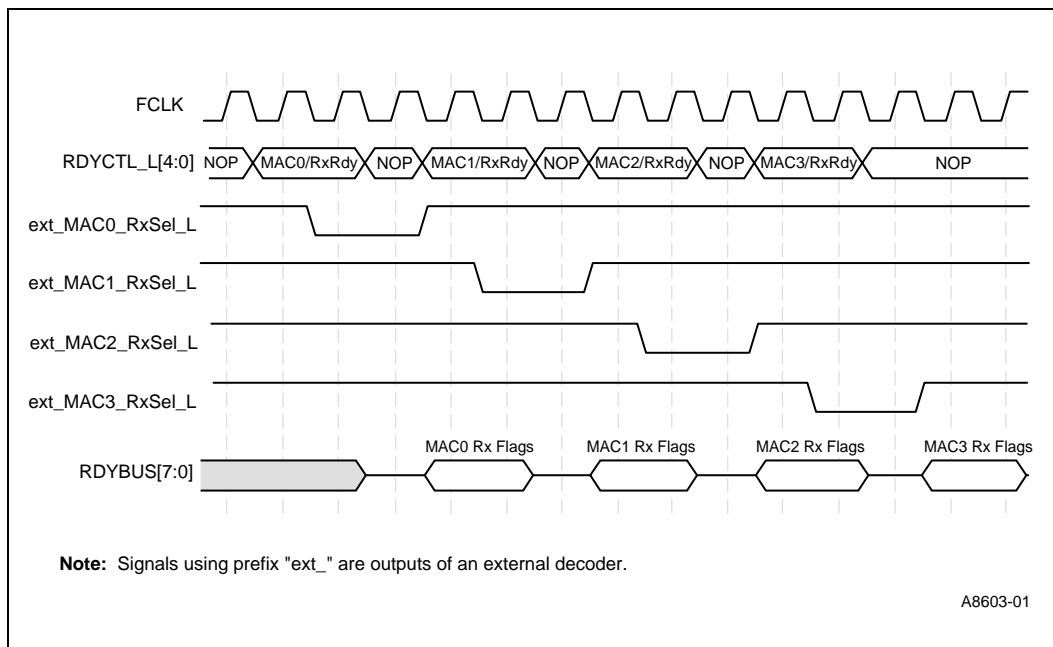
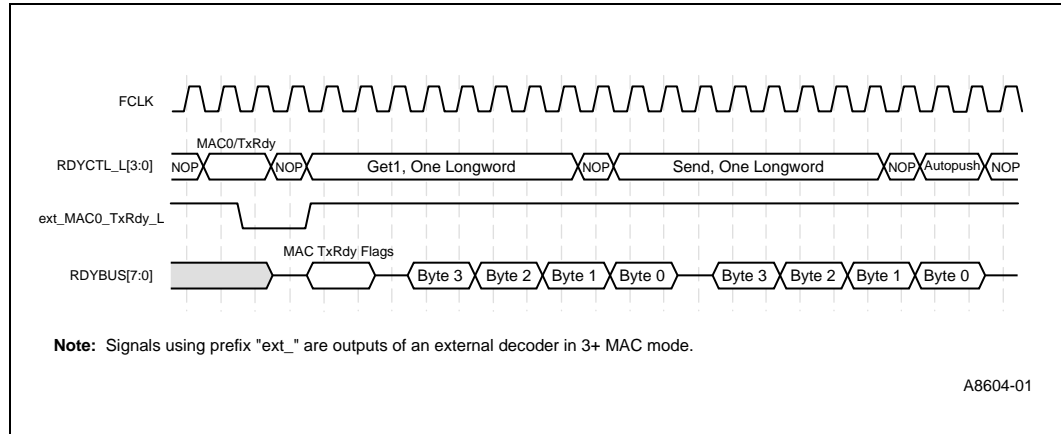


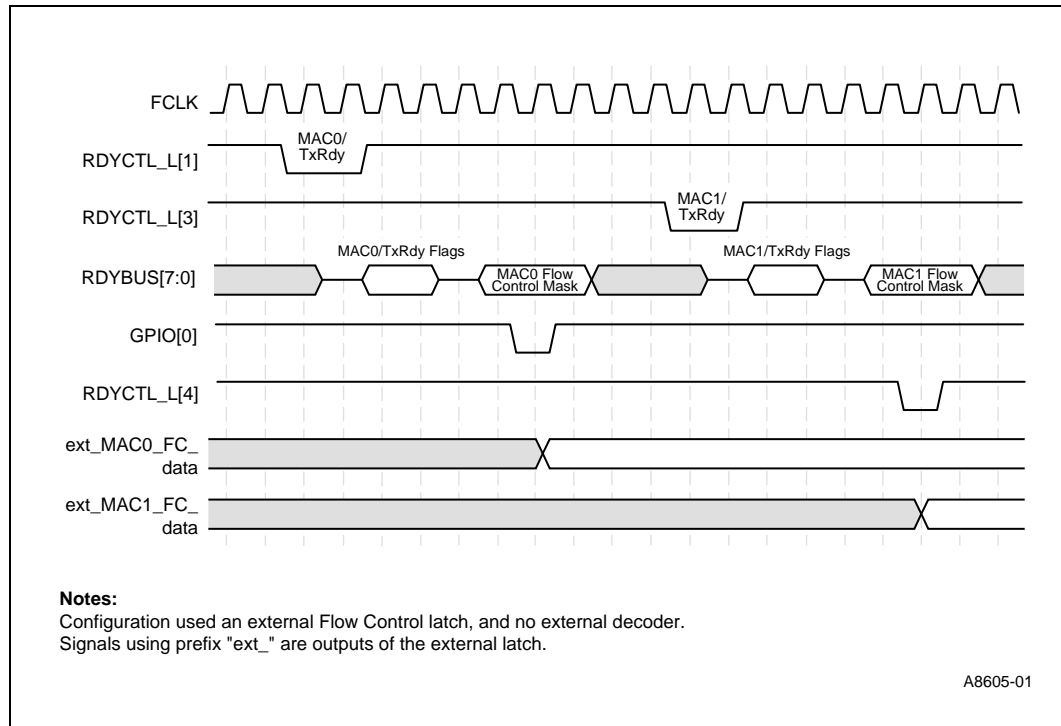
Figure 56. Consecutive Fetch Ready Flags, 3+ MAC Mode (with External Decoder) - RDYBUS\_TEMPLATE\_CTL[10]=0



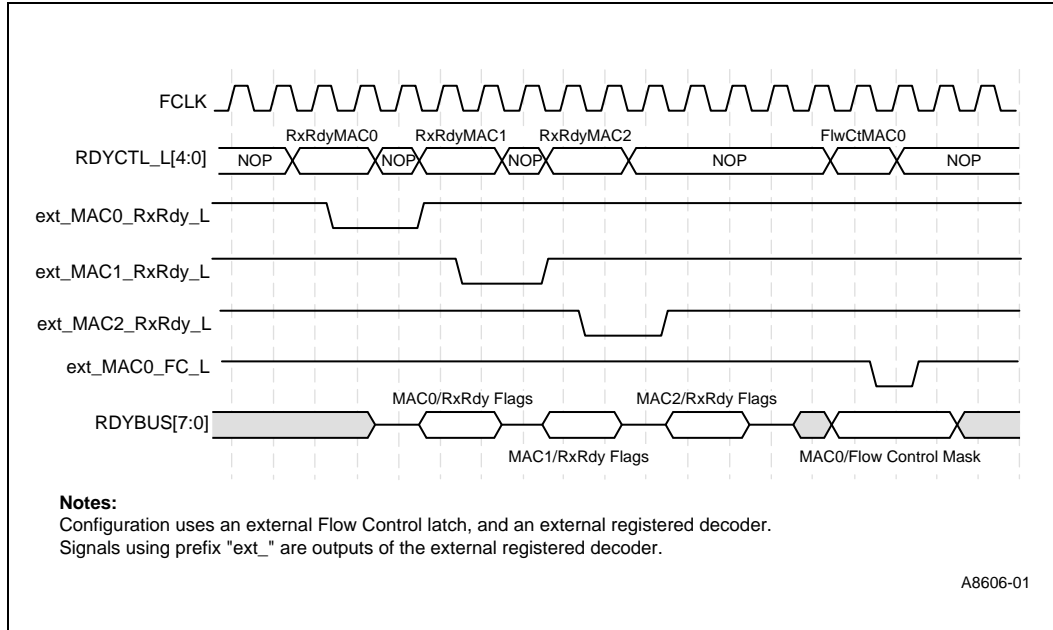
**Figure 57. Fetch Ready Flags, Get/Send Commands, 3+ MAC Mode (with External Registered Decoder) - RDYBUS\_TEMPLATE\_CTL[10]=0**



**Figure 58. Ready Bus Control Timing, Fetch Ready Flags - Flow Control - Fetch Ready Flags, 1-2 MAC Mode (with No External Registered Decoder) - RDYBUS\_TEMPLATE\_CTL[10]=1**



**Figure 59. Ready Bus Control Timing, Fetch Ready Flags - Flow Control - Fetch Ready Flags, 3+ MAC Mode (with External Registered Decoder) - RDYBUS\_TEMPLATE\_CTL[10]=0**

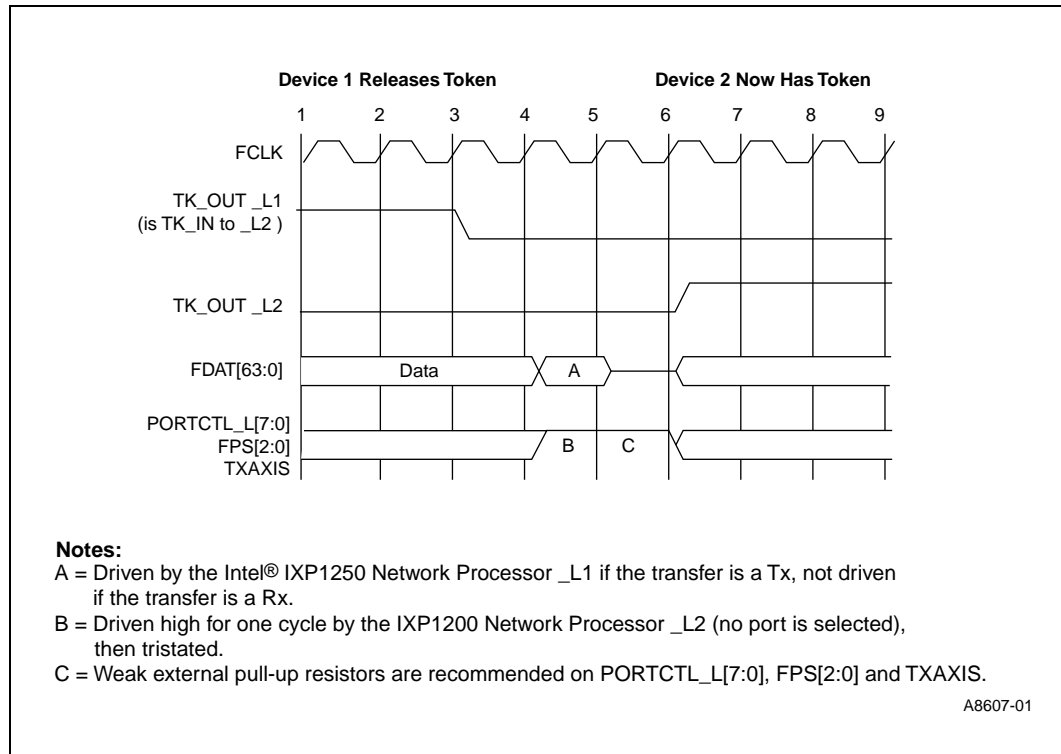


#### 4.3.7.5 TK\_IN/TK\_OUT

The following timing diagrams show the transition from one IX Bus owner to another. Note that prior to giving up the bus, the PORTCTL[4:0] signals are driven high which will not select any ports. Then the signal is tri-stated and must be held up with pullup resistors.



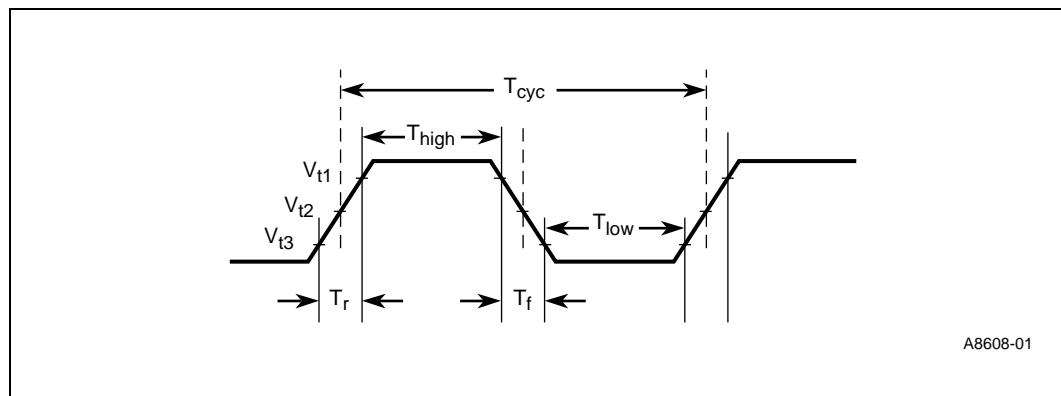
Figure 60. IX Bus Ownership Passing



### 4.3.8 SRAM Interface

#### 4.3.8.1 SRAM SCLK Signal AC Parameter Measurements

Figure 61. SRAM SCLK Signal AC Parameter Measurements



$V_{t1} = 0.5 * V_{DDX}$   
 $V_{t2} = 0.4 * V_{DDX}$   
 $V_{t3} = 0.3 * V_{DDX}$

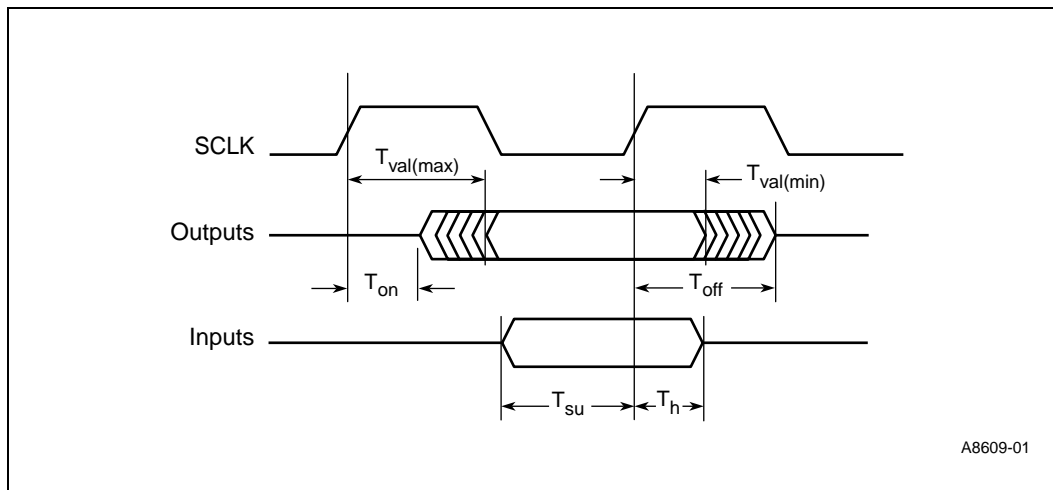
A8608-01

Table 47. SRAM SCLK Signal AC Parameter Measurements

Symbol	Parameter	Minimum (IXP1250 Core Speed)			Maximum (IXP1250 Core Speed)			Unit
		166 MHz	200 MHz	232 MHz	166 MHz	200 MHz	232 MHz	
Freq	Clock frequency	—	—	—	83	100	116	MHz
$T_{cyc}$	Cycle time	12	10	8.62	—	—	—	ns
$T_{high}$	Clock high time	4.02	4	3.3	—	—	—	ns
$T_{low}$	Clock low time	4.02	4	3.3	—	—	—	ns
$T_r, T_f$	SCLK rise/fall time	0.29	0.25	0.21	1.16	1	0.83	ns

#### 4.3.8.2 SRAM Bus Signal Timing

Figure 62. SRAM Bus Signal Timing



**Table 48. SRAM Bus Signal Timing<sup>1,2</sup>**

Symbol	Parameter	Minimum (IXP1250 Core Speed)			Maximum (IXP1250 Core Speed)			Unit
		166 MHz	200 MHz	232 MHz	166 MHz	200 MHz	232 MHz	
$T_{val}$	Clock to data output valid delay <sup>3,4</sup>	1.0	1.0	0.5	5.0	4.5	3.35	ns
$T_{ctl}$	Clock to control outputs valid delay <sup>3,4</sup>	1.25	1.0	0.5	5.0	4.5	3.05	ns
$T_{suf}$	Data input setup time before NA/SACKL for Flowthru SRAM	2	2	2	---	---	---	ns
$T_{sup}$	Data input setup time before SCLK for Pipelined SRAM <sup>5</sup>	5.5	5.0	3.10	---	---	---	ns
$T_{hf}$	Input signal hold time from NA/SACKL for Flowthru SRAM	1	1	1	---	---	---	ns
$T_{hp}$	Input signal hold time from SCLK for Pipelined SRAM	1	1	0.75	---	---	---	ns
$T_{on}^6$	Float-to-active delay from clock	1	1	1	---	---	---	ns
$T_{off}^6$	Active-to-float delay from clock	---	---	---	3	3	3	ns

1. Timing parameters assume that the system uses a zero delay clock buffer for SCLK before it is distributed to SRAM.
2. When used as a rdy input, HIGH\_EN\_L is asynchronous and can change anywhere relative to SCLK.
3. Capacitive loading effects on signal lines are shown in [Table 49](#).
4.  $T_{val}(\min)$  and 166 MHz and 200 MHz  $T_{ctl}(\min)$  parameters are tested under 0 pF load best case conditions ( $V_{dd}=2.1$ ,  $V_{ddx}=3.6$ ,  $Temp=0$  degrees C) at 1.15 nsec with an uncertainty of 0.25 nsec. The parameter specified is guaranteed by design in a minimally configured system environment.
5. Timings are what the tester must measure. Add 0.25 nsec to these numbers to obtain system AC parameter. This additional 0.25 nsec is needed to allow for SRAM drive derating.
6. Not tested. Guaranteed by design.

**Table 49. Signal Delay Deratings for  $T_{val}$  and  $T_{ctl}$** 

Signal	Maximum Derating (ns/pF) (IX Bus Speed)			Minimum Derating (ns/pF) (IX Bus Speed)		
	83 MHz	100 MHz	116 MHz	83 MHz	100 MHz	116 MHz
SCLK	0.053	—	—	0.025	—	—
SLOW_EN_L	0.065	0.06	0.031	0.03	0.025	0.015
SWE_L	0.065	0.06	0.031	0.03	0.025	0.015
MRD_L	0.065	0.06	0.031	0.03	0.025	0.015
MCE_L	0.065	0.06	0.031	0.03	0.025	0.015
SOE_L	0.065	0.06	0.031	0.03	0.025	0.015
HIGH_EN_L	0.065	0.06	0.031	0.03	0.025	0.015
LOW_EN_L	0.065	0.06	0.031	0.03	0.025	0.015
CE_L[3:0]	0.065	0.06	0.031	0.03	0.025	0.015
A[18:0]	0.065	0.06	0.031	0.03	0.025	0.015
DQ[31:0]	0.065	0.06	0.031	0.03	0.025	0.015
FWE_L	0.065	0.06	0.031	0.03	0.025	0.015

### 4.3.8.3 SRAM Bus - SRAM Signal Protocol and Timing

Figure 63. Pipelined SRAM Read Burst of Eight Longwords

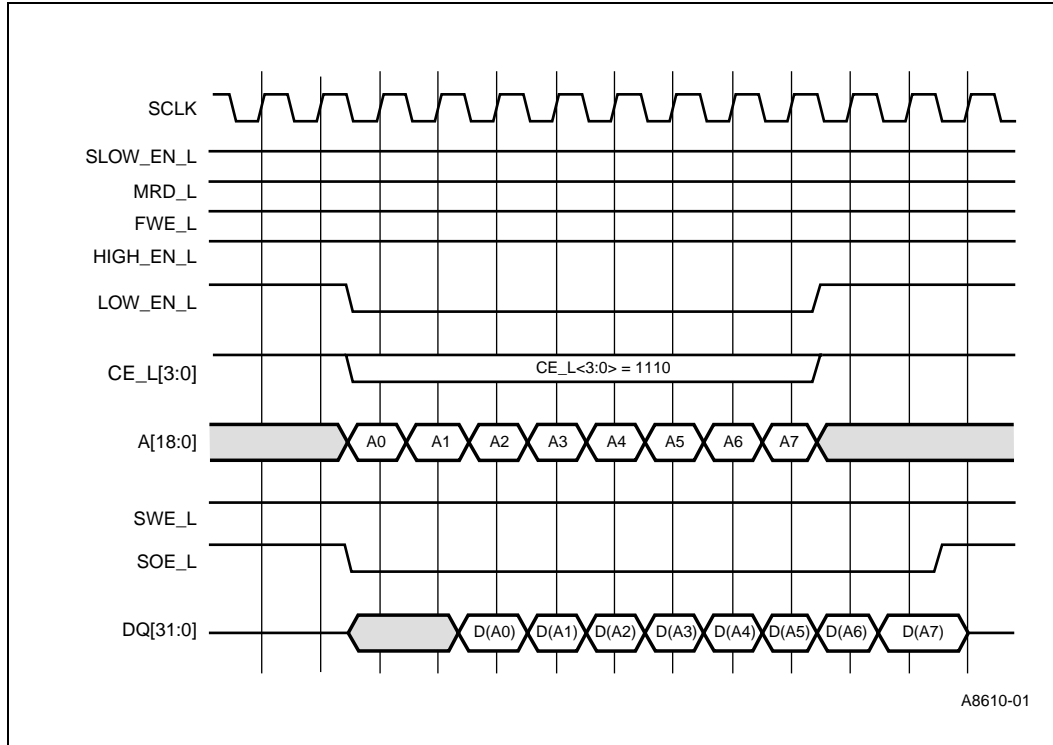
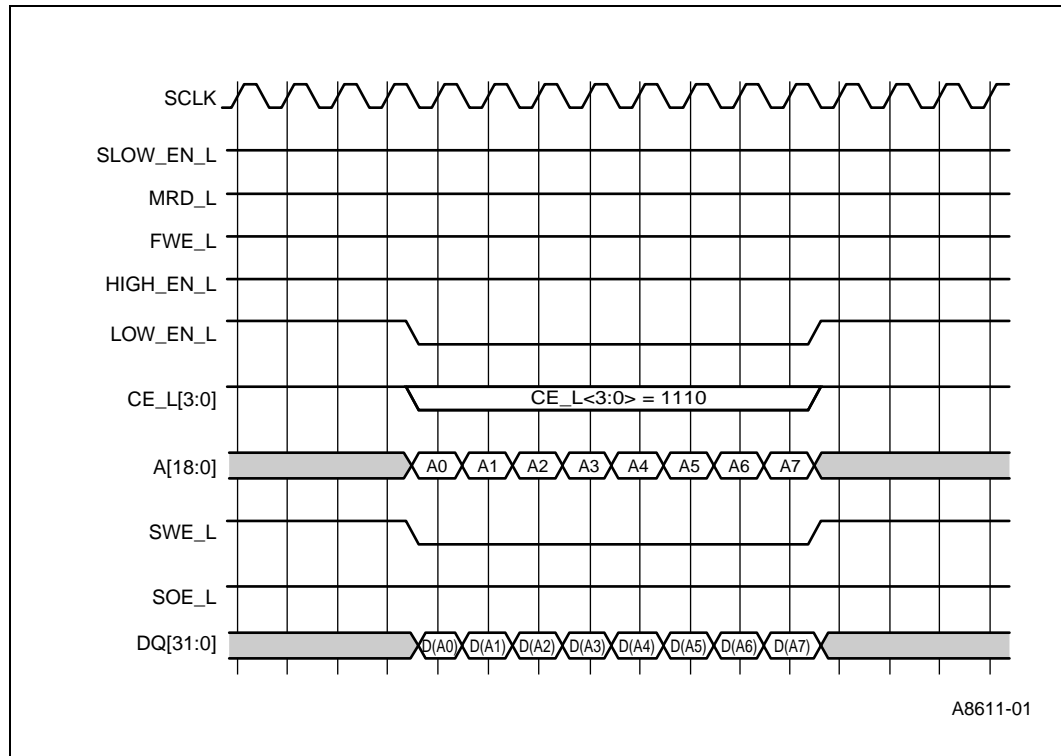
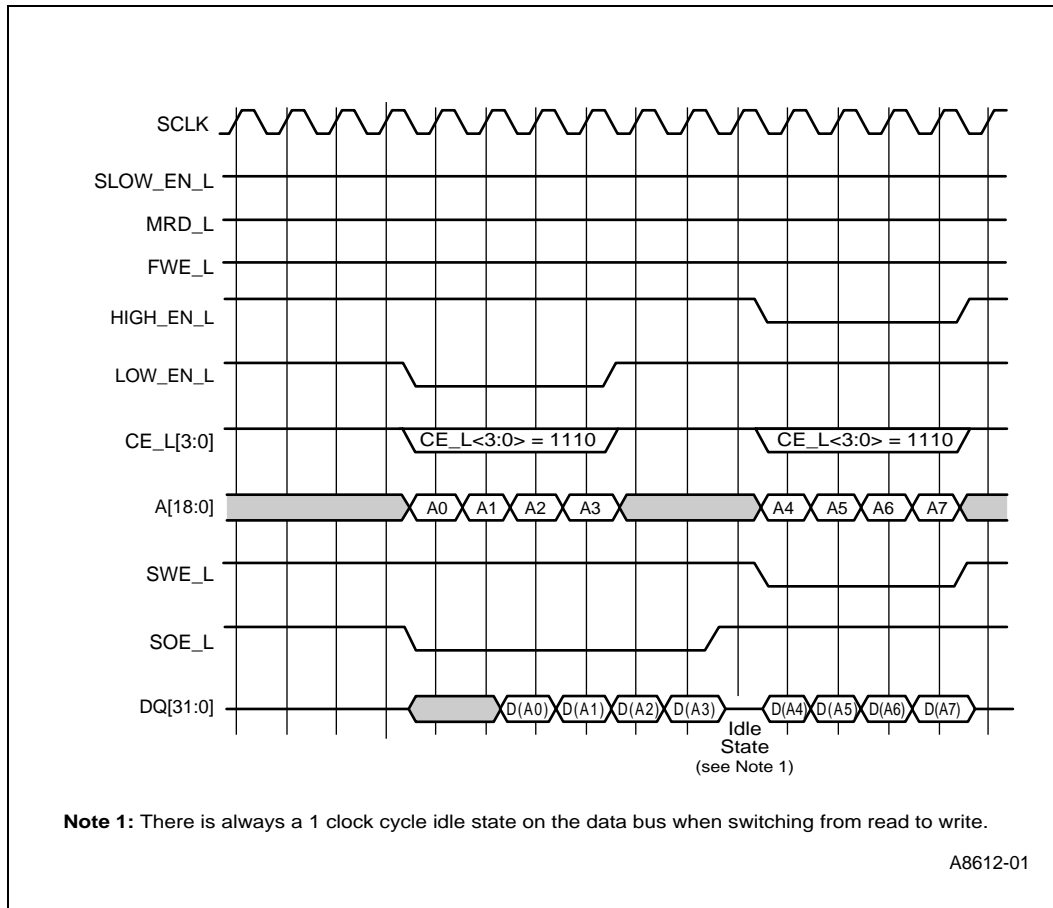


Figure 64. Pipelined SRAM Write Burst of Eight Longwords



**Figure 65. Pipelined SRAM Read Burst of Four From Bank 0 Followed by Write Burst of Four From Bank 8**



**Figure 66. Pipelined SRAM Longword Write Followed by 2 Longword Burst Read Followed by 4 Longword Burst Write**

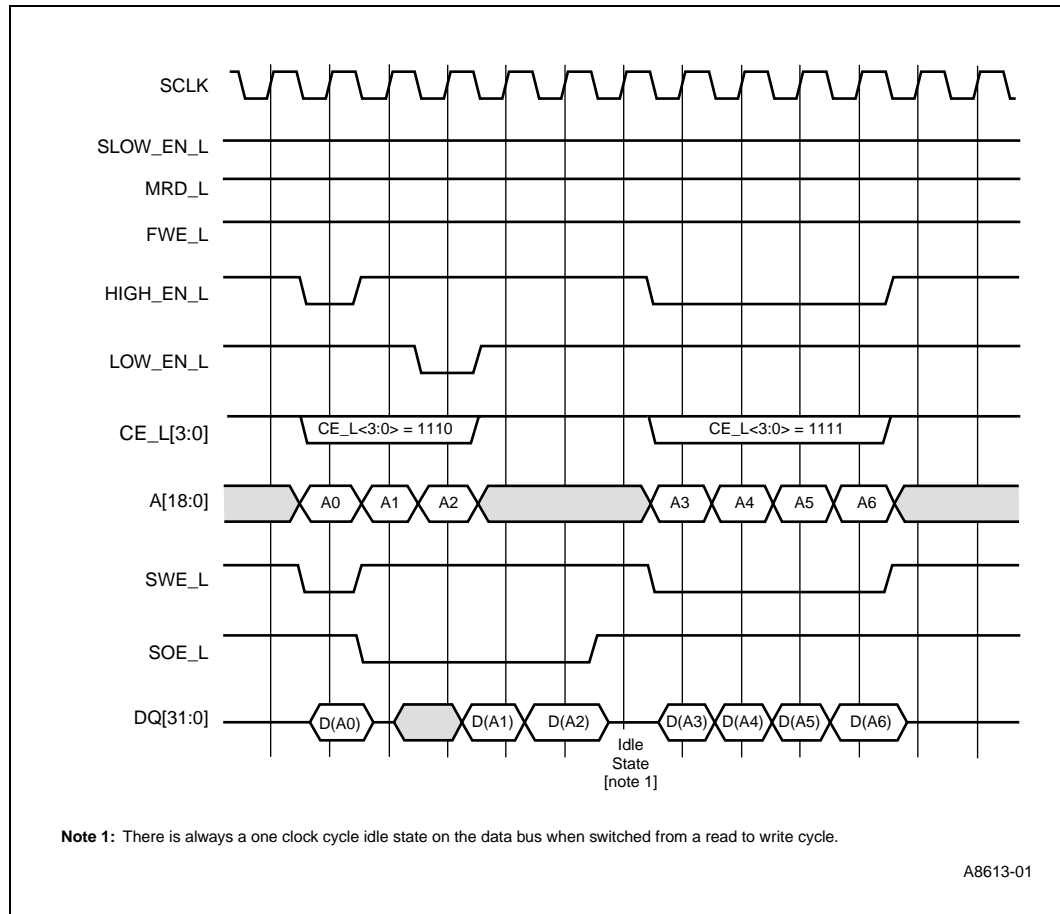
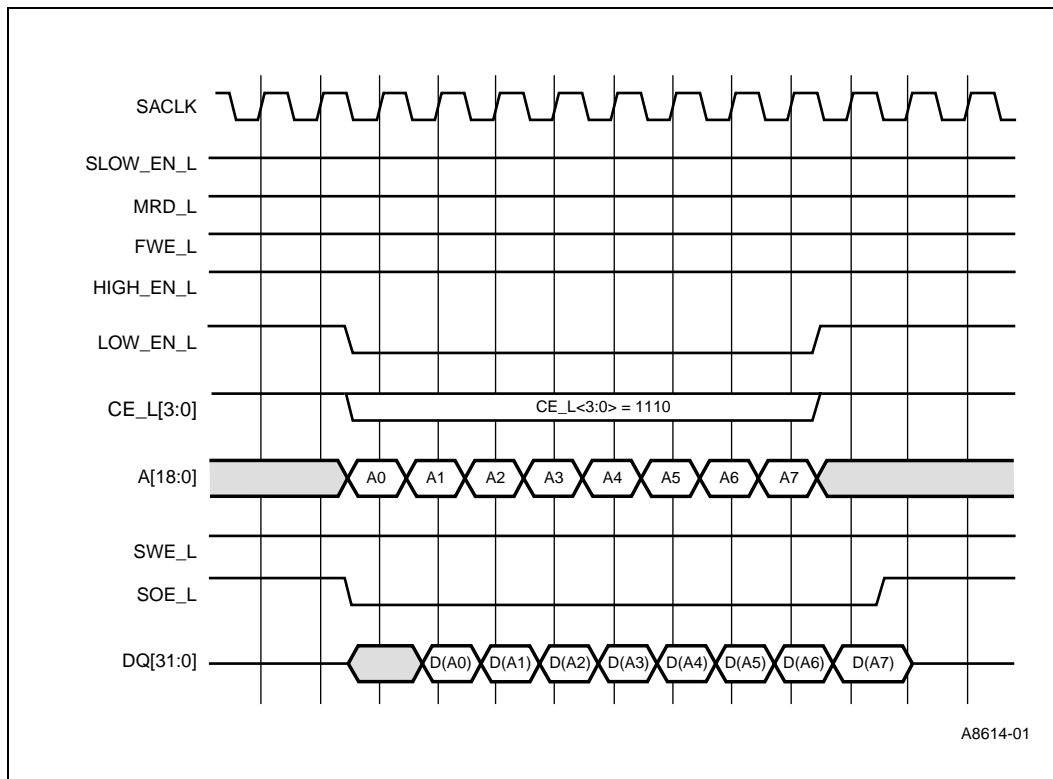


Figure 67. Flowthrough SRAM Read Burst of Eight Longwords





### 4.3.8.4 SRAM Bus - BootROM and SlowPort Timings

Timing for the BootROM and SlowPort areas are programmable through the SRAM configuration registers described in the *IXP1200 Network Processor Family Microcode Programmer's Reference Manual Manual*. The designer should refer to this manual to understand restrictions in selecting timing values. Each timing illustration shows the appropriate register settings to generate the timing shown.

### 4.3.8.5 SRAM Bus - BootRom Signal Protocol and Timing

Figure 68. BootROM Read

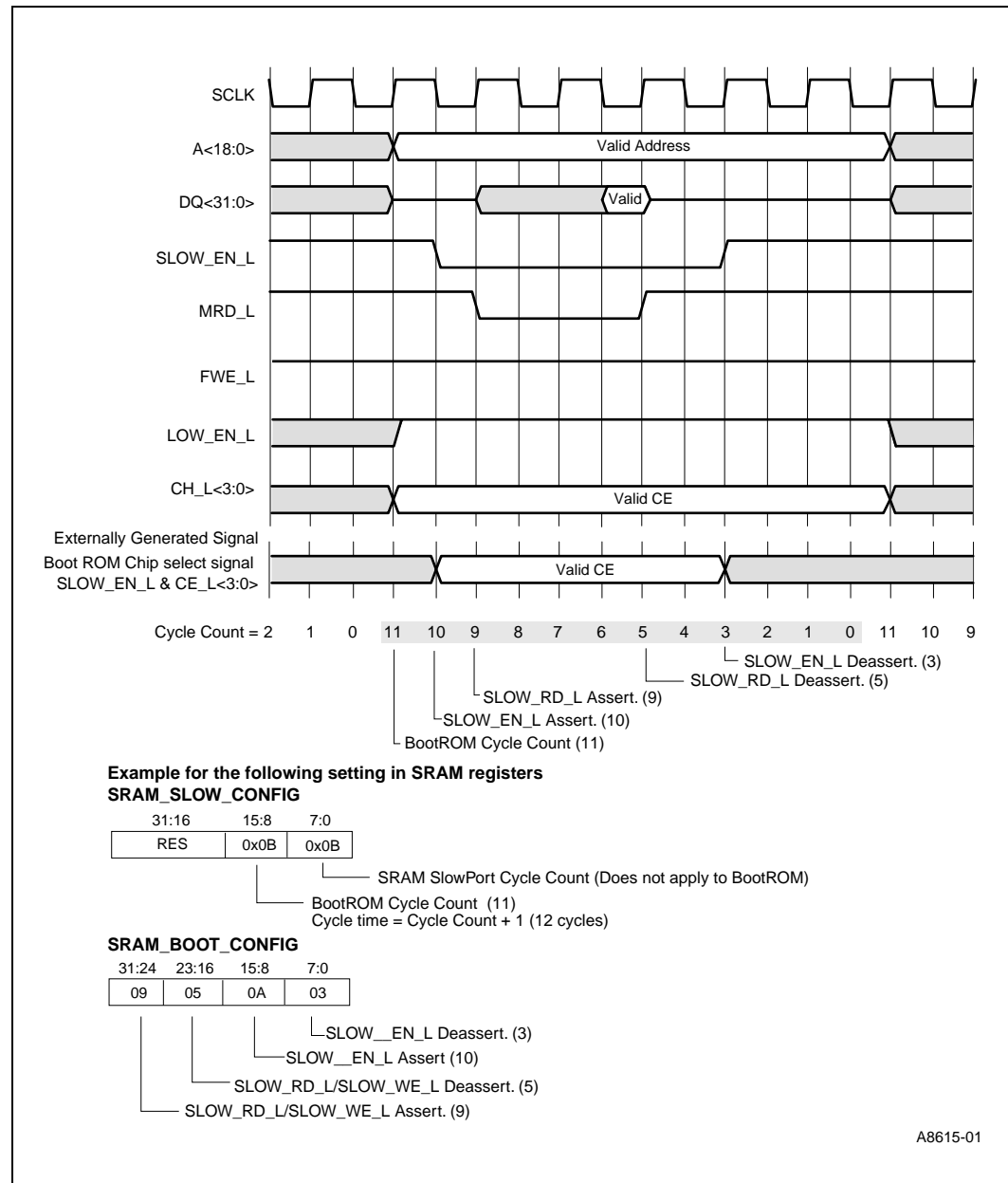


Figure 69. BootROM Write

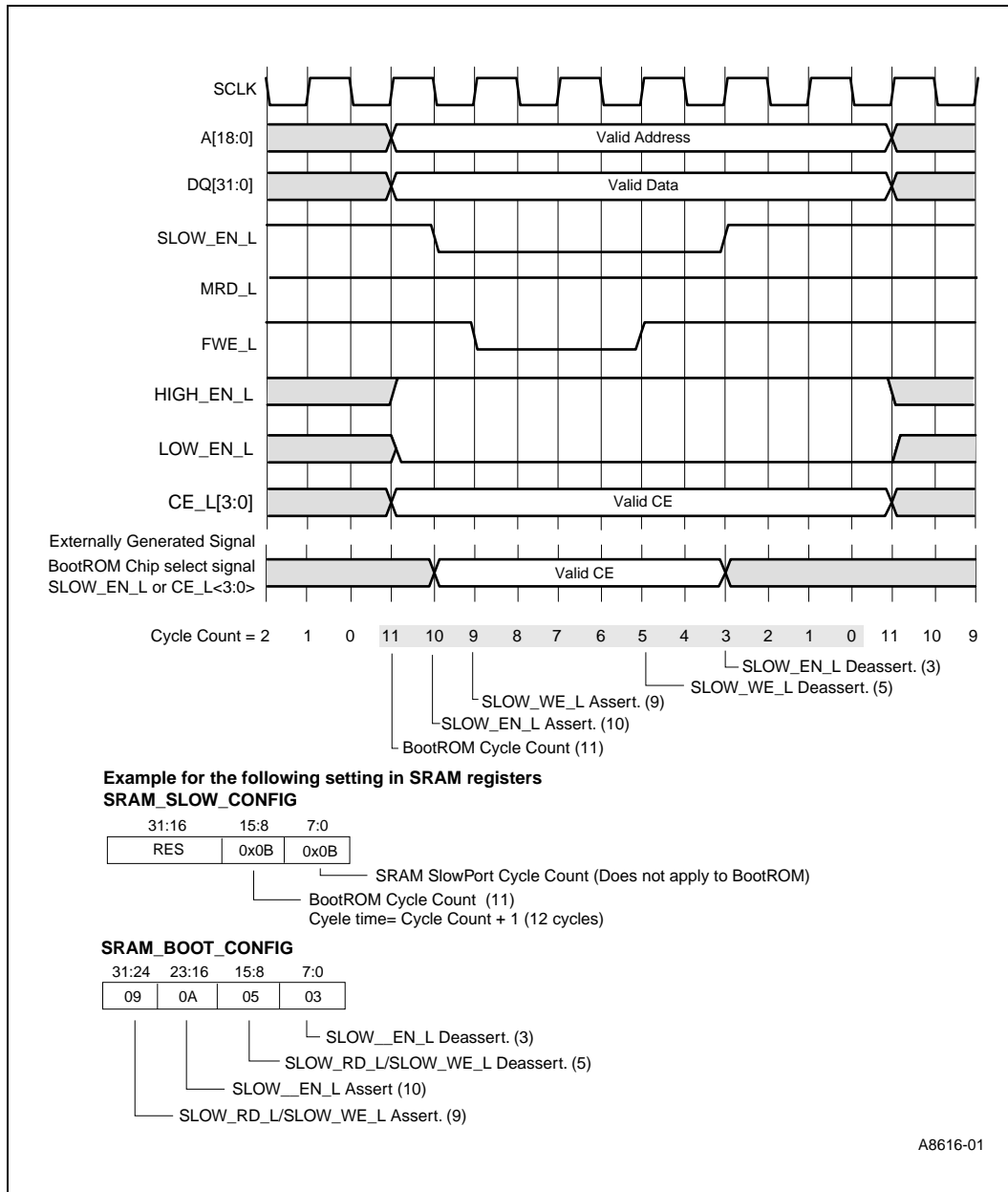
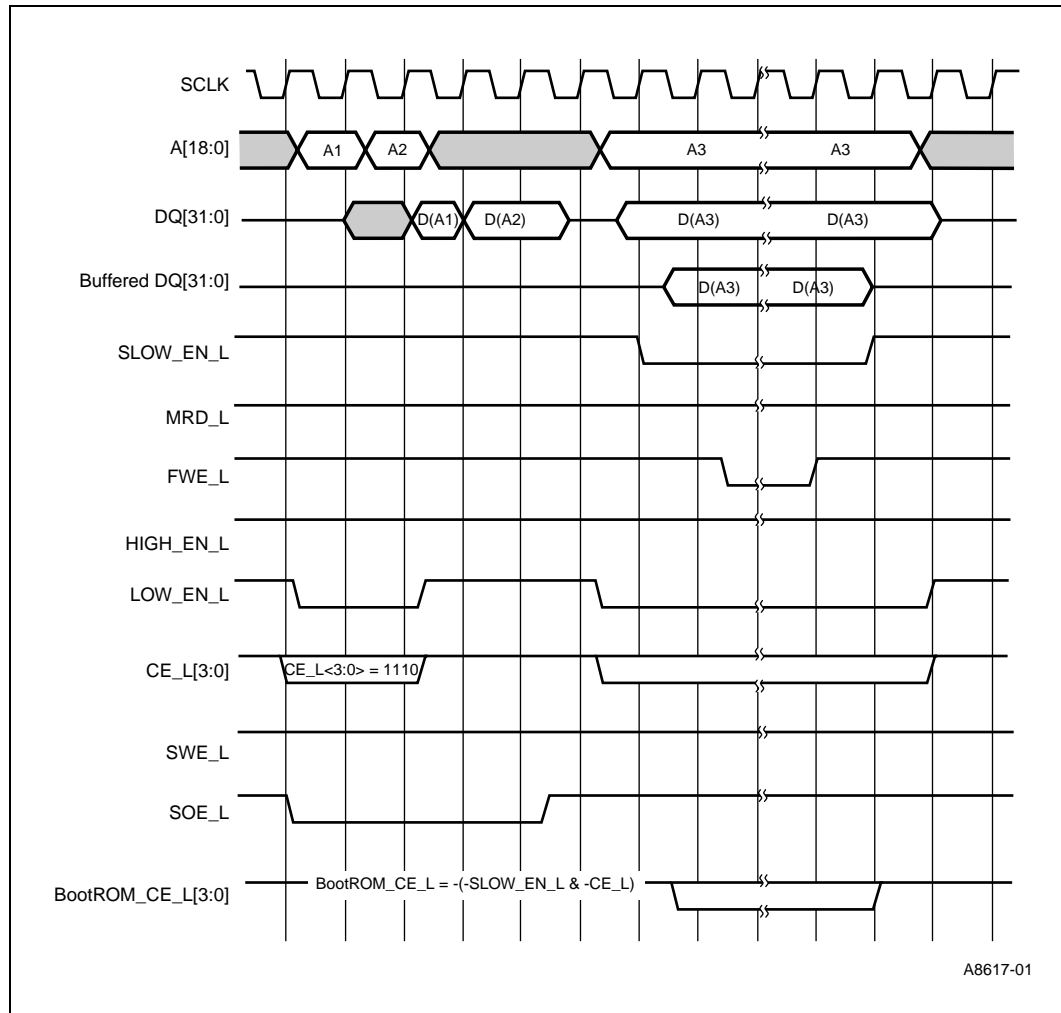


Figure 70. Pipelined SRAM Two Longword Burst Read Followed by BootROM Write



### 4.3.8.6 SRAM Bus - Slow-Port Device Signal Protocol and Timing

Figure 71. SRAM SlowPort Read

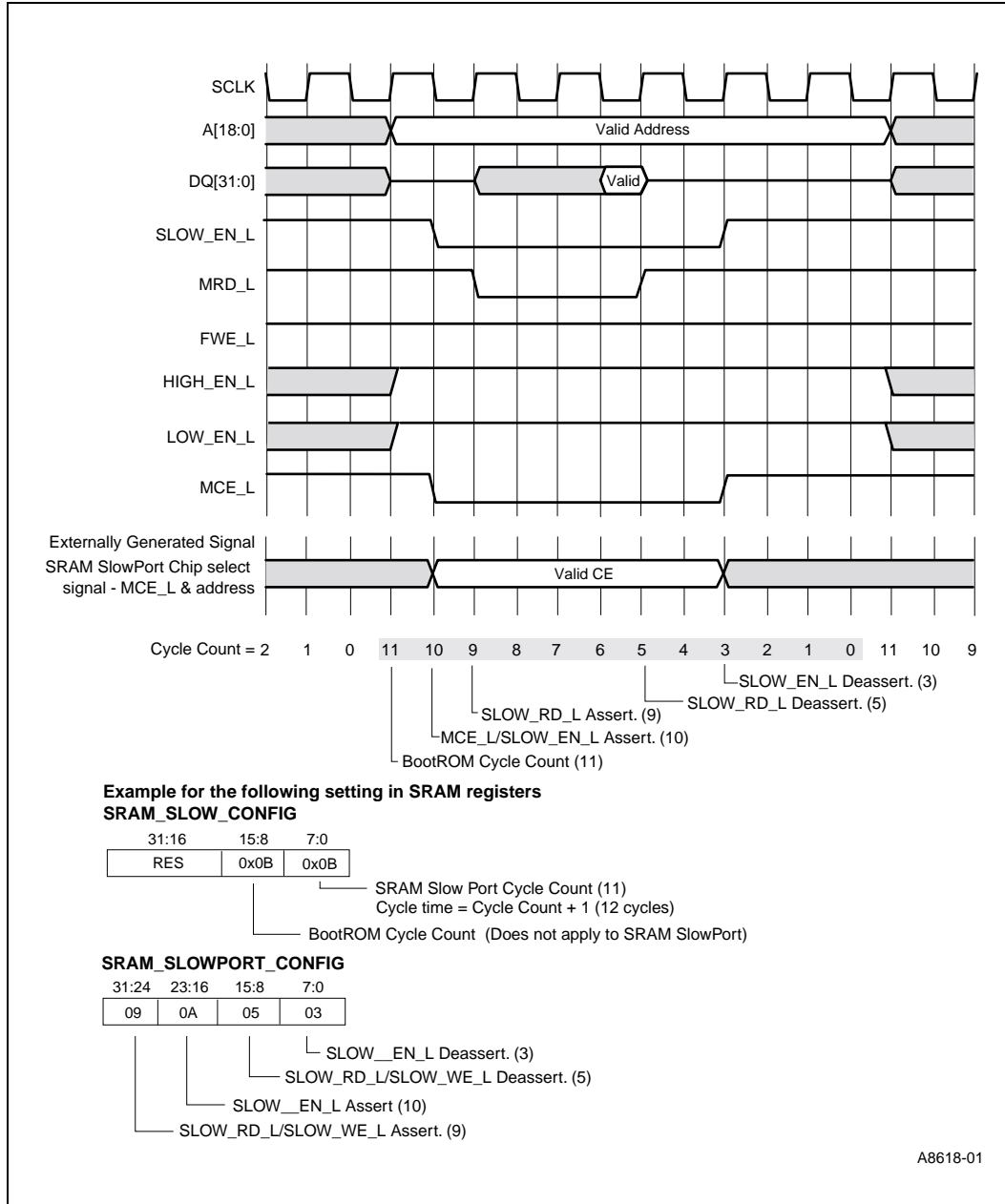


Figure 72. SRAM SlowPort Write

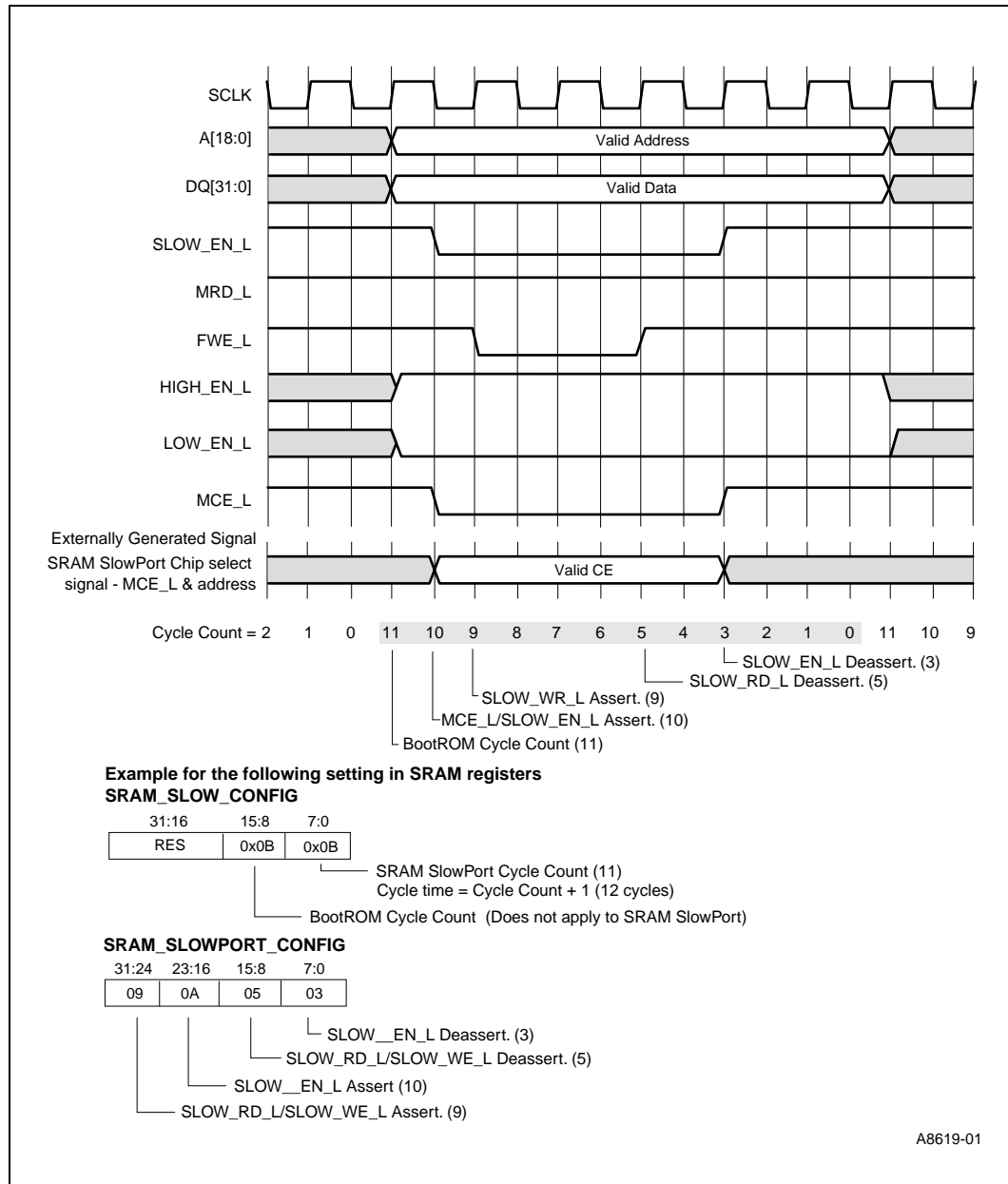


Figure 73. SRAM SlowPort RDY\_L

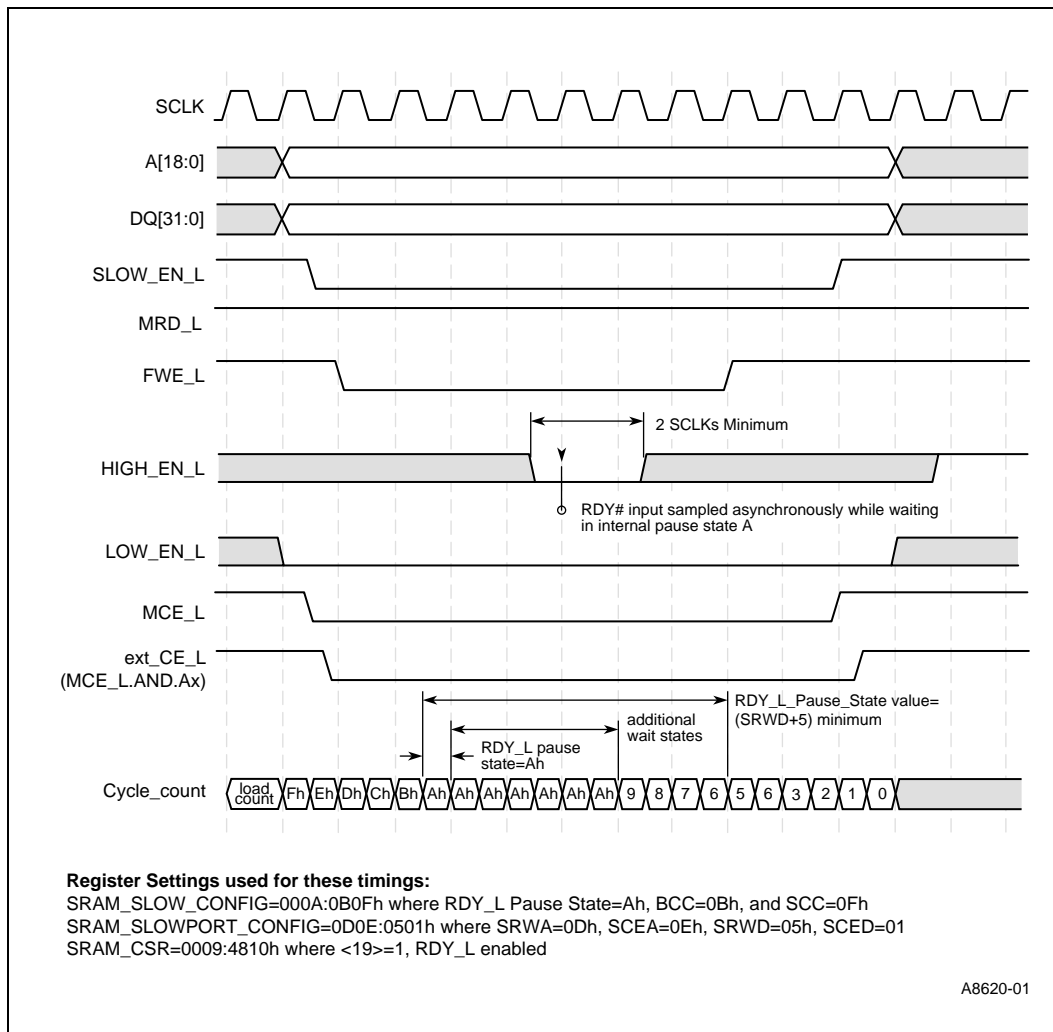
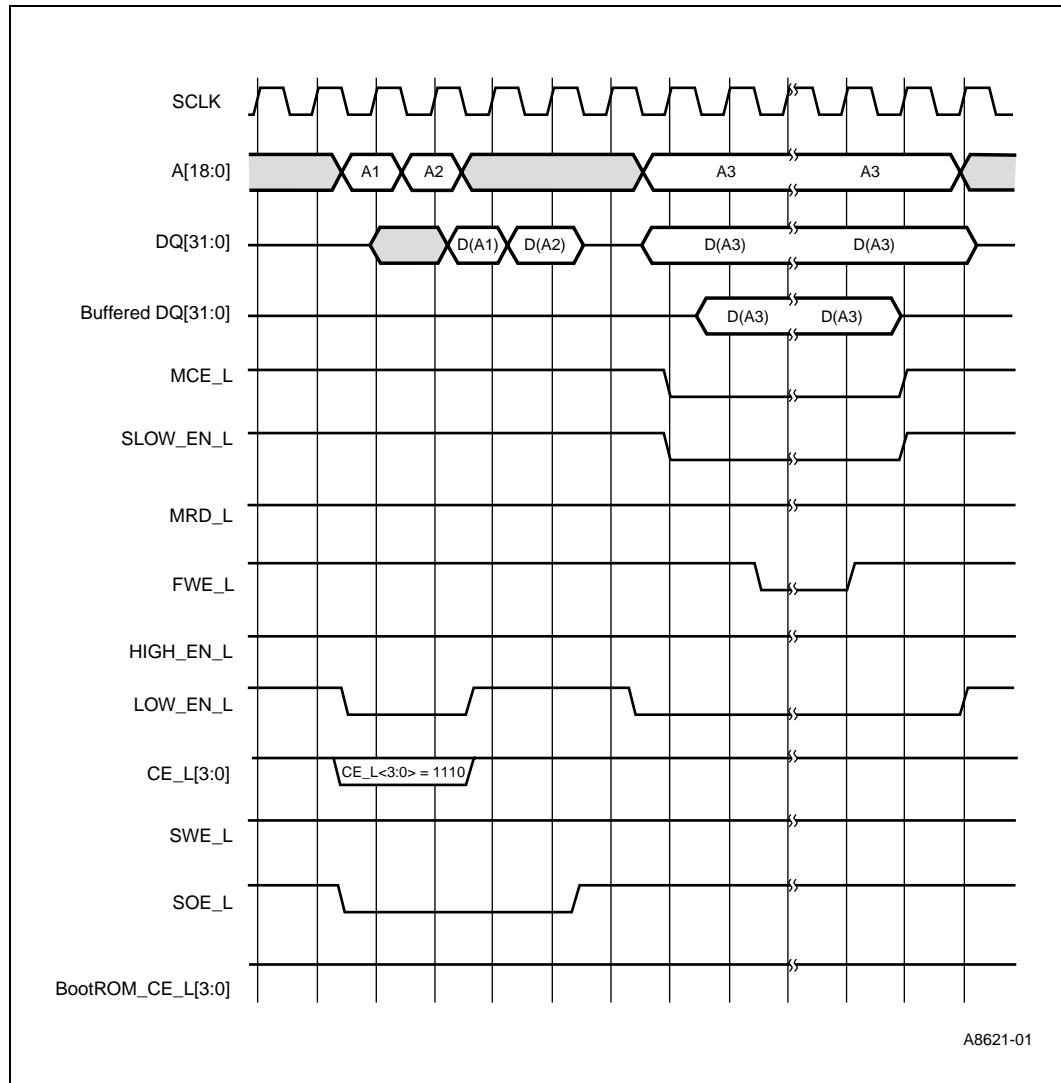


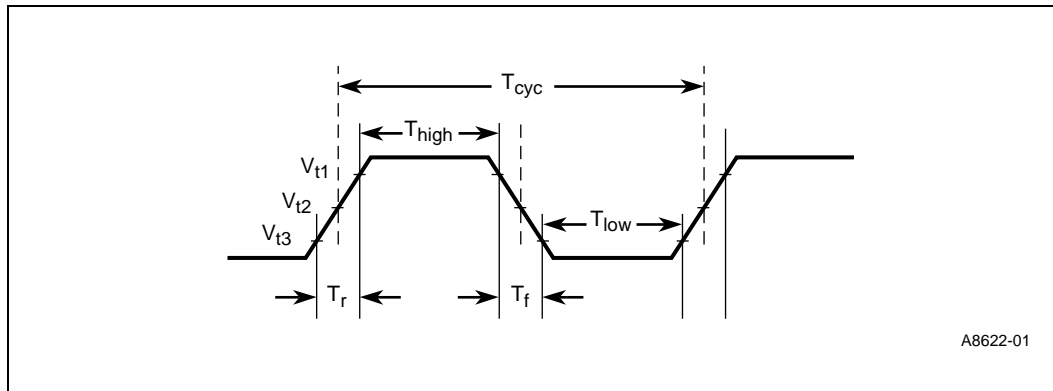
Figure 74. Pipelined SRAM Two Longword Burst Read Followed By SlowPort Write



## 4.3.9 SDRAM Interface

### 4.3.9.1 SDCLK AC Parameter Measurements

Figure 75. SDCLK AC Timing Diagram



$V_{t1} = 0.5 \cdot V_{DDX}$   
 $V_{t2} = 0.4 \cdot V_{DDX}$   
 $V_{t3} = 0.3 \cdot V_{DDX}$

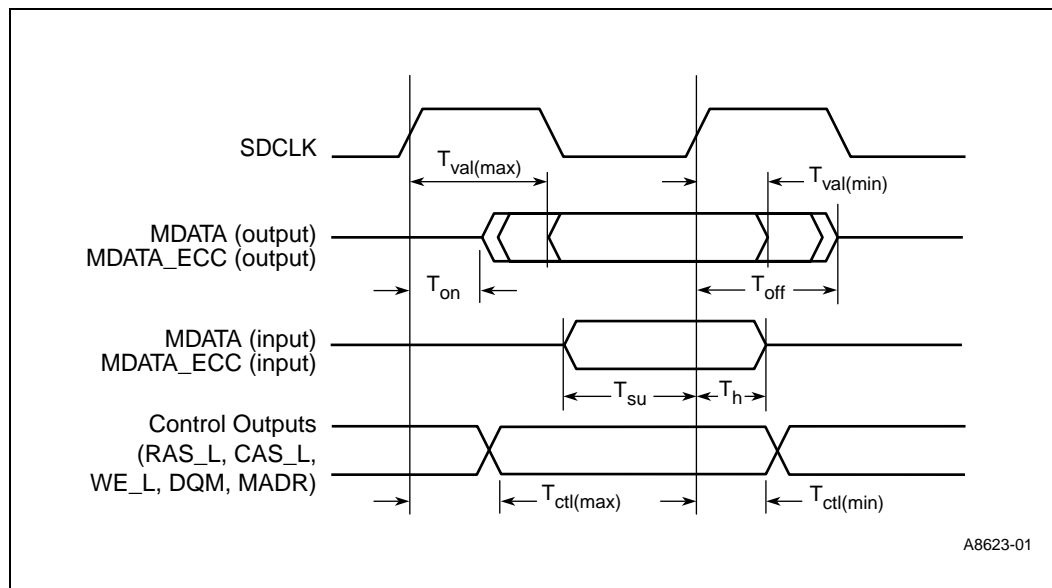
Table 50. SDCLK AC Parameter Measurements

Symbol	Parameter	Minimum (IXP1250 Core Speed)			Maximum (IXP1250 Core Speed)			Unit
		166 MHz	200 MHz	232 MHz	166 MHz	200 MHz	232 MHz	
Freq	Clock frequency	—	—	—	83	100	116	MHz
$T_{cyc}$	Cycle time	12	10	8.62	—	—	—	ns
$T_{high}$	Clock high time	4.02	4	3.3	—	—	—	ns
$T_{low}$	Clock low time	4.02	4	3.3	—	—	—	ns
$T_r, T_f$	SDCLK rise/fall time	0.29	0.25	0.21	1.16	1	0.83	ns



### 4.3.9.2 SDRAM Bus Signal Timing

Figure 76. SDRAM Bus Signal Timing



A8623-01

Table 51. SDRAM Bus Signal Timing Parameters<sup>1</sup>

Symbol	Parameter	Minimum (IXP1250 Core Speed)			Maximum (IXP1250 Core Speed)			Unit
		166 MHz	200 MHz	232 MHz	166 MHz	200 MHz	232 MHz	
$T_{val}$	Clock to data output valid delay <sup>2,3</sup>	1.25	1.0	0.5	4.5	4.0	3.3	ns
$T_{ctl}$	SDCLK to control output valid delay <sup>2,3</sup>	1.25	1.0	0.5	4.5	4.0	2.90	ns
$T_{su}$	Data input setup time before SDCLK <sup>4</sup>	4.25	3.70	3.70	---	---	---	ns
$T_h$	Data input hold time from SDCLK	1	1	0.75	---	---	---	ns
$T_{on}^5$	Float to data driven delay from SDCLK	1.25	1	0.75	---	---	---	ns
$T_{off}^5$	Data driven to float delay from SDCLK	---	---	---	3	3	3	ns

1. Timing parameters assume that the system uses a zero delay clock buffer for SDCLK before it is distributed to SDRAM.
2. Capacitive loading effects on signal lines are shown in Table 52.
3.  $T_{val}(\min)$  and 166 MHz and 200 MHz  $T_{ctl}(\min)$  parameters are tested under 0 pF load best case conditions ( $V_{dd}=2.1$ ,  $V_{ddx}=3.6$ ,  $Temp=0$  degrees C) at 1.15 nsec with an uncertainty of 0.25 nsec. The parameter specified is guaranteed by design in a minimally configured system environment.
4. Unlike the SRAM setup timing parameter  $T_{sup}$ , the  $T_{su}$  timings are both what the tester must measure and what the SDRAM parts will deliver. Increased performance on the SDRAM bus occurs because the data pins only drive one load.
5. Not tested. Guaranteed by design.

Table 52. Signal Delay Deratings for  $T_{val}$  and  $T_{ctf}$ 

Signal	Maximum Derating (ns/pF) (IX Bus Speed)			Minimum Derating (ns/pF) (IX Bus Speed)		
	83 MHz	100 MHz	116 MHz	83 MHz	100 MHz	116 MHz
SDCLK	0.053	—	—	0.025	—	—
DQM	0.065	0.06	0.031	0.03	0.025	0.015
WE_L	0.065	0.06	0.031	0.03	0.025	0.015
RAS_L	0.065	0.06	0.031	0.03	0.025	0.015
CAS_L	0.065	0.06	0.031	0.03	0.025	0.015
MADR[14:0]	0.065	0.06	0.031	0.03	0.025	0.015
MDATA[63:0]	0.095	0.09	0.035	0.03	0.025	0.015
MDATA_ECC[7:0]	0.095	0.09	0.035	0.03	0.025	0.015

### 4.3.9.3 SDRAM Signal Protocol

This section describes the SDRAM timing parameters referenced in the SDRAM timing diagrams that follow. This nomenclature is consistent with most JEDEC standard SDRAM devices.

#### tRP

tRP is the minimum number of cycles after a precharge cycle that a bank may be opened (or "RASd"). The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tRP Precharge Time. Also referred to as "PRECHARGE command period" in SDRAM datasheets.

#### tRASmin

tRASmin is the minimum number of cycles that a bank must be open before it can be closed using a precharge command. The maximum time that a bank may be open, tRASmax, is not checked, because the IXP1250 SDRAM Controller methodology is to close all banks after the usage is complete. The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tRASmin Active Command Period. Also referred to as "ACTIVE to PRECHARGE command period" in SDRAM datasheets.

#### tRCD

tRCD is the number of cycles between the bank opening (or "RAS") and any read or write command (or "CAS"). The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tRCD RAS to CAS Delay. Also referred to as "ACTIVE to READ or WRITE delay" in SDRAM datasheets.

#### tRRD

tRRD is the number of cycles between successive bank openings, or RAS cycles. The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tRRD Bank to Bank Delay Time. Also referred to as "ACTIVE bank A to ACTIVE bank B command" in SDRAM datasheets.

#### tRC

tRC is the SDRAM bank cycle time, indicating that the minimum time that a command may be active. For most cases, this is the sum of tRP and tRASmin, although there are some SDRAM data sheets where the absolute time for tRC (in ns) is not equal to the sum (in ns) of tRP and tRASmin. In these cases, typically when rounding up to an even number of clock cycles, they are equivalent. Since the SDRAM Controller CSRs are programmed with a number of clock cycles, these

SDRAMs timing values would appear consistent. tRC is used only to specify the number of cycles between Refresh cycles during initialization of the SDRAM parts. It is possible to eliminate it altogether, and simply have this time be the sum of tRP and tRASmin, as discussed above. The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tRC Bank Cycle Time. Also referred to as "ACTIVE to ACTIVE command period" in SDRAM datasheets.

#### **tDPL**

tDPL is the number of cycles after the final data write that a precharge may occur. tDPL = 1 indicates that a precharge may occur on the next cycle. The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tDPL Data In to Precharge Time. Also referred to as "Data-in to PRECHARGE command time" in SDRAM datasheets.

#### **tDQZ**

tDQZ indicates the number of cycles of latency after DQM is seen that the SDRAMs will go into a high-impedance state. For tDQZ = 2, DQM get sampled on the first edge, the SDRAMs get off the bus on the next edge, and the bus may be driven on the third edge. The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tDQZ DQM Data Out Disable Latency. Also referred to as "DQM to data high-impedance during READs" in SDRAM datasheets.

#### **tRWT**

Note that for most designs, there may be a requirement to add one or more dead cycles after the SDRAMs get off the bus to avoid possible bus contention on the DQM bus. This will be a function of the design itself (i.e., component placement, bus loading, the SDRAMs used and tHZ, the time that it takes for the SDRAM to go to a high-Z state) and the frequency at which the SDRAM interface is running. If extra dead cycles are necessary on a write following read bus turnaround, the tRWT should be programmed to a non-zero value. If tRWT is one, then one dead cycle will be added following the completion of a read prior to a write access taking place. The *IXP1200 Network Processor Family Microcode Programmer's Reference Manual* refers to this as the tRWT Read/write Turnaround Time. Not explicitly specified in SDRAM data sheets, but is a function of memory system design, loading. Most PC100 type SDRAM devices allow a zero-delay read-write turnaround. However, tHZmax for PC100 devices is 5.4ns (CASL=2) or 7 ns (CASL=3) and tON for the IXP1250 is 1 ns, so a 1 clock tRWT would be required to avoid bus contention.

Figure 77. SDRAM Initialization Sequence

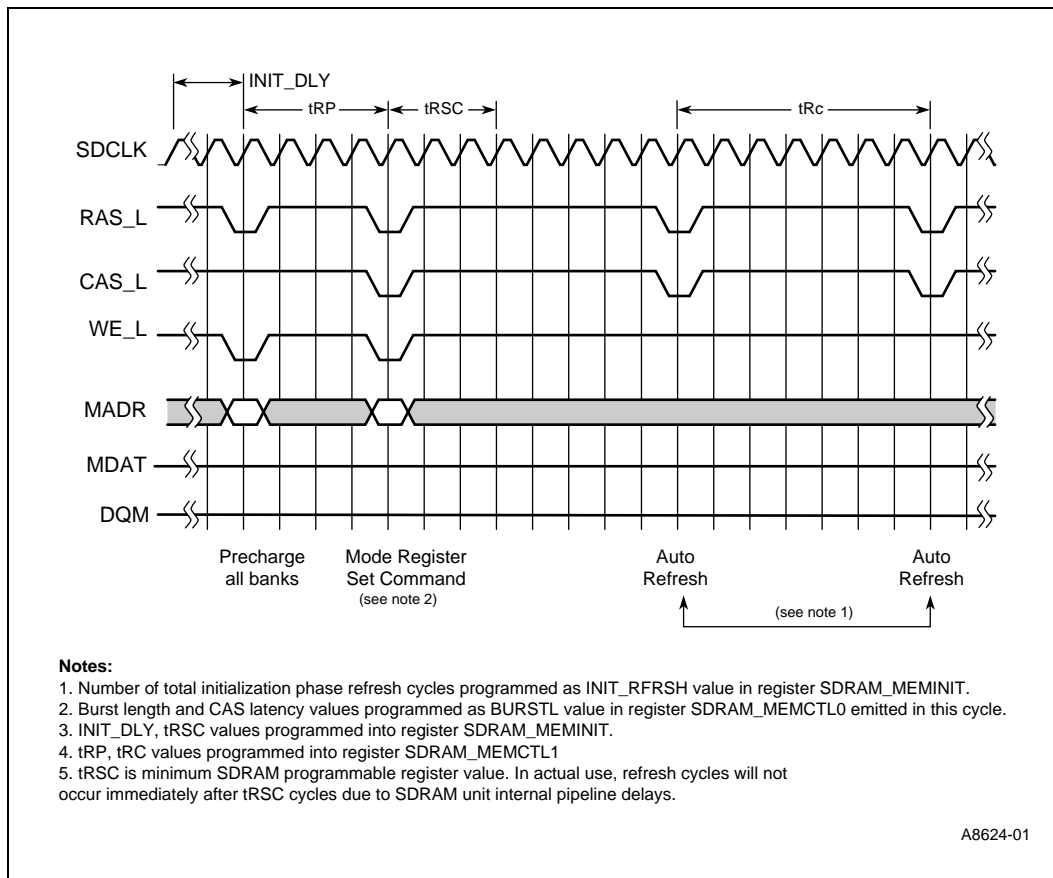


Figure 78. SDRAM Read Cycle

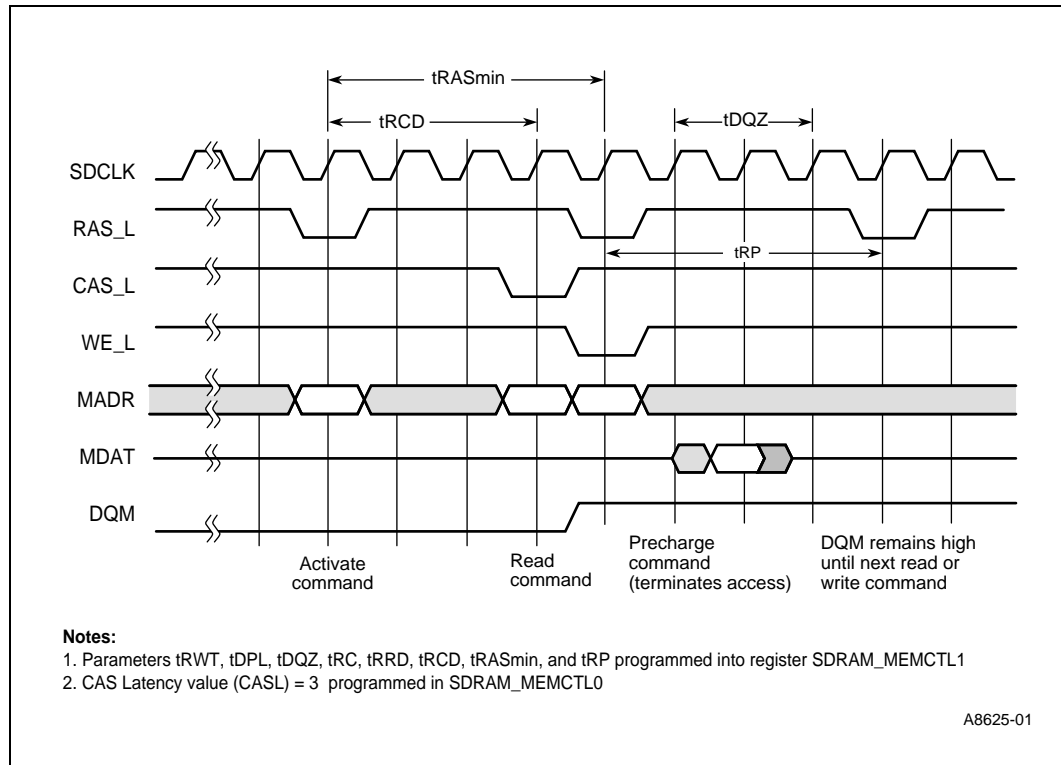


Figure 79. SDRAM Write Cycle

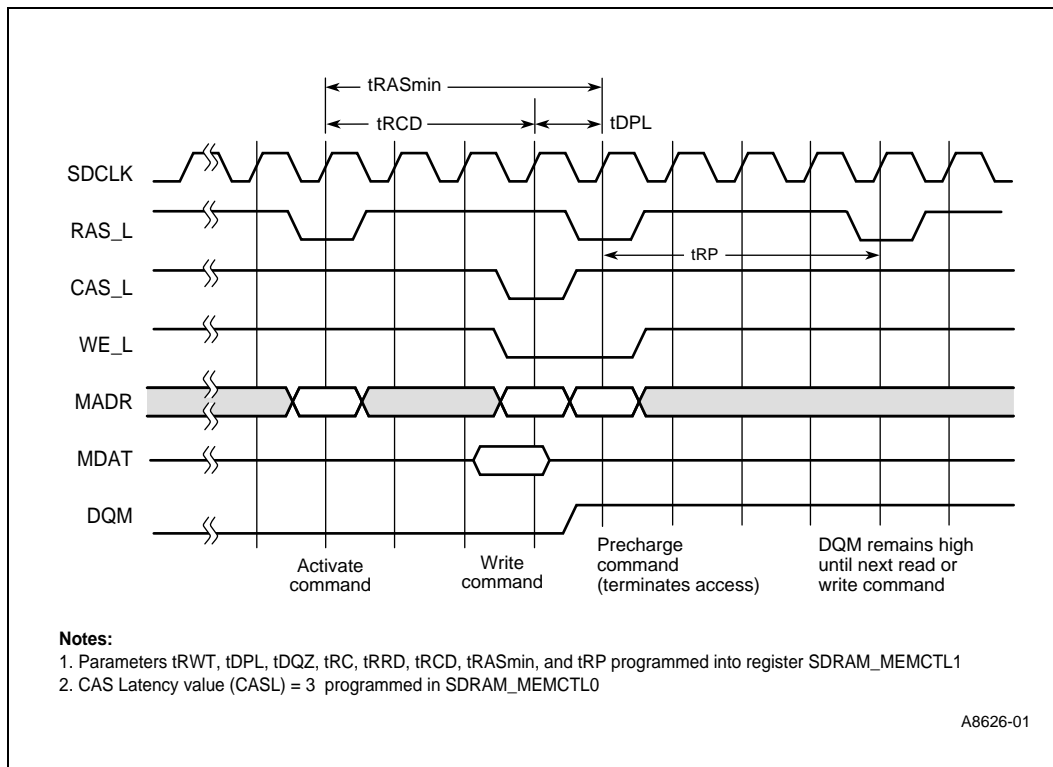
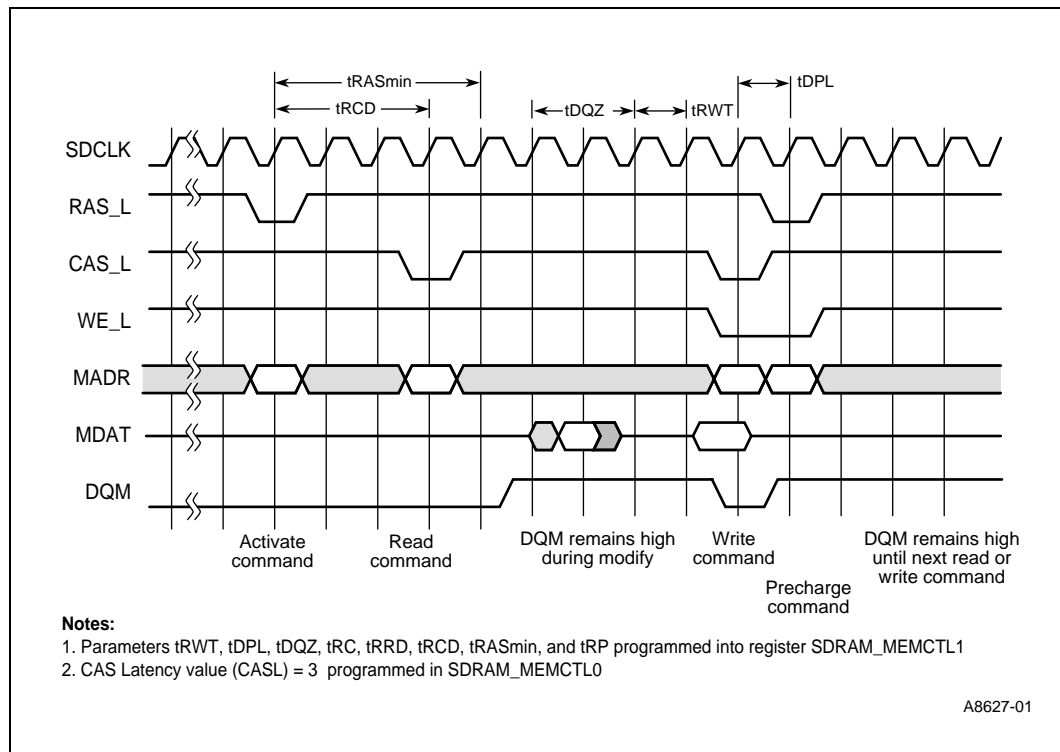


Figure 80. SDRAM Read-Modify-Write Cycle



## 4.4 Asynchronous Signal Timing Descriptions

**RESET\_IN\_L** Must remain asserted for 150 ms after VDD and VDDX are stable to properly reset the IXP1250.

**RESET\_OUT\_LIs** asserted for all types of reset (hard, watchdog, and software) and appears on the pin asynchronously to all clocks.

**GPIO[3:0]** Are read and written under software control. When writing a value to these pins, the pins transition approximately 20 ns after the write is performed. When reading these pins, the signal is first synchronized to the internal clock and must be valid for at least 20 ns before it is visible to a processor read.

**TXD, RXD** Are asynchronous relative to any device outside the IXP1250.

## 5.0 Mechanical Specifications

### 5.1 Package Dimensions

The IXP1250 is contained in a 520-HL-PBGA package, as shown in [Figure 81](#).

**Figure 81. IXP1250 Part Marking**

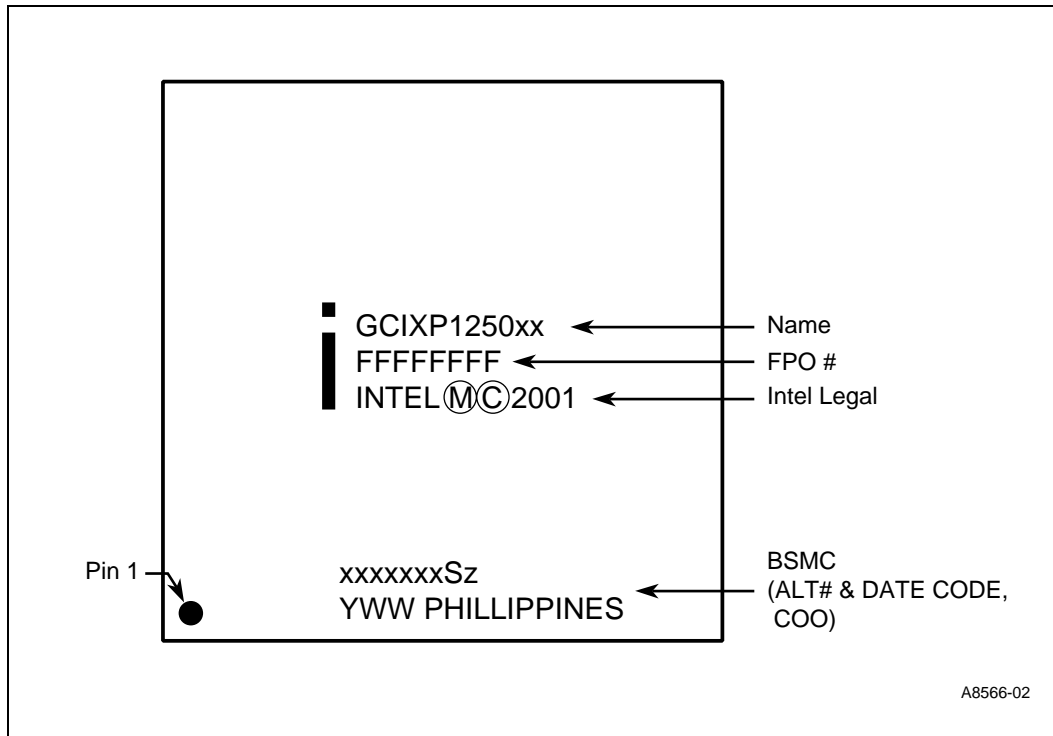




Figure 82. 520-HL-PBGA Package - Bottom View

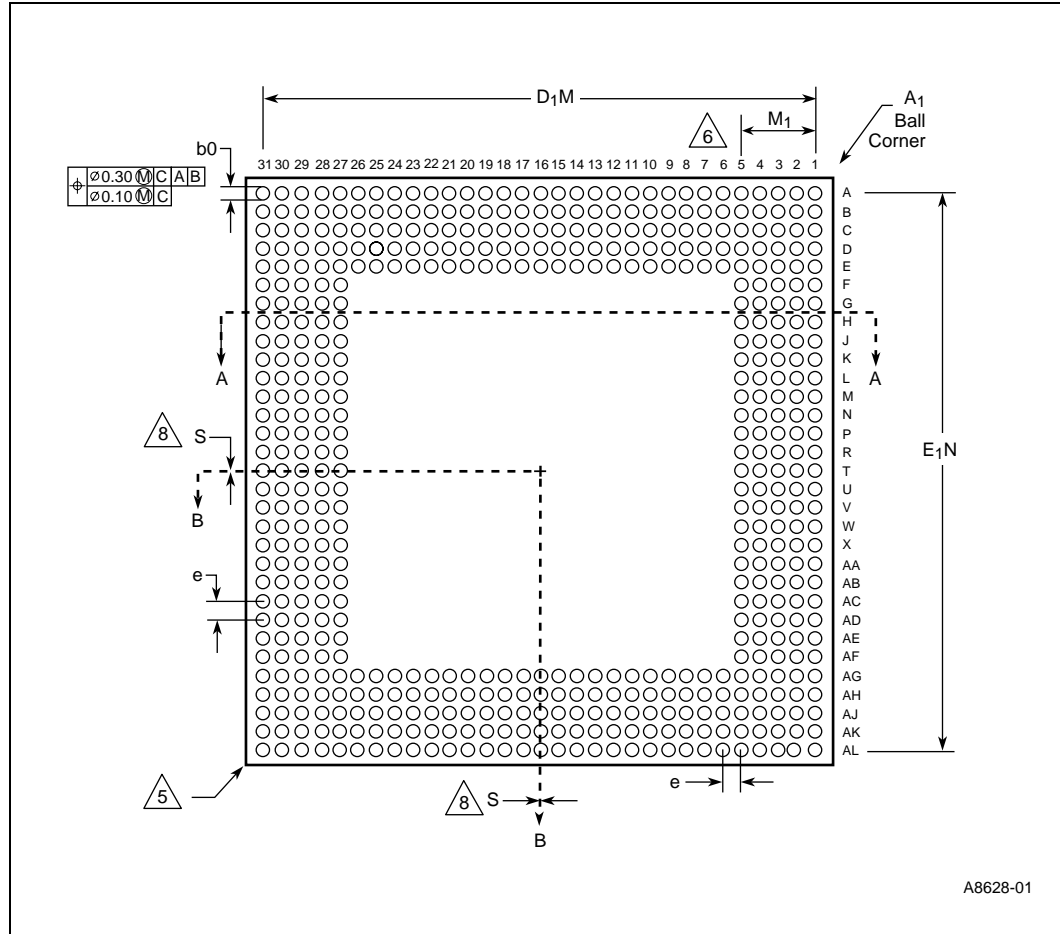


Figure 83. IXP1250 Side View

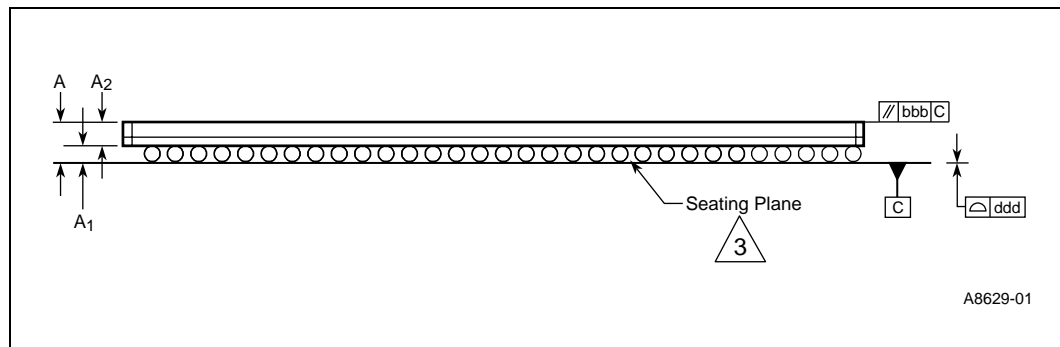
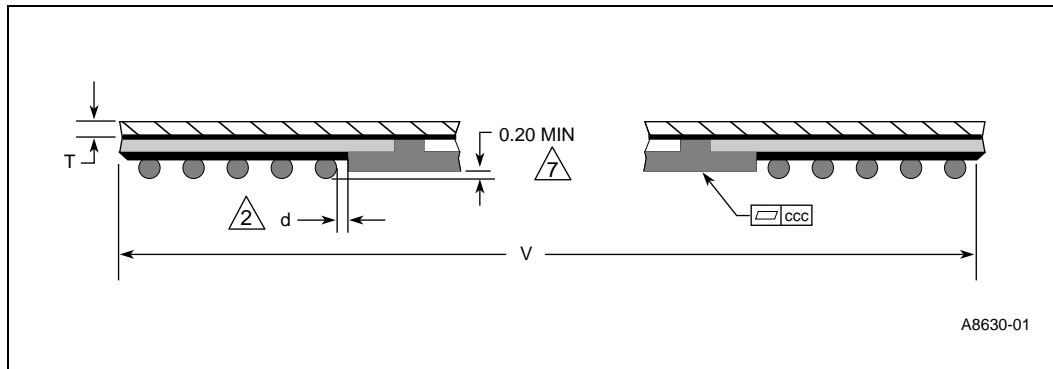


Figure 84. IXP1250 A-A Section View



## 5.2 IXP1250 Package Dimensions (mm)

**Table 53. IXP1250 Package Dimensions (mm)**

Symbol	Definition	Minimum	Nominal	Maximum
A	Overall thickness	—	—	1.70
A1	Ball height	0.50	0.60	0.70
A2	Body thickness	0.80	0.91	1.00
D	Body size	—	40.00	—
D1	Ball footprint	38.00	38.10	38.20
E	Body size	—	40.00	—
E1	Ball footprint	38.00	38.10	38.20
M, N	Ball Matrix	—	31 x 31	—
M1 [6]	Number of rows deep	—	5	—
b	Ball diameter	0.60	0.75	0.90
d	Minimum distance encap to balls	0.25	—	—
e	Ball pitch	—	1.27	—
aaa	Package body profile	—	—	0.20
bbb	Parallel	—	—	0.25
ccc	Encap flatness over die	—	—	0.10
ddd	Coplanarity	—	—	0.20
S	Solder ball placement	—	0.00	—
T	V-score web thickness	0.050	0.125	0.175
V	V-score bottom size	39.2	—	39.9

**NOTES:**

All notes are related to [Figure 82](#) through [Figure 84](#). All dimensions are in millimeters.

Unless otherwise specified:

- All dimensions and tolerances conform to ANSI Y1.45M-1994.
- Dimension “d” is measured at the maximum solder ball diameter parallel to primary datum “c”.
- Primary datum “c” and seating plane are defined by the spherical crowns of the solder balls.
- Pin A1 I.D. marked by laser.
- Shape at corner, single form.
- Number of rows in from edge to center.
- Seating plane clearance: Minimum height of encapsulant above seating plane.
- S is measured with respect to -A- and -B- and defines the position of the center solder ball in the outer row. When there is an odd number of solder balls in the outer row,  $S=0.000$ ; when there is an even number of solder balls in the outer row, the value  $S=e/2$ . S can be either 0.000 or  $e/2$  for each variation.
- Equivalent to ANAM P/N 71290

