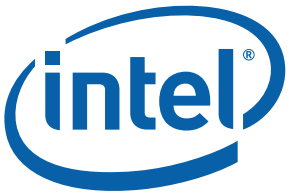

Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor

Hardware Design Guidelines

December 2007

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Contents

Figures

Tables

Revision History

Date	Revision	Description
December 2007	008	1. Updated Section 3.1.3 with updated SDRAM initialization information.
February 2007	007	1. Added a new Appendix A, "Design Checklist". 2. Changed RCOMP signal to be an Output signal. 3. Updated Figure 2 by replacing RJ11 block connection to the RS-232 Serial Port block with a DB9 block. 4. Updated Section 3.2.3 by replacing Intel StrataFlash® memory (J3) with Intel® Embedded Flash Memory (J3 v.D). 5. Updated Figure 17 to more clearly show power-up sequence requirements. 6. Removed information regarding using a crystal as the system clock source. 7. Changed some of the I/O signals pins from *pulled low* to *pulled high* when not in use for new designs. These include signal pins of MII, PCI, UART, HSS, Expansion Bus, UTOPIA, GPIO. No changed required for existing designs. 8. Updated Figure 14 by pulling the unused pins high. 9. Updated Intel® product branding. References to Intel XScale core were updated to Intel XScale Processor. 10. Updated figures with references to *Intel® IXP4XX* by changing to *Intel® IXP42X*.
June 2004	006	Updated Intel® product branding.
April 2004	005	Added information for Intel® IXP420 Network Processor variants.
February 2004	004	Updated clock references from 33.333MHz to 33.33MHz as specified in the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet*.
September 2003	003	Updated JTAG signal descriptions.
August 2003	002	Improved guidelines in Sections 3, 5, 6, and 7. Other minor updates throughout the document.
April 2003	001	Initial release.

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1.0 Introduction

This document provides design recommendations for hardware and systems designers using the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor. Information on the generic hardware interface, PCB, and bus topologies are also included.

Design recommendations are necessary to meet the timing and signal quality specifications. The guidelines recommended in this document are based on experience and simulation work done at Intel while developing the Intel® IXDP425 Development Platform. These recommendations are subject to change.

1.1 About this Document

This document is intended for hardware and systems designers who are experienced with systems and board design. The hardware design guidelines assume that the designer has a working knowledge of the vocabulary and practices of systems and hardware design.

This document contains the following sections:

Chapter Name	Description
Chapter 1.0, "Introduction"	Conventions used in this manual and related documentation
Chapter 2.0, "System Architecture"	Shows how the processors implement and interface to other devices.
Chapter 3.0, "General Hardware Design Considerations"	Describes the interfaces between the processors and other devices.
Chapter 4.0, "PBGA Package"	Describes package information for the processors.
Chapter 5.0, "General PCB Guide"	Provides recommended guidelines for printed circuit board setup.
Chapter 6.0, "General Layout and Routing Guide"	Provides routing guidelines for layout and design of a printed circuit board.
Chapter 7.0, "Critical Routing Topologies"	Describes PC133 and SDRAM and PCI-bus routing topologies.
Appendix A, "Design Checklist"	Highlights design considerations that should be reviewed prior to manufacturing a system board.

Chapter 3.0, "General Hardware Design Considerations" and Chapter 4.0, "PBGA Package" contain specific design considerations for each on-chip peripheral interface within the processors. Not all sections are applicable to all designs because not all units of the processors are used in every design.

1.2 Related Documentation

Title	Document #
Intel® IXP4XX Product Line of Network Processors Specification Update	306428
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479
Intel® IXP400 Software Specification Update	307310
Intel® IXP400 Software Programmer's Guide	252539

Title	Document #
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor: Spread-Spectrum Clocking to Reduce EMI	254028
Intel® IXP42X Product Line and IXC1100 Control Plane Processors: I^2C Implementation Using the GPIO Pins	252137
Intel® XScale™ Core Developer's Manual	273473
Intel XScale® Microarchitecture *Technical Summary*	—
Intel StrataFlash® Embedded Memory (P30) to Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Design Guide - Application Note 832	308294
Intel StrataFlash® Memory J3 to Intel StrataFlash®Embedded Memory (P30) Migration Guide - Application Note 812	306667
PCI Local Bus Specification, Rev. 2.2	N/A
Universal Serial Bus Specification, Revision 1.1	N/A
PC133 SDRAM Specification	N/A
UTOPIA Level 2 Specification, Revision 1.0	N/A
IEEE 802.3 Specification	N/A
IEEE 1149.1 Specification	N/A
I^2C-Bus Specification from Philips Semiconductors*	(Available at http:// www.semiconductors.philips.com)
Note: For Intel documentation, see the Intel Technical Documentation Center, available at http://www.intel.com/products/index.htm.	

1.3 Acronyms and Abbreviations

Acronym or Abbreviation	Description
AHB	Advanced High-Performance Bus
ATM	Asynchronous Transfer Mode
EMI	Electro-Magnetic Interference
GPIO	General Purpose Input/Output
HSS	High Speed Serial
LAN	Local Area Network
MII	Media-Independent Interface
NPE	Network Processor Engine
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PHY	Physical Layer Interface
PLL	Phase-Locked Loop
PMU	Performance Monitoring Unit
SDRAM	Synchronous Dynamic Random Access Memory
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

1.4 Overview

The IXP42X product line and IXC1100 control plane processors are multi-function processors and incorporate many advanced architecture features, including an industry-standard, 32-bit PCI controller, UART, PC133 SDRAM memory controller, interrupt controller, Intel XScale® Microarchitecture compliant with the ARM* Version 5TE instruction set architecture (ISA), USB (device only), UTOPIA-2, GPIO, 133-MHz internal bus, AHB bridges, timers, 8-Kbyte Queue Manager, PMU, Network Processor Engines (NPEs), and industry-standard Media Independent Interfaces (MII).

With the highly integrated solution and rich feature set, the processors deliver high performance system-on-chip and helps to reduce the overall cost of system implementations.

The processors can operate at a variety of frequencies, allowing systems designers to trade off performance for lower power consumption. The Intel XScale® Microarchitecture and the internal components are clocked from an internal PLL. The internal and external interfaces use a 66/133-MHz, 32-bit data bus; a 32-bit address bus; and control signals that enable the interface between the Intel XScale® Microarchitecture and peripheral logic to optimize performance.

1.5 Key Features

- Intel XScale® Processor (compliant with Intel® StrongARM* architecture)
  - — High-performance processor based on Intel XScale® technology
  - — Seven/eight-stage Intel® Super-Pipelined RISC Technology
  - — Management unit
    - 32-entry, data memory management unit
    - 32-entry, instruction memory management unit
    - 32-Kbyte, 32-way, set associative instruction cache
    - 32-Kbyte, 32-way, set associative data cache
    - 2 Kbyte, two-way, set associative mini-data cache
    - 128-entry, branch target buffer
    - Eight-entry write buffer
    - Four-entry fill and pend buffers
  - — Clock speeds:
    - 266 MHz
    - 400 MHz
    - 533 MHz
  - — ARM* Version 5TE Compliant
  - — Intel® Media Processing Technology
    Multiply-accumulate coprocessor
  - — Debug unit. Accessible through JTAG port
- PCI interface
  - — 32-bit interface
  - — Selectable clock
    - 33-MHz clock output derived from either GPIO14 or GPIO15
    - 0- to 66-MHz clock input
  - — *PCI Local Bus Specification*, Rev. 2.2 compatible
  - — PCI arbiter supporting up to four external PCI devices (four REQ/GNT pairs)
  - — Host/option capable
  - — Master/target capable

  - — Two DMA channels
- USB v 1.1 device controller
  - — Full-speed capable
  - — Embedded transceiver
  - — 16 endpoints
- SDRAM interface
  - — 32-bit data
  - — 13-bit address
  - — 133 MHz
  - — Up to eight open pages simultaneously maintained
  - — Programmable auto-refresh
  - — Programmable CAS/data delay
  - — 8 MB minimum up to 256 MB maximum supported
- Expansion interface
  - — 24-bit address
  - — 16-bit data
  - — Eight programmable chip selects
  - — Supports Intel and Motorola* microprocessor style bus cycles
    - Multiplexed-style bus cycles
    - Simplex-style bus cycles
  - — Texas Instruments* DSPs supporting HPI-8 and HPI-16 bus cycles
- High-speed UART
  - — 1,200 Baud to 921 Kbaud
  - — 16550 compliant
  - — 64-Byte Tx and Rx FIFOs
  - — CTS and RTS modem control signals
- Console UART
  - — 1,200 Baud to 921 Kbaud
  - — 16550 compliant
  - — 64-byte Tx and Rx FIFOs
  - — CTS and RTS modem control signals
- Internal bus performance monitoring unit
  - — Seven 27-bit event counters
  - — Monitors internal bus occurrence and duration events
- 16 GPIOs
- Four internal timers
- Packaging
  - — 492-pin PBGA
  - — Commercial temperature (0° to +70° C)
  - — Extended temperature (-40° to +85° C)
  - — Lead free support

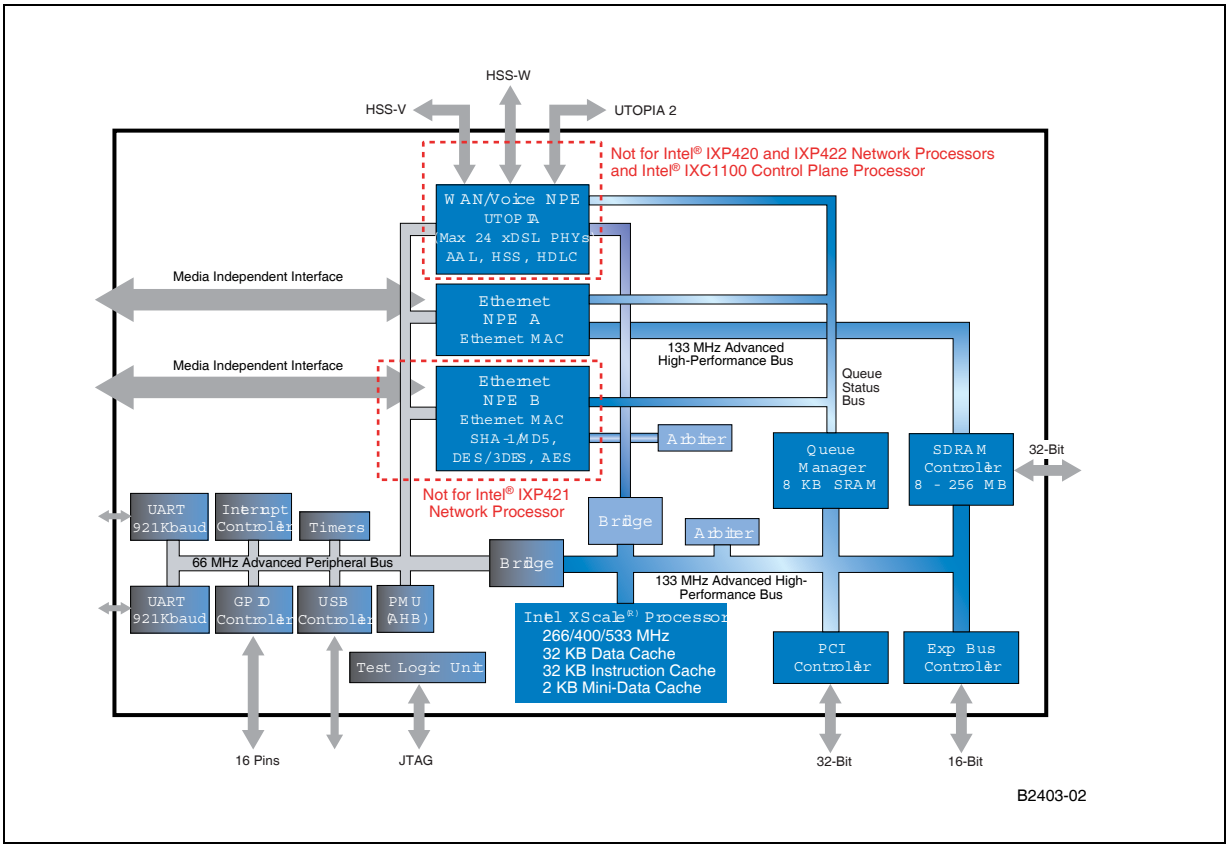
The remaining features described in the product line features list require software in order for these features to be functional. To determine if the feature is enabled, see the *Intel® IXP400 Software Programmer's Guide*.

- Three network processor engines (NPEs)
  Used to off load typical Layer-2 networking functions like:
  - Ethernet filtering
  - ATM SARing
  - HDLC
- Encryption/Authentication
  - DES
  - Triple-DES (3DES)
  - AES 128-bit and 256-bit
  - ARC4/WEP-CRC
  - SHA-1
  - MD5
- Two MII interfaces
  - 802.3 MII interfaces
  - Single MDIO interface to control both MII interfaces
- UTOPIA-2 Interface
  - Eight-bit interface
  - Up to 33 MHz clock speed
  - Five transmit and five receive address lines
- Two high-speed, serial interfaces
  - Six-wire
  - Supports speeds up to 8.192 MHz
  - Supports connection to T1/E1 framers
  - Supports connection to CODEC/SLICs
  - Eight HDLC Channels

Figure 1 illustrates the major internal components of the IXP42X product line and IXC1100 control plane processors.

Refer to the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for complete feature list and block diagram description.

Figure 1. Devices' Component Block Diagram



The *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* lists the feature set for each of the IXP42X product line and IXC1100 control plane processors.

1.6 Typical Applications

- High-performance DSL modem
- High-performance cable modem
- Residential gateway
- SME router
- Integrated access device (IAD)
- Set-top box
- Access points 802.11a/b/g
- Industrial controllers
- Network printers
- Control plane

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2.0 System Architecture

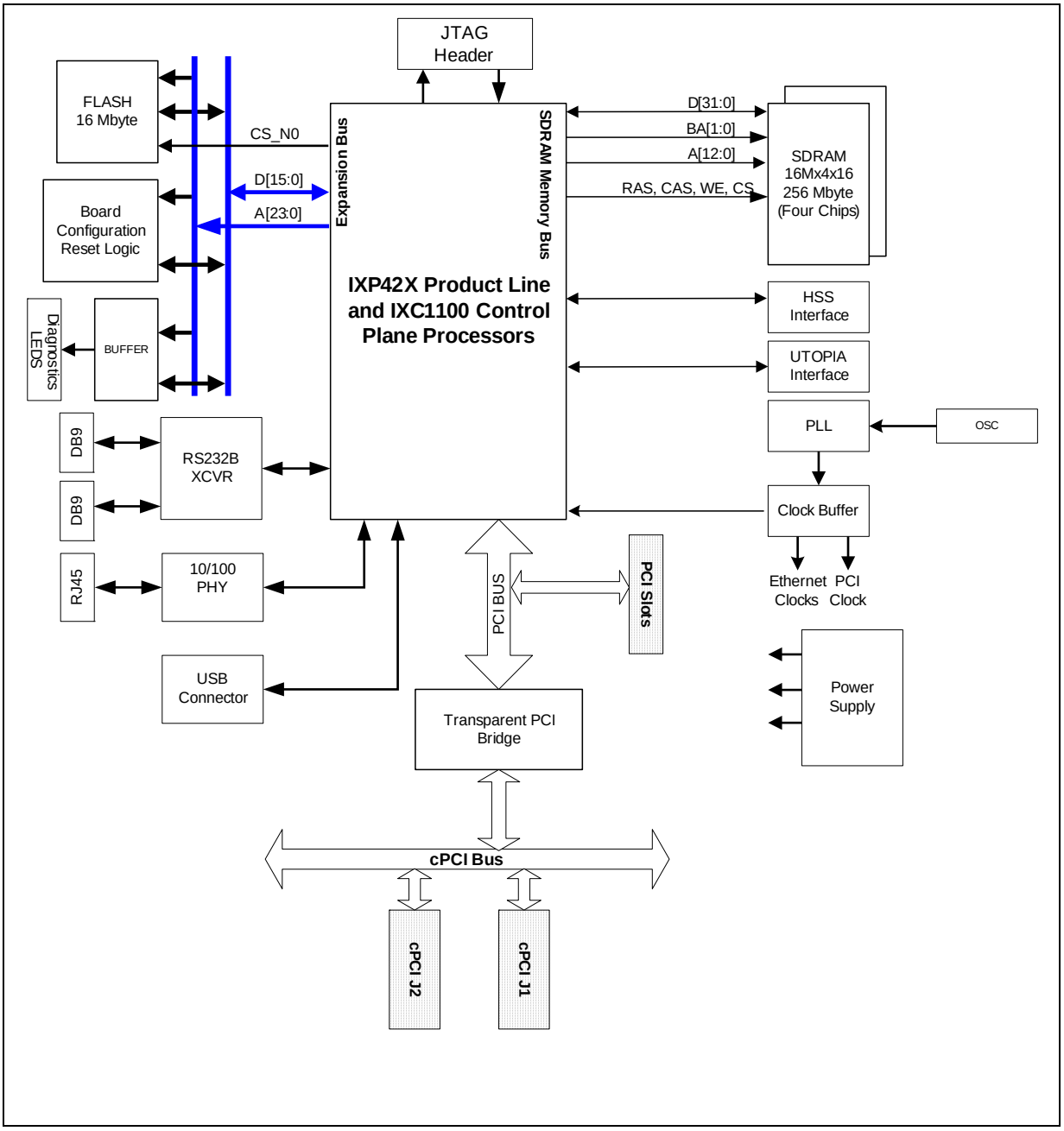
2.1 System Architecture Description

The Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor are multi-function processors that integrate the Intel XScale® Processor (ARM* architecture compliant) with intelligent peripheral controllers, including a 32-bit PCI controller that can be used in many applications such as networking and communications.

The processors are highly integrated and designed and manufactured with Intel's 0.18-micron production semiconductor process technology. This process technology — along with numerous, dedicated-function peripheral interfaces and many features with the Intel XScale processor — addresses the needs of many system applications and helps reduce system costs. The processors can be configured to meet many system application and implementation needs.

Figure 2 illustrates one of many applications that the processors can be implemented and interfaced. For detailed functional descriptions, see the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*.

Figure 2. Devices' System Block Diagram



2.2 System Memory Map

The IXP42X product line and IXC1100 control plane processors implement a single address map that is used for all internal memory and register space. The complete address space consists of 2^32 byte addressable location.

Table 1 shows the memory map of peripherals connected to the AHB.

Table 1. Memory Map

Start Address	End Address	Size	Use
0000_0000	0FFF_FFFF	256 MB	Expansion Bus Data (Mirrored)/SDRAM Data†
0000_0000	2FFF_FFFF	768 MB	SDRAM Data (Aliased)†
3000_0000	3FFF_FFFF		(Reserved)
4000_0000	47FF_FFFF		(Reserved)
4800_0000	4FFF_FFFF	128 MB	PCI Data
5000_0000	5FFF_FFFF	256 MB	Expansion Bus Data
6000_0000	63FF_FFFF	64 MB	Queue manager
6400_0000	BFFF_FFFF		(Reserved)
C000_0000	C3FF_FFFF	64 MB	PCI Controller Configuration and Status Registers
C400_0000	C7FF_FFFF	64 MB	Expansion Bus Configuration Registers
C800_0000	C800_0FFF	1 KB	High-Speed UART
C800_1000	C800_1FFF	1 KB	Console UART
C800_2000	C800_2FFF	1 KB	Internal Bus Performance Monitoring Unit
C800_3000	C800_3FFF	1 KB	Interrupt Controller
C800_4000	C800_4FFF	1 KB	GPIO Controller
C800_5000	C800_5FFF	1 KB	Timers
C800_6000	C800_6FFF	1 KB	WAN/HSS NPE = NPE A (IXP400 software definition) – Not User Programmable
C800_7000	C800_7FFF	1 KB	Ethernet NPE A = NPE B (IXP400 software definition) – Not User Programmable
C800_8000	C800_8FFF	1 KB	Ethernet NPE B = NPE C (IXP400 software definition) – Not User Programmable
C800_9000	C800_9FFF	1 KB	Ethernet MAC A
C800_A000	C800_AFFF	1 KB	Ethernet MAC B
C800_B000	C800_BFFF	1 KB	USB Controller
C800_C000	C800_FFFF		(Reserved)
C801_0000	CBFF_FFFF		(Reserved)
CC00_0000	CC00_00FF	256 Byte	SDRAM Configuration Registers
CC00_0100	FFFF_FFFF		(Reserved)

† The lowest 256 Mbyte of address space is configurable based on the value of a configuration register bit located in the Expansion Bus Controller (bit 31 of EXP_CNFG0.)

- When bit 31 (MEM_MAP) of configuration register #0 (EXP_CNFG0) is set to logic 1, the Expansion Bus occupies the lowest 256 Mbytes of address space.
- When bit 31 (MEM_MAP) of configuration register #0 (EXP_CNFG0) is set to logic 0 the SDRAM occupies the lowest 256 Mbytes of address space starting at 5000_0000 while the SDRAM occupies the lowest 256 MB of address address space.

  In both cases, regardless of the value of MEM_MAP, the SDRAM occupies the 768 MB (1000_0000 to 2FFF_FFFF) immediately following the lowest 256 MB and the Expansion Bus can be accessed starting at address 5000_0000.

  The largest SDRAM memory size supported by the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor is 256 Mbytes. The actual memory implemented in any given configuration will be aliased (repeated) to fill the 1-Gbyte SDRAM address space. Due to aliasing, all of the SDRAM will be accessible even when the Expansion Bus occupies the lowest 256 Mbytes of address space. On reset, bit 31 (MEM_MAP) of the Configuration Register #0 (EXP_CNFG0) will be set to logic 1. This setting is required because the dedicated boot memory is flash memory located on the Expansion Bus.

  Details in the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*.

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3.0 General Hardware Design Considerations

This chapter contains information on how to implement and interface the SDRAMs, flash, SRAM, Ethernet PHYs, UART and other peripherals to the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor.

This chapter's signal-definition tables list pull-up and pull-down resistor recommendations that are required when the particular enabled interface is *not* being used in the application. These external resistor requirements are only needed if the particular model of Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor has the particular interface *enabled* and the interface is *not required* in the application.

Warning: All IXP42X product line and IXC1100 control plane processors I/O pins are *not* 5-V tolerant.

Disabled features, within the IXP42X product line and IXC1100 control plane processors, do not require external resistors as the processor will have internal pull-up or pull-down resistors enabled as part of the *disabled* interface.

3.1 PC133 SDRAM Interface

The SDRAM memory controller, integrated into the IXP42X product line and IXC1100 control plane processors, supports a 32-bit data bus interface operating at 133 MHz, eight open pages, two external banks with memory configuration from 8 to 256 Mbytes.

General SDRAM routing guidelines can be found in Section 7.1, "PC133 SDRAM Topologies" on page 73. For more detailed information, see the PC133 SDRAM Specification.

These are the features:

- Performs eight word length burst size to SDRAM
- Supports bursts up to eight words internally
- Is a target device on the Internal Buses and does not split any transactions
- Has RAS-to-CAS delay of three clocks
- Has a CAS-to-data latency of two or three clocks, as programmed by the configuration register
- Runs at 133 MHz frequency (same as the internal bus frequency)
- Maintains up to eight open pages
- Supports a total of two physical banks totaling to 8 Mbytes/256 Mbytes of memory space
- Handles transactions from the internal bus in a big-endian manner
- Automatically refreshes the SDRAM devices using an internal refresh counter

3.1.1 SDRAM Interface Signals

Table 2. SDRAM Interface Signals

Name	Type*	Description
SDM_ADDR[12:0]	O	SDRAM Address: A0-A12 are output during the READ/WRITE command and ACTIVE command to select a location in memory.
SDM_DATA[31:0]	I/O	SDRAM Data: bidirectional data bus used to transfer data to and from the SDRAM.
SDM_CLKOUT	O	SDRAM Clock: All SDRAM input signals are sampled on the rising edge of SDM_CLKOUT. All output signals are driven with respect to the rising edge of the Clock.
SDM_BA[1:0]	O	SDRAM Bank Address: SDM_BA0 and SDM_BA1 define the bank the current command is accessing.
SDM_RAS_N	O	SDRAM Row Address strobe/select (active low): Along with SDM_CAS_N, SDM_WE_N, and SDM_CS_N signals determines the current command to be executed.
SDM_CAS_N	O	SDRAM Column Address strobe/select (active low): Along with SDM_RAS_N, SDM_WE_N, and SDM_CS_N signals determines the current command to be executed.
SDM_CS_N[1:0]	O	SDRAM Chip select (active low): CS# enables the command decoder in the external SDRAM when logic low and disables the command decoder in the external SDRAM when logic high.
SDM_WE_N	O	SDRAM Write enable (active low): Along with SDM_CAS_N, SDM_RAS_N, and SDM_CS_N signals determines the current command to be executed.
SDM_CKE	O	SDRAM Clock Enable: CKE is driving high to activate the clock to an external SDRAM and driver low to de-activate the CLK to an external SDRAM.
SDM_DQM[3:0]	O	SDRAM Data bus mask: DQM is used to bytes select data during read/write access to an external SDRAM.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.1.2 SDRAM Block Diagrams

The IXP42X product line and IXC1100 control plane processors support the PC133-compatible SDRAM 16 and 32-bit wide devices. The banks are accessed 32 bits at a time. The maximum configuration is two physical banks of SDRAM devices (each bank consists of two SDRAM 16-bit devices or single SDRAM 32-bit device), using two independent chip-selects.

The supported memory types are listed in Table 3. The processors' SDRAM interfaces support a maximum of 256 Mbytes of SDRAM and a minimum of 8 Mbytes, using two SDRAM devices. The PC133 SDRAM memory bus I/O buffers are designed to support up to four loads total for two banks of PC133 of SDRAM memory.

Table 3. SDRAM Memory Types

SDRAM Technology	SDRAM Arrangement	Number of Chips	Number of Banks (Systems)	Total Memory Size
64 Mbit	2M x 32	1	1	8 Mbytes
	2M x 32	2	2	16 Mbytes
	4M x 16	2	1	16 Mbytes
	4M x 16	4	2	32 Mbytes

Note: The 4 M x 32, * 8 M x 32 and * 16 M x 32 devices have not been fully validated by Intel.

Table 3. SDRAM Memory Types

SDRAM Technology	SDRAM Arrangement	Number of Chips	Number of Banks (Systems)	Total Memory Size
128 Mbit	8M x 16	2	1	32 Mbytes
	8M x 16	4	2	64 Mbytes
	* 4M x 32	1	1	16 Mbytes
	* 4M x 32	2	2	32 Mbytes
256 Mbit	16M x 16	2	1	64 Mbytes
	16M x 16	4	2	128 Mbytes
	* 8M x 32	1	1	32 Mbytes
	* 8M x 32	2	2	64 Mbytes
512 Mbit	32M x 16	2	1	128 Mbytes
	32M x 16	4	2	256 Mbytes
	* 16M x 32	1	1	64 Mbytes
	* 16M x 32	2	2	128 Mbytes

Note: The 4 M x 32, * 8 M x 32 and * 16 M x 32 devices have not been fully validated by Intel.

Figure 3, Figure 4, and Figure 5 illustrate how the PC133 SDRAM interfaces to the processors' memory bus. The figures do not include any termination resistors that may be needed. For best signal integrity results the designer may perform simulations.

Note: The SDM_CLKOUT is the reference clock signal for all SDRAM devices and generated by the onchip PLL. Layout guidelines can be found in Section 7.1.1, "PC 133 SDRAM Clock" on page 74.

Figure 3. Dual-Bank SDRAM System Block Diagram (x32 Devices)

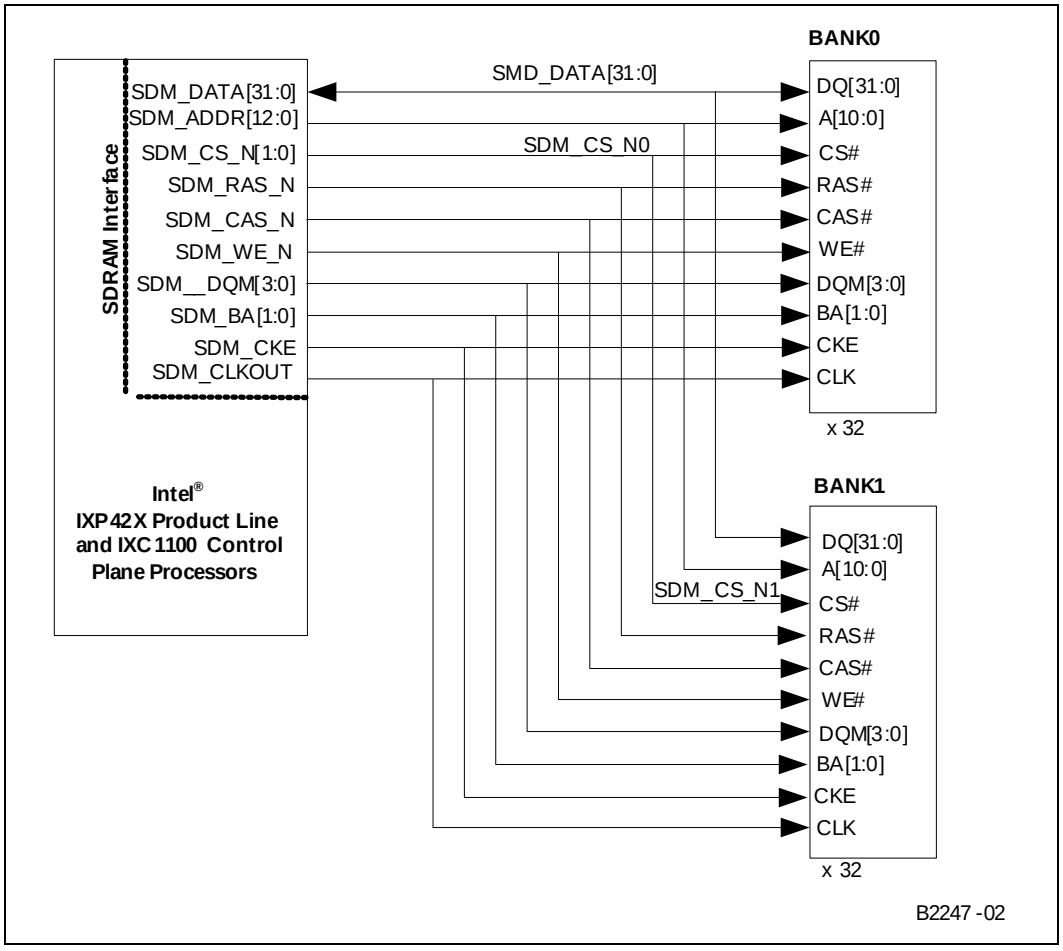


Figure 4 illustrates how the IXP42X product line and IXC1100 control plane processors' interfaces to one bank (2 Chips) of the PC133 SDRAM using the 8 M x 16 (128-Mbit), 16 M x 16 (256-Mbit), or 32 M x 16 (512-Mbit).

Figure 4. Single Bank SDRAM System Block Diagram (x16 Devices)

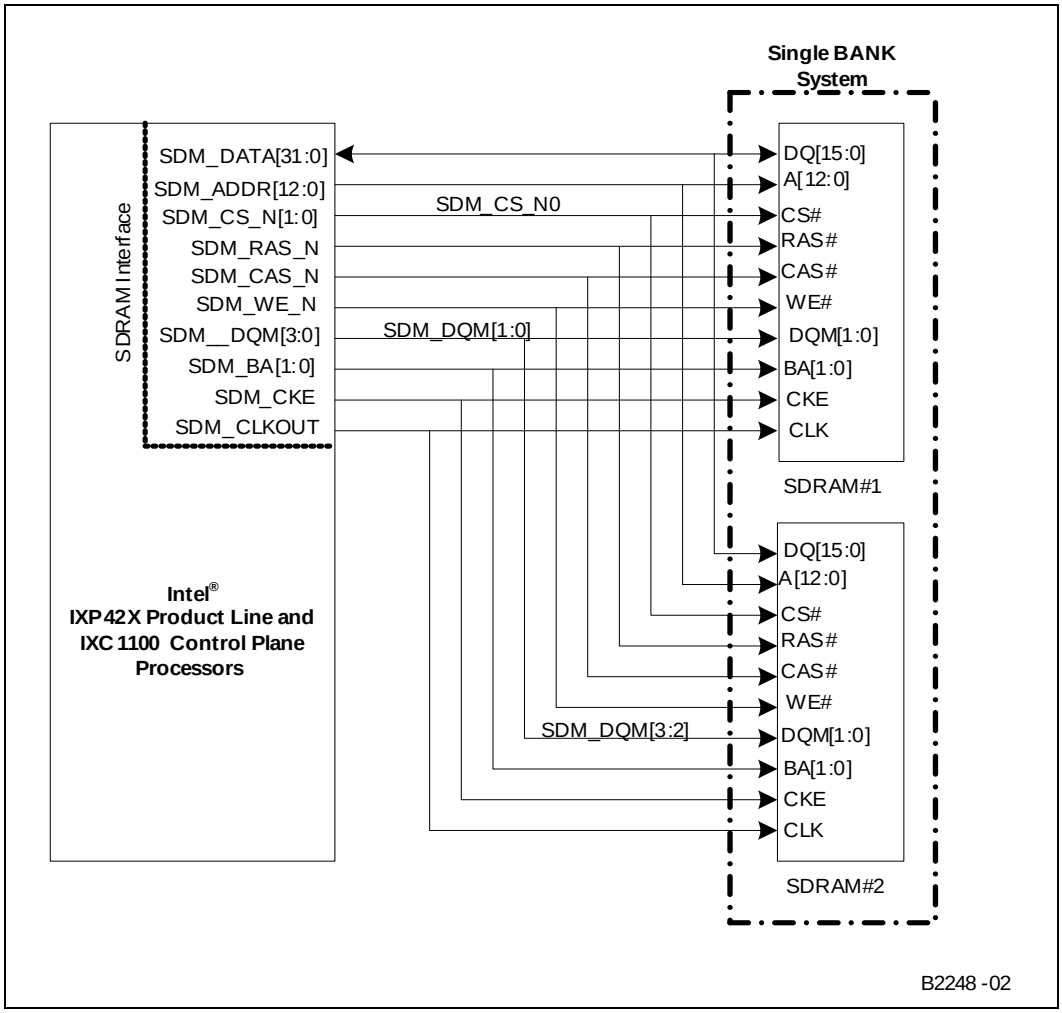
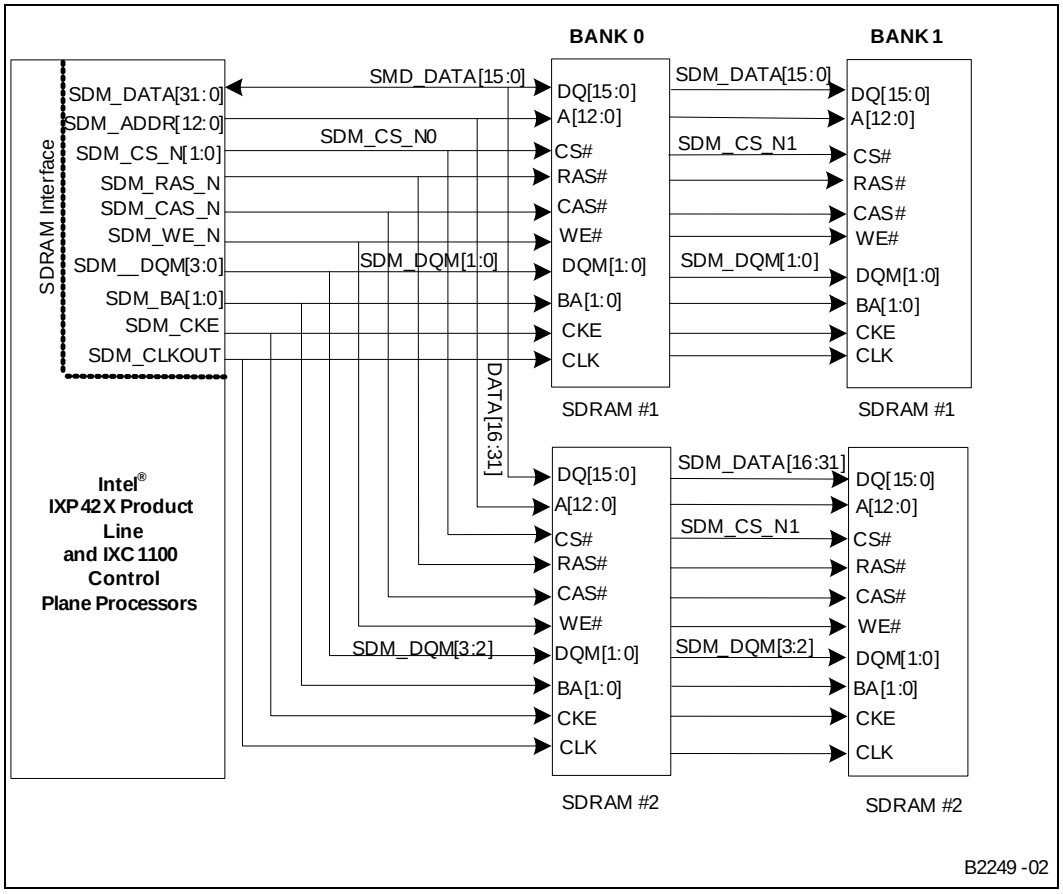


Figure 5 illustrates how the IXP42X product line and IXC1100 control plane processors' interfaces to two banks (4 Chips) of the PC133 SDRAM using the 8 M x 16 (128-Mbit), 16 M x 16 (256-Mbit), or 32 M x 16 (512-Mbit).

Figure 5. Dual Bank SDRAM System Block Diagram (x16 Devices)



3.1.3 SDRAM Initialization

Initialization of the SDRAM devices is performed by the operating system. The following sequence must be followed:

- The memory controller applies the clock enable pin (SDM_CKE) during power up and must stabilize the clock signal within 100 µs after power stabilizes.
- The memory controller holds all the control pins to the memory inactive (SDM_RAS_N, SDM_CAS_N, SDM_WE_N, SDM_CS_N[1:0]=1) for a minimum of 1 ms after supply voltage reaches the desired level.
- SDM_CKE is driven to VCC all the time. The IXP42X product line and IXC1100 control plane processors never de-assert SDM_CKE
- Software disables the refresh counter by setting the SDRAM Refresh (SDR_REFRESH) Register to zero.
- Software issues one NOP cycle after the 1ms SDRAM device deselect. A NOP is accomplished by setting the SDRAM Instruction (SDR_IR) Register to 011. The memory controller asserts SDM_CKE with the NOP.
- Software pauses 200 µs after the NOP.

- Software issues a precharge-all command to the SDRAM interface by setting SDR_IR to 010
- Software provides eight auto-refresh cycles. An auto-refresh cycle is accomplished by setting SDR_IR to 100. Software must ensure at least T_{rc} cycles between each auto-refresh command. T_{rc} (active to active command period) is determined by the SDRAM being used
- Software issues a mode-register-select command by writing to SDR_IR to program the SDRAM parameters. Setting SDR_IR to 000 programs the MCU for CAS latency of two, while setting the SDR_IR to 001 programs the memory controller and SDRAM for CAS latency of three.
- The memory controller may issue a row activate command three clocks after the mode register set command (T_{mrd}).
- Software re-enables the refresh counter by setting the SDR_REFRESH to the required value.

Note: The SDRAM clock starts with the release of PWRON_RESET_N. The first access made by the internal auto-refresh counter (set to default value of 0x384) happens ~7µs after RESET_IN_N is released. Software will not be able to disable this counter before the first access is made. To meet a specific SDRAMs 100-200 ms requirement before the first access, the designer may have to add additional delay between PWRON_RESET_N and RESET_IN_N beyond the required minimum of 10 ns.

3.2 Expansion Bus

The IXP42X product line and IXC1100 control plane processors' expansion bus supports a variety of types and speeds of I/O accesses and is specifically designed for compatibility with Intel and Motorola* microprocessor style bus cycles and the Texas Instruments* DSP standard Host-Port Interfaces (HPI).

All of these modes are supported seamlessly, without any additional glue logic. Other cycle types may be supported due to the programmability of the access phases defined for each cycle type.

The processors' expansion bus provides a 24-bit address bus and a 16-bit-wide data interface for each of its eight independent chip-selects and maps transfers between the internal bus and the external devices. Multiplexed and non-multiplexed address/data buses are both supported.

Applications having less than 16-bit external data paths may connect to less than the full 16 bits. Devices with a wider than 16-bit data bus interface are not supported. The address range of the processors' expansion bus is from 512 bytes to 16 Mbytes and provides glueless connection of up to eight independent external devices.

3.2.1 Expansion Bus Interface Signals

Table 4. Expansion Bus Interface Signals

Name	Type*	Description
EX_CLK	I	Input clock signal used to sample all expansion interface inputs and clock all expansion interface outputs.
EX_ALE	O	Address-latch enable used for multiplexed address/data bus accesses. Used in Intel and Motorola* multiplexed modes of operation.
EX_ADDR[23:0]	I/O	Expansion-bus address used as an output for data accesses over the expansion bus. Also, used as an input during reset to capture device configuration. These signals have a weak pull-up resistor attached internally. Based on the desired configuration, various address signals must be tied low in order for the device to operate in the desired mode. (For details, see the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*.)
EX_WR_N	O	Intel-mode write strobe / Motorola-mode data strobe (EXP_MOT_DS_N) / TI*-mode data strobe (TI_HDS1_N).
EX_RD_N	O	Intel-mode read strobe / Motorola-mode read-not-write (EXPB_MOT_RNW) / TI mode read-not-write (TI_HR_W_N).
EX_CS_N[7:0]	O	External chip selects for expansion bus. • Chip selects 0 through 7 can be configured to support Intel or Motorola bus cycles. • Chip selects 4 through 7 can be configured to support TI HPI bus cycles.
EX_DATA[15:0]	I/O	Expansion-bus, bidirectional data
EX_IOWAIT_N	I	Data ready/acknowledge from expansion-bus devices. Expansion-bus access is halted when an external device sets EX_IOWAIT_N to logic 0 and resume from the halted location once the external device sets EX_IOWAIT_N to logic 1. This signal affects accesses that use EX_CS_N[7:0] when the chip select is configured in Intel- or Motorola-mode operation. Should be pulled high through a 10-kΩ resistor, when the signal is not being used in the system.
EX_RDY[3:0]	I	HPI interface ready signals. Can be configured to be active high or active low. These signals are used to halt accesses using chip Selects 7 through 4 when the chip selects are configured to operate in HPI mode. There is one RDY signal per chip select. This signal only affects accesses that use EX_CS_N[7:4]. Should be pulled high through a 10-kΩ resistor when the signal is not being used in the system.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.2.2 Configuration Straps

At power up or whenever a reset is asserted, the expansion-bus address outputs are switched to inputs and the states of the bits are captured and stored in Configuration Register 0, bits 23 through 0. This occurs on the first cycle after the synchronous de-assertion of the reset signal.

These configuration bits are made available to the system through the expansion-bus address lines. To set a bit to 0, place a 4.7-kΩ, pull-down resistor on the appropriate address line. Weak pull-up resistors are placed on each expansion-bus address pin; so no population is needed to set the bit to 1.

Table 5. Expansion Bus Address Description

Bit	Name	Description
31	MEM_MAP	Location of Expansion Bus in memory map space: 0 = Located at “50000000” (normal mode) 1 = Located at “00000000” (boot mode)
30:24		(Reserved)
23:21	Intel XScale® Processor Clock Set[2:0]	Allow a slower Intel XScale® Processor clock speed to override device fuse settings; however, cannot be used to over-clock processor speed. Refer to Table 30 on page 88, for additional details.
20:17		User-configurable. See Section 3.2.2.1 for further details.
16:6		(Reserved)
5		(Reserved)
4	PCI_CLK	Enables the clock speed of the PCI Interface 0 = 33 MHz 1 = 66 MHz
3		(Reserved) EX_ADDR[3] must not be pulled down during address strapping. This bit must be written to ‘1’ if performing a write to this register.
2	PCI_ARB	Enables the PCI Controller Arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled
1	PCI_HOST	Configures the PCI Controller as PCI Bus Host 0 = PCI as non-host 1 = PCI as host
0	8/16 FLASH	Specifies the data bus width of the flash memory device 0 = 16-bit data bus 1 = 8-bit data bus

The chip-level memory map used is determined by the state of bit 31. At system reset this bit is a ‘1’ and the memory map places the expansion bus at address 0x00000000 through 0x0FFFFFFF. This allows boot code stored in flash to be retrieved and executed as required.

Once the boot sequence completes this bit is written to a ‘0,’ switching the default system memory map to place the SDRAM controller at address 0x00000000 to 0x0FFFFFFF. The Expansion Bus Controller now resides at address 0x50000000 to 0x5FFFFFFF. Refer to Table 1 on page 17 for the complete memory map.

The Intel XScale® Processor can operate at slower speeds than the factory-programmed speed setting. This is done by placing a value on expansion-bus address bits 23, 22, and 21 at the de-assertion of RESET_IN_N and knowing the speed grade of the part from the factory. Column 1 of Table 30 on page 88 denotes the speed grade of the part from the factory. Columns 2, 3, and 4 denote the values captured on the Expansion-Bus address bits at the de-assertion of reset. Column 5 represents the speed at which the Intel XScale processor speed will operate.

3.2.2.1 User-Configurable Field

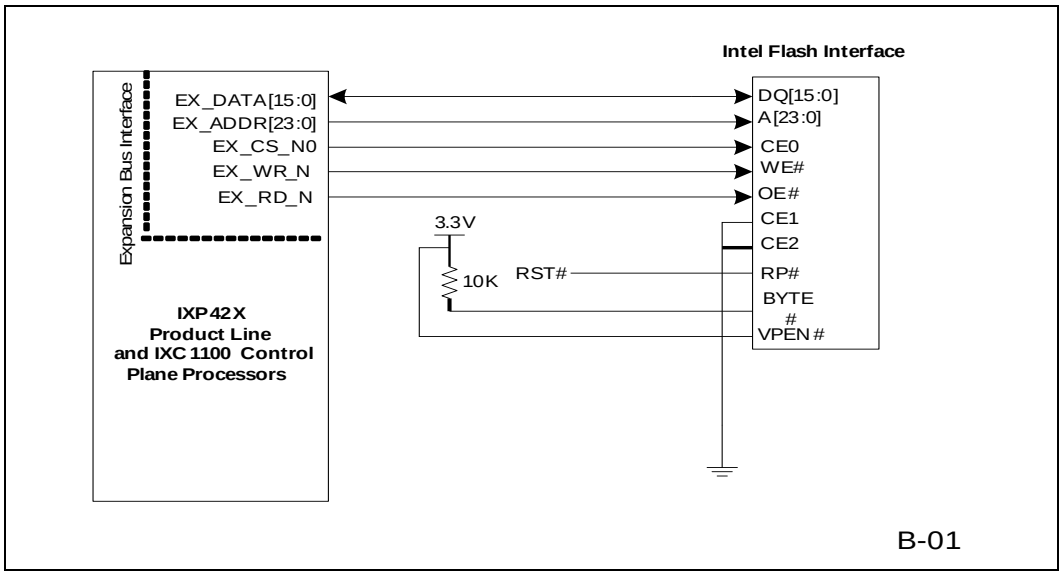
On the Intel® IXP42X product line and IXC1100 control plane processors, the expansion bus address lines for the user-configurable bit-field are internally pulled up. Users may then change the values by adding weak pull-down resistors (~4.7 kΩ). Switches can also be used so that changeable values are available for the user configuration bits.

The user-defined bit-field can be used in many ways. For example, this field could be used for board-revision identification; a series of board revisions may be made over the course of development. To indicate a particular board revision, one of the 16 possible values can be encoded using hardware configuration as stated above. Another potential use for this field would be to predefine a set of values to indicate a particular board configuration — for example, one with a different set of devices and memory map. Many other creative options, not identified in this document, are possible.

3.2.3 Flash Interface

Figure 6 illustrates how the boot ROM is connected through the expansion bus. The flash used in the block diagram is the Intel® Embedded Flash Memory (J3 v.D) 28F128J3D. The boot ROM address space supports up to 16-Mbyte (128-Mbit) of flash. The boot ROM maps to the Intel XScale® Processor physical address 0x00. At startup (reset), the Intel® IXP42X product line and IXC1100 control plane processors begin to fetch and execute instructions from address 0x00.

Figure 6. Expansion Bus Flash Interface

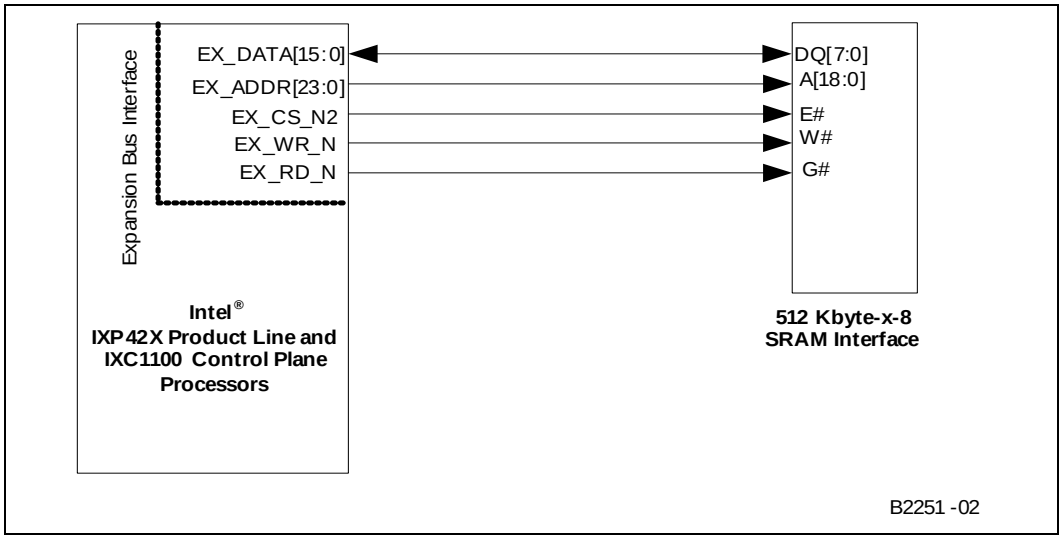


See Intel StrataFlash® memory *(J3) to* Intel® Embedded Flash Memory (J3 v.D) *Conversion Guide - Application Note 835* for more detailed information. For information on design with Intel StrataFlash® Embedded Memory (P30), see the Intel StrataFlash® Embedded Memory (P30) *to* Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor *Design Guide - Application Note 832*. For information on migrating from J3 to P30 Intel StrataFlash® Embedded Memory (P30), see the Intel StrataFlash® Memory J3 to Intel StrataFlash®Embedded Memory (P30) Migration Guide - Application Note 812.

3.2.4 SRAM Interface

Figure 7 shows a typical connection for SRAM connected on the IXP42X product line and IXC1100 control plane processors' expansion bus.

Figure 7. Expansion Bus SRAM Interface



3.2.5 Design Notes

The IXP42X product line and IXC1100 control plane processors' expansion bus I/O buffers are designed to support up to eight loads, but the devices on the bus may not be able to quickly drive the large load. To account for this, timings on the expansion bus may be adjusted using registers internal to the processors. If an edge rises slowly due to low drive strength, the processors should wait an extra cycle before the value is read.

3.3 UART Interface

The IXP42X product line and IXC1100 control plane processors provide two dedicated, asynchronous, serial I/O ports (UARTs): the high-speed UART and the console UART. These UARTs are 16550-compliant with the enhancement of larger 64-byte transmit and receive buffers.

3.3.1 UART Interface Signals

Table 6. UART Interface Signals (Sheet 1 of 2)

Name	Type*	Description
RXDATA0	I	UART serial data input. Fast UART pins. When not being used in the system, should be pulled high with a 10-kΩ resistor.
TXDATA0	O	UART serial data output. The TXD signal is set to the MARKING (logic 1) state upon a Reset operation. High-speed serial UART pins.
CTS0_N	I	UART CLEAR-TO-SEND input to High-Speed UART Pins. When logic 0, this pin indicates that the modem or data set connected to the UART interface of the processor is ready to exchange data. The CTS_N signal is a modem status input whose condition can be tested by the processor. When not being used in the system, should be pulled high with a 10-kΩ resistor.

Table 6. UART Interface Signals (Sheet 2 of 2)

Name	Type*	Description
RTS0_N	O	UART REQUEST-TO-SEND output: When logic 0, this informs the modem or the data set connected to the UART interface of the processor that the UART is ready to exchange data. A reset sets the request to send signal to logic 1. Loop-mode operation holds this signal in its inactive state (logic 1). High-Speed UART pins.
RXDATA1	I	UART serial data input. When not being used in the system, should be pulled high with a 10-kΩ resistor.
TXDATA1	O	UART serial data output. The TXD signal is set to the MARKING (logic 1) state upon a reset operation. Console UART pins.
CTS1_N	I	UART CLEAR-TO-SEND input to Console UART pins. When logic 0, this pin indicates that the modem or data set connected to the UART interface of the processor is ready to exchange data. The CTS_N signal is a modem status input whose condition can be tested by the processor. When not being used in the system, should be pulled high with a 10-kΩ resistor.
RTS1_N	O	UART REQUEST-TO-SEND output: When logic 0, this informs the modem or the data set connected to the UART interface of the processor that the UART is ready to exchange data. A reset sets the request to send signal to logic 1. Loop-mode operation holds this signal in its inactive state (logic 1). Console UART pins.

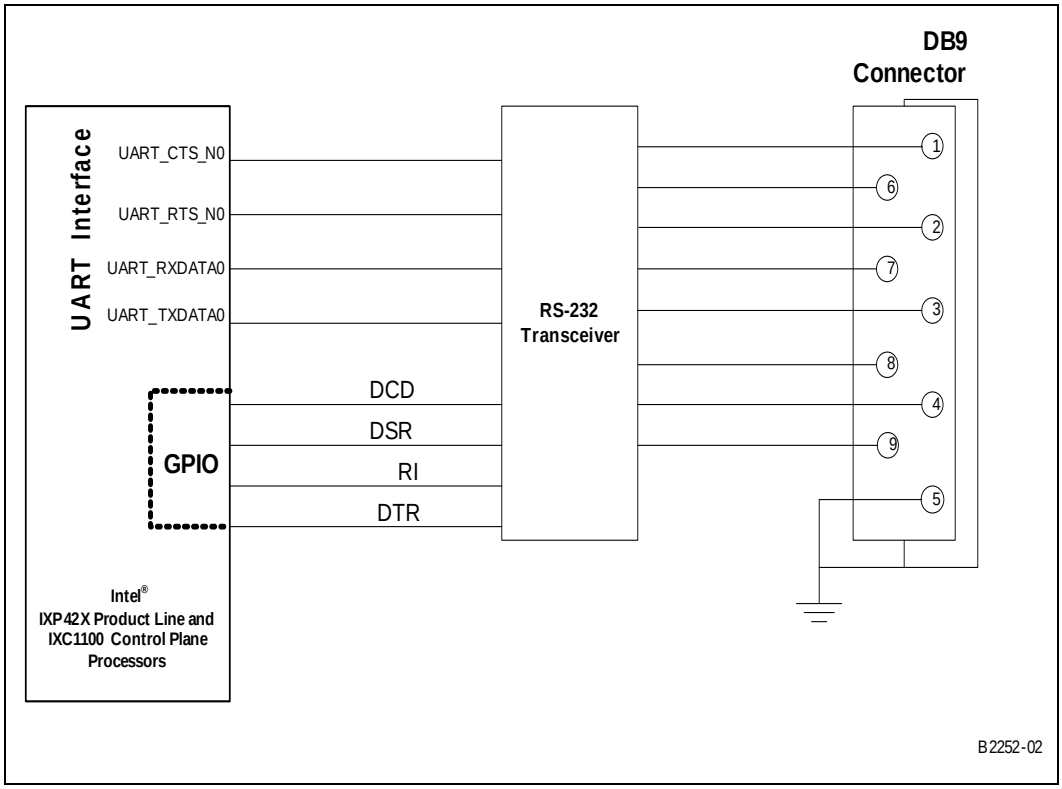
3.3.2 High-Speed UART

The High-Speed UART interface for the IXP42X product line and IXC1100 control plane processors can be configured to support speeds from 1,200 baud to 921 Kbaud. This interface supports five, six, seven, or eight data bit transfers, one or two stop bits, as well as even-, odd-, or no-parity configurations.

Figure 8 illustrates how the processors' UART signals are connected to the RS-232 transceiver. This RS-232 transceiver has five transmit and three receive signals to handle all modem control signals.

For Mbaud signals, options are provided for pull up so that 1-Mbps transmission rate is achieved, or pull down so that 250 Kbps transmission rate can be set. The default setting is 1 Mbps. To allow full modem control on the fast UART connection, system designers have to use four GPIO pins to generate the RS-232 signals (DTR, DSR, RI, and DCD) that are not available on the processor high-speed UART interfaces.

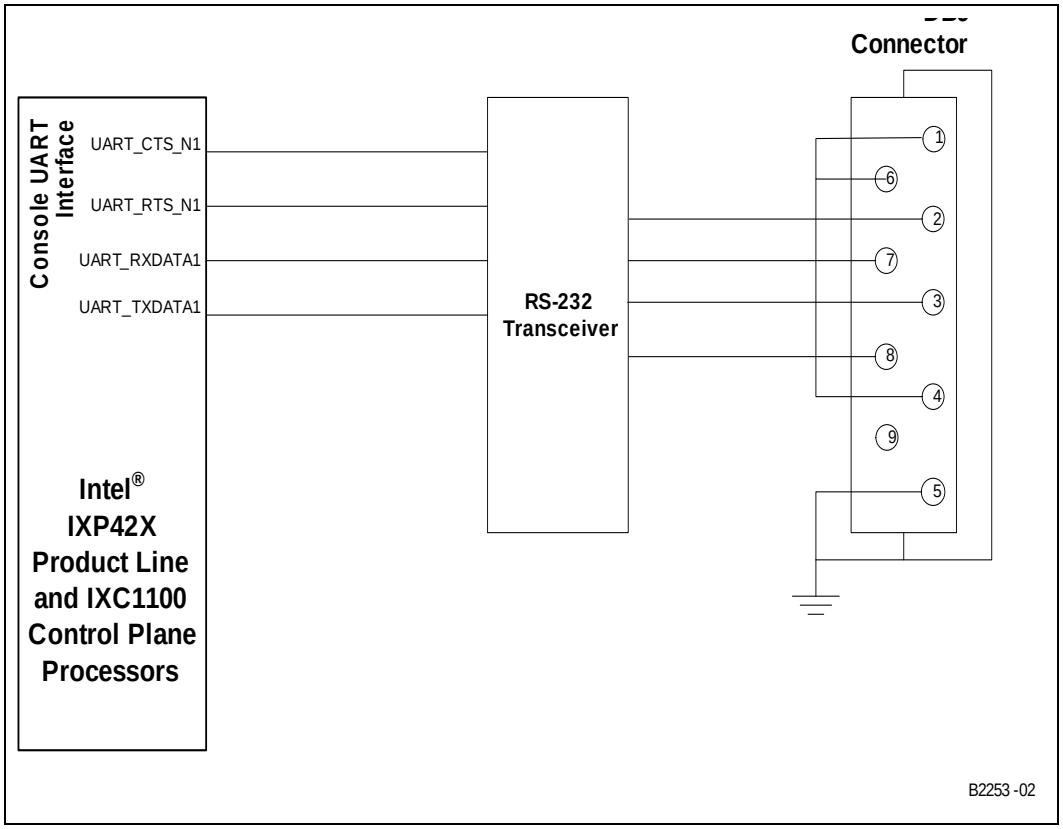
Figure 8. Fast UART Interface



3.3.3 Console UART

The Console UART on the IXP42X product line and IXC1100 control plane processors has the same features as the High-Speed UART. The baud rate supported is from 1,200 baud to 921 Kbaud. As illustrated in Figure 9, the console UART is typically used for debugging and other purposes.

Figure 9. Console UART Interface



3.4 MII Interface

The IXP42X product line and IXC1100 control plane processors have two integrated 10/100-Mbps MAC with two industry-standard Media Independent Interfaces (MII), except for the IXP422, which has only one MII. The processors include a single Management Data Interface – Management Data Input Output (MDIO) and Management Data Clock (MDC). The MII interfaces and the single management data interface are used to communicate, control, and configure PHY devices.

Figure 10 illustrates how to interface an IEEE 802.3 standard Ethernet PHY to the processors' MII port. Rates of 25 MHz for 100-Mbps operation or 2.5 MHz 10-Mbps operation clocks for TX and RX MII interface (ETH_TX_CLK, ETH_RX_CLK) for each Ethernet PHY are expected to be supplied from onboard oscillators or PLL.

General LAN routing guidelines can be found in Section 6.3.2, "LAN Signal Considerations" on page 66. For more detailed information, see the IEEE 802.3 Specification.

3.4.1 Ethernet Interface Signals

Table 7. Ethernet Interface Signals (Sheet 1 of 2)

Name	Type*	Description
ETH_TXCLK0	I	Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC interface does not contain hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_TXDATA0[3:0]	O	Transmit data bus to PHY, asserted synchronously with respect to ETH_TXCLK0. This MAC interface does not contain hardware hashing capabilities.
ETH_TXEN0	O	Indicates that the PHY is being presented with nibbles on the MII interface. Asserted synchronously with respect to ETH_TXCLK0 at the first nibble of the preamble, and remains asserted until all the nibbles of a frame are presented. This MAC interface does not contain hardware hashing capabilities.
ETH_RXCLK0	I	Externally supplied receive clock. • 25 MHz for 100-Mbps operation • 2.5 MHz for 10 Mbps This MAC interface does not contain hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_RXDATA0[3:0]	I	Receive data bus from PHY, data sample synchronously with respect to ETH_RXCLK0. This MAC interface does not contain hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_RXDV0	I	Receive data valid, used to inform the MII interface that the Ethernet PHY is sending data. This MAC interface does not contain hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_COL0	I	Asserted by the PHY when a collision is detected by the PHY. This MAC interface does not contain hardware hashing capabilities. Should be pulled low through a 10-kΩ resistor when not being used in the system.
ETH_CRS0	I	Asserted by the PHY when the transmit medium or receive medium are active. De-asserted when both the transmit medium and receive medium are idle. Remains asserted throughout the duration of collision condition. PHY asserts CRS asynchronously and de-asserts synchronously with respect to ETH_RXCLK0. This MAC interface does not contain hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_MDIO	I/O	Management data output. Provides the write data to both PHY devices connected to each MII interface. Must be pulled high through a 1.5-kΩ resistor when connected. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_MDC	I/O	Management data clock. Management data interface clock used clock the MDIO signal as an output and sample the MDIO as an input. The ETH_MDC is an input on power up and can be configured to be an output through an Intel API, which can be found in the *Intel® IXP400 Software Programmer's Guide.*
ETH_TXCLK1	I	Externally supplied transmit clock. • 25 MHz for 100-Mbps operation • 2.5 MHz for 10 Mbps This MAC contains hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_TXDATA1[3:0]	O	Transmit data bus to PHY, asserted synchronously with respect to ETH_TXCLK1. This MAC contains hardware hashing capabilities.
ETH_TXEN1	O	Indicates that the PHY is being presented with nibbles on the MII interface. Asserted synchronously with respect to ETH_TXCLK1, at the first nibble of the preamble, and remains asserted until all the nibbles of a frame are presented. This MAC contains hardware hashing capabilities.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

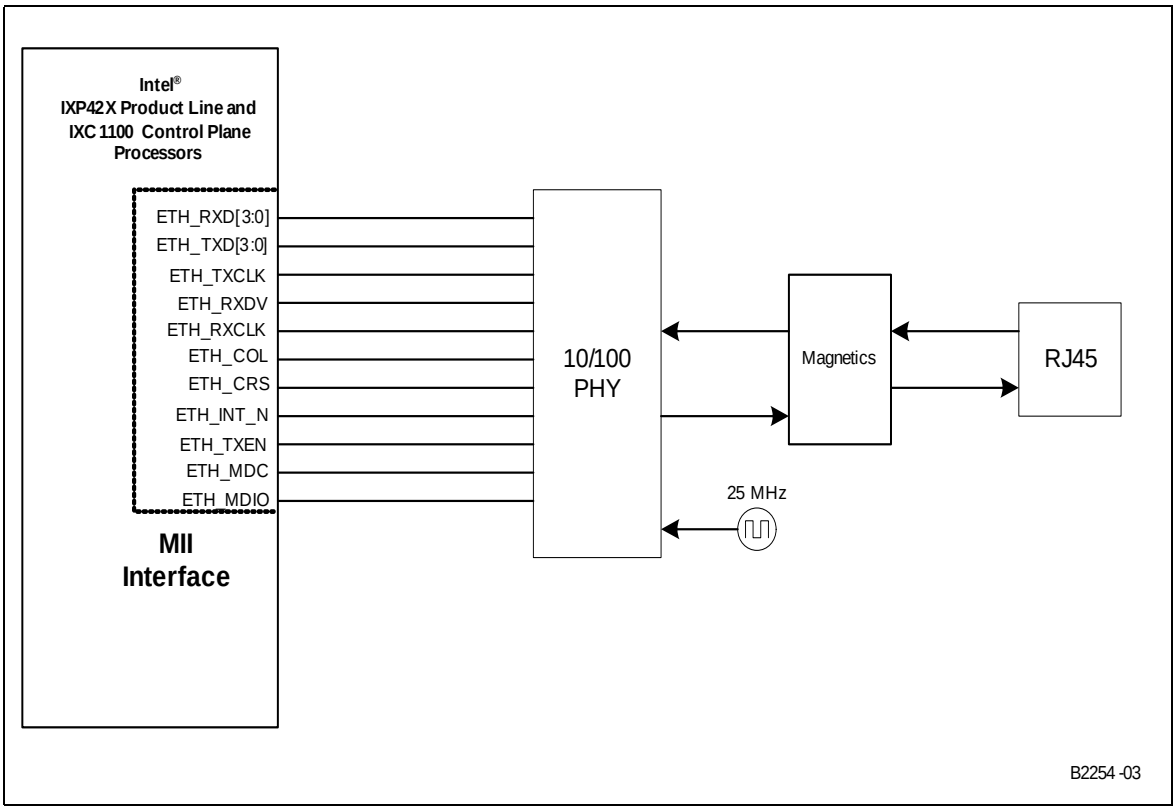
Table 7. Ethernet Interface Signals (Sheet 2 of 2)

Name	Type*	Description
ETH_RXCLK1	I	Externally supplied receive clock. • 25 MHz for 100-Mbps operation • 2.5 MHz for 10 Mbps This MAC contains hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_RXDATA1[3:0]	I	Receive data bus from PHY, data sample synchronously with respect to ETH_RXCLK1. This MAC contains hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_RXDV1	I	Receive data valid, used to inform the MII interface that the Ethernet PHY is sending data. This MAC contains hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.
ETH_COL1	I	Asserted by the PHY when a collision is detected by the PHY. This MAC contains hardware hashing capabilities. Should be pulled low through a 10-kΩ resistor when not being used in the system.
ETH_CRS1	I	Asserted by the PHY when the transmit medium or receive medium are active. De-asserted when both the transmit medium and receive medium are idle. Remains asserted throughout the duration of collision condition. PHY asserts CRS asynchronously and de-asserts synchronously with respect to ETH_RXCLK1. This MAC interface contains hardware hashing capabilities. Should be pulled high through a 10-kΩ resistor when not being used in the system.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.4.2 MII Block Diagram

Figure 10. MII Block Diagram



3.5 GPIO Interface

The IXP42X product line and IXC1100 control plane processors provide 16 general-purpose input/output pins for use in generating and capturing application specific input and output signals. Each pin can be programmed as either an input or output. When programmed as an input, GPIO0 through GPIO12 can be used as an interrupt source. In addition, GPIO14 and GPIO15 can be programmed to provide a user-programmable frequency source up to 33 MHz.

During a reset all pins are configured as inputs and remain in this state until configured otherwise, with the exception of GPIO15, which by default provides a clock output. Each GPIO pin is capable of driving external LEDs. There are eight distinct register functions used in the GPIO module. When used as an interrupt source, the interrupt capable pin can detect interrupts as active high, active low, rising edge, falling edge, or transitional.

GPIO[13:0] are general-purpose, configurable I/O pins, GPIO[12:0] can be used to capture interrupts from I/O devices connected to the GPIO interface. In addition, GPIO14 and GPIO15 can be configured as clock outputs.

3.5.1 GPIO Interface Signals

Table 8. GPIO Interface Signals

Name	Type*	Description
GPIO[12:0]	I/O	General-purpose input/output pins. May be configured as an input or an output. As an input, each signal may be configured as processor interrupts. After reset, configured as inputs by default. When not being used, pulled high with a 10-kΩ resistor.
GPIO[13]	I/O	General-purpose input/output pins can be configured as an input or an output. Default after reset is to be configured as inputs. When not being used, pulled high with a 10-kΩ resistor.
GPIO[14]	I/O	General-purpose input/output pins can be configured similar to GPIO pin 13 or as a clock output. Configuration as an output clock can be set at various speeds of up to 33 MHz with various duty cycles. Configured as an input, upon reset. When not being used, pulled high with a 10-kΩ resistor.
GPIO[15]	I/O	General-purpose input/output pins can be configured similar to GPIO pin 13 or as a clock output. Configuration as an output clock can be set at various speeds of up to 33 MHz with various duty cycles. GPIO Pin 15 is configured as an output, upon reset. GPIO Pin 15 can be used to clock the expansion interface, after reset. When not being used, pulled high with a 10-kΩ resistor.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.5.2 Design Notes

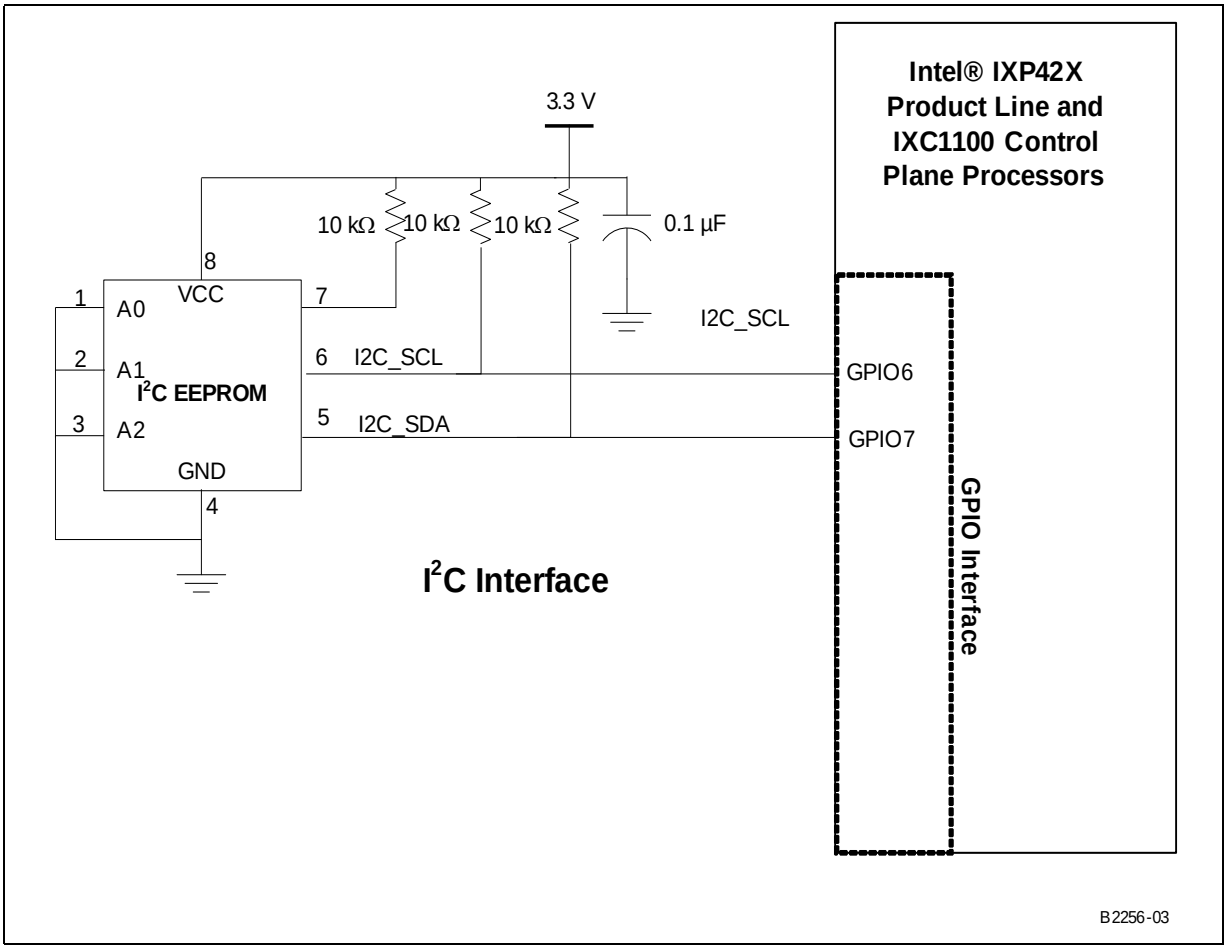
The drive strength for GPIO[15:14] is only 8 mA, so LEDs driven by these signals are not as bright. The drive strength for GPIO [13:0] is 16 mA.

3.6 I²C Interface

To provide a simple, bidirectional, two-wire serial interface called the I²C, a standardized peripheral bus connection bus can be used. While the IXP42X product line and IXC1100 control plane processors do not possess dedicated on-chip I²C support hardware, this I²C-bus can be simulated by software control of two processors' GPIO pins.

Figure 11 shows the schematic for connecting the I²C interface to a 256-byte I²C EEPROM, 7-bit addressing mode (Philips* PC8582C-2T/03) using two processors' GPIO pins (GPIO6 and GPIO7).

Figure 11. I²C EEPROM Interface



All devices connected to the I²C-bus other than the GPIO controller are automatically considered slaves. As shown in Figure 11, the I²C EEPROM acts as either a slave transmitter or slave receiver. Because the processors do not have I²C-bus interface controller on-chip, the I²C protocol is emulated on the processors using two pins of the GPIO controller (GPIO6 and GPIO7), and this component depends on functionality provided by the GPIO driver.

The GPIO software driver is used to toggle two pins on the GPIO controller, which represent the SDA and SCL lines of an I²C-bus.

The official I²C-bus protocol supports three modes of transfer rates:

- Standard Mode — up to 100 Kbps
- Fast Mode — up to 400 Kbps
- High Speed Mode — up to 3.4 Mbps

More information is available in the *Intel® IXP42X Product Line and IXC1100 Control Plane Processors: I²C Implementation Using the GPIO Pins Application Note*.

3.6.1 Pull-Ups and Pull-Downs

The *I²C-Bus Specification*, available from Philips Semiconductors*, states:

"The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit. The actual value of the pull-up is system dependent and a guide is presented in the *I²C-Bus Specification* on determining the maximum and minimum resistors to use when the system is intended for standard or fast-mode I²C bus devices."

3.6.2 Layout Notes

The maximum switching frequency of the PWM signals is 400 kHz. Therefore, layout and routing considerations are not overly stringent; however, for best results, it is recommended to adhere to standard layout practices.

Separate the physical routing of the data and clock signals and ensure that lines are not routed near other potential noise sources, such as switching regulators or signals with high switching frequencies.

3.7 USB Interface

This section describes guidelines to interface the IXP42X product line and IXC1100 control plane processors' USB device controller to an USB connector.

The processors' USB is integrated, USB 1.1-compliant and supports all standard device requests issued by any USB host controller. It is an USB device-only controller. The interface supports full-speed operation and 16 endpoints and includes an integrated transceiver.

There are:

- Six isochronous endpoints (three input and three output)
- One control endpoint
- Three interrupt endpoints
- Six bulk endpoints (three input and three output)

General USB routing guidelines can be found in Section 6.3.3, "USB Considerations" on page 67. For more detailed information, see the *Universal Serial Bus Specification*, Revision 1.1.

3.7.1 Signals

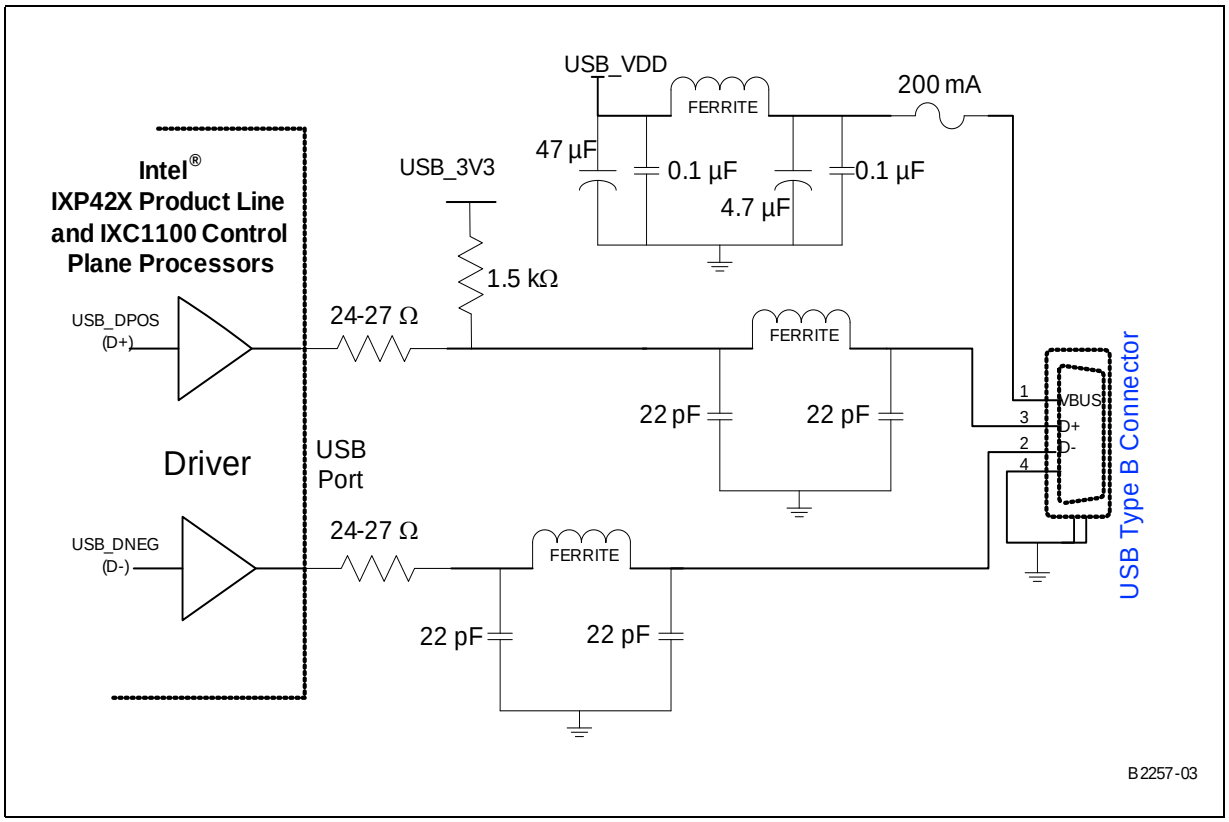
Table 9. Signals

Name	Type*	Description
USB_DPOS	I/O	Positive signal of the differential USB receiver/driver.
USB_DNEG	I/O	Negative signal of the differential USB receiver/driver.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.7.2 USB Interface

Figure 12. USB Interface



3.7.3 Design Notes

The integrated USB in the IXP42X product line and IXC1100 control plane processors is an USB-device-only controller, and it can get its power from the bus or supplies its power: bus or self-powered devices. To maintain the signal integrity and to minimize end-user termination problems, the termination is required for the processors' USB design, based on what kind of driver is used, whether the transceiver operates in full-speed (12 Mbps) or low-speed (1.5 Mbps), and if the port is upstream or downstream. For more details, refer to the *Universal Serial Bus Specification*, Revision 1.1.

The USB device controller, client only, integrated in the IXP42X product line and IXC1100 control plane processors, is compliant with the *Universal Serial Bus Specification*, Revision 1.1, and uses USB_DPOS and USB_DNEG as a differential output driver to drive the USB data signal onto the USB cable. If designers want to implement the USB_DPOS and USB_DNEG lines as downstream lines, 15-kΩ, pull-down resistors must be used on the USB_DPOS and USB_DNEG lines.

Note that:

- If a 1.5-kΩ, pull-up resistor is connected to USB_DPOS line, the USB port is identified as full-speed (12 Mbps). (See Figure 12 on page 39) If a 1.5-kΩ, pull-up resistor is connected to USB_DNEG line, the USB port is identified as low-speed (1.5 Mbps).

- The processors' USB drivers are the CMOS drivers. To achieve matching impedance, series resistors are included on both USB_DPOS and USB_DNEG differential driver lines. The value of the series resistor depends upon the variation of the driver's impedance.

3.8 UTOPIA Interface

The IXP421 and IXP425 processors have the UTOPIA-2 coprocessor and provide an interface between an internal network processing engine and UTOPIA-2 interface, and the UTOPIA-2 interface is an industry-standard bus for connecting to ATM physical devices (PHYs).

The UTOPIA-2 coprocessor is configured as a master. The UTOPIA-2 interface supports up to four external UTOPIA-2 devices and eight logical channels with cell-level or octet-level handshaking. The network processing engine handles segmentation and reassembly of ATM cells, CRC checking/generation, and transfer of data to/from memory. This allows parallel processing of data traffic on the UTOPIA-2 interface, off-loading processor overhead required by the Intel XScale® Processor.

The IXP421 and IXP425 processors are compliant with the ATM Forum, *UTOPIA Level-2 Specification*, Revision 1.0; for optimal design results, it is recommended to follow the guidelines of the Specification.

3.8.1 Interface Signals

Table 10. Interface Signals (Sheet 1 of 2)

Signal	I/O*	Description
UTP_OP_CLK	I	UTOPIA Transmit clock input. Also known as UTP_TX_CLK. This signal is used to synchronize all UTOPIA-transmit outputs to the rising edge of the UTP_OP_CLK. This signal should be pulled high through a 10-kΩ resistor, if not being used.
UTP_OP_FCO	O	UTOPIA flow control output signal. Also known as the TXENB_N signal. Used to inform the selected PHY that data is being transmitted to the PHY. Placing the PHY's address on the UTP_OP_ADDR — and bringing UTP_OP_FCO to logic 1, during the current clock — followed by the UTP_OP_FCO going to a logic 0, on the next clock cycle, selects which PHY is active in MPHY mode. In SPHY configurations, UTP_OP_FCO is used to inform the PHY that the processor are ready to send data.
UTP_OP_SOC	O	Start of Cell. Also known as TX_SOC. Active high signal is asserted when UTP_OP_DATA contains the first valid byte of a transmitted cell.
UTP_OP_DATA[7:0]	O	UTOPIA output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA-Level-2-compliant PHY.
UTP_OP_ADDR[4:0]	O	Transmit PHY address bus. Used by the processor when operating in MPHY mode to poll and select a single PHY at any given time.
UTP_OP_FCI	I	UTOPIA Output data flow control input: Also known as the TXFULL/CLAV signal. Used to inform the IXP42X product line and IXC1100 control plane processors of the ability of each polled PHY to receive a complete cell. For cell-level flow control in an MPHY environment, TxClav is an active high tri-stateable signal from the MPHY to ATM layer. The UTP_OP_FCI, which is connected to multiple MPHY devices, will see logic high generated by the PHY, one clock after the given PHY address is asserted — when a full cell can be received by the PHY. The UTP_OP_FCI will see a logic low generated by the PHY one clock cycle, after the PHY address is asserted — if a full cell cannot be received by the PHY. This signal should be pulled high through a 10-kΩ resistor if not being used.
UTP_IP_CLK	I	UTOPIA Receive clock input. Also known as UTP_RX_CLK. This signal is used to synchronize all UTOPIA-received inputs to the rising edge of the UTP_IP_CLK. This signal should be pulled high through a 10-kΩ resistor, if not being used.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

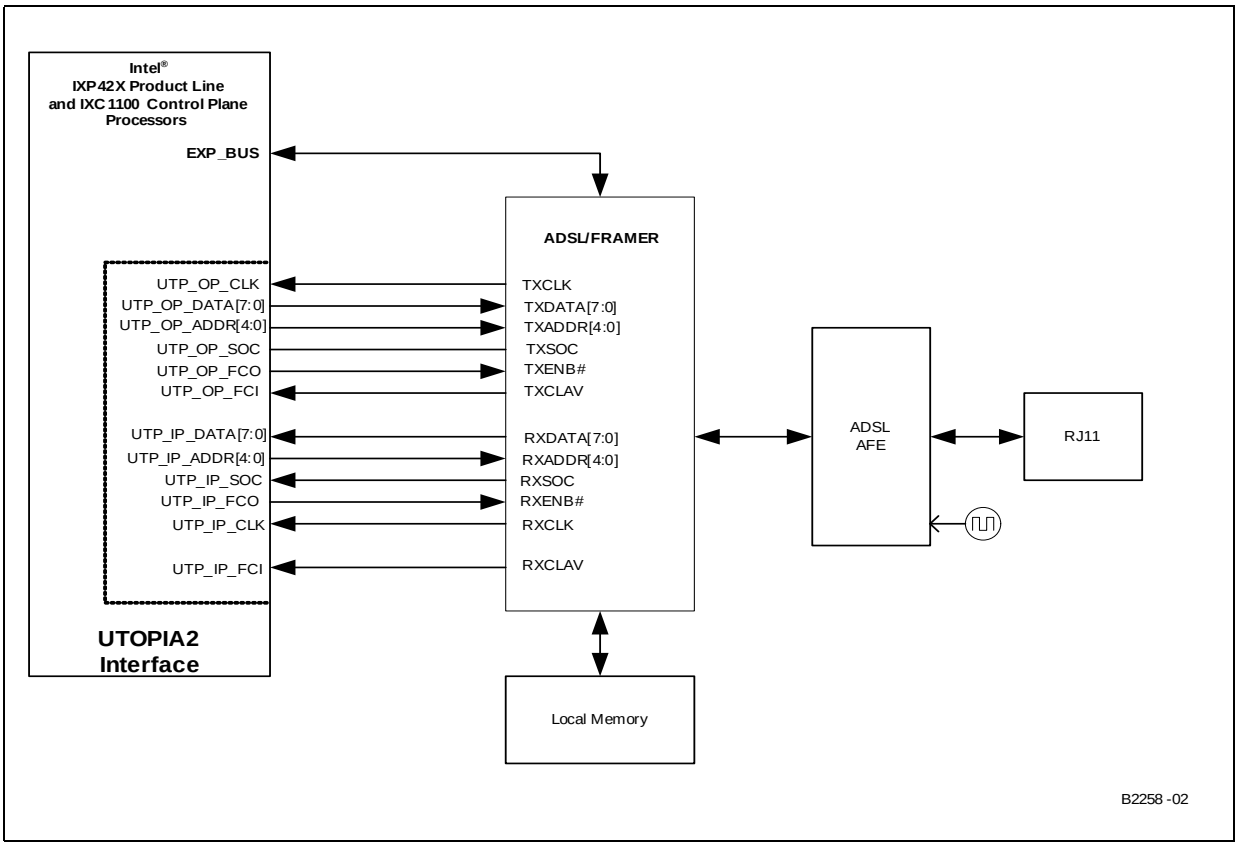
Table 10. Interface Signals (Sheet 2 of 2)

Signal	I/O*	Description
UTP_IP_FCI	I	UTOPIA Input Data flow control input signal. Also known as RXEMPTY/CLAV. Used to inform the processor of the ability of each polled PHY to send a complete cell. For cell-level flow control in an MPHY environment, RxClav is an active-high tri-stateable signal from the MPHY to ATM layer. The UTP_IP_FCI, which is connected to multiple MPHY devices, will see logic high generated by the PHY, one clock after the given PHY address is asserted, when a full cell can be received by the PHY. The UTP_IP_FCI will see a logic low generated by the PHY, one clock cycle after the PHY address is asserted if a full cell cannot be received by the PHY. In SPHY mode, this signal is used to indicate to the processor that the PHY has an octet or cell available to be transferred to the processor. The signal should be tied high through a 10-kΩ resistor when not being used in the system.
UTP_IP_SOC	I	Start of Cell. RX_SOC Active-high signal that is asserted when UTP_IP_DATA contains the first valid byte of a transmitted cell. The signal should be pulled high through a 10-kΩ resistor, when not being used in the system.
UTP_IP_DATA[7:0]	I	UTOPIA input data. Also known as RX_DATA. Used by to the processor to receive data from an ATM UTOPIA-Level-2-compliant PHY. Should be tied high through a 10-kΩ resistor, when not being used in the system.
UTP_IP_ADDR[4:0]	O	Receive PHY address bus. Used by the processor when operating in MPHY mode to poll and select a single PHY at any one given time.
UTP_IP_FCO	O	UTOPIA Input Data Flow Control Output signal: Also known as the RX_ENB_N. In SPHY configurations, UTP_IP_FCO is used to inform the PHY that the processor is ready to accept data. In MPHY configurations, UTP_IP_FCO is used to select which PHY will drive the UTP_RX_DATA and UTP_RX_SOC signals. The PHY is selected by placing the PHY's address on the UTP_IP_ADDR and bringing UTP_OP_FCO to logic 1 during the current clock, followed by the UTP_OP_FCO going to a logic 0 on the next clock cycle.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.8.2 UTOPIA-2 Interface Block Diagram

Figure 13. UTOPIA Interface



3.9 HSS Interface

The IXP421 and IXP425 processors have the High Speed Serial (HSS) coprocessor integrated, and its primary function is to provide connection between an internal network processing engine and an external HSS interface.

The HSS can directly interface to SLIC/CODEC devices for voice applications, to serial DSL framers and also support the serial protocols, including T1, E1, and MVIP.

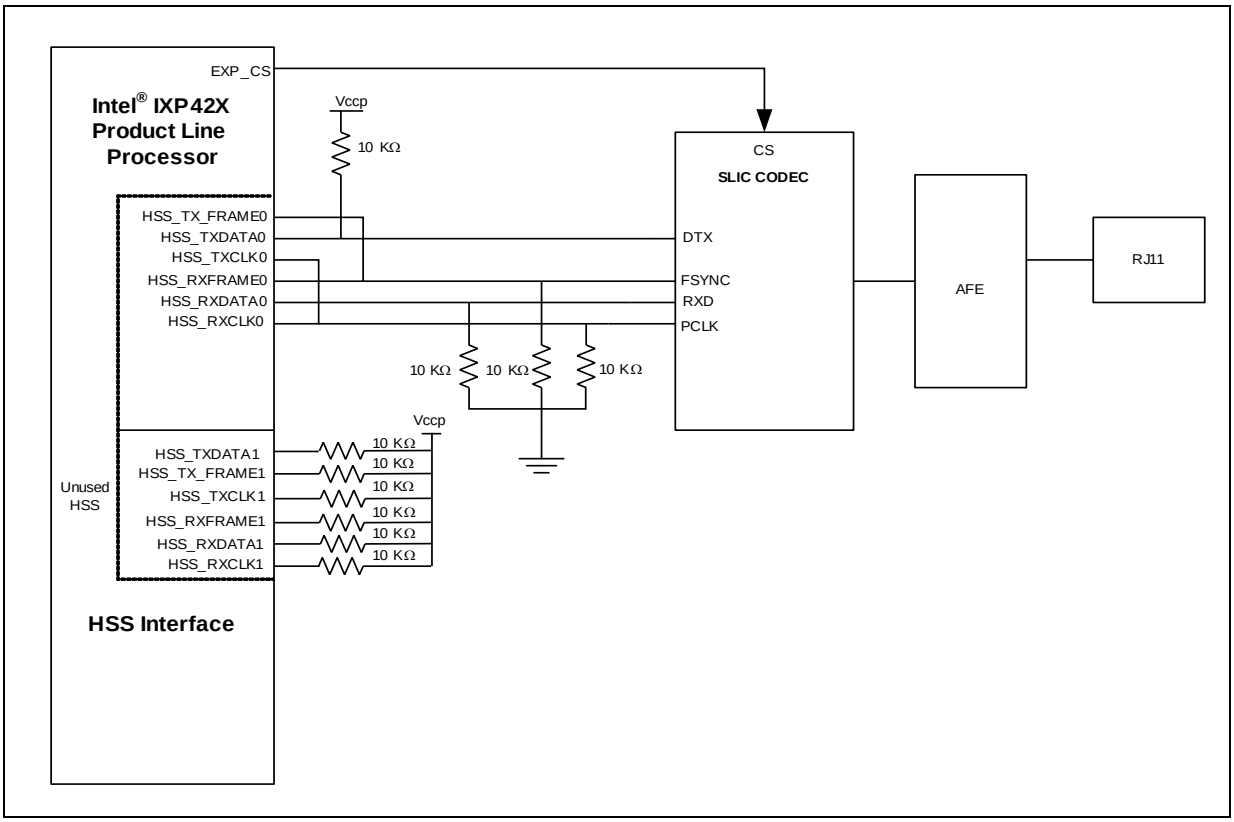
3.9.1 Interface Signals

Name	Type	Description
HSS_TXFRAME1	I/O	The High-Speed Serial (HSS) transmit frame signal can be configured as an input or an output to allow an external source to be synchronized with the transmitted data. Often known as a Frame Sync signal. Configured as an input upon reset. Should be pulled high through a 10-kΩ resistor when not being used in the system.
HSS_TXDATA1	O/D	Transmit data out. Open-drain output. Must be pulled up with a 10-kΩ resistor to V_{CCP}.
HSS_TXCLK1	I/O	The High-Speed Serial (HSS) transmit clock signal can be configured as an input or an output. The clock can be a frequency ranging from 512 KHz to 8.192 MHz. Used to clock out the transmitted data. Configured as an input upon reset. Frame sync and Data can be selected to be generated on the rising or falling edge of the transmit clock. Should be pulled high through a 10-kΩ resistor when not being used in the system.
HSS_RXFRAME1	I/O	The High-Speed Serial (HSS) receive frame signal can be configured as an input or an output to allow an external source to be synchronized with the received data. Often known as a Frame Sync signal. Configured as an input upon reset. Should be pulled high through a 10-kΩ resistor when not being used in the system.
HSS_RXDATA1	I	Receive data input. Can be sampled on the rising or falling edge of the receive clock. Should be pulled high through a 10-kΩ resistor when not being used in the system.
HSS_RXCLK1	I/O	The High-Speed Serial (HSS) receive clock signal can be configured as an input or an output. The clock can be from 512 KHz to 8.192 MHz. Used to sample the received data. Configured as an input upon reset. Should be pulled high through a 10-kΩ resistor when not being used in the system.
HSS_TXFRAME0	I/O	The High-Speed Serial (HSS) transmit frame signal can be configured as an input or an output to allow an external source become synchronized with the transmitted data. Often known as a Frame Sync signal. Configured as an input upon reset. Should be pulled high through a 10-kΩ resistor when not being used in the system.
HSS_TXDATA0	O/D	Transmit data out. Open-drain output. Must be pulled up with a 10-kΩ resistor to V_{CCP}.
HSS_TXCLK0	I/O	The High-Speed Serial (HSS) transmit clock signal can be configured as an input or an output. The clock can be a frequency ranging from 512 KHz to 8.192 MHz. Used to clock out the transmitted data. Configured as an input upon reset. Frame sync and data can be selected to be generated on the rising or falling edge of the transmit clock. Should be pulled high through a 10-kΩ resistor when not being used in the system.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.9.2 HSS Interface Block Diagram

Figure 14. HSS Interface



3.10 PCI Interface

The IXP42X product line and IXC1100 control plane processors' PCI controller is an industry-standard, 32-bit interface, high-performance, low-latency system bus that operates at either 33 or 66 MHz. It is compliant with the *PCI Local Bus Specification*, Rev. 2.2.

The PCI Controller supports operation as a PCI host and implements a PCI arbiter for a system containing up to four external PCI devices.

As indicated in Figure 15, a PCI transparent bridge is needed to support compactPCI.

General PCI routing guidelines can be found in Section 7.2, "PCI Topologies" on page 75. For more detailed information, see the *PCI Local Bus Specification*, Rev. 2.2.

3.10.1 PCI Interface Signals

Table 11. PCI Bus Signals (Sheet 1 of 2)

Name	Type*	Description
PCI_AD[31:0]	I/O	PCI Address/Data bus used to transfer address and bidirectional data to and from multiple PCI devices. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_CBE_N[3:0]	I/O	PCI Command/Byte Enables used as a command word during an PCI address cycles and byte enables for data cycles. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_PAR	I/O	PCI Parity used to check parity across the 32 bits of PCI_AD and the four bits of PCI_CBE_N. Should be pulled high with a 10-kΩ resistor when not being used in the system.
PCI_FRAME_N	I/O	PCI Cycle Frame used to signify the beginning and duration of a transaction. The signal will be inactive prior to or during the final data phase of a given transaction. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_TRDY_N	I/O	PCI Target Ready informs that the target of the PCI bus is ready to complete the current data phase of a given transaction. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_IRDY_N	I/O	PCI Initiator Ready informs that the initiator to complete the current data phase of a given transaction. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_STOP_N	I/O	PCI Stop indicates that the current target is requesting the current initiator to stop the current transaction. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_PERR_N	I/O	PCI Parity Error is asserted when a PCI parity error is detected between the PCI_PAR and the associated information on the PCI_AD bus and PCI_CBE_N during all PCI transactions except for special cycles. The agent that is receiving data will drive this signal. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_SERR_N	I/OD	PCI System Error asserted when a parity error occurs on special cycles or any other error that will cause the PCI bus not to function properly. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_DEVSEL_N	I/O	PCI Device Select: • When used as an output, PCI_DEVSEL_N indicates that device has decoded that address as the target of the requested transaction. • When used as an input, PCI_DEVSEL_N indicates if any device on the PCI bus exists with the given address. Should be pulled high with a 10-kΩ resistor when not being used in the system.
PCI_IDSEL	I	PCI Initialization Device Select is a chip select during configuration reads and writes. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.
PCI_REQ_N[3:1]	I	PCI arbitration request: Used by the internal PCI arbiter to allow an agent to request the PCI bus. Should be pulled high with a 10-kΩ resistor when the PCI bus is not being used in the system.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

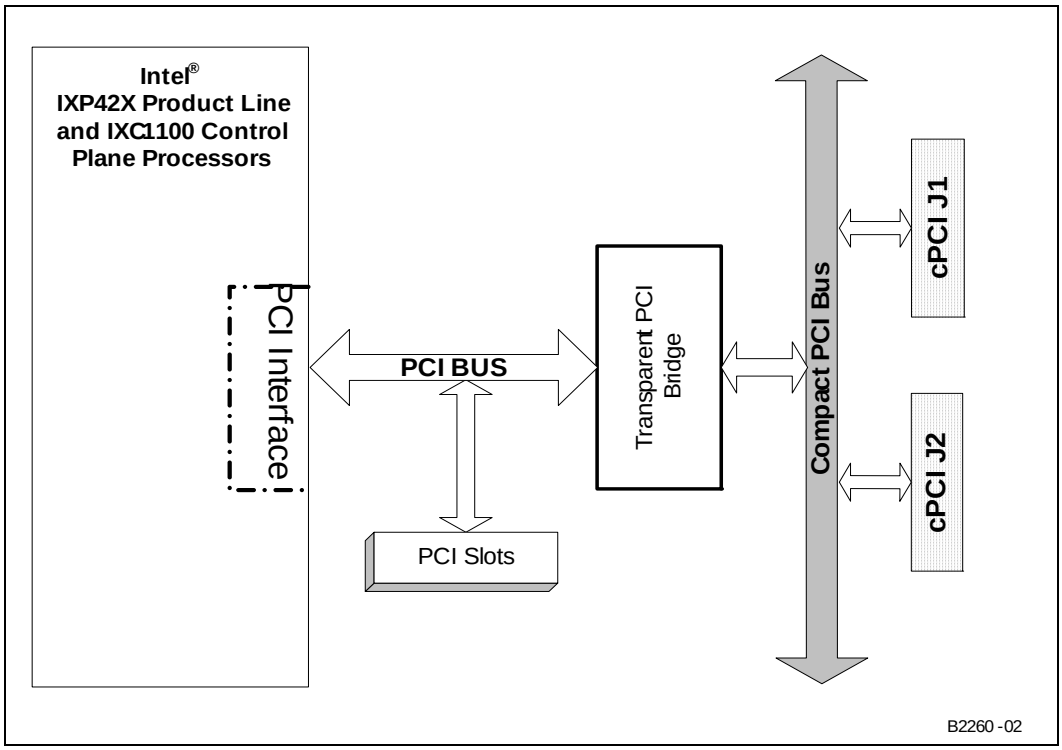
Table 11. PCI Bus Signals (Sheet 2 of 2)

Name	Type*	Description
PCI_REQ_N[0]	I/O	PCI arbitration request: • When configured as an input (PCI arbiter enabled), the internal PCI arbiter will allow an agent to request the PCI bus. • When configured as an output (PCI arbiter disabled), the pin will be used to request access to the PCI bus from an external arbiter. Should be pulled high with a 10-kΩ resistor, when the PCI bus is not being used in the system.
PCI_GNT_N[3:1]	O	PCI arbitration grant: Generated by the internal PCI arbiter to allow an agent to claim control of the PCI bus.
PCI_GNT_N[0]	I/O	PCI arbitration grant: • When configured as an output (PCI arbiter enabled), the internal PCI arbiter to allow an agent to claim control of the PCI bus. • When configured as an input (PCI arbiter disabled), the pin will be used to claim access of the PCI bus from an external arbiter. Should be pulled high with a 10-kΩ resistor when not being used in the system.
PCI_INTA_N	O/D	PCI interrupt: Used to request an interrupt. Should be pulled high with a 10-kΩ resistor.
PCI_CLKIN	I	PCI Clock: Clock provides timing for all transactions on PCI. All PCI signals, except **INTA**#, **INTB**#, **INTC**#, and **INTD**#, are sampled on the rising edge of **CLK** and timing parameters are defined with respect to this edge. The PCI clock rate can operate at up to 66 MHz. Should be pulled high with a 10-kΩ resistor when the PCI bus is not used in the system.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.10.2 PCI Interface Block Diagram

Figure 15. PCI Interface



When one of the IXP42X product line and IXC1100 control plane processors is host, it may interface to four PCI slots at 33 MHz or two PCI slots at 66 MHz. The limitation to two slots at 66 MHz is due to load requirements to maintain signal integrity at the higher frequency.

The PCI-to-PCI bridge must be used in order to address the PCI requirement that no more than one load may be placed on the CompactPCI connector unless it is through a PCI-to-PCI bridge. The IDSEL signals on the PCI slots can be connected onto the PCI_AD bus.

3.10.3 Design Notes

- The processors do not support a 5-V PCI signal interface. They support 3.3-V signal interfaces only.
- The *PCI Local Bus Specification*, Rev. 2.2 requires that the bus is always “parked.” Some device is always driving the AD lines so there should NOT be any pull-ups on these signals. The specification states that the following control lines should be pulled up: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, and INTD#.
- The processors’ GPIO pins can be used by PCI devices on PCI slots to request an interrupt from the processors’ PCI controller.
- PCI_INTA_N is an open-drain signal and is used to request an interrupt from an external PCI host if the processors implements PCI in option mode.

3.11 JTAG Interface

JTAG is the IEEE Standards 1149.1-1990 and 1149.1a-1993, *IEEE Standard Test Access Port and Boundary-Scan Architecture*, with support for:

- Board-level boundary-scan connectivity testing
- Connection to software debugging tools through the JTAG interface
- In-system programming of programmable memory and logic devices on the PCB

Refer to the IEEE 1149.1 standard for an explanation of the terms used in this section and a complete description of the TAP-controller states. The interface is controlled through five dedicated test access port (TAP) pins: TDI, TMS, TCK, nTRST, and TDO, as described in Table 12. The boundary-scan test-logic elements include the TAP pins, TAP controller, instruction register, boundary-scan register, bypass register, device identification register, and data-specific registers. These are described in the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*.

The IXP42X product line and IXC1100 control plane processors may be controlled during debug through a JTAG interface to the processor, the debug tools such as the Macraigor* Raven*, EPI* Majic*, Wind River Systems* visionPROBE* / visionICE* or various other JTAG tools plug into the JTAG interface through a connector.

3.11.1 Interface Signals

Table 12. JTAG Interface Signals

Name	Type*	Description
JTG_TMS	I	Test mode select for the IEEE 1149.1 JTAG interface.
JTG_TDI	I	Input data for the IEEE 1149.1 JTAG interface.
JTG_TDO	O	Output data for the IEEE 1149.1 JTAG interface.
JTG_TRST_N	I	Used to reset the IEEE 1149.1 JTAG interface. The JTG_TRST_N signal must be asserted (driven low) during power-up, otherwise the TAP controller may not be initialized properly, and the processor may be locked. When the JTAG interface is not being used, the signal must be pulled low using a 10-kΩ resistor.
JTG_TCK	I	Used as the clock for the IEEE 1149.1 JTAG interface.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.11.2 Pull-Up/Down Resistors

The IEEE 1149.1 standard effectively requires that JTG_TDI, JTG_TMS, and JTG_TRST_N have internal pull-up resistors. It is recommended that the JTG_TDI and JTG_TMS pins be left unconnected when not in use. To initialize JTAG, JTG_TRST_N must be asserted at power-on. JTG_TRST_N must be tied low in cases where JTAG is not used.

3.12 Clock

The IXP42X product line and IXC1100 control plane processors require a 33.33-MHz reference clock that generates all processor and most internal peripheral clocks. The 33.33-MHz reference clock may be generated using onboard oscillator or PLL chip. This clock is multiplied internally by the processors to 133 MHz and driven to the PC133 SDRAM interface.

The interfaces require oscillators on the board.

- Processors' system clock – 33.33 MHz
- PCI host clock – 33 MHz and 66 MHz selectable
- Expansion bus clock – This expansion bus clock may be driven through GPIO15 or using an external oscillator.

Although some interfaces require similar frequency oscillators (for example, the expansion bus, and PCI), separate oscillators are used for each to allow oscillator frequencies to be altered on each interface independently.

The PCI clock is driven out of the PCI-to-PCI bridge when one of the processors is in option mode and is driven by either the processors (GPIO14) or an external oscillator when one of the processors is host.

3.12.1 Clock Signals

Table 13. Clock Signals

Name	Type*	Description
OSC_IN	I	33.33-MHz sinusoidal input signal. Can be driven by an oscillator.
OSC_OUT	O	33.33-MHz sinusoidal output signal. Left disconnected when being driven by an oscillator.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

3.12.2 Using Oscillator

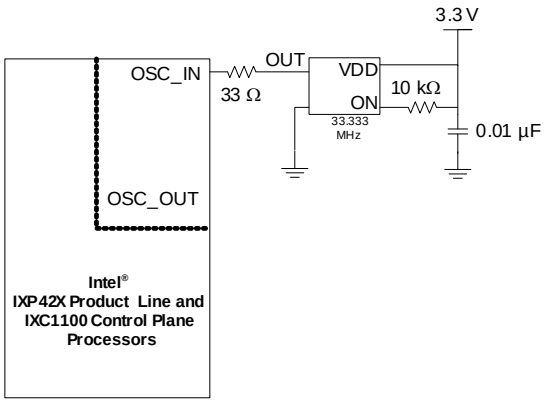
When an external oscillator is used to supply the 33.33-MHz clock, connect the oscillator output to the OSC_IN pin. Leave the OSC_OUT pin floating. Figure 16 shows the connections of an oscillator to the IXP42X product line and IXC1100 control plane processors.

3.12.3 Design Notes

When an external oscillator is used to supply the 33.33-MHz clock, it takes about 9.0 µs for the internal IXP42X product line and IXC1100 control plane processors' PLL to lock.

3.12.4 Block Diagram

Figure 16. Clock Connections



Oscillator Connection

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3.13 Power

Table 14. Power Pins (Sheet 1 of 2)

Name	Type*	Description
VCC	I	1.3-V power supply input pins used for the internal logic of the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor.
VCCP	I	3.3-V power supply input pins used for the peripheral (I/O) logic of the IXP42X product line and IXC1100 control plane processors.
VSS		Ground power supply input pins used for both the 3.3-V and the 1.3-V power supplies.
VCCOSCP	I	3.3-V power supply input pins used for the peripheral (I/O) logic of the analog oscillator circuitry on the IXP42X product line and IXC1100 control plane processors. Require special power-filtering circuitry. Refer to the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for proper implementation.
VSSOSCP	I	Ground input pins used for the peripheral (I/O) logic of the analog oscillator circuitry on the IXP42X product line and IXC1100 control plane processors. Used in conjunction with the VCCOSCP pins. Require special power filtering circuitry. Refer to the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for proper implementation.
VCCOSC	I	1.3-V power supply input pins used for the internal logic of the analog oscillator circuitry on the IXP42X product line and IXC1100 control plane processors. Require special power-filtering circuitry. Refer to the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for proper implementation.
VSSOSC	I	Ground power supply input pins used for the internal logic of the analog oscillator circuitry on the IXP42X product line and IXC1100 control plane processors. Used in conjunction with the VCCOSC pins. Refer to the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for proper implementation.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

Table 14. Power Pins (Sheet 2 of 2)

Name	Type*	Description
VCCPLL1	I	1.3-V power supply input pins used for the internal logic of the analog, phase-lock loop circuitry on IXP42X product line and IXC1100 control plane processors. Require special power-filtering circuitry. Refer to the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for proper implementation.
VCCPLL2	I	1.3-V power supply input pins used for the internal logic of the analog, phase-lock loop circuitry on IXP42X product line and IXC1100 control plane processors. Refer to the*Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet* for proper implementation.

Note: For explanations of the **Type** column abbreviations, see Table 21 on page 81.

To enable low power system design, the IXP42X product line and IXC1100 control plane processors have separate power supply domains for the processor core, SDRAM memory, and peripherals.

3.13.1 Power Supply Requirements

The main power supply domains for the IXP42X product line and IXC1100 control plane processors are 1.3 V (VCC) for the Intel XScale® Processor and 3.3 V (VCCP) for I/O signaling voltage.

3.13.2 +3.3 V DC

It is suggested that the +3.3-V supply tolerance is +/-5% and a maximum current of 3 A and is provided by an on-board DC-DC switch-mode voltage regulator.

3.13.3 +1.3 V DC

The +1.3V DC needed for the Intel XScale® Processor can be generated using a DC-DC switch-mode voltage regulator and derived from the +3.3-V rail.

3.13.4 Power Up

The 3.3-V I/O voltage (V_{CCP}) must be powered up 1 µs before the processor voltage (V_{CC}). The IXP42X product line and IXC1100 control plane processors' voltage (V_{CC}) must never become stable prior to the 3.3-V I/O voltage (V_{CCP}). The V_{CCOSC}, V_{CCPLL1}, and V_{CCPLL2} voltages follow the V_{CC} power-up pattern. The V_{CCOSCP} follows the V_{CCP} power-up pattern. The value for T_{POWER_UP} must be at least 1 µs. The T_{POWER_UP} timing parameter is measured from V_{CCP} at 3.3 V and V_{CC} at 1.3 V.

Note: The PWRON_RESET_N signal is a 1.3-V signal.

Note: The SDRAM clock starts with the release of PWRON_RESET_N. The first access made by the internal auto-refresh counter (set to default value of 0x384) happens ~7µs after RESET_IN_N is released. Software will not be able to disable this counter before the first access is made. To meet a specific SDRAMs 100-200 ms requirement before the first access, the designer may have to add additional delay between PWRON_RESET_N, and RESET_IN_N beyond the required minimum of 10 ns.

Figure 17 and Figure 18 show the relationship between power up, and reset timings.

Figure 17. Power-up Sequence Timing

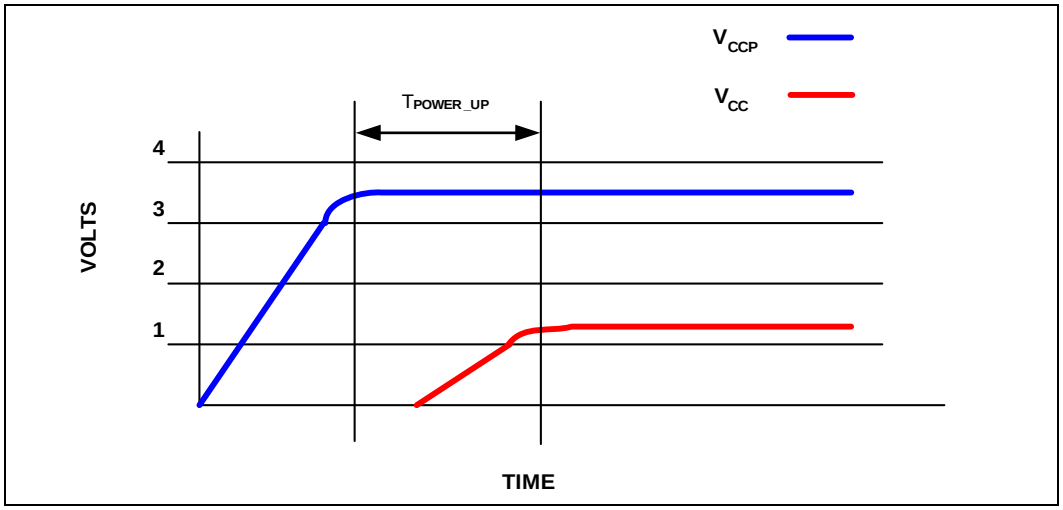

Figure 18. Reset Timings

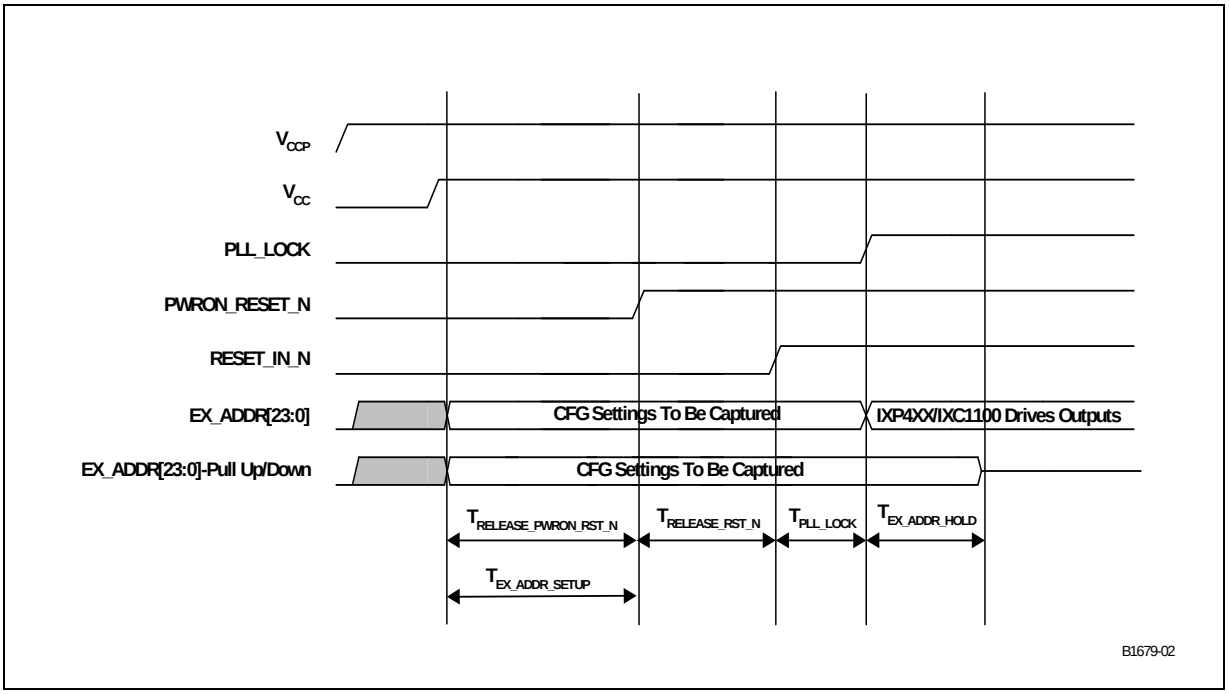

Table 15. Reset Timings Table Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Note
$T_{RELEASE\_PWRON\_RST\_N}$	Minimum time required to hold PWRON_RESET_N at logic 0 after a stable power has been applied to the IXP42X Product Line and IXC100 Plane Processors.	2000			ns	1
$T_{RELEASE\_RESET\_IN\_N}$	Minimum time required to hold the RESET_IN_N at logic 0 state after PWRON_RST_N has been released to a logic 1 state. The RESET_IN_N signal must be held low when the PWRON_RST_N signal is held low.	10			ns	
T_{PLL_LOCK}	Maximum time for PLL_LOCK signal to drive to logic 1 after RESET_IN_N is driven to logic 1 state. The boot sequence does not occur until this period is complete.			10	µs	3
$T_{EX\_ADDR\_SETUP}$	Minimum time for the EX_ADDR signals to drive the inputs prior to RESET_IN_N being driven to logic 1 state. This is used for sampling configuration information.	50			ns	2
$T_{EX\_ADDR\_HOLD}$	Minimum/maximum time for the EX_ADDR signals to drive the inputs prior to PLL_LOCK being driven to logic 1 state. This is used for sampling configuration information.	0		20	ns	2
T_{WARM_RESET}	Minimum time required to hold RESET_IN_N at logic 0 to cause a Warm Reset in the IXP42X Product Line and IXC1100 Plane Processors. During this period, the power supply must not be disrupted and PWRON_RESET_N must remain at logic high during the entire process.	500			ns	

Notes:

1. $T_{RELEASE\_PWRON\_RST\_N}$ is the time required for the internal oscillator to reach stability.
2. The expansion bus address is captured during RESET_IN_N signal transition from low to high. When a programmable-logic device is used to drive the EX_ADDR signals, instead of pull-downs, the signals must be held stable until the PLL_LOCK goes high.
3. PLL_LOCK is deasserted immediately when watchdog timer event occurs, or when RESET_IN_N is asserted, or when PWRON_RST_N is asserted. PLL_LOCK remains deasserted for ~24 ref_clocks after the watchdog reset is deasserted (internal to the chip). A ref clock time period is 1/CLKIN.

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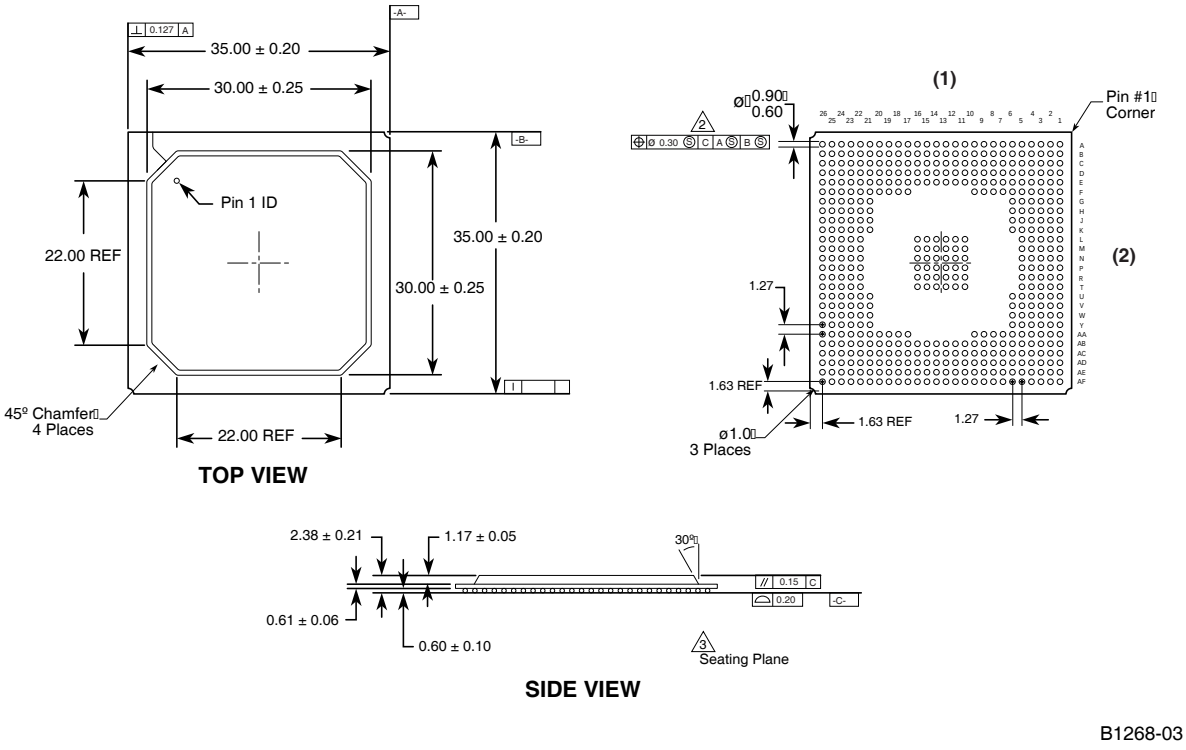
4.0 PBGA Package

4.1 PBGA Package Overview

The Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor have a 492-ball, PBGA package for commercial temperature applications and a pin-for-pin-compatible, 492-ball, PBGA with a drop-in heat spreader for extended temperature applications. Figure 19 shows the top and bottom view of the processors.

For detailed signal descriptions, see the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet*.

Figure 19. 492-Ball PBGA Package

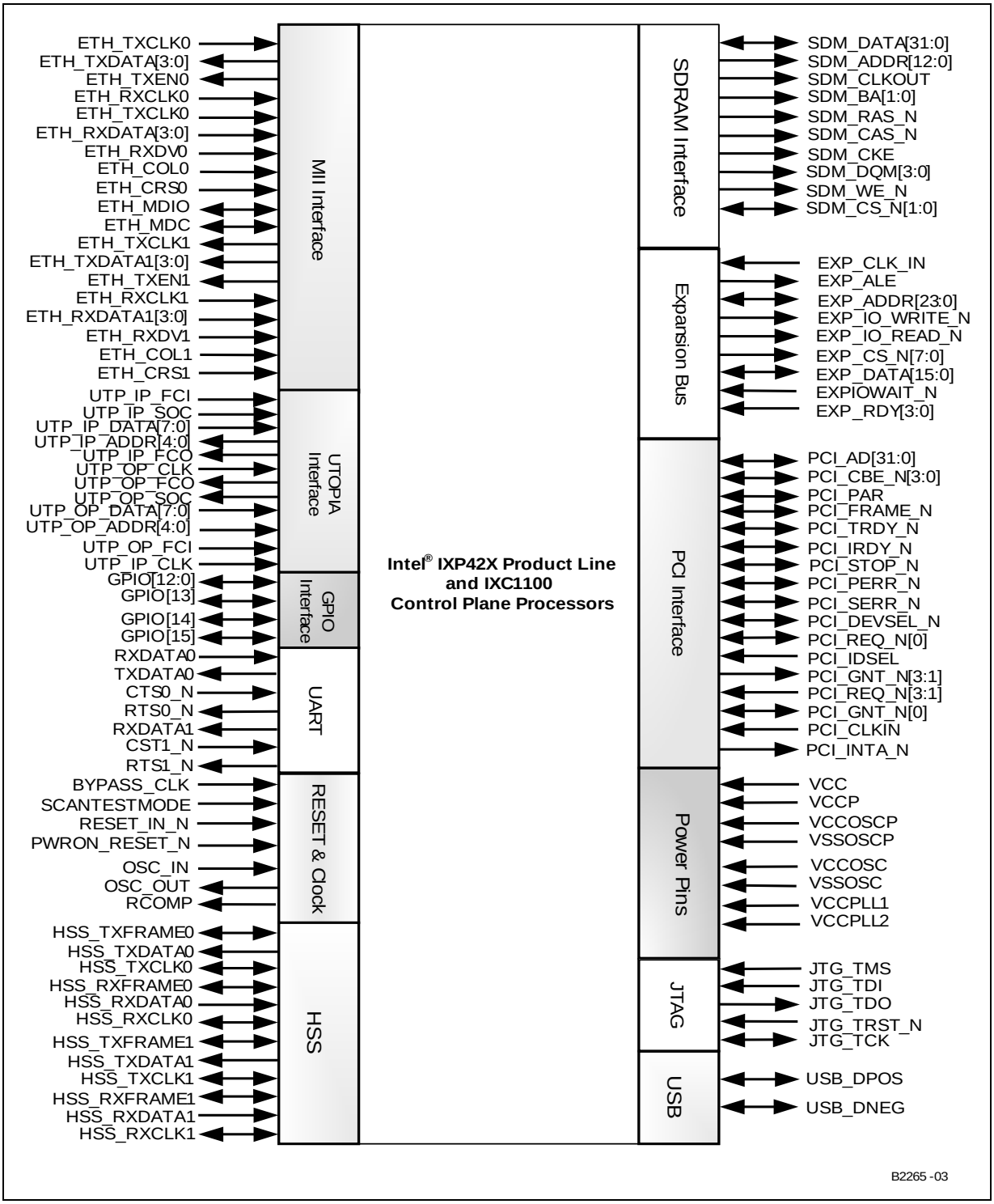


Notes:
1. All measurements are in millimeters (mm).
2. The size of the land pad at the interposer side (1) is 0.81 mm.
3. The size of the solder resist at the interposer side (2) is 0.66 mm.

4.2 Signal Grouping

Figure 20 illustrates how function pins are grouped on the IXP42X product line and IXC1100 control plane processors. This diagram is helpful in placing components around the processors for the layout of a PCB. Consider this signal layout to simplify routing and minimize the number of cross traces.

Figure 20. Devices' Signals by Function



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5.0 General PCB Guide

5.1 PCB Overview

Beginning with components selection, this chapter presents general PCB guidelines. In cases where it is too difficult to adhere to a guideline, engineering judgment must be used. The methods are listed below as simple DOs and DON'Ts.

This chapter does not discuss the functional aspects of any bus, or layout guides for any interfaced devices.

5.2 General Recommendations

It is recommended that boards based on the IXP42X product line and IXC1100 control plane processors employ a PCB stackup yielding a target impedance of 50 Ω ± 10% with 5 mil nominal trace width; that is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces.

When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce cross-talk and settling time.

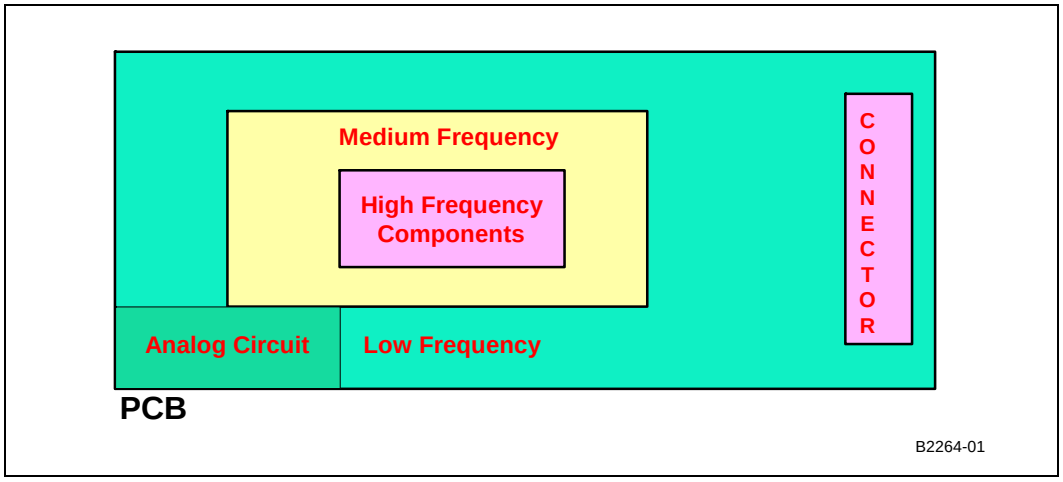
5.3 Component Selection

- Do not use components faster than necessary
  - — Clock rise (fall) time should be as slow as possible, as the spectral content of the waveform decreases
- Use components with output drive strength (slew-rate) controllable if available
- Use SMT components (not through-hole components) as through-hole (leaded) components have more stub inductance due to the protruding leads.
- Avoid sockets when possible
- Minimize number of connectors

5.4 Component Placement

Place ALL high-frequency components in the middle; medium-frequency around the high-frequency components; and the low-frequency components around the edge of the printed circuit board, as shown in "Component Placement on a PCB" on page 58.

Figure 21. Component Placement on a PCB



- Place noisy parts (clock, processor, video, etc.) at least 1.5 – 3 inches away from the edge of the printed circuit board.
- Do not place noisy components close to internal/external cables
  - — they will pick up the noise and radiate
  - — Be aware of the peak in-rush surge current into the device pins. This surge current may inject high-frequency switching noise into power planes of the printed circuit board.
- Place high-current components near the power sources.
- Do not share the same physical components (buffers, inverters, etc.) between high-speed and low-speed signals. Use separate parts.
- Place clock drivers and receivers such that clock trace length is minimized.
- Place clock generation circuits near a ground stitch location. Place a localized ground plane around the clock circuits and connect the localized plane to system ground plane.
- Install clock circuits directly on the printed circuit board; not on sockets.
- Clock crystals should lie FLAT against the board to provide better coupling of electromagnetic fields to the board.

5.5 Stack Up Selection

Stack-up selection directly affects the trace geometry which, in turn, affects the characteristic impedance requirement for the printed-circuit board. Additionally, the “clean,” noise-free-planes design and placement is significantly important as components run at higher speeds requiring more power. Considerations include:

- Low-speed, printed-circuit-board construction — for example two-layer boards:
  - — Advantages:
    - Inexpensive
    - Manufactured by virtually all printed-circuit-board vendors
  - — Disadvantages:
    - Poor routing density
    - Uncontrolled signal trace impedance

    - Lack of power/ground planes, resulting in unacceptable cross-talk
    - Relatively high-impedance power distribution circuitry, resulting in noise on the power and ground rails
- High-speed circuits require multi-layer printed circuit boards;
  — Advantages:
    - Controlled-impedance traces
    - Low-impedance power distribution

  — Disadvantages:
    - Higher cost
    - More weight
    - Manufactured by fewer vendors
- Symmetry is essential to keep the board stack-up symmetric about the center
  — This minimizes warping
- For best impedance control, have:
  — No more than two signal layers between every power/ground plane pair
  — No more than one embedded micro-strip layer under the top/bottom layers
- For best noise control, route adjacent layers orthogonally. Avoid layer-to-layer parallelism.
- Fabrication house must agree on design rules, including:
  — Trace width, trace separation
  — Drill/via sizes
- The distance between the signal layer and ground (or power) should be minimized to reduce the loop area enclosed by the return current
  — Use 0.7:1 ratio as a minimum.
  For example: 5-mil traces, 7-mil prepreg thickness to adjacent power/ground

An example for a six-layer and eight-layer board is shown below. For stripline (signals between planes), the stackup should be such that the signal line is closer to one of the planes by a factor of five or more. Then the trace impedance is controlled predominantly by the distance to the nearest plane. Figure 22 and Figure 23 illustrate the proposed stackup for the six- and eight-layer boards.

Figure 22. 8-Layer Stackup

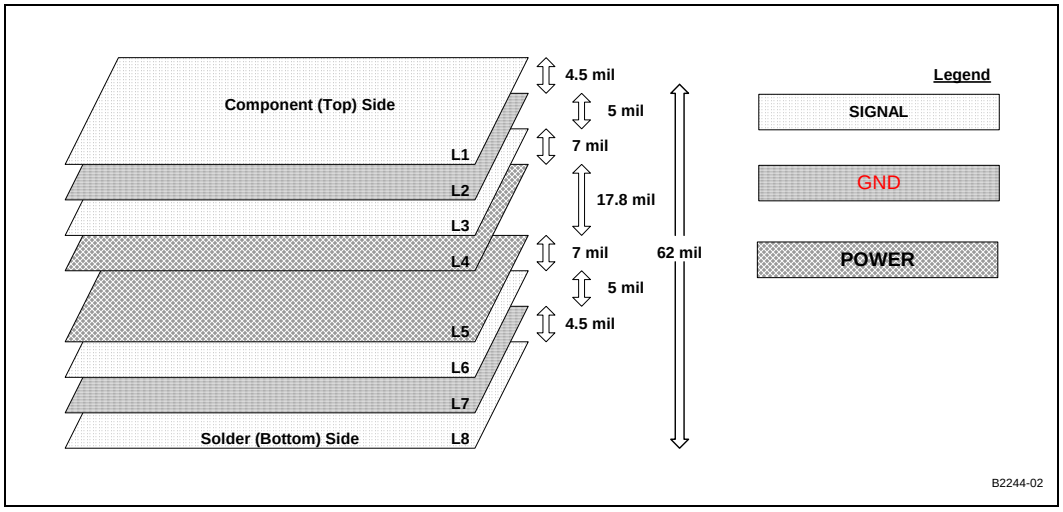
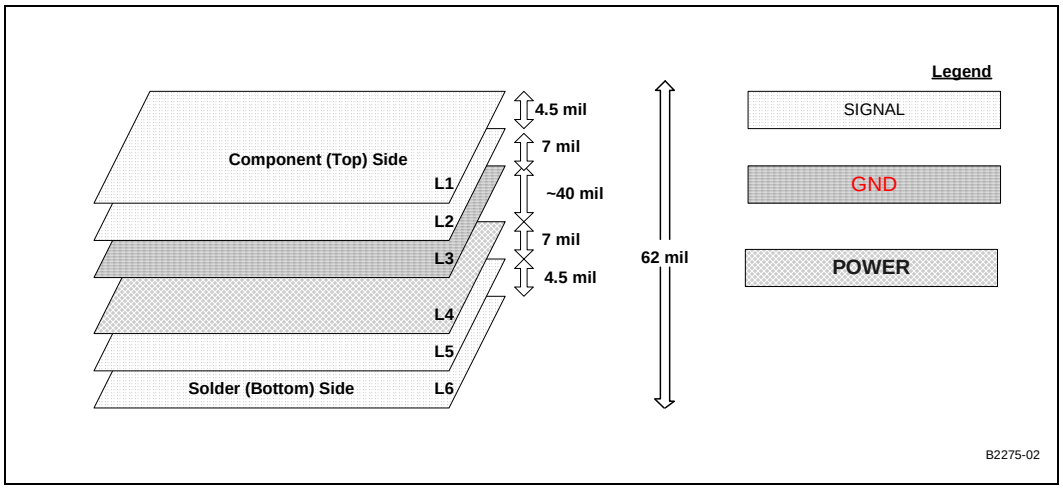


Figure 23. 6-Layer Stackup



- Fast and slow transmission line networks have to be considered
- PCB-board velocities
- Board FR4 ~ 4.3
- Target impedance of 50 Ω ± 10%
- Trace width: 5 mils
- Signal Layers (1/2 oz. Cu)
- Power Layer (1 oz. Cu)
- Ground (GND) Layer (1 oz. Cu)

§ §

6.0 General Layout and Routing Guide

6.1 Overview

This chapter provides routing and layout guides for the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor-based hardware and systems design.

The high-speed clocking required when designing with the processors requires special attention to signal integrity. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. The information in this chapter provides guidelines to aid designers with board layout. In cases where it is too difficult to follow a design rule, engineering judgment must be used.

Several factors influence the signal integrity of an processors design. These factors include:

- Power distribution
- Minimizing crosstalk
- 133-MHz SDRAM memory
- Decoupling
- Layout considerations when connecting the processors to the PCI bus

6.2 General Layout Guidelines

The layout guidelines recommended in this section are based on the experience and knowledge gained from the previous projects. The type and number of layers for the PCB need to be chosen to balance many requirements. That includes the following requirements as well:

- Providing enough routing channels to support minimum and maximum timing requirements of the IXP42X product line and IXC1100 control plane processors and other components
- Most major critical and important components, connectors, and mounting holes must be placed based on product design guidelines and handled with care
- Providing uniform impedance for the processors SDRAM-memory bus and other signals
- Components of same type should be aligned in the same orientation
- Minimizing coupling and crosstalk between networks
- Minimizing RF/EMI and EMC emissions
- Providing stable voltage distribution for each of components
- Decoupling capacitors must be placed next to power pins
- Series termination resistors must be placed close to source
- Silk screen (reference designator) for all parts on both sides: top and bottom
- The trace is X mils wide, with Y mils space between adjacent. It is pitch/width is greater than 3 (>3)
- Traces/connections of mixed and analog devices must be physically isolated from other components on the board. Component spacing between line-side components and chassis ground must be adequately provided. No internal ground, power planes and signal traces are allowed to cross isolation zone. Use appropriate-size PCB traces for line-side traces and should be larger enough to handle peak current. Keep away from high-speed digital signals.

6.2.1 General Component Spacing

- Maintain a minimum of component pad spacing of 100 mils for auto-insertion equipment for mixed assemblies.
- Do not place any components within 125 mils of the printed circuit board edge. This is required to bed-of-nails test fixture.
- The minimum spacing between the via and the solder pad is 25 mils.

Figure 24. Good Design Practice for VIA Hole Placement

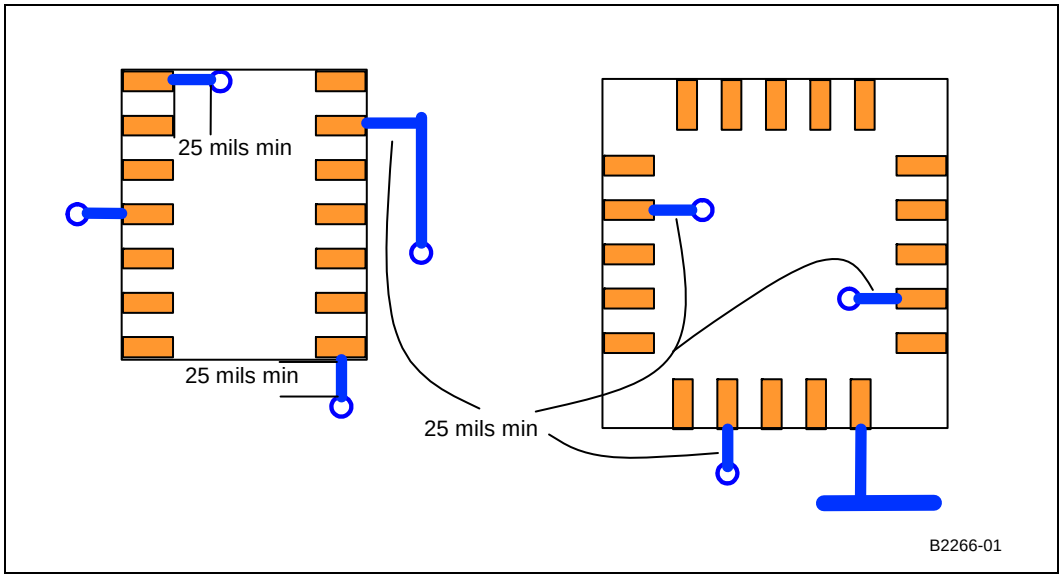


Figure 24 and Figure 25 show good and poor design practices for via placement on surface-mount boards.

Figure 26 shows minimum pad-to-pad clearance for surface-mount passive components and PGA or BGA components.

Figure 25. Poor Design Practice for VIA Placement

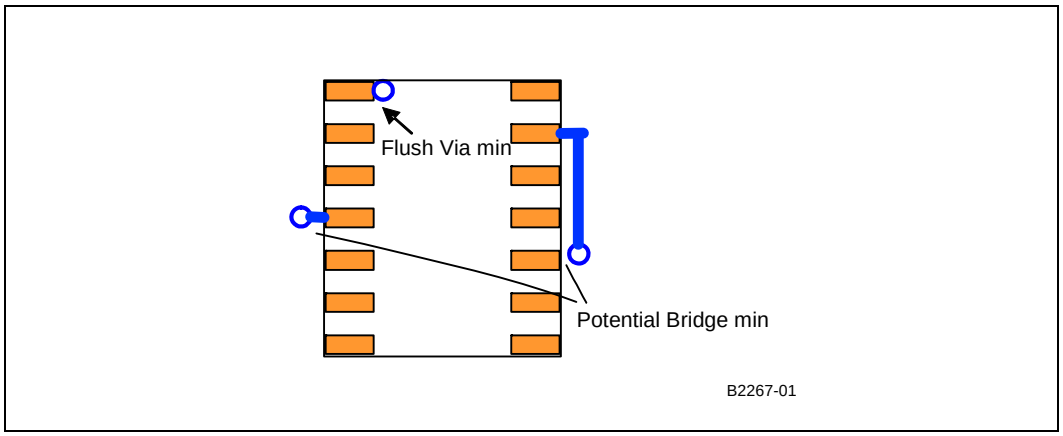
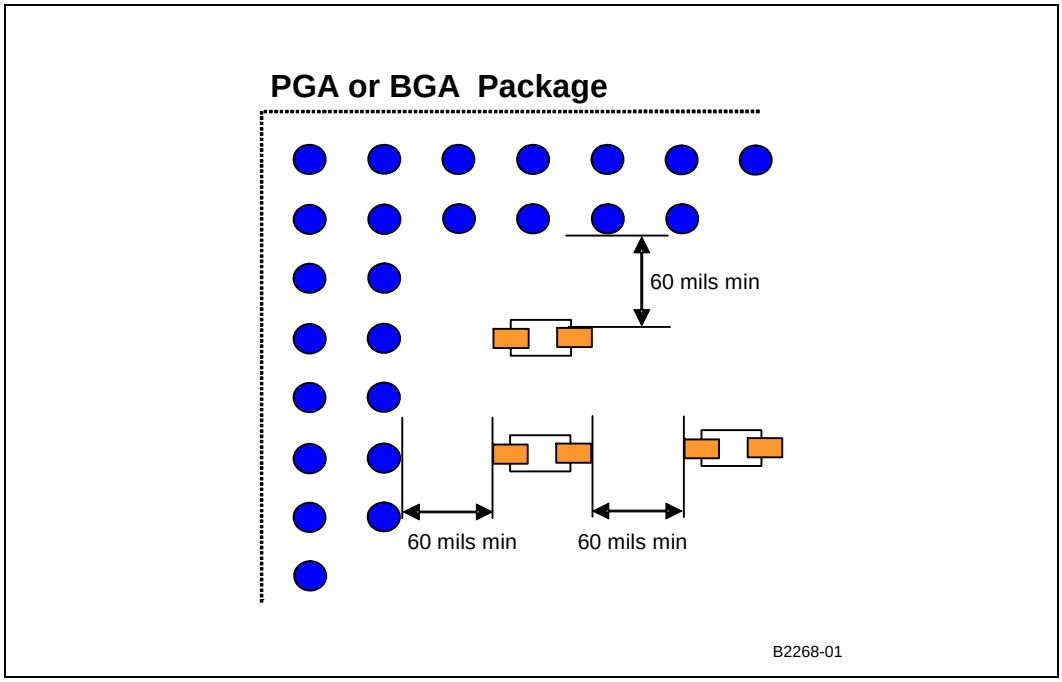


Figure 26. Pad-to-Pad Clearance of Passive Components to a PGA or BGA



6.3 General Routing Guides

This section details general routing guidelines for connecting the IXP42X product line and IXC1100 control plane processors. The specific details on the layout of the PCI, 133-MHz memory interface are discussed in later sections.

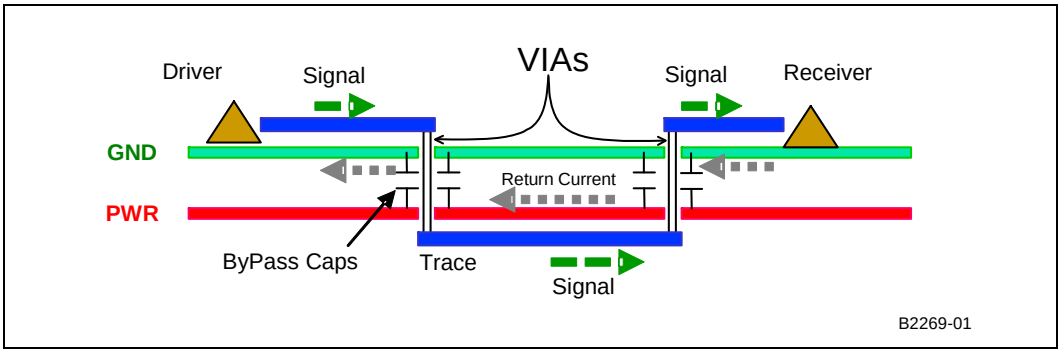
The order in which signals are routed varies from designer to designer. Some designers prefer to route all clock signals first, while others prefer to route all high-speed-bus signals first. Either order can be used, provided the guidelines listed here are followed.

- Route the processor address/data and control signals using a “daisy-chain” topology; this topology assumes that no stubs are used to connect any devices on the net
- Keep stubs as short as possible (preferably, the electrical length of the stub less than half of the length of the rise time of signal)
- All critical signals need to be routed once the power planes are done
- Use proper topology for the specific application
  Stripline traces are covered by a power or ground plane on the top and bottom. Microstrip traces are shielded only on one side. Therefore, EMI from signal traces is lower for stripline.
- Do not route any signals in the ground and power planes.
- Do not route signals close to the edge of the PCB board.
- If a trace is routed along the edge of the plane, the capacitance is reduced and there is an impedance change, causing a discontinuity. Route signal at least 5H away from the edge of the plane where H is the distance of the trace from the plane.
- Don’t route within 100 mils from the edge of the ground plane on the PCB.

- Route similar signal types together to avoid crosstalk with other functions and interfaces.
- Provide a ground return shield connected at both sides of each group to further reduce cross talk.
- Each layer should have a 100-mil-wide ring of copper around the edge of the PCB. This ring should be connected to ground plane to reduce the EMI from the board.
- Provide sufficient return paths for the processor power and ground.
- Minimize number of vias and corners.
- Keep high-speed switching buses and logic away from the clock chip.
- Do not route under crystals, oscillators, clock synthesizers, or magnetic devices (ferrites, toroids).
- Route all high-frequency traces (clocks, etc.) on one layer.
- Minimize ground loops between fast-rise-time circuits and system ground and functional subsections.
- Match length, and width of differential signal traces.
- Keep space between differential signal traces uniform along the length.
- Keep differential signals away from long and parallel high speed paths, such as clock signals and data strobe signals.
- Position input/output circuitry close to input/output connections.
- Avoid placing high-power circuits close to sensitive circuits and avoid long parallel traces between them.
- Do not locate high-frequency oscillators and switching networks close to sensitive analog circuits.
- Arrange the board so that the return currents for high-speed traces never have to jump between planes. Restrict traces to remain on either side of whichever ground plane they start out nearest; this is to allow the use of naturally grouped horizontal and vertical routing layers.

If the signal jumps planes, its reference will change, as shown in Figure 27; therefore, there will be a discontinuity in the path of the signal.

Figure 27. Signal Changing Reference Planes



When the signal jumps from the GND plane to PWR plane, the return current will have to flow to the ground plane through local capacitance, and hence the path for the return currents will be more inductive.

- Provide ground vias next to every signal via explicitly for the purpose of letting return currents jump between layers.
- Select type of grounding: single- or multi-point

  - Use single-point grounding for low-frequency applications (audio, etc.) with clock rates of 1 MHz or lower.
  - Use multi-point grounding for high-frequency circuits with clock rates of 1 MHz or higher.

6.3.1 Clock Signal Considerations

- Provide return paths of board power and ground close to clock traces.
  - Option 1: Route clock over a continuous plane.
  - Option 2: Provide wide Power and Ground traces next to and on upper or lower layer.
- There should be a ground plane adjacent to the layer where the clock traces are routed

  If there is a power plane, instead of a ground plane, make sure that the power plane has adequate decoupling to ground, especially at the clock drivers and receivers.
- Keep clock traces away from the edge of the board.
- Keep clock traces away from I/O area.
- Keep clock traces away from analog signals, including voltage reference signals
- Clock signals should not cross over a split in the plane.
- Route clock signals in stripline-like structures when possible.
- Eliminate all traces and vias under crystals or oscillator circuits unless there is a plane between the trace and the component.
- Do not route parallel signal traces directly above or below clock traces unless there is at least one ground and or power plane separation between those layers.
- Select type of grounding: single-point or multi-point.
- Route clock traces with a minimum number of vias.
  - Do not jump layers with high-speed signals. Doing so disrupts RF coupling between the trace and the plane. Disruption prevents RF current from completing its route uninterrupted from source to load in a continuous manner. If traces must jump layers, use ground vias at each and every layer jump to maintain image plane continuity.
- Space clock traces with other signals three times the trace width on each side.
  - It is not necessary to put ground shield traces around the clock signals except when the clock trace is close to the edge of the board. in that case 3x trace width distance should also be kept to ground shield to avoid lowering the impedance of the clock trace. Crosstalk may be eliminated or reduced by guard traces or 3x spacing. This fence should be stitched to ground through vias at varying distances not to exceed 0.5 inches.
  - Place guard traces around each and every clock trace if the board is single- or double-sided (no ground plane) with minimal distance between signal and the guard trace or otherwise follow the 3x rule; this minimizes crosstalk and provides a return path for the RF current.
  - Do not route two different signals between the same guard traces, since crosstalk may develop. If the traces are differential, then only these two traces may be routed with the same guard trace.
- If possible, route all clock signals in a radial manner.
  - Do not daisy-chain. Provide a series resistor for each radial trace.
  - Do not use stubs or “T” connections on clock signals unless electrically short.

  - — Keep impedances of clock traces balanced and short to minimize reflections and functionality degradation. The wider the trace, the lower the impedance presented to the circuit.
- Maintain impedance control for all clock traces. Calculate the impedance for both microstrip and stripline.
  - — Be aware of the propagation delay of signal traces for both microstrip and stripline.
  - — Calculate capacitive loading of all components and properly compensate with a series resistor and/or an end termination.
- Measure the actual routed trace lengths of all clocks and determine if the actual routed length is longer than maximum allowable calculated length. If so, termination is required.
  - — With the current circuit speeds, all clock signals require termination. If traces must be electrically long, route the traces using transmission line theory. terminate all clock traces in their characteristic impedance.
- Route clock traces on one routing layer only, adjacent to a solid plane. If possible, route all clock traces on stripline.
  - — Microstrip allows for fastest transition of signal edges while permitting greater amount of RF currents to be radiated from the trace. Stripline allows for optimal suppression of RF currents, but at the expense of slowing down signal edges (picoseconds) due to capacitive loading between the trace and surrounding planes. Routing in internal layers reduces EMI by about 20 dB.

6.3.2 LAN Signal Considerations

- Keep the two traces in a differential pair close to each other. Ideally, traces should be within 30 mils (edge-to-edge). Except within 0.5 inches of entering an integrated circuit or a magnetics, or connector solder pads, the distance between the two traces should be kept uniform. It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. Keeping them close means lower emissions (for FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.008 inch to 0.012 inch trace-to-trace spacing is recommended.
- Wherever possible, use a perfect symmetry within a differential pair; use equal lengths/distances to any vias or common components.
- Wherever possible, minimize discontinuities. Discontinuities are caused by solder pads, test points, vias, changes in trace-to-trace spacing, and changes in trace width.
- Avoid routing other signals close by and/or parallel to differential pairs. No signal should be closer to a differential pair than 0.100 inches.
- Avoid routing high-speed LAN or telephone-line traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.
- If there is a ground-fill or power-fill within 30 mils of one side of a differential pair, then there must be a very similar fill the same distance away on the other side of the differential pair.
- For LAN designs, the length of the differential traces between the transformer's solder pads to the PHY's transmit and receive solder pads should preferably be less than three inches, and never more than four inches.

- For LAN designs, the length of the differential traces between the RJ connector solder pads to transformer's transmit and receive solder pads should preferably be less than three inches, and never more than four inches.
- LAN differential traces must be impedance matched to the wire on the connector side of the transformer and the terminating resistance on the other side of the transformer. For Ethernet, the wire side impedance is approximately 100 Ω. The differential impedance on the transformer side of the magnetics should be between 95 – 115 Ω. The calculated impedance of the trace should be about 100 Ω.
- Capacitors for LAN:
  - One capacitor of at least 4.7 µF, within 0.2 inches of each side of the LAN ICs; these capacitors may be placed on the back of the printed circuit board.
  - One capacitor of 820 pF to 0.120 µF within 0.2 inches of each side of the LAN ICs. Placing these capacitors on the back is also acceptable.
  - Termination resistance tolerance must be 1% or better (as 5% or greater will cause excessive output amplitude deviation from IEEE spec limits).
  - Capacitors connected between TDP and TDN traces should not exceed 22 pF for 100Base-TX and faster data rate (keep around 12 pF).

6.3.3 USB Considerations

In order to meet the voltage drop and EMI requirements in the *Universal Serial Bus Specification*, Revision 1.1 the following guidelines must be considered:

- Use separate ground and power planes if possible.
- The impedance is 90 Ωs between the differential pair USB_DPOS and USB_DNEG to match the 90 Ω twisted pair cable impedance. Note that the twisted pair characteristics impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as "critical signals" (for example, hand routing is preferred). The USB_DPOS/USB_DNEG signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the USB_DPOS/USB_DNEG signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two USB_DPOS/USB_DNEG signal traces. The USB_DPOS/USB_DNEG signal traces must also be the same length. This will minimize the effect of common mode current on EMI.
- Route the signals close to each other as parallel traces on the PCB
- Match the trace length as closely as possible (within +/- 0.5 inches)
- Before entry to the connector, use ferrite beads on the USB_DPOS and USB_DNEG lines. Use high value ferrite beads (100 MHz/60 Ω – 100 MHz/240 Ω)
- Ferrite beads at the Vcc and GND connections of the connector are also strongly recommended to isolate noise from the power supplies.

6.3.4 Crosstalk

Crosstalk is caused by capacitance and inductance coupling between signals. Crosstalk is composed of both backward and forward cross-talk components. Backward crosstalk creates an induced signal on the network that propagates in the opposite direction of the aggressor signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor signal.

Circuit board analysis software should be used to analyze your board layout for crosstalk problems.

- To effectively route signals on the PCB, signals are grouped (address, data, etc.). The space between groups can be 3 w (where w is the width of the traces). Space within a group can be just 1 w. Space between clock signals or clock to any other signal should be 3 w. The coupled noise between adjacent traces decreases by the square of the distance between the adjacent traces.
- It is also recommended to specify the height of above the reference plane when laying out traces and provide this parameter to the PCB manufacturer. By moving traces closer to the nearest reference plane the coupled noise decreases by the square of the distance to the reference plane.

6.3.5 EMI Design Considerations

It is strongly recommended that good electromagnetic interference (EMI) design practices be followed when designing with the IXP42X product line and IXC1100 control plane processors.

- Information on spread-spectrum clocking is available in *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor: Spread-Spectrum Clocking to Reduce EMI Application Note.*
- To minimize EMI on your PCB, do not extend the power planes to the edge of the board.
- Another technique is to surround the perimeter of your PCB layers with a GND trace. This helps to shield the PCB with grounds, minimizing radiation.
- Keep crystal and oscillators away from the processor I/O ports and SDRAM bus and board edges. EMI from these devices can be coupled onto the I/O ports and SDRAM bus.
- Connect the crystal retaining straps to the ground plane. These straps, if ungrounded, can behave as antennae and radiate.
- Place high-current devices as closely as possible to the power sources.
- Locate grounds to minimize the loop area between a signal path and its return path.
- Provide a ground pad of equal or larger footprint under crystals and oscillators on the component side of the board. This ground pad should be tied to the ground plane(s) with multiple vias.
- Proper termination of signals can reduce the reflections. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.
- Ferrite beads may be used to add high frequency loss to a circuit without introducing power loss at DC and low frequencies. They are effective when used to dampen high-frequency oscillations from switching transients or parasitic resonances within a circuit.
- Keep rise and fall times as slow as possible. Signals with fast rise and fall times contain many high-frequency harmonics which may radiate significantly.
- A solid ground is essential at the I/O connector to chassis and ground plane.
- Route all traces over a continuous ground plane, with no interruptions. If there are vacant areas on a ground or power plane, do not allow signal conductors to cross the vacant area. This increases inductance and radiation levels.
- Connect all the SDRAM signals and sensitive signal returns closest to the chassis ground.
- Keep the power plane shorter than the ground plane by at least 5x the spacing between the power and ground planes.

- Carefully match the type and value of capacitor to the range of frequencies it must bypass (i.e., tantalum capacitors are more effective at higher frequencies than aluminum electrolytic capacitors, and capacitors of different values are effective at different frequencies).
- Place all components associated with one clock trace closely together. This reduces the trace length and reduces radiation.

6.3.6 Trace Impedance

All signal layers require controlled impedance of 50 Ω ±10 % microstrip or stripline where appropriate unless otherwise specified. Selecting the appropriate board stack-up to minimize impedance variations is very important. When calculating flight times, it is important to consider the minimum and maximum trace impedance based on the switching neighboring traces. Wider spaces between traces may be used since this can minimize trace-to-trace coupling, and reduce cross talk.

All recommendations, described in this document assume a 5-mil 50 Ω ± 10% signal trace unless otherwise specified. When a different stack up is used the trace widths must be adjusted appropriately. When wider traces are used, the trace spacing must be adjusted accordingly (linearly). It is highly recommended that a 2D Field Solver be used to design the high-speed traces.

6.3.7 Power and Decoupling

The power planes should have ample decoupling to ground to minimize the effects of the switching currents. The decoupling should consist of three types: the bulk, the high-frequency ceramic, and the inter-plane capacitors.

- Bulk capacitance consist of electrolytic or tantalum capacitors. These capacitors supply large reservoirs of charge, but are only useful at lower frequencies due to lead inductance effects. The bulk capacitors can be located anywhere on the board.
- For fast switching currents, high-frequency low-inductance capacitors are most effective. These capacitors should be placed as close to the device being decoupled as possible. This minimizes the parasitic resistance and inductance associated with board traces and vias.
- Use an inter-plane capacitor between power and ground planes to reduce the effective plane impedance at high frequencies. The general guideline for placing capacitors is to place high-frequency ceramic capacitors as close as possible to the module.
- Uniformly distributed and connected across the power planes on the PCB.
- Provide Power (Vcc) Island and Vss, and Vccp and Vss on the package and PCB. Use symmetry for I/O pads and Vccp/Vss return.
- Insert additional pairs of Vccp, Vssp for longer (corner) traces in the package.
- Place Vccp/Vss pins and I/Os on the outer rows of the package to avoid crossing the split in Vcc planes.
- Place Vcc/Vss pads in pairs and place processor Vcc/Vss near the center of the package.
- Separately route Vcc internal to package and on the die and use symmetry for processor Vcc/Vss pads and pins.
- It is recommended that with the requirements for 1.3 V and 3.3 V supplies for the IXP42X product line and IXC1100 control plane processors, it is not necessary to add completely new power supply layers to the circuit board to facilitate this. It is possible to create supply ‘islands’ underneath the processor in the existing power supply plane.

Other important considerations are:

- The “island” must be large enough to include the required power supply decoupling capacitance, and the necessary connection to the voltage source.
- Minimize signal degradation, the gap between the supply island and the voltage plane should be kept to a minimum: typical gap size is about 0.02 inches.
- Minimize the number of traces routed across the power plane gap, since each crossing introduces signal degradation due to the impedance discontinuity that occurs at the gap. For traces that must cross the gap, route them on the side of the board next to the ground plane to reduce or eliminate the signal degradation caused by crossing the gap. When this is not possible, then route the trace to cross the gap at a right angle (90°).

6.4 Devices’ Decoupling

The purpose of bypass capacitors is to provide a regulated power and ground to the circuits for the short time needed until the regular power supply can provide the necessary current, when the circuits are switching and therefore they need quick additional currents. The transient currents needed flow to and from the capacitors.

The IXP42X product line and IXC1100 control plane processors has two supply voltages: VCC (processor voltage) and VCCP (I/O voltage).

Simulation is recommended to determine if using capacitors smaller than 0.1-µF capacitors yield better impedance at higher frequencies in your application.

6.4.1 General Decoupling/Bypass Guidelines

Analysis of the complete decoupling circuit may be quite complex. The following implementation — based on experience — is highly recommended:

Bulk bypassing:

- In general, tantalum capacitors are used
  - — Tantalum capacitors may have very low impedance, for example 100 µF, 10v tantalum capacitor may have a resistance of 140 mΩ and inductance of 3 nH.
  - — However, the design may need to be guarded by specifying at least 2:1 voltage margin as such capacitors can explode.
  - — In systems where more power variations are designed in, for example local power downs, additional voltage margin may be required

Local bypassing:

- In general, high-quality MLC capacitor may be used
  - — Such capacitors also have low impedance, for example, a 0.1-µF, 50-V capacitor may have resistance of 50 mΩ and inductance of 0.8 nH.
- Bypassing every Vcc pin is not necessarily required.
  - — Place one small capacitor per each fast IC (integrated circuit)
  - — Place one small capacitor for every two slow ICs.
  - — Place one small capacitor for every four power pins on BGA components
  - — Place one 1000-pF capacitor for each power pin on clock buffers and clock synthesizer components.
- Use the right value capacitor
  - — Use 10-pF ceramic SMT capacitors for decoupling clock signals for EMI control.

  - — Use 470-pF or 1,000-pF SMT ceramic capacitors for decoupling all connector pins for EMI control.
  - — Use 0.1-µF SMT ceramic capacitors for general IC decoupling and ESD protection. X7R or X7S dielectric is preferred for ceramic capacitors due to their superior temperature and aging characteristics. Use Z5U or Y5V dielectric only if a large capacitance is required in a small package.
  - — If two different values of small capacitors are needed, separate the values by at least two order of magnitude; like, 0.001 µF and 0.1 µF, or 0.01 µF and 1.0 µF, or 100 µF and 0.01 µF
  - — Bulk capacitors should be at least 10 times the value of the largest decoupling capacitors.
  - — Use 22-µF or 47-µF electrolytic SMT capacitors for general bulk decoupling
  - — Use 100-µF tantalum SMT capacitors for voltages with large current steps, like 3.3-V supplies.
- Capacitors should be as physically close to the chip as possible. Keep the total trace length less than 0.3 in. It is better to have short trace to a ground or power via than a longer trace going to a ground or power pin since the inductance of the planes is relatively lower. Trace inductance (~8 nH per in) is a large part of the total effective capacitor inductance.
- Use only SMT capacitors where possible. A capacitor size of 0805 achieves the minimum inductance and is therefore preferred. Use 1206 capacitors only for very large values (> 1 µF). Avoid 0603 capacitors since they show higher failure rates.
- For capacitors on signal traces; connect capacitors directly to pin, not splitting the signal trace.

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7.0 Critical Routing Topologies

This chapter contains information for recommended trace lengths, size, and routing guidelines for the PC133 SDRAM and PCI bus.

7.1 PC133 SDRAM Topologies

The Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor SDRAM Memory Bus is designed to four loads and allows two banks of PC 133 of SDRAM memory. Figure 28 illustrates the topologies of two banks of PC 133 SDRAM interfaced to the processors memory bus.

Note: The figures in this section do not include any termination resistors that may be needed. For best signal integrity results, the designer may perform simulations.

Figure 28. SDRAM Topology

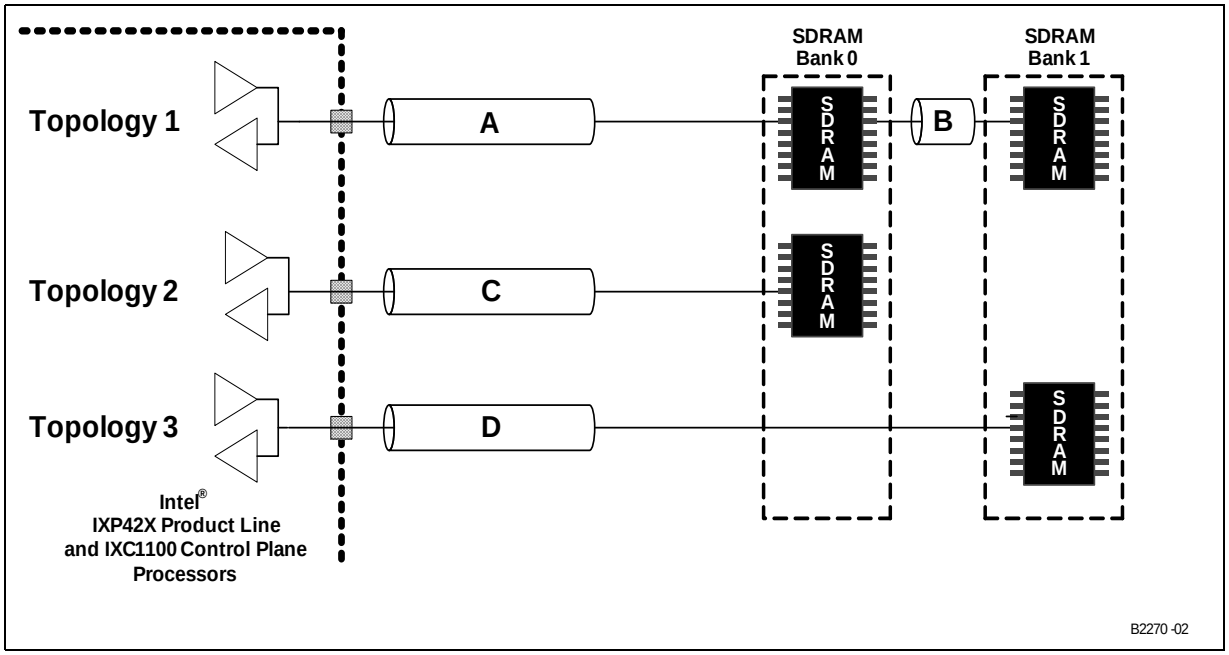

Table 16. SDRAM Address/Data/Control Routing Guidelines

SIGNAL	Trace (Mils)			Trace Lengths (Inches)							
				A		B		C		D	
	Top.	Width	Spacing	Min	Max	Min	Max	Min	Max	Min	Max
SDM_CS_N0	2	5	10					0.2	3.5		
SDM_CKE	1	10	10	0.2	3.5	0.2	1.0				
SDM_DATA[31:0]	1	5	10	0.2	3.5	0.2	1.0				
SDM_DQM[3:0]	1	10	10	0.2	3.5	0.2	1.0				
SDM_CAS_N SDM_RAS_N SDM_WE_N	1	5	10	0.2	3.5	0.2	1.0				
SDM_CS_N1	3	5	10							3.7	1.0
SDM_ADDR[12:0]	1	5	10	0.2	3.5	0.2	1.0				

Note: Since all designs are unique, consult your SDRAM component vendor for routing and layout recommendations.

- Look carefully at signal line lengths and try to match them as closely as possible.
- Pay particular attention to data bus layout.
- Hand-route critical path signals if possible.
- Dedicate power and ground planes with bypass caps placed as close as possible to the SDRAMs.
- One via for each power and ground pin per device is highly recommended
- 25-mil traces for power and ground pins is highly recommended and should not be less than 10 mil

To ensure the signal quality and functionality of the SDRAM bus, it is strongly recommended that signal integrity simulations must be performed.

7.1.1 PC 133 SDRAM Clock

These are the general clock guidelines:

- Clock signals must have 1-4 SDRAM loads with 3.3-pF cap load
- PCB Impedance: 50 Ω ± 10%

Figure 29 shows the PC 133 SDRAM clock topology.

Figure 29. SDRAM Clock Topology

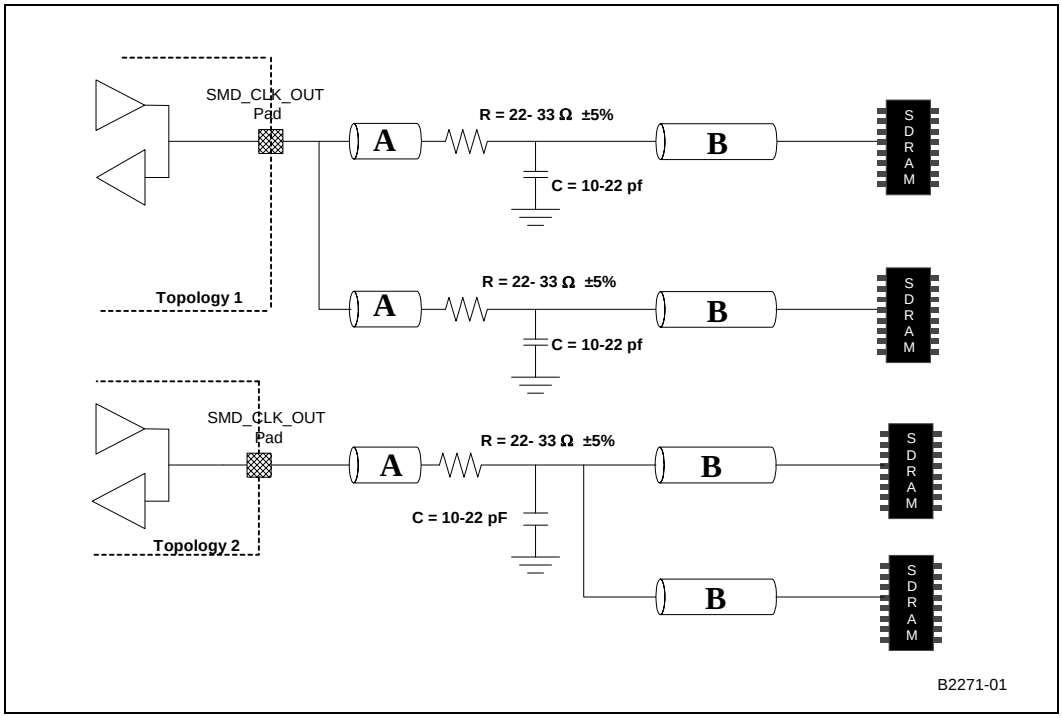

Table 17. SDRAM Clock Routing Guidelines

Signal	Trace (Mils)			Trace Lengths (Inches)			
				A		B	
	Topology .	Width	Spacing	Min	Max	Min	Max
SDM_CLK	1	5	15	0.2	0.5	0.1	4.0
SDM_CLK	2	5	15	0.2	0.5	0.1	2.0

- Clocks must be routed with as much of the trace on inner signal layer as possible.
- Clocks on the inner layer have a 5-mil ground trace surrounding them with vias stitched to ground at 0.5” intervals.
- Clock traces must be 5 mil wide with 15 mil spacing to any other signals.
- All the SDM_CLK trace should be equal in length, and Topology 1 is also recommended for two banks of SDRAM implementation.

7.2 PCI Topologies

The IXP42X product line and IXC1100 control plane processors’ PCI controller is designed and provides a PCI-bus interface that is compliant with the *PCI Local Bus Specification*, Rev. 2.2. For more information on the PCI Bus interface, see the *PCI Local Bus Specification*, Rev. 2.2.

Figure 30. PCI Address/Data Topology

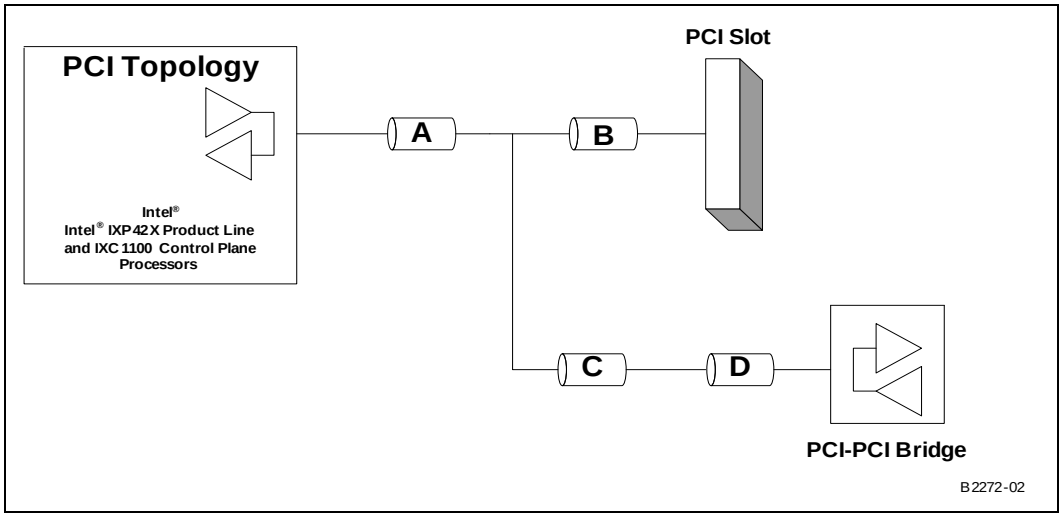

Table 18. PCI Address/Data Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Address/Data
Topology	Daisy Chain
Reference Plane Ground	Ground
Characteristic Trace Impedance	50 Ω ±10%
Nominal Trace Width	4 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace length A	Max 2,500 mils
Trace length B	Max 200 mils
Trace length C	Max 1,800 mils
Trace length D	Max 200 mils
Maximum VIAS Count per Signal	12

Figure 31. PCI Address/Data Topology (PCI Bridge to cPCI Bridge Connector)

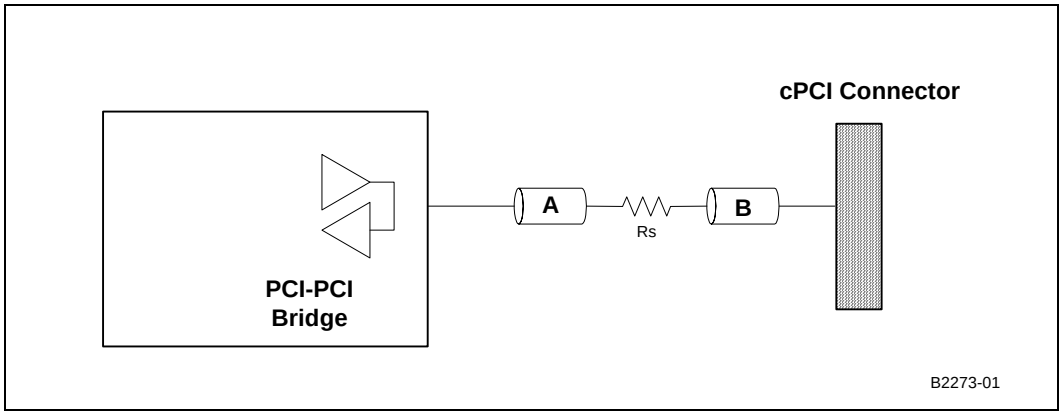

Table 19. PCI Address/Data Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Address/Data
Topology	Daisy Chain
Reference Plane Ground	Ground
Characteristic Trace Impedance	50 Ω ±10%
Nominal Trace Width	4 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace length A	Max 2,500 mils
Trace length B	Max 200 mils
Resistor Rs	30 Ω ±10%
Maximum VIAS	8

Figure 32. PCI Clock Topology

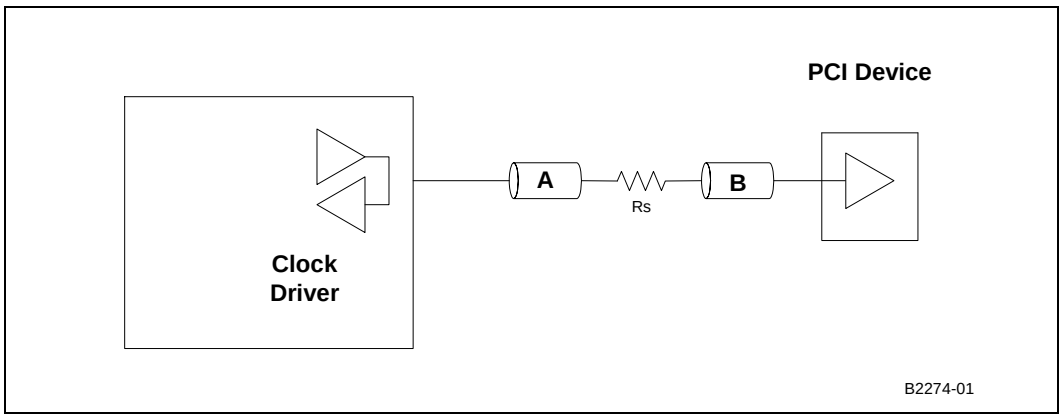

Table 20. PCI Clock Routing Guidelines

Parameter	Routing Guidelines
Signal Group	PCI Clock
Topology	Point to-Point
Reference Plane Ground	Ground
Characteristic Trace Impedance	50 Ω ±10%
Nominal Trace Width	4 mils
Nominal Trace Separation	9 mils
Spacing to Other Groups	20 mils
Trace length A	Max 200 mils
Trace length B	Max 11,000 mils
Resistor Rs	30 Ω ±10%
Maximum VIAS	6

7.2.1 Trace Length Limits

For acceptable signal integrity with the PCI bus speeds up to 66 MHz, it is very important to PCB design layout to have controller impedance:

- Avoid routing signals >8 inches
- The maximum trace lengths for each 32-bit interface signal from IXP42X product line and IXC1100 control plane processors to PCI Bus is limited to 1.5 inches for all 32-bit cards
- Trace lengths for the PCI clock signal from processors to PCI connector must be 2.5 inches ± 0.1 inches and must be routed to only one load.

For add-in cards, trace lengths from the top of the card edge connector to the processors are:

- The maximum trace length for all 32-bit interface signals should not exceed 1.5 inches for 32-bit cards. This includes all signals except those listed as “Signal Pins,” “Interrupt Pins,” and “JTAG Pins,” as per *PCI Local Bus Specification*, Rev. 2.2.
- The trace length for the PCI_CLK signal is 2.5 inches ± 0.1 inch for 32-bit cards and should be routed to only a single load.

7.2.2 Routing Guidelines

The recommended routing solution is to arrange the signal level layouts so that no high-speed data bus (33 MHz) is referenced to the 3.3-V plane and 5-V plane.

Signal traces should either remain entirely over the 3.3-V or 5-V plane. Signals that must cross from one domain to the other should be routed on the opposite side of the board so that they are referenced to the ground plane, which is not split. If this is not possible, signals must be routed over the plane split — the two planes capacitatively tied together. The 5-V and 3.3-V planes should be tied together with 0.01-µF, high-speed capacitors for each of the four signals crossing the split. The capacitor should be placed not more that 0.25 inches from the point the signals cross the split.

7.2.3 Signal Loading

Shared PCI signals must be limited to one load on each of the PCI slots. Any violation of expansion board or add-on device trace length or loading limits compromises system-signal integrity.

The *PCI Local Bus Specification*, Rev. 2.2 allows a maximum PCI clock skew of 2 ns between any two devices connected on the PCI bus. (The allowable clock skew for 66 MHz is 1 ns.)

To minimize skew on the primary PCI bus, place the IXP42X product line and IXC1100 control plane processors as close as possible to the PCI edge connector. Trace length from the PCI edge connector to the processors' PCI_CLK input must be as short as physically possible — the maximum length being 2.5 inches.

For the secondary PCI bus, the allowable skew is 2 ns between any device on the secondary PCI bus. (The allowable clock skew for 66 MHz is 1 ns.) Keep these secondary clock routes between 1.0 to 8.0 inches to provide a skew of less than 1 ns.

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Appendix A Design Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a system board that implements an Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor. A check box labeled "complete?" is provided to the user to mark completion while they go through the checklist.

This is not a complete list and does not guarantee that a design will function properly. For more detailed information, see the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet*, *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*, and the following chapters of this document.

The *Intel® IXP4XX Product Line of Network Processors Specification Update* should be reviewed to ensure that specification and documentation updates have been incorporated into the design properly.

A.1 Checklist

The following set of tables provide design considerations for the various interfaces of a design. Each table describes one of those portions and is titled accordingly. Contact your Intel field representative in the event of questions or issues regarding the interpretation of the information in these tables.

Listed in the signal definition tables — starting at Table 22, "SDRAM Interface" on page 82 — are pull-up an pull-down resistor recommendations that are required when the particular *enabled* interface is not being used in the application. These external resistor requirements are only needed if the particular model of IXP42X product line or IXC1100 control plane processor has the particular interface *enabled* and the interface is not required in the application. Unless noted otherwise, all recommendations for signals that should be pulled high imply pulling them high to Vccp (3.3 V).

Warning: All IXP42X product line and IXC1100 control plane processors' I/O pins are *not* 5-V tolerant.

Table 21 presents the legend for interpreting the **Type** field in the other tables in this document.

Table 21. Signal Type Definitions

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open Drain pin
PWR	Power pin
GND	Ground pin
N/C	No Connect

A.2 SDRAM Interface

These series resistors should be placed as close as possible to processor. It is recommend that values are tuned based on signal integrity simulations using the processors IBIS model.

Table 22. SDRAM Interface

Name	Type†	Recommendation	Complete?
SDM_ADDR[12:0]	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_DATA[31:0]	I/O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_CLKOUT	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_BA[1:0]	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_RAS_N	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_CAS_N	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_CS_N[1:0]	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_WE_N	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_CKE	O	Series Resistors are recommended. Typical value is 22 Ω.	
SDM_DQM[3:0]	O	Series Resistors are recommended. Typical value is 22 Ω.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

A.3 PCI Interface

Table 23. PCI Interface (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
PCI_AD[31:0]	I/O	Should be pulled high†† with a 10-KΩ resistor when not being utilized in the system.	
PCI_CBE_N[3:0]	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_PAR	I/O	Should be pulled high†† with a 10-KΩ resistor when not being utilized in the system.	
PCI_FRAME_N	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_TRDY_N	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_IRDY_N	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_STOP_N	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_PERR_N	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_SERR_N	I O/D	This signal can function as an input or an open drain output. Should be pulled high with a 10-KΩ resistor.	
PCI_DEVSEL_N	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_IDSEL	I	Should be pulled high†† with a 10-KΩ resistor when not being utilized in the system.	
PCI_REQ_N[3:1]	I	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_REQ_N[0]	I/O	Should be pulled high with a 10-KΩ resistor, when the PCI bus is not being utilized in the system.	
† For a legend of the **Type** codes, see Table 21 on page 81. †† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.			

Table 23. PCI Interface (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
PCI_GNT_N[3:1]	O	No external circuitry needed.	
PCI_GNT_N[0]	I/O	Should be pulled high with a 10-KΩ resistor when not being utilized in the system.	
PCI_INTA_N	O/D	Should be pulled high with a 10-KΩ resistor.	
PCI_CLKIN	I	Should be pulled high†† with a 10-KΩ resistor when not being utilized in the system.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

A.4 High-Speed Serial Interface

The High-Speed Serial interface is disabled on the IXP420 and IXP422 and IXC1100. Pull-ups and pull-downs are not needed on the signals when using one of these processors.

Table 24. High-Speed, Serial Interface 0

Name	Type†	Recommendation	Complete?
HSS_TXFRAME0	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_TXDATA0	O	• Must be pulled high with a 10-KΩ resistor to V_{CCP} in a system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100	
HSS_TXCLK0	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_RXFRAME0	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_RXDATA0	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_RXCLK0	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	

† For a legend of the **Type** codes, see Table 21 on page 81
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

Table 25. High-Speed, Serial Interface 1 (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
HSS_TXFRAME1	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

Table 25. High-Speed, Serial Interface 1 (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
HSS_TXDATA1	O	• Must be pulled high with a 10-KΩ resistor to V_{CCP} in a system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_TXCLK1	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_RXFRAME1	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_RXDATA1	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
HSS_RXCLK1	I/O	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

A.5 MII Interface

The MII-1 interface is disabled on the IXP421. Pull-ups and pull-downs are not needed on the interface when using this processor.

Table 26. MII Interfaces (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
ETH_TXCLK0	I	Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
ETH_TXDATA0[3:0]	O	No extra circuitry required.	
ETH_TXEN0	O	No extra circuitry required.	
ETH_RXCLK0	I	Externally supplied receive clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
ETH_RXDATA0[3:0]	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
ETH_RXDV0	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
ETH_COL0	I	Should be pulled low through a 10-KΩ resistor when not being utilized in the system.	
ETH_CRS0	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

Table 26. MII Interfaces (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
ETH_MDIO	I/O	Must be pulled high through a 1.5-KΩ resistor when being utilized in the system. Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
ETH_MDC	O	No external circuitry needed.	
ETH_TXCLK1	I	Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system. This signal is a N/C on the IXP421,	
ETH_TXDATA1[3:0]	O	No external circuitry needed. This signal is a N/C on the IXP421.	
ETH_TXEN1	O	No external circuitry needed. This signal is a N/C on the IXP421.	
ETH_RXCLK1	I	Externally supplied receive clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system. This signal is a N/C on the IXP421,	
ETH_RXDATA1[3:0]	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system. This signal is a N/C on the IXP421,	
ETH_RXDV1	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
ETH_COL1	I	Should be pulled low through a 10-KΩ resistor when not being utilized in the system. This signal is a N/C on the IXP421.	
ETH_CRS1	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system. This signal is a N/C on the IXP421.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

A.6 UTOPIA-2 Interface

Table 27. UTOPIA-2 Interface (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
UTP_OP_CLK	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_OP_FCO	O	• No external circuitry needed. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_OP_SOC	O	• No external circuitry needed. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

Table 27. UTOPIA-2 Interface (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
UTP_OP_DATA[7:0]	O	• No external circuitry needed. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_OP_ADDR[4:0]	O	• No external circuitry needed. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_OP_FCI	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_IP_CLK	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_IP_FCI	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_IP_SOC	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_IP_DATA[7:0]	I	• Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system using the IXP421 or IXP425. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_IP_ADDR[4:0]	O	• No external circuitry needed. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	
UTP_IP_FCO	O	• No external circuitry needed. • This signal is a N/C on the IXP420, IXP422, and IXC1100.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

A.7 Expansion Bus Interface

Table 28. Expansion Bus Interface (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
EX_CLK	I	Input clock signal used to sample all expansion interface inputs and clock all expansion interface outputs. GPIO15 maybe used as the clock source.	
EX_ALE	O	Used in Intel and Motorola* multiplexed modes of operation. No external circuitry needed.	
EX_ADDR[23:0]	I/O	Expansion-bus address used as an output for data accesses over the expansion bus. Also, used as an input during reset to capture device configuration. Based on the desired configuration, various address signals must be tied low in order for the device to operate in the desired mode. The configurations available are shown in Table 29 on page 87. These signals have a weak internal pull-up resistor to Vccp. A 4.7-KΩ pull-down resistor may used to set a “0.”	
EX_WR_N	O	No external circuitry needed,	
EX_RD_N	O	No external circuitry needed,	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

Table 28. Expansion Bus Interface (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
EX_CS_N[7:0]	O	External chip selects for expansion bus. Chip selects 0 through 7 can be configured to support Intel or Motorola bus cycles. Chip selects 4 through 7 can be configured to support TI* HPI bus cycles.	
EX_DATA[15:0]	I/O	No external circuitry needed,	
EX_IOWAIT_N	I	Should be pulled high through a 10-KΩ resistor when not being utilized in the system.	
EX_RDY[3:0]	I	When configured to operate in HPI mode there is one RDY signal per chip select. This signal only affects accesses that use EX_CS_N[7:4]. Should be pulled high†† though a 10-KΩ resistor when not being utilized in the system.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

A.7.1 Expansion Bus Configuration Strappings

At power up or whenever a reset is asserted, the expansion-bus address outputs are switched to inputs and the states of the bits are captured and stored in Configuration Register 0, bits 23 through 0. This occurs on the first cycle after the synchronous de-assertion of the reset signal.

The Expansion Bus address bit all have internal pull-up resistors. Each bit may be pulled low by placing a pull-down resistor on the address signal.

These configuration bits are made available to the system as outputs from the Expansion Bus Controller block. With the exception of bits 23, 22 and 21, which are read only, all other bits may be written and read from the South AHB.

Table 29. Expansion Bus Configuration Register 0 (Sheet 1 of 2)

Bit	Name	Description
23:21	Intel XScale® Processor Clock Set[2:0]	Allow a slower Intel XScale® Processor clock speed to override device fuse settings. However cannot be used to overclock processor speed. For additional details, see Table 30 on page 88.
20:17		User Configurable
16:6		(Reserved)
5		(Reserved)
4	PCI_CLK	Sets the PCI Controller Speed. • 0 = 33 MHz • 1 = 66 MHz
3		(Reserved) EX_ADDR[3] must not be pulled down during address strapping. This bit must be written to '1' if performing a write to this register.
2	PCI_ARB	Enables the PCI Controller Arbiter. • 0 = PCI arbiter disabled • 1 = PCI arbiter enabled
1	PCI_HOST	Configures the PCI Controller as PCI Bus Host. • 0 = PCI as non-host • 1 = PCI as host

Table 29. Expansion Bus Configuration Register 0 (Sheet 2 of 2)

Bit	Name	Description
0	8/16 FLASH	Specifies the data bus width of the FLASH memory device. • 0 = 16-bit data bus • 1 = 8-bit data bus

Table 30. Setting the Intel XScale® Processor Operation Speed

Intel XScale® Processor Speed (Factory Part Speed)	CFG_EN_N EX_ADDR(23)	CFG1 EX_ADDR(22)	CFG0 EX_ADDR(21)	Actual ProcessorSpeed (MHz)
533 MHz	1	0	0	533 MHz
533 MHz	0	0	0	533 MHz
533 MHz	0	0	1	400 MHz
533 MHz	0	1	1	266 MHz
400 MHz	1	0	0	400 MHz
400 MHz	0	0	0	400 MHz
400 MHz	0	0	1	400 MHz
400 MHz	0	1	1	266 MHz
266 MHz	1	0	0	266 MHz
266 MHz	0	0	0	266 MHz
266 MHz	0	0	1	266 MHz
266 MHz	0	1	1	266 MHz

Note that the Intel XScale processor can operate at slower speeds than the factory programmed speed setting. This is done by placing a value on Expansion bus address bits 23,22,21 at the de-assertion of RESET_IN_N and knowing the speed grade of the part from the factory. Column 1 of Table 30 denotes the speed grade of the part from the factory. Columns 2, 3, and 4 denote the values captured on the Expansion Bus address bits at the de-assertion of reset. Column 5 represents the speed at which the Intel XScale processor speed will now be operating.

A.8 UART Interface

Table 31. UART Interfaces (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
RXDATA0	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
TXDATA0	O	No external circuitry needed.	
CTS0_N	I	Should be pulled high through a 10-KΩ resistor when not being utilized in the system.	
RTS0_N	O	No external circuitry needed.	
RXDATA1	I	Should be pulled high†† through a 10-KΩ resistor when not being utilized in the system.	
TXDATA1	O	No external circuitry needed.	

† For a legend of the **Type** codes, see Table 21 on page 81.
†† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.

Table 31. UART Interfaces (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
CTS1_N	I	Should be pulled high through a 10-KΩ resistor when not being utilized in the system.	
RTS1_N	O	No external circuitry needed.	
† For a legend of the **Type** codes, see Table 21 on page 81. †† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.			

A.9 USB Interface

Table 32. USB Interface

Name	Type†	Recommendation	Complete?
USB_DPOS	I/O	N/C when not being utilized in the system.	
USB_DNEG	I/O	N/C when not being utilized in the system.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

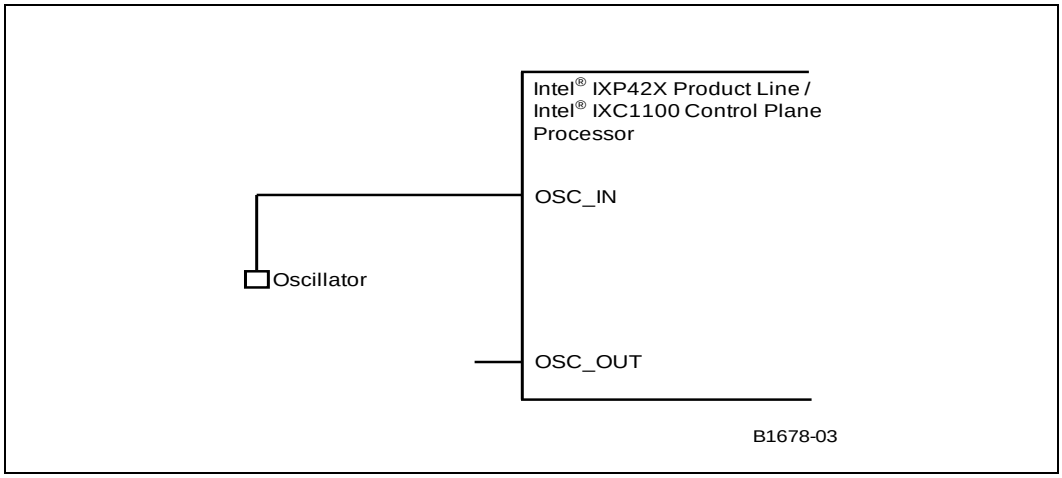
A.10 Oscillator Interface

Table 33. Oscillator Interface

Name	Type†	Recommendation	Complete?
OSC_IN	I	33.33-MHz, sinusoidal input signal. Must be 50 ppm or better to ensure all interfaces meet specification requirements. Can be driven by an oscillator. For Spread Spectrum Clocking information, see Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor*: Spread-Spectrum Clocking to Reduce EMI*	
OSC_OUT	O	33.33-MHz, sinusoidal output signal. Left disconnected when being driven by an oscillator. See Figure 33.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

A.10.1 Oscillator Interface

Figure 33. Typical Connection to an Oscillator



A.11 GPIO Interface

Table 34. GPIO Interface

Name	Type†	Recommendation	Complete?
GPIO[12:0]	I/O	Should be pulled high†† using a 10-KΩ resistor or configured as an output and written a 0 when not being utilized in the system.	
GPIO[13]	I/O	Should be pulled high†† using a 10-KΩ resistor or configured as an output and written a 0 when not being utilized in the system.	
GPIO[14]	I/O	Should be pulled high†† using a 10-KΩ resistor or configured as an output and written a 0 when not being utilized in the system.	
GPIO[15]	I/O	Should be pulled high†† using a 10-KΩ resistor or configured as an output and written a 0 when not being utilized in the system.	
† For a legend of the **Type** codes, see Table 21 on page 81. †† For new designs, this signal should be pulled high with a 10-KΩ resistor when not being utilized in the system. No change is required to existing designs that have this signal pulled low.			

A.12 JTAG Interface

Table 35. JTAG Interface

Name	Type†	Recommendation	Complete?
JTG_TMS	I	Connect appropriately to JTAG interface.	
JTG_TDI	I	Connect appropriately to JTAG interface.	
JTG_TDO	O	Connect appropriately to JTAG interface.	
JTG_TRST_N	I	Connect appropriately to JTAG interface. This JTG_TRST_N signal must be asserted (driven low) during power-up, otherwise the TAP controller may not be initialized properly, and the processor may be locked. Pull low using a 10-KΩ resistor.	
JTG_TCK	I	Connect appropriately to JTAG interface.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

A.13 System Interface

Table 36. System Interface (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
BYPASS_CLK	I	Pin requires a pull-up resistor to Vccp. A 10-KΩ resistor is recommended.	
SCANTESTMODE_N	I	Pin requires a pull-up resistor to Vccp. A 10-KΩ resistor is recommended.	
RESET_IN_N	I	Used as a reset input to the device after power up conditions have been met. Power up conditions include the power supplies reaching a safe stable condition and the PLL achieving a locked state and the PWRON_RESET_N coming to an active state prior to the RESET_IN_N coming to an active state.	
PWRON_RESET_N	I	The PWRON_RESET_N signal is a 1.3-V signal. Do not connect to 3.3 V.	
HIGHZ_N	I	Pin requires a pull-up resistor to Vccp. A 10K-Ω resistor is recommended.	
PLL_LOCK	O	No external logic required.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

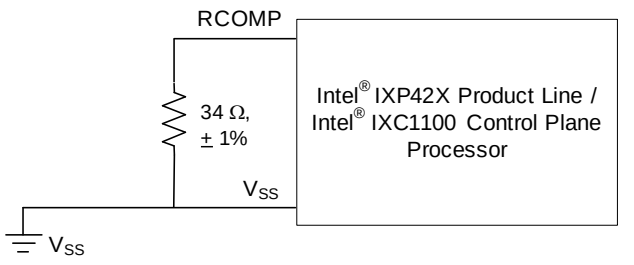
Table 36. System Interface (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
RCOMP	O	Pin requires a 34-Ω +/- 1% tolerance resistor to ground. Refer to Figure 34.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

A.13.1 RCOMP Pin Requirements

Figure 34 shows the requirements for the RCOMP pin.

Figure 34. RCOMP Pin External Resistor Requirements



A.14 Power Interface

Table 37. Power Interface (Sheet 1 of 2)

Name	Type†	Recommendation	Complete?
VCC	I	The 1.3-V power supply input pins used for the internal logic.	
VCCP	I	The 3.3-V power supply input pins used for the peripheral (I/O) logic.	
VSS		Ground power supply input pins used for both the 3.3-V and the 1.3-V power supplies.	
VCCOSCP	I	The 3.3-V power supply input pins used for the peripheral (I/O) logic of the analog oscillator circuitry. Require special power filtering circuitry. Refer to Figure 37 on page 93.	
VSSOSCP	I	Ground input pins used for the peripheral (I/O) logic of the analog oscillator circuitry. Used in conjunction with the VCCOSCP pins. Requires special power filtering circuitry. Refer to Figure 37 on page 93.	
VCCOSC	I	1.3-V power supply input pins used for the internal logic of the analog oscillator circuitry. Requires special power filtering circuitry. Refer to Figure 38 on page 94.	
VSSOSC	I	Ground power supply input pins used for the internal logic of the analog oscillator circuitry. Used in conjunction with the VCCOSC pins. Requires special power filtering circuitry. Refer to Figure 38 on page 94.	
VCCPLL1	I	The 1.3-V power supply input pins used for the internal logic of the analog phase lock-loop circuitry. Requires special power filtering circuitry.Refer to Figure 35 on page 92.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

Table 37. Power Interface (Sheet 2 of 2)

Name	Type†	Recommendation	Complete?
VCCPLL2	I	The 1.3-V power supply input pins used for the internal logic of the analog phase lock-loop circuitry. Requires special power filtering circuitry.Refer to Figure 36 on page 93.	
† For a legend of the **Type** codes, see Table 21 on page 81.			

A.15 V_{CCPLL1}, V_{CCPLL2}, V_{CCOSCP}, V_{CCOSC} Pin Requirements

To reduce voltage-supply noise on the analog sections of the IXP42X product line and IXC1100 control plane processors, the phase-lock loop circuits (V_{CCPLL1}, V_{CCPLL2}) and oscillator circuit (V_{CCOSCP}, V_{CCOSC}) require isolated voltage supplies.

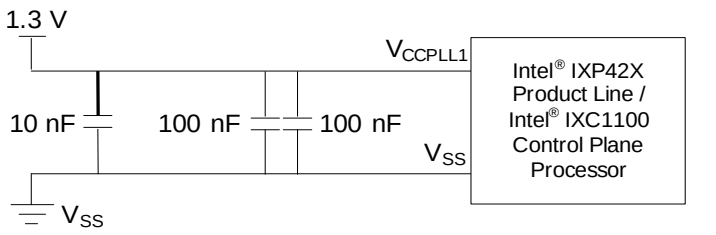
The filter circuits for each supply are shown in the following sections.

A.15.1 V_{CCPLL1} Requirement

A parallel combination of a 10-nF capacitor — for bypass — and a 200-nF capacitor — for a first-order filter with a cut-off frequency below 30 MHz — must be connected to the V_{CCPLL1} pin of the IXP42X product line and IXC1100 control plane processors.

The ground of both capacitors should be connected to the nearest V_{SS} supply pin. Both capacitors should be located less than 0.5 inch away from the V_{CCPLL1} pin and the associated V_{SS} pin. In order to achieve the 200-nF capacitance, a parallel combination of two 100-nF capacitors may be used as long as the capacitors are placed directly beside each other.

Figure 35. V_{CCPLL1} Power Filtering Diagram

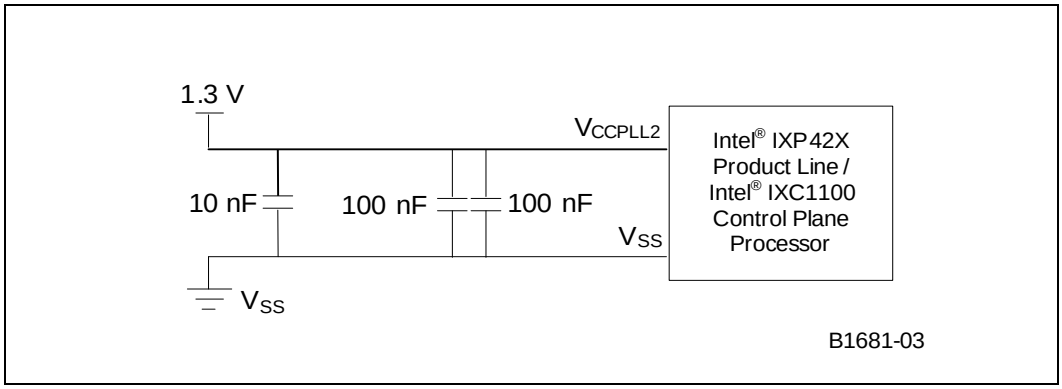


A.15.2 V_{CCPLL2} Requirement

A parallel combination of a 10-nF capacitor — for bypass — and a 200-nF capacitor — for a first-order filter with a cut-off frequency below 30 MHz — must be connected to the V_{CCPLL2} pin of the IXP42X product line and IXC1100 control plane processors.

The ground of both capacitors should be connected to the nearest V_{SS} supply pin. Both capacitors should be located less than 0.5 inch away from the V_{CCPLL2} pin and the associated V_{SS} pin. In order to achieve the 200-nF capacitance, a parallel combination of two 100-nF capacitors may be used as long as the capacitors are placed directly beside each other.

Figure 36. V_{CCPLL2} Power Filtering Diagram



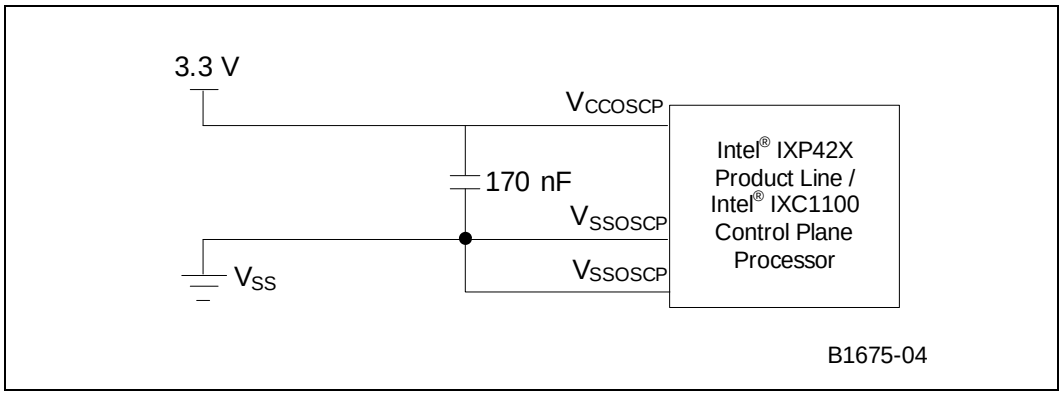
A.15.3 V_{CCOSCP} Requirement

A single 170-nF capacitor must be connected between the V_{CCP_OSC} pin and V_{SSP_OSC} pin of the IXP42X product line and IXC1100 control plane processors. This capacitor value provides both bypass and filtering.

When 170 nF is an inconvenient size, capacitor values between 150 nF to 200 nF could be used with little adverse effects, assuming that the effective series resistance of the 200-nF capacitor is under 50 mΩ.

In order to achieve a 200-nF capacitance, a parallel combination of two 100-nF capacitors may be used as long as the capacitors are placed directly beside each other. V_{SSP_OSC} consists of two pins, AD10 and AF10. Ensure that both pins are connected as shown in Figure 37.

Figure 37. V_{CCOSCP} Power Filtering Diagram



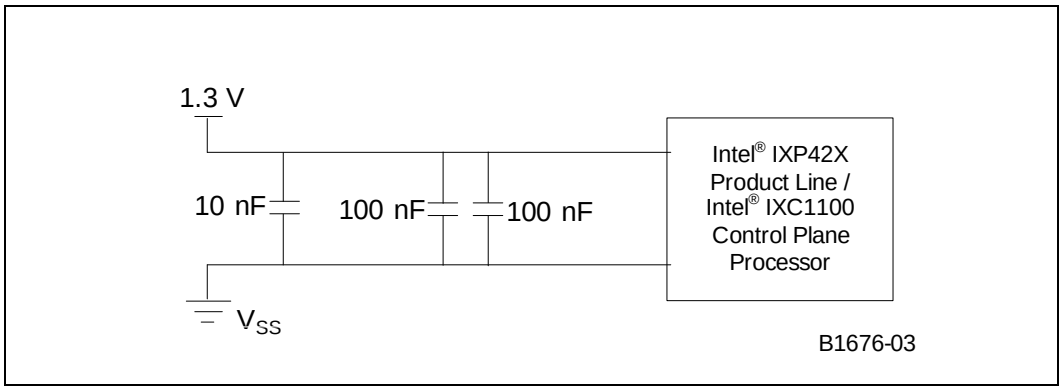
A.15.4 V_{CCOSC} Requirement

A parallel combination of a 10-nF capacitor — for bypass — and a 200-nF capacitor — for a first-order filter with a cut-off frequency below 33 MHz — must be connected to both of the V_{CCOSC} pins of the IXP42X product line and IXC1100 control plane processors.

The grounds of both capacitors should be connected to the V_{SSOSC} supply pin. Both capacitors should be located less than 0.5 inch away from the V_{CCOSC} pin and the associated V_{SSOSC} pin.

In order to achieve a 200-nF capacitance, a parallel combination of two 100-nF capacitors may be used as long as the capacitors are placed directly beside each other.

Figure 38. V_{CCOSC} Power Filtering Diagram



A.16 Common Issues

Completing the checklist in Section A.1, "Checklist" on page 81 helps the user review schematics prior to manufacturing a system board that implements an Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor. This section highlights some commonly overlooked issues that deserve extra attention as they could be a "show-stopper" if handled incorrectly.

The following points should be reviewed prior to manufacturing:

- The PWRON_RST_N signal is a 1.3-V signal.
  This signal should *not* be pulled up to 3.3 V.
- The JTG_TRST_N signal must be asserted during reset to properly initialize the TAP controller.
  This signal should be pulled low using a 10-KΩ resistor.
- If either MII interface has been used, the ENET_MDIO signal must be pulled high with a 1.5-KΩ resistor.
- The RCOMP signal, pin D25, requires a 34-Ω +/- 1% tolerance pull-down resistor. (See Figure 34 on page 91.)
- The phase-lock loop circuits (V_{CCPLL1} and V_{CCPLL2}) and oscillator circuit (V_{CCOSCP} and V_{CCOSC}) require isolated voltage supplies. V_{CCPLL1}, V_{CCPLL2} and V_{CCOSC} are 1.3-V signals.
  It is important to note that V_{CCOSCP} is a 3.3-V signal. Detailed information is shown in Section A.15.
- The 3.3-V I/O voltage (V_{CCP}) must be powered up 1 µs before the processor voltage (V_{CC}).
  The IXP42X product line and IXC1100 control plane processors' voltage (V_{CC}) must never become stable prior to the 3.3-V I/O voltage (V_{CCP}). The complete power-sequencing requirements, given in the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet*, should be reviewed.
- Ensure that the proper Expansion Bus Configuration Resistors are populated.
  For more detail, see Section A.7.1, "Expansion Bus Configuration Strappings" on page 87.
- Ensure that the proper SDRAM Chip Select was used to access either common or different SDRAM banks.

A.17 Design Considerations

This section highlights design considerations that a user may find helpful. The considerations include:

- Designs that need to pass FCC Class B testing may want to consider Spread Spectrum Clocking.

  For more detailed information, see Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor*: Spread-Spectrum Clocking to Reduce EMI Application Note* (254028).

- For recommendations and guidelines on PCB layout and stackup, signal routing, component selection and placement, and decoupling, refer to the respective chapters of the document.

§ §