nP7250

OC-48c Network Processor (1xOC-48 / 2xGE)

General Description

The nP7250 represents the third generation in packet and cell processing technology from the original pioneering vendor of software-programmable network processors. The nP7250 offers Layer 2, 3, 4, and above packet and cell processing at wire speed for multiservice cell/packet switching and routing systems in both clear channel (OC-48c) and multi-channel (OC-48, 4xOC-12, 2xGE, 16xOC-3) modes. The device provides two identical frame interfaces — usually employed as one to framer device and one to a switch fabric or traffic manager — each supporting UTOPIA L3, SPI-3 (POS-PHY level 3), Flex Bus 3, Dual RGGI, and ViX™ v3 interfaces.

The nP7250 combines gluelessly with AMCC's traffic manager, switch fabric, framer, MAC, and search coprocessor products to provide complete data-plane solutions or can be used easily with an OEM's own technologies in any or all of these areas.

AMCC's nPsoft™ Development Environment speeds creation of vendor-differentiating features by combining the fundamentally simplified, nPcore™-based programming model of all AMCC NPUs with advanced development tools, rich application reference libraries, real hardware-based development systems, and the services of the industry's most experienced network processor-based system design staff.

Features

- OC-48 bandwidth Network Processor
- Packet-Over-SONET (POS), ATM, and Gigabit Ethernet support
- Channelized modes supporting 1xOC-48, 2xOC-24/GE, 4xOC-12, or 16xOC-3
- Dual multi-threaded nPcores™ implementing AMCC's patented, highly efficient Network Instruction Set Computing (NISC) architecture, optimized for high-speed cell/packet processing
- Simplified single-stage / single-image model for multiprocessor programming
- Seamless interface to AMCC traffic managers / switch fabrics
- Seamless interface to search coprocessors
- nPsoft Development Environment
- nP Workbench software development systems with NPU, TM, and framers
- Application reference libraries for IP routing, ATM, MPLS, L2+ switching, and more
- Embedded hardware coprocessors, including Policy Engine search coprocessor, Statistics Engine, and Special Purpose Unit for Metering, Policing, etc.
- Integrated PLL for internal clocks
- JTAG Test Support
- 1.8V core with 3.3V I/O

Applications

- Core Routers
- MPLS Switch Routers
- ATM Switches
- Subscriber Services
- Voice Gateways
- Edge Router
- Optical Access
- Multi Service Switches
- Remote Access Servers
- Content/Web Switches, Load Balancers
- LAN Switching
- DSLAM

Benefits

Third-Generation Silicon

Along with the nPX5700 10 Gbps traffic manager and nPX5800 20-160 Gbps switch fabric, the nP7250 represents our third generation of packet and cell processing, queuing, scheduling, and switching technology, starting with MMC Networks, the original pioneer of software-programmable network processors, which merged with AMCC in 2000. With switching and network processing solutions in designs by over 100 different customers, including every "Tier-1" networking equipment vendor, AMCC's technology has matured through years of invaluable real-world use to become the world's most field-proven network processor technology. And focused purely on the networking and communications industry, our vast experience has produced the industry's most experienced, world-class network processor-based design services team to support our high-performance products.

Flexible, Efficient nPcore™ Model

Each AMCC network processor is built around our patented nPcore technology, which offers a unique combination of performance and flexibility. Using hardware multi-threading, zero-cycle context switching, and powerful on-chip coprocessors to implement key atomic, single-instruction operations, the nP7250 achieves extreme efficiency – OC-48c with just two low-power cores. And yet the nPcore model still preserves complete programming flexibility, allowing the developer to arbitrarily program his algorithms without restrictions from fixed stages or elements. AMCC NPUs thus offer the flexibility of more general-purpose core-based NPUs, with the efficiency of more fixed-function NPUs.

Fundamentally Simplified Multi-Processor Programming Model

With multiple multi-threaded nPcores, the nP7250 can process many packets or cells simultaneously, but with AMCC's single-stage, "run-to-completion" programming model, each packet or cell executes in a single thread on a single core. In this way, the software developer simply creates a single program without being forced to break up and load-balance algorithms across multiple "pipelined" cores, as is the case with many NPUs based on more general-purpose processor core architectures. Future migrations are simpler, too, since once an algorithm is developed it never has to be re-subdivided across a different number of cores in a next-generation device.

Glueless Framer Interface Support

The nP7250 has dual symmetric frame interfaces configurable in the following formats: UTOPIA L3, POS-PHY L3, Flex Bus 3, RGGI or ViX-V3. The OC-48 port can also be used as streams of channelized 4xOC-12, 16xOC-3 for UTOPIA L3, POS-PHY L3 and Flex Bus 3. The nP7250 is fully standards-compliant with the OIF's SPI-3 and ATM Forum's UTOPIA 3 specifications.

Packet and Cell Processing

The nP7250's flexibility to process both cells and packets sets it apart from almost all other NPU offerings today. Each port can be configured to process cells, packets, or both simultaneously.

Embedded Network Coprocessors

Multiple on-chip coprocessors further enhance the nP7250's performance.

- ***Packet Transform Engine*** – Specially optimized for packet and cell manipulation, performs special commands on frames as a service and in parallel to the nPcores. Insert/delete data, compute and attach CRC32, and attach packet header components can all be performed by a single instruction.
- ***Special Purpose Engine*** – Eliminates the need for semaphores and other software-based constructs to dramatically reduce the number of instructions needed for operations related to external memory access, especially the synchronization of access to shared data by multiple threads, as is common with multiple packets or cells "in flight" from the same flow.
- ***Policy Engine*** – Essentially an on-chip packet classification and search coprocessor, it allows flexible, programmable policy enforcement. Several lookups – up to 512 bits in multiple keys – are returned simultaneously with fixed latency. A key application of the Policy Engine is as a "Network-Aware CASE Statement," using multiple simultaneous classifications to eliminate nested If-Then-Else software structures, reducing code size and yielding both improved and more deterministic performance.
- ***Statistics Engine*** – Automatically collects RMON statistics.

Documents & Related Products

Documents*

There are no related documents at this time

* Additional related documentation is available to approved registered users. You may apply for a ***Login Account*** to request access.

Products

Framer/Mapper
nPC1140
nPC1110
S4806
S4804

Network Processor
nPC2110

Traffic Manager
nPX5700

Switch Fabric
nPX5700
nPX8005

Storage Silicon
nP7510
nPX8005