an Intel company

2.5 Gbit/s Transponder Chip Set with Digital “Wrapping” GD16556/GD16557*

Preliminary

General Description

The GD16556 and GD16557 constitute a high performance multi-bitrate transponder chip set designed for Optical Network applications. The devices are available with either LVDS or LVPECL low-speed I/Os.

The chip set is compatible with the line rates:

- SDH STM-1 / SONET OC3
- SDH STM-4 / SONET OC12
- SDH STM-16 / SONET OC48
- Gigabit Ethernet

Switching between the bit rates is possible on-the-fly through select pins.

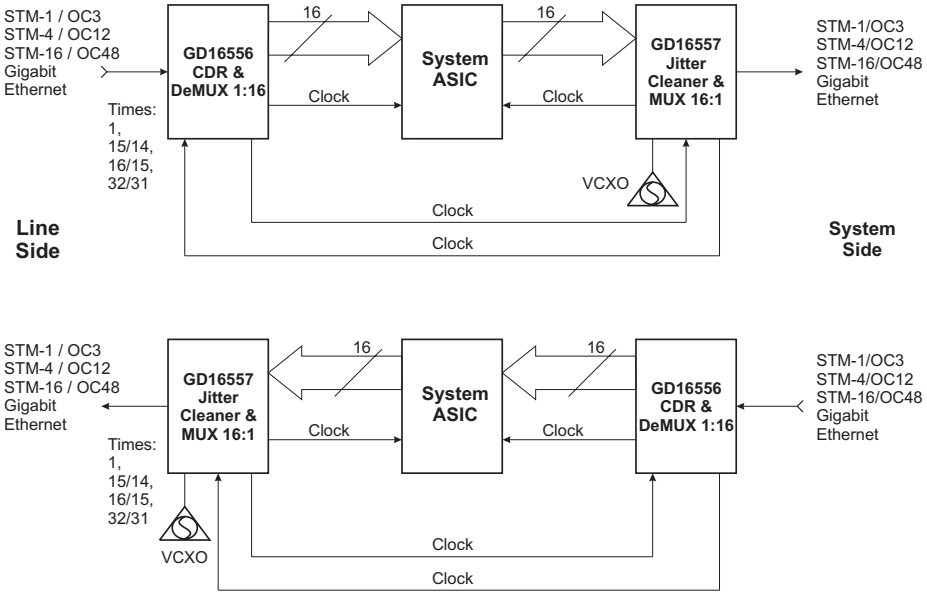
The chip set is designed for interconnecting the high-speed line interface to standard CMOS ASICs or FPGAs. The on-chip VCO and PLL blocks eliminate external high-speed clock signals and complicated timing relations.

Digital “Wrapping” Modes
GD16556 and GD16557 are capable of transmitting and receiving data at increased rates if overhead is needed for system level service purposes. The devices can operate with STM-1 (OC3), STM-4 (OC12), STM-16 (OC48) and Gigabit Ethernet line rates multiplied by a fraction. Fractions available are 32/31, 16/15 and 15/14. Thus, for example, data might be transmitted (or received) at a rate of 32/31 times 2.488 Gbit/s with a high- speed clock of 2.568 GHz. The fractions are available through selection of programmable dividers.

Signal Levels and Power Supply
Low speed interfaces are LVDS/LVPECL compatible. The high-speed output from the transmitter GD16557 is of CML-type (open collector). Select pins are LVTTL compatible.

Low power consumption is achieved by a single +3.3 V power supply and by omitting all circuitry, which can easily be implemented in the low speed system ASIC.

The devices are housed in 100 pin TQFP EDQUAD thermal enhanced packages.



Features

General

- SDH (SONET) STM-1(OC3) / STM-4(OC12) / STM-16(OC48) / GE compatible
- True on-the-fly multi-bit rate operation
- Bypass for non-compatible bit rates
- Loop-back for system test mode
- Overhead data rate capability
  - 15/14 (7% overhead)
  - 16/15 (6% overhead)
  - 32/31 (3% overhead)
- LVDS/LVPECL low-speed I/O
- Single power supply: +3.3 V
- 100 pin TQFP EDQUAD packages

GD16556 (Receiver)

- Clock and Data Recovery
- 1:16 Demultiplexer
- Differential input with 5 mV_{PP} sensitivity
- Loss of signal monitor
- Bit consecutive monitor
- Lock detect monitor
- Power dissipation: 1.3 W (typ.)

GD16557 (Transmitter)

- 16:1 Multiplexer
- Optional double PLL jitter-clean up
- Counter or forward clocked low-speed interface
- PLL lock-detect
- Power dissipation: 1.3 W (typ.)

Applications

- Digital “Wrappers”
- Optical Networking
- Transponders
- SDH/SONET FEC out-of-band systems
- Network interconnects
- Gateways
- Datacom

: Patent pending

Functional Details

General

The transmitter and receiver chip set is optimised for transponder solutions and Optical Network interconnects such as bridges and gateways. The intended transponder system is shown on page 1.

Transponder System Jitter Specifications

The transponder system exceeds ITU-T (recommendation G.825 for a Type B regenerator) and Bellcore recommendations with respect to output jitter.

The jitter-tolerance on the input side exceeds ITU-T (recommendation G.958) and Bellcore recommendations.

GD16556 - The Receiver

The GD16556 receiver integrates:
- a Limiting Input Amplifier (LIA)
- a Bang-Bang Phase Detector
- a Phase Frequency Detector
- a Voltage Controlled Oscillator

into a complete Clock Data Recovery (CDR) system. The CDR is followed by a 1:16 de-multiplexer. A lock-detect output monitors if the CDR is locked onto the received serial data.

GD16557 - The Transmitter

The GD16557 transmitter is a 16:1 multiplexer with an integrated double PLL topology requiring an external VCXO to achieve a superior jitter clean-up.

System Speed

The pins RSEL1 and RSEL2 choose the line rate (155 Mbit/s, 622 Mbit/s, 2.488 Gbit/s and 1.250 Gbit/s). It is the responsibility of the system to monitor the bit rate and assert the signals RSEL1 and RSEL2.

Bypass Data Path

To enable handling of non-compatible bit rates a bypass data path is featured. This path bypasses the CDR in the receiver and the multiplexer in the transmitter. The bypass data I/O (BP, BPN) are CML compatible with a LVTTL compatible active low enable pin BPEN in order to reduce noise at the printed circuit board when disabled. The system needs to monitor the incoming bit rate and assert the BPEN signal properly.

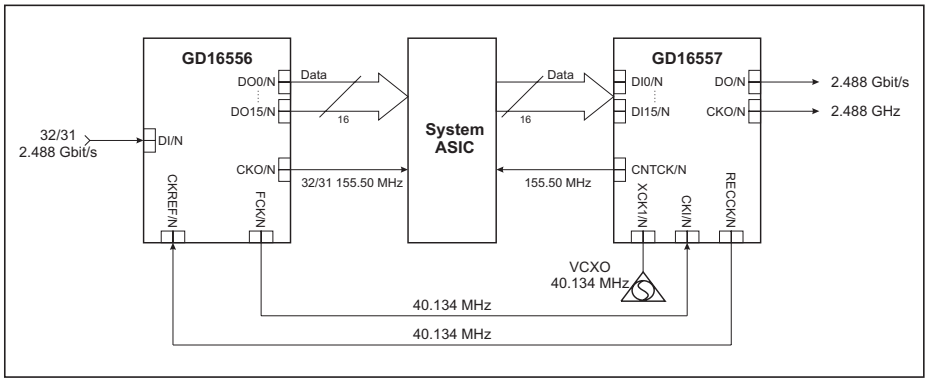


Figure 1. *An example configuration of a channel in a transponder system*

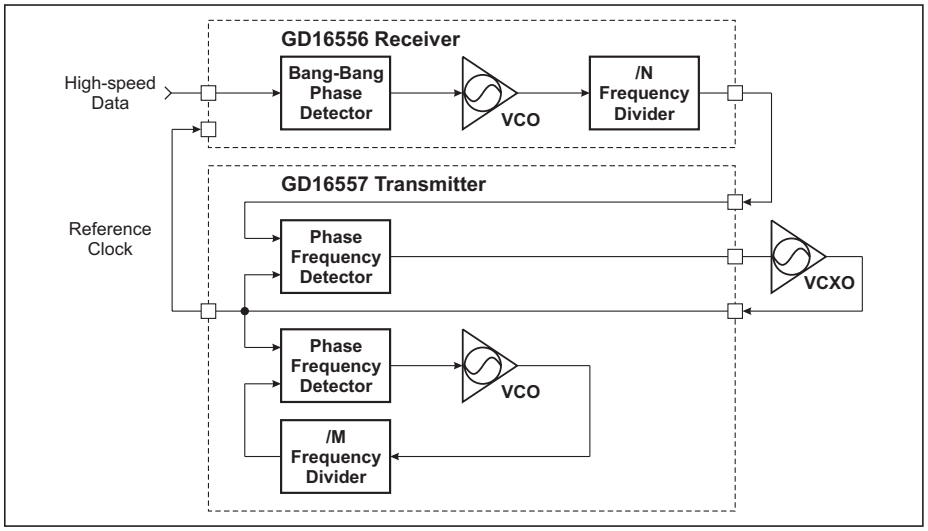


Figure 2. *The core circuit*

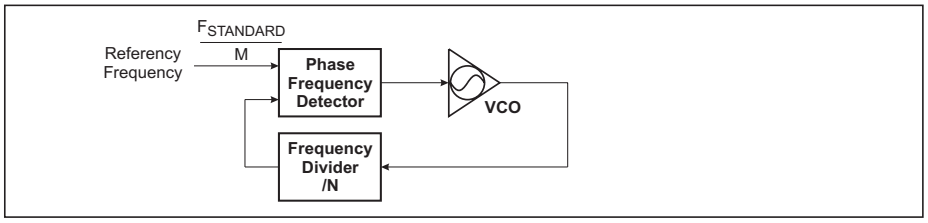


Figure 3. *Basic PLL frequency syntesis*

Loop-back Data and Clock Path

A loop-back data path is featured to enable easy means of fault diagnostics and system verification etc. The loop-back data and clock path bypasses the de-multiplexer in the receiver and the multiplexer in the transmitter. The loop-back data I/O is named LB, LBN and the loop-back clock I/O is named LBCK, LBCKN. To enable the loop-back paththe system needs to assert the signal LBEN.

The Transponder System

The chip set is designed for the transponder system shown on the front page. The system consists of a receiver GD16556, a system ASIC tailored for the application and a transmitter GD16557. Such a three-device configuration is needed for each direction.

Appropriate timing relations are assured by the PLL topology of the system. Furthermore, the choice of PLL topology as-

sures that the transponder system meets the jitter specifications.

The core circuit is illustrated on Figure 2 For simplicity the system ASIC and connections to this device have been omitted. Also, the PLLs have been somewhat simplified omitting the charge pumps and loop-filters.

Referring to Figure 2 the functionality of the system is as follows; looking at the CDR device GD16556 the incoming high-speed data signal is sampled by the bang-bang detector. The bang-bang detector outputs a signal that drives a charge pump and hence controls the on-chip VCO in the CDR. This causes the VCO frequency to match the data frequency. A reference frequency for the CDR is supplied from the VCXO located on the transmit side. The reference frequency assures that the VCO frequency does not deviate too much from the (expected) bit rate. Since the CDR in the receiver needs to be within 500 ppm of the bit rate, the VCXO frequency should not deviate more than 200 ppm (TBD) from its proper centre frequency under any conditions. Please refer to the section on the GD16556 device on page 5 for a detailed discussion of the CDR functionality. Valid VCXO centre frequencies are outlined on Table 1 on page 11.

Turning to the transmit device GD16557 the device implements a double PLL topology. The double PLL is required to make the system exceed the ITU-T / Bellcore jitter recommendations independent of the bit rate. On the CDR side a trade-off exists between jitter-tolerance and jitter-transfer. It is difficult to achieve a proper jitter-tolerance and simultaneously a proper jitter-transfer no matter the bit rate not having the possibility to modify the loop-filter. However, by implementing a PLL with a low bandwidth (typ. less than 10 kHz) it is possible to equalize penalty in jitter- transfer. The result is an excellent jitter- tolerance no matter the bit rate. The drawback of this solution is the need for a high-Q oscillator. Since it is not possible to realise a high-Q on-chip oscillator the high-Q oscillator is added as an external crystal type VCO (VCXO). Figure 2 shows the double PLL implemented in the GD16557. The VCXO is locked to the divided clock output from the CDR device. Now, the transmitter on-chip VCO is locked to the VCXO in a second PLL. This causes the VCO to track the VCXO achieving superior phase-noise properties of the high-speed output data.

The transponder system allows for increased bit rates. The use of increased standard bit rates is commonly known as “digital wrapping”. The chip set supports digital wrapping by implementing programmable frequency dividers (prescalers). By proper setting of the dividers the transponder system will comply with bit rates equal to a standard bit rate (STM-1 / OC3, STM-4 / OC12, STM-16 / OC48, GE) multiplied by a fraction larger than one. Supported fractions are 15/14, 16/15 and 32/31.

Supporting digital wrapping corresponds with an ability to tune the VCOs in the CDR and transmit device onto the proper frequency. Basic frequency synthesis is applied to implement this functionality. The principle is illustrated on Figure 3. By choosing the frequency of the reference clock signal as a standard bit rate frequency (denoted $f_{STANDARD}$) divided by M, the frequency of the VCO (denoted f_{VCO}) becomes:

$$f_{VCO} = \frac{f_{STANDARD} \times N}{M}$$

The on-chip frequency dividers implements divide by 56, 60, 62 and 64. Signals MSEL1 and MSEL2 choose the divide ratio. It is the responsibility of the system to configure the GD16556/ GD16557 with respect to the bit rate (RSEL1, RSEL2) and the overhead fraction factor (MSEL1, MSEL2). Table 1 on page 11 outline the recommended VCXO frequencies with respect to the settings of RSEL1, RSEL2 and MSEL1, MSEL2.

Practical Considerations

The PCB Layout

The PCB must be designed with shortest possible conductors for the data interfaces and clock distribution. Design these connections as transmission lines.

The LVTTL compatible select pins are supplied with an on-chip pull-up resistor (Figure 4) given a default “1" when not connected.

The LVDS connection scheme is shown on Figure 5. The LVDS I/Os have an impendance of 100 Ω and do not require external termination resistors.

LVPECL connection schemes are shown on Figures 6 and 7 .

The high-speed CML type input buffers are supplied with on-chip termination resistors as shown on Figure 9.

The heatsink on the TQFP EDQUAD package should be connected to a VEE power supply plane on the PCB with capability to carry away the dissipated heat.

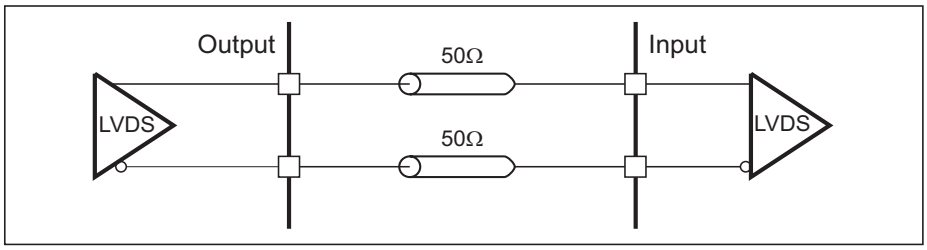


Figure 5. *LVDS connection*

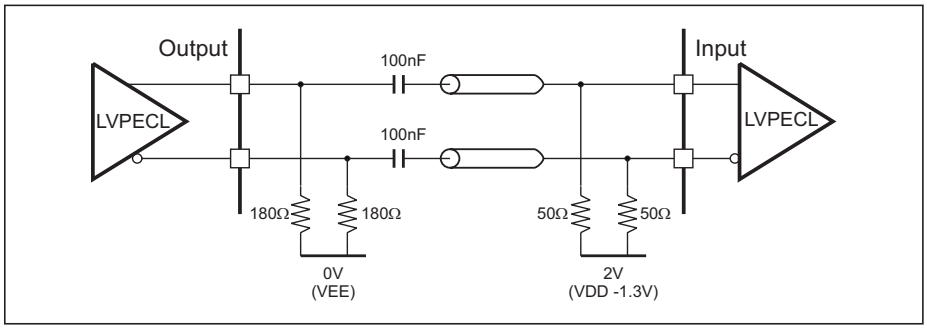


Figure 6. *LVPECL output termination, AC-coupled.*

Noise Considerations

When designing the PCB utmost importance should be put on noise isolation. De-coupling capacitors should be applied to each supply pin. Care should be taken to reduce ground bounces. Be aware that any noise added to the VCXO output signal translates directly into jitter on the high-speed output clock. Hence, the VCXO(s) should be differential and located close to the transmit device.

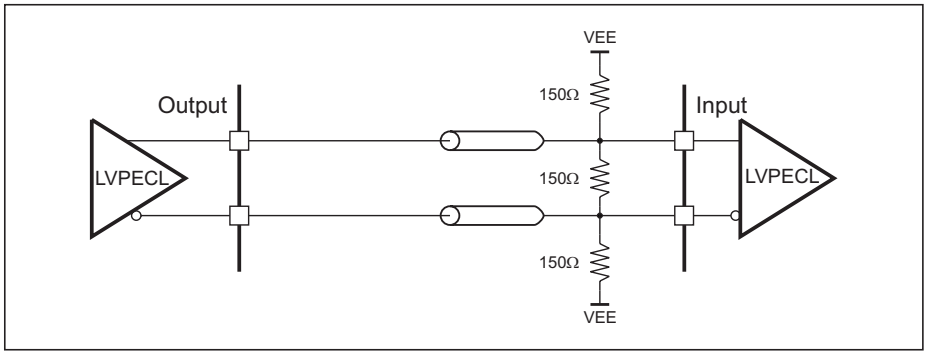


Figure 7. *LVPECL output termination, DC-coupled.*

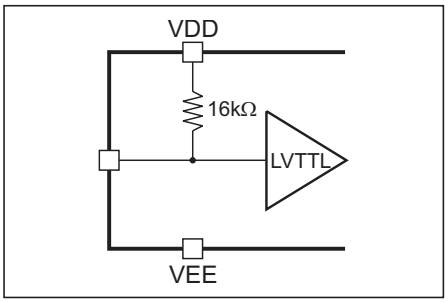


Figure 4. *LVTTL pull-up resistor*

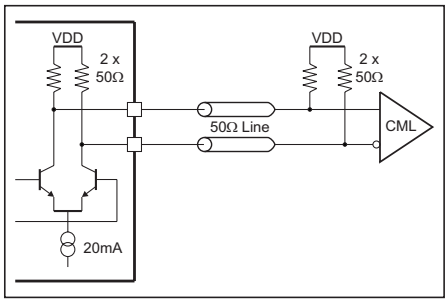


Figure 8. *CML output buffer*

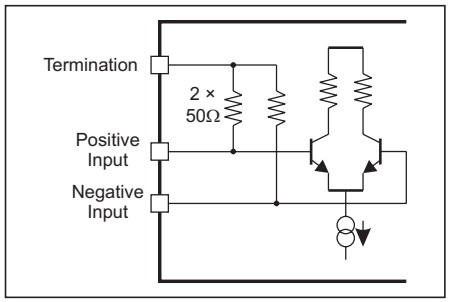


Figure 9. *CML input buffer*

General

The GD16556 is an on-the-fly programmable multi-bitrate CDR and 1:16 demultiplexer with emphasis put on transponder applications. The device is capable of demultiplexing a serial bit stream at 155 Mbit/s, 622 Mbit/s, 1.250 Gbit/s or 2.488 Mbit/s into 16 parallel low speed channels.

When operated in non-transponder applications the device meets all ITU-T / Bellcore jitter specifications when used with the recommended loop filter (Refer to Figure 19). Note that the loop-filter is dependent on the bit-rate in order to achieve the jitter specifications. In this case true on-the-fly multi-bitrate operation is not an option.

When operated in the transponder configuration Figure 1 true multi-bitrate operation is made possible by a trade-off between jitter-tolerance and jitter-transfer in the receiver. By allowing an increase in jitter-transfer the jitter tolerance is achieved at any bitrate. The double-PLL jitter clean-up system on the transmitter "equalizes" this penalty on the transmit side.

Hence, the overall transponder system will be well within the jitter specifications.

Select pins are LVTTL compatible. The LVTTL inputs are internally pulled high by default.

The device operates from a single 3.3 V positive power-supply and the consumption is 1.3 W (typ.).

Digital "Wrapping" Modes

The GD16556 is capable of receiving data at increased bit rates if overhead capability for system purposes is needed. Table 1 on page 11 outlines the constraints on the reference clock and the setting of the MSEL1, MSEL2 signals for the transponder system shown on Figure 1.

Clock Generator Circuit

The clock generator circuit in the GD16556 contains two independent dividers.

One divider (divide by 1 for STM-16/OC 48, divide by 2 for Gigabit Ethernet, divide by 4 for STM-4/OC 12 and divide by 16 for STM-1/OC 3) generates the line rate clock to the Bang-Bang phase detector plus decision sampling gaate.

A second divider (56, 60, 62 and 64) divides the VCO frequency to generate a signal that is compared with the reference clock in the Phase Frequency Detector (PFD). This signal is also forwarded to the transmitter GD16557 when operated in a transponder system.

The circuit topology allows for a straightforward increase in line rates by a fraction. The simplest illustration is by example.

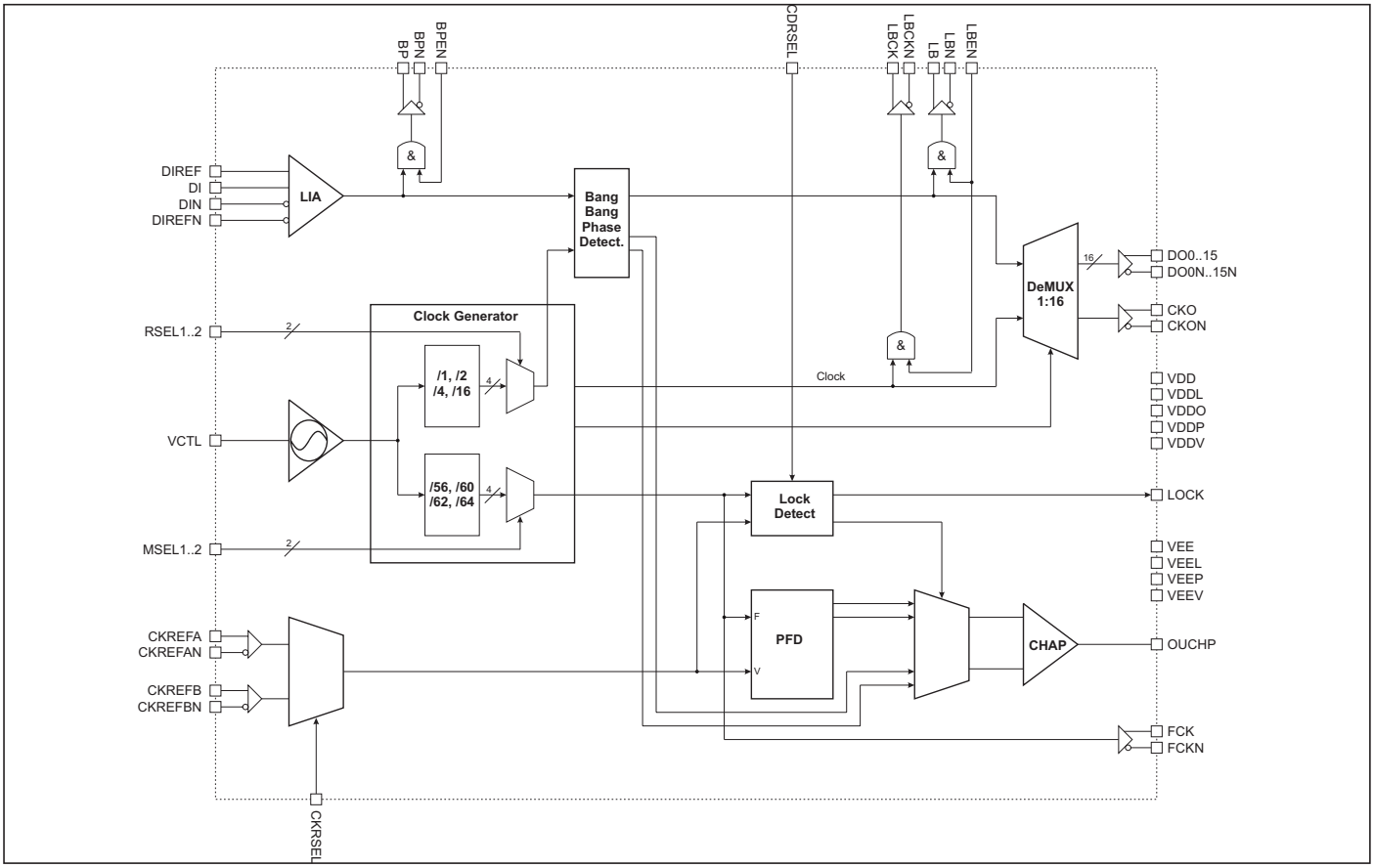


Figure 10.*GD16556 - Block diagram*

Assume the incoming line rate equals 32/31 times 2.488 Gbit/s. Thus, the VCO frequency should equal 2.568 GHz. The reference clock input (CKREF, CKREFN) is defined as 2.488 GHz/62 equal to 40.134 MHz. Now the VCO frequency is divided by 64 and compared on the PFD. This will cause the VCO to tune onto a frequency of 64/62 that is 32/31 times 2.488 GHz due to the PLL feedback.

The topology of the circuit splits the line rate generation from the fraction select allowing any combination of the two.

For simplicity a third divider that generates clocks to the de-multiplexer is not shown on the block diagram.

Lock Detect Circuit

The Lock Detect Circuit continuously monitors the frequency difference between the reference clock and the divided VCO clock. If the reference clock and the divided VCO frequency differ by more than 500 ppm it switches the PFD into the PLL in order to pull the VCO back inside the lock-in range. This mode is called *the acquisition mode.*

The PFD is used to ensure predictable lock up conditions for the GD16556 by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock range where the Bang-Bang Phase Detector is capable of acquiring lock to incoming data. The PFD is digital with true Phase/Frequency detectability.

Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called *CDR mode*.

Bang-Bang Phase Detector

The Bang-Bang Phase Detector is used in *CDR mode* as a true digital type detector, producing a binary output. It samples the incoming data twice each bit period: once in the transition of the (previous) bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits will show whether the VCO clock leads or lags the data. Hence the bit transition point controls the PLL, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter components control the characteristics of the PLL.

The binary output of either the PFD or the Bang-Bang Phase Detector (depending of the mode of the lock-detection circuit) is fed to a Charge Pump capable to sink/source current or tristate. The output of the Charge Pump is filtered through the Loop Filter and controls the tuning-voltage of the VCO.

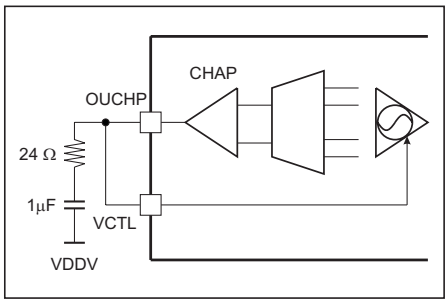


Figure 11.*GD16556 - Loop filter*

As a result of the continuous monitoring Lock Detect Circuit the VCO frequency never deviates more than 500 ppm from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock (CKOUT) is always kept within the 500 ppm limit, ensuring safe clocking of down stream circuitry.

The LOCK Signal

The status of the lock-detection circuit is given by the LOCK signal. In CDR mode LOCK is steady high. In acquisition mode LOCK is alternating indicating the continuous shifts between the Bang-Bang Detector (high) and the PFD (low).

The BC_DET Signal

An internal circuit monitors input data transitions and gives a BC_DET output signal which is asserted if more than 256 consecutive identical bits, 0s or 1s, are detected.

BC_DET will be de-asserted only after approximately 16 bit transitions are detected within a time period proportional to the selected data rate (50 ns at STM 16 / OC-48).

The LOCK_DET Signal

The LOCK_DET signal is a status output, which monitors the status of the internal lock detect circuit of the GD16556 CDR logic and the output of the BC_DET circuit.

LOCK_DET is asserted (set HIGH) if the VCO frequency differs from the reference frequency by ±500 ppm. This ' out of lock' condition is detected by the internal Lock Detect circuit described previously. LOCK_DET is also asserted in the case of the absence of data, which is detected by the BC_DET circuit within the reaction time of the internal PLL lock detect system.

If data is absent, the divided VCO frequency will drift away from the reference frequency until they differ by ±500 ppm. The internal Lock Detect logic will alternate between CDR and acquisition mode until data returns, enabling the GD16556 to acquire lock and function in CDR mode.

The LOCK_DET signal, however, will remain asserted until BC_DET is de- asserted and the internal lock detect circuit is operating in CDR mode.

The CDR circuitry of the GD16556 has been fine-tuned to provide an accurate stable clock output from the VCO when data is present. Due to the precise nature of the internal VCO, when data is absent the clock output frequency will drift slowly from the recovered clock frequency until an out of lock condition is detected. The time taken for the GD16556 to go 'out of lock' in the absence of data will typically be at least 3 ms, unless an external circuit is used to pull the VCO frequency away from the reference frequency.

When loss of data is detected, i.e. BC_DET is asserted, or the divided VCO frequency differs from the reference frequency by ±500 ppm, LOCK_DET is asserted and the internal lock detect circuit switches to acquisition mode. This will give a stable output clock during a loss of data condition.

When BC_DET is de-asserted and the divided VCO frequency is within 500 ppm of the reference frequency, LOCK_DET will be de-asserted within 500 μs, independent of selected data rate.

LOS_DET

The Loss Of Signal DETection (LOS_DET) alarm output is low during normal operation.

The LOS_DET signal is the output from a digital Bit Error Flag (BEF) circuit which monitors the number of false bit transitions in the data signal. An internal flag is raised if the number of false transitions is above a predefined level, i.e. if the Bit Error Rate (BER) is above the corresponding BER level.

This has been realised by counting the false bit transitions. If this counter runs out within a time period the BEF flag is set. The length of the counter may be set by external select signals (SBER0 and SBER1). The time period that the false errors are counted within is 64 kbit/s corresponding to 26 μs at STM 16 / OC-48 data rate. The length of the counter may be set to detect approximate Bit Error Rates of 0.5E-3, 1E-3, 2E-3 or 4E-3.

The input to the BEF circuit is derived from Bang-Bang detector sample data. As discussed above, the Bang-Bang detector samples the incoming data twice each bit period, once at the transition and once in the middle of the eye. If the value of the samples in the middle of the eye for two consecutive bits is equal but the value of the transition sample is different then a bit error has occurred.

As the BEF system detects false bit transitions between two consecutive bits, only bit errors due to high frequency noise are detected. Therefore there will not be a 1:1 correlation between the actual BER of the signal and the number of errors detected by the BEF system. However the actual bit error rate is correlated to the number of errors detected in the BEF system. This means that by choosing the appropriate counter length, it will be possible for the BEF system to set the BEF flag at a user selectable bit error rate.

Once the LOS_DET signal has been asserted, it will be de-asserted only when the BER is less than ¼ of the set rate for a period which is proportional to the selected data rate. (at least 125 μs at STM16 / OC-48).

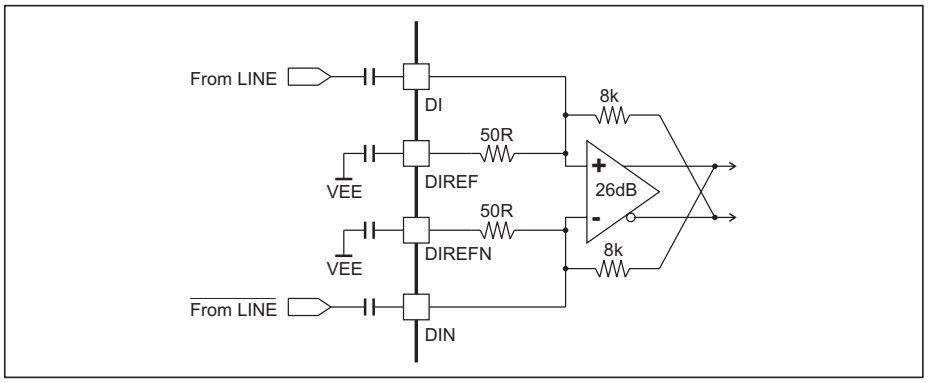


Figure 12.*AC coupled input (using internal offset compensation).*

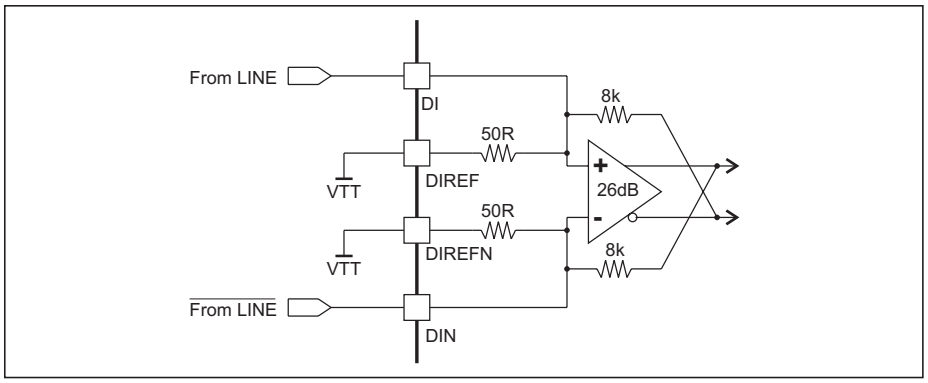


Figure 13.*DC coupled input (ignoring internal offset compensation). V_{TT} depends on the termination requirements of the previous stage, and the resulting amplitude on the input.*

Data Input

The input amplifier (DI / DIN) is designed as a Limiting Amplifier (LIA) with a sensitivity better than 10 mV (differential).

The inputs may be either AC or DC coupled. If the inputs are AC coupled the amplifier features an internal offset cancelling DC feedback. Notice that the offset cancellation will only work when the input is differential and AC-coupled as shown on Figure 12.

Bit Order

The serial data stream is output with the first bit received on DO0, the second on DO1 and the last bit in a 16 bit frame on DO15.

General

The GD16557 is an on-the-fly programmable multi-bitrate multiplexer with emphasis put on transponder applications. The device is capable of multiplexing 16 independent low speed channels into one serial bit stream at 155 Mbit/s, 622 Mbit/s, 1.250 Gbit/s or 2.488 Mbit/s.

The device meets all ITU-T jitter requirements when used with the recommended loop filter (refer to Figure 19).

The device can be either counter or forward clocked.

Low-speed data and clock I/O are LVDS/LVPECL compatible. The high-speed outputs are open collectors (CML-type). Select pins are LVTTL compatible. The LVTTL inputs are internally pulled high by default. The VCXO clock inputs are LVPECL compatible.

The device operates from a single 3.3 V positive power-supply and the consumption is 1.3 W (typ.).

Digital “Wrapping” Modes

The fraction is chosen by the signals MSEL1 and MSEL2. Table 1 on page 11 outlines the constraints on the bit rates with respect to the VCXO frequencies. Select signal settings are listed along. The table is valid for the transponder system shown on Figure 1.

Clock Generator Circuit

The Clock Generator circuit in the GD16557 is much alike the one in the receiver GD16556. Please refer to the discussion in the section *Clock Generator Circuit* in the GD16556 description.

Counter Clocking Scheme

When the GD16557 is used in transponder applications the input reference clock to the transmitter (CKI, CKIN) is generated by the receiver GD16556. Please refer to Figure 10.

In non-transponder applications the GD16557 may be operated with jitter clean-up (including VCXO) or without leaving the possibility to omit the VCXO. If operation is desired without the VCXO (i.e. omitting the double PLL jitter-clean up) the reference clock input VCK is available. Select between the clock inputs XCK1/XCK2 and VCK through the signal VSEL.

The reference clock frequency should in any case be chosen according to Table 1 on page 11.

To ease the interfacing between the GD16557 and the system ASIC the relation between the counter clock (CNTCK) and the input data (DI0..15) is adjustable. Pins PHA1 and PHA2 define the valid timing relation.

Note: When enabling LBEN or BPEN the VCO is disabled for noise reduction.

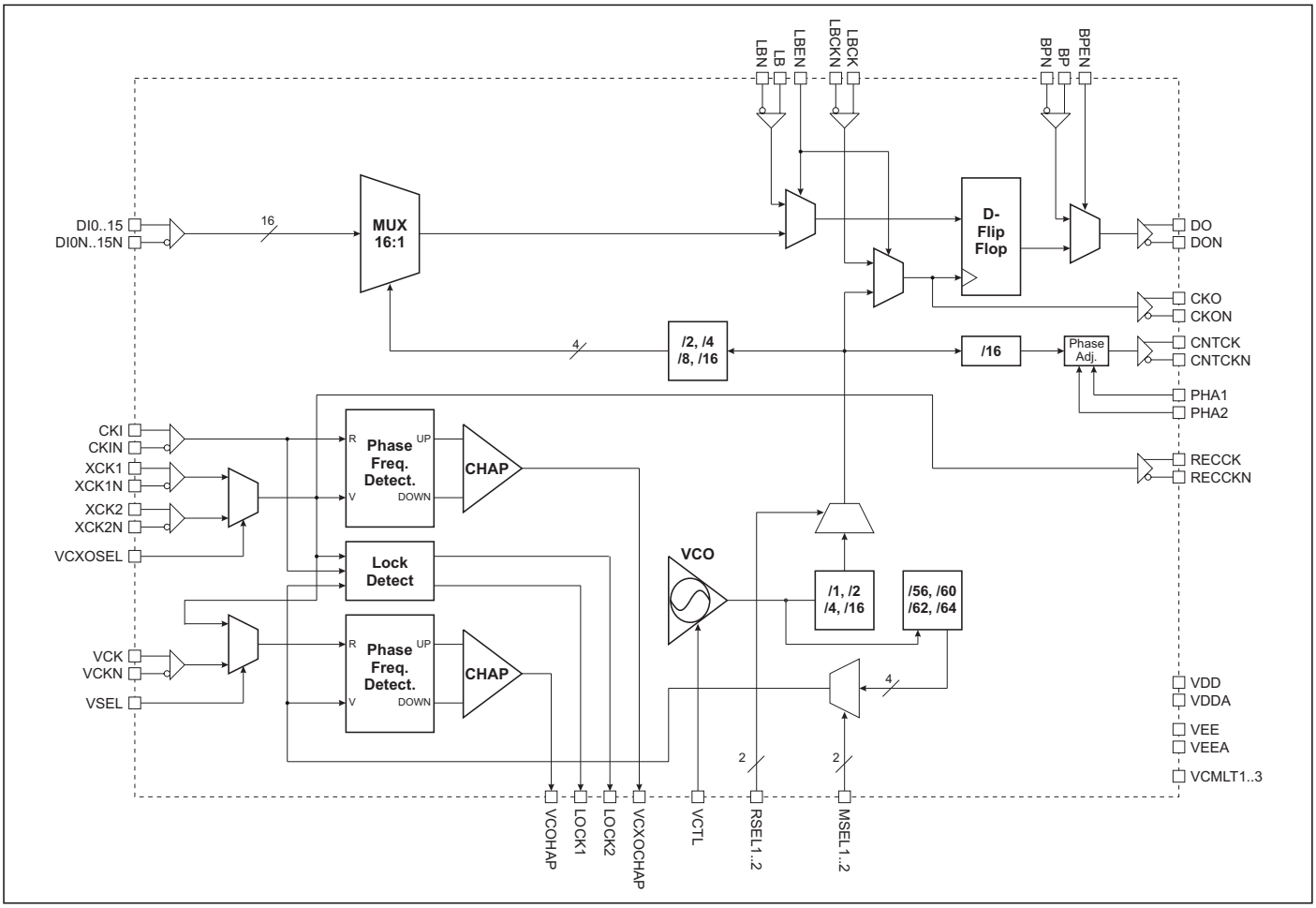


Figure 14.*GD16557 - Block diagram*

Forward Clocking Scheme

GD16557 has been designed as a reverse clocked MUX. Typically this is a sound way to use the device in a transponder system, because of the relatively long (6400 ps) bit period at the 16 bit interface. However in some systems it is an advantage to be able to use forward clocking. This is possible on GD16557 because the device has build in two phase detectors and because the relation between the counter clock and the input sampling time is very well defined.

In a forward-clocked system an external VCXO is locked to the internal VCO using PFD2, as shown in the Figure 15. The VCO signal is internally fed to PFD2 and LPF2 is the loop filter. This loop determines the jitter generation of the output data. The resulting locked VCO is called VCOL.

This resulting jitter free VCO (locked to the VCXO) is locked to the forward clock using PFD1 as shown below. This ensures that the VCO will follow changes in the phase of the forward clock for modulation frequencies below the bandwidth of LPF1. For modulation frequencies above the bandwidth of LPF1 VCOL phase changes will be tracked. Assume the phase error between the forward clock and the counter clock is zero and that the sampling time has been adjusted to occur in the middle of the eye according to the set-up and hold times. Then the phase margin is determined by set-up and hold time between the counter clock and the input data signal. On GD16557 this phase margin is 6400 ps – 1500 ps or 4900 ps. However if the phase error between the forward clock and the counter clock is not zero, then any uncertainty will degrade the phase margin. Any leakage current on the output of PFD1 will cause a phase error.

Leakage current can occur from the charge pump in PFD1 or from input leakage current into the VCXO. The charge pump leakage is less than 5%. 5% leakage causes ±0.05 UI phase error or ±340 ps phase error. Therefore the phase margin will be 4220 ps if the VCXO does not have any leakage current.

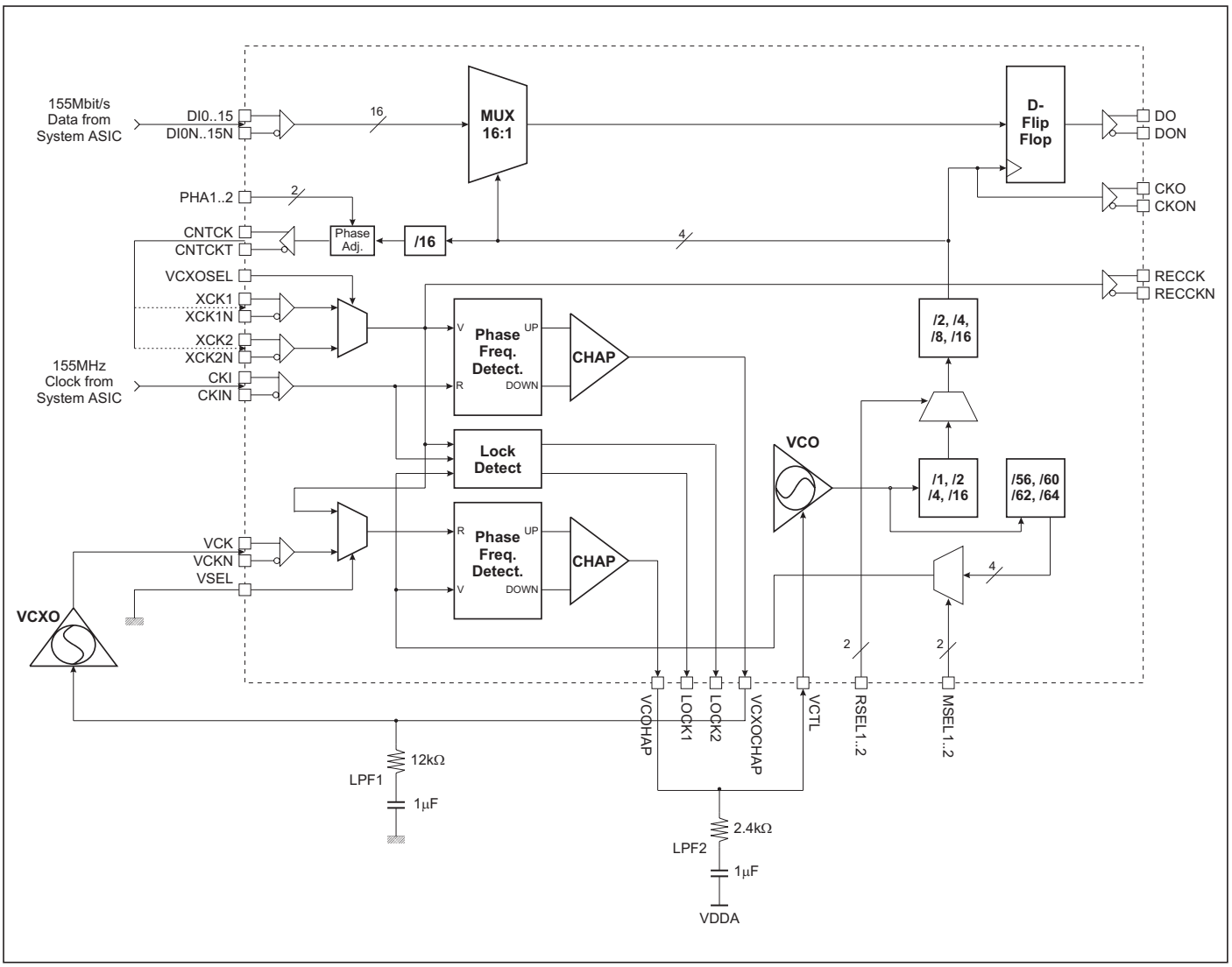


Figure 15.*Forward Clocking Scheme*

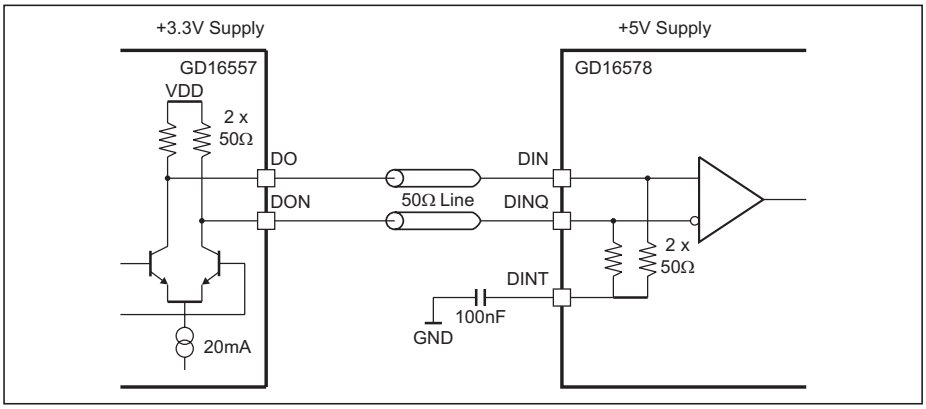


Figure 16.*GD16557/GD16578 DC-connection*

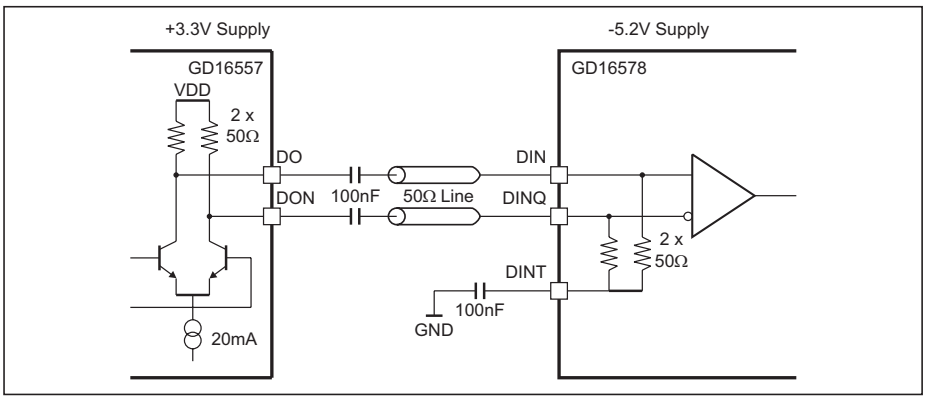


Figure 17.*GD16557/GD16578 AC-connection*

High-speed Clock and Data Outputs

The high-speed clock output (CKO, CKON) and the serial data output (DO, DON) are CML (with internal 50 Ω collector impendance) type outputs. They should be connected as shown on Figure 18.

The high-speed outputs of the GD16557 are suited to drive the GIGA GD16578 high-current laser driver. Connection schemes are shown on Figure 16 and Figure 17.

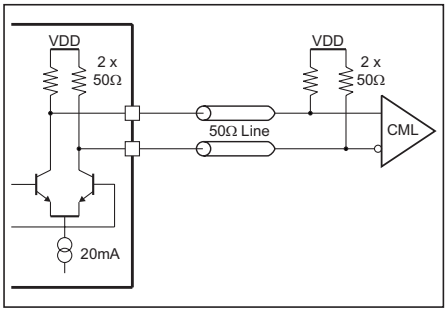


Figure 18.*GD16557 and GD16557/ECL CML output driver.*

Double PLL for Jitter Clean-up

The device implements a double PLL for high performance jitter-transfer characteristics. It integrates:

- a low-noise LC-type Voltage Controlled Oscillator (VCO)
- two digital Phase Frequency Detectors (PFDs)
- two tristate-type Charge Pumps (CHAPs)

To complete the PLLs it is only necessary to add loop-filter components and a low-noise crystal oscillator (VCXO) at the board.

Loop Filters

The recommended loop filters are simple first-order RC-filters as shown on Figure 19. Note that the on-chip VCO loop-filter is terminated to the positive VCO power supply VDDA.

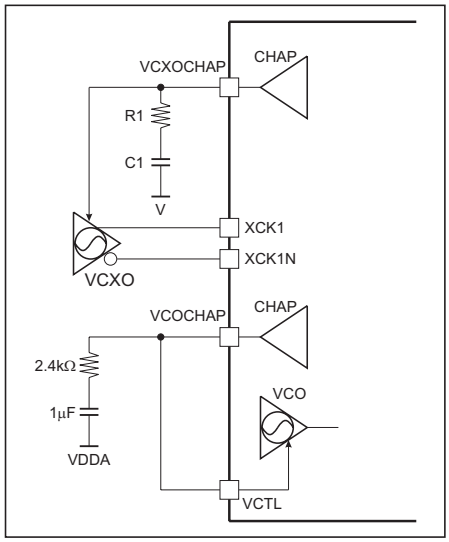


Figure 19.*GD16557 - Loop filters*

Note: Values for “R1” and “C1” depend on the specific VCXO. “V” must be connected to the same power supply reference point as the VCXO.

Charge Pump Polarity

The pin VCOCHAP will sink current (decrease the voltage on the loop-filter capacitor) when the on-chip VCO is to increase the frequency. When the on-chip VCO is to decrease the frequency the pin VCOCHAP will source current. This corresponds to a negative VCO tuning constant.

The VCXO control pin VCXOCHAP will source a current when the VCXO is to increase the frequency and sink a current when the VCXO is to decrease its frequency. If neither is to happen the pin VCXOCHAP tristates. This corresponds to a positive VCO tuning constant.

Lock Detect

Each PLL is equipped with a LVTTL lock detect output that signals whether or not the PLL is locked. A logic “1" indicates no lock and a logic ”0" indicates in lock. The pins LOCK1 and LOCK2 should be connected to a 10 nF capacitance (Figure 20). The LVTTL output LOCK1A indicates the state of the VCXO based PLL and the LVTTL output LOCK2A indicates the state of the on-chip VCO based PLL.

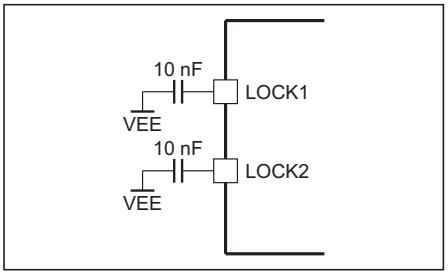


Figure 20.*Lock detect*

Jitter Transfer

The basic idea of the double PLL system is to create a narrow bandwidth jitter transfer performance of the system. The jitter-transfer of the double PLL system is shown on Figure 21.

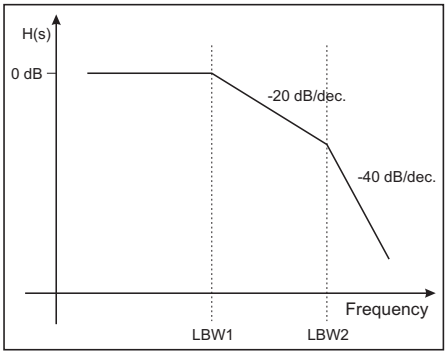


Figure 21.*The closed-loop transfer function of the double PLL system.*

The bandwidth of the VCXO based PLL is denoted LBW1 and the bandwidth of the VCO based PLL is denoted LBW2.

The VCXO PLL is locked to the incoming clock (CKI, CKIN). Since the loop bandwidth of the VCXO based PLL (LBW1) can be chosen to a few kHz, jitter on the incoming clock is suppressed above the VCXO PLL loop bandwidth. The on-chip high-speed VCO used for clock multiplication tracks the VCXO through the second PLL. This generates a very low-noise high-speed clock. The loop bandwidth of the VCO based PLL is made wide (typ. 2 MHz) for suppression of the intrinsic phase noise present in the VCO.

Jitter Generation

The overall jitter performance of the device is the sum of the jitter on the input clock with respect to the jitter-transfer of the device and the jitter generation of the device itself. The choice of loop bandwidths and VCXO for the double PLL will assure that the transponder system meets the jitter requirements. The jitter generation of the GD16557 is minimised through a careful design and layout of the device and a low-noise on-chip VCO.

Multi Bitrate Operation and Gigabit Ethernet

Operation of the device transmitting STM-1 (OC3), STM-4 (OC12) and STM-16 (OC48) bit rates requires a single VCXO with a centre frequency according to Table 1 on page 11. However, to achieve the line rate for Gigabit Ethernet it is most likely necessary to add a second VCXO (Due to the usual limited tuning range of VCXOs). This is made possible by adding two VCXO inputs in parallel (XCK1, XCK1N and XCK2, XCK2N) selectable by the signal VCXOSEL. The concurrent use of two VCXOs requires a slightly modified loop-filter that will be determined during prototype test. When using several VCXOs it is important to consider the possibility of crosstalk between the VCXO clock signals. It is recommended to disconnect the power supply for the VCXO not in use.

Bit Order

The bits DI0..DI15 are multiplexed into a serial stream with DI0 as the first bit transmitted and DI15 as the last bit in a 16 bit frame.

Standard Bit Rate	"Wrap" fraction	VCXO Centre Frequency [MHz]	GD16556 select pin settings RSEL1/2	GD16556 select pin settings MSEL1/2	GD16557 select pin settings RSEL1/2	GD16557 select pin settings MSEL1/2
STM-1 / OC 3	None. Only standard bit rates available.	38,880000	"10"	"11"	"10"	"11"
STM-4 / OC 12		38,880000	"01"	"11"	"01"	"11"
STM-16 / OC 48		38,880000	"11"	"11"	"11"	"11"
GE		39,062500	"00"	"11"	"00"	"11"
STM-1 / OC 3	Standard bit rates with programmable 15/14 overhead.	44,434286	"10"	"00"	"10"	"00"
STM-4 / OC 12		44,434286	"01"	"00"	"01"	"00"
STM-16 / OC 48		44,434286	"11"	"00"	"11"	"00"
GE		44,642857	"00"	"00"	"00"	"00"
STM-1 / OC 3	15/14 on receiving side	44,434286	"10"	"01"	"10"	"00"
STM-4 / OC 12		44,434286	"01"	"01"	"01"	"00"
STM-16 / OC 48		44,434286	"11"	"01"	"11"	"00"
GE		44,642857	"00"	"01"	"00"	"00"
STM-1 / OC 3	15/14 on transmitting side	44,434286	"10"	"00"	"10"	"01"
STM-4 / OC 12		44,434286	"01"	"00"	"01"	"01"
STM-16 / OC 48		44,434286	"11"	"00"	"11"	"01"
GE		44,642857	"00"	"00"	"00"	"01"
STM-1 / OC 3	15/14 on transmitting side and receiving side	44,434286	"10"	"01"	"10"	"01"
STM-4 / OC 12		44,434286	"01"	"01"	"01"	"01"
STM-16 / OC 48		44,434286	"11"	"01"	"11"	"01"
GE		44,642857	"00"	"01"	"00"	"01"
STM-1 / OC 3	Standard bit rates with programmable 16/15 overhead.	41,472000	"10"	"01"	"10"	"01"
STM-4 / OC 12		41,472000	"01"	"01"	"01"	"01"
STM-16 / OC 48		41,472000	"11"	"01"	"11"	"01"
GE		41,667000	"00"	"01"	"00"	"01"
STM-1 / OC 3	16/15 on receiving side	41,472000	"10"	"11"	"10"	"01"
STM-4 / OC 12		41,472000	"01"	"11"	"01"	"01"
STM-16 / OC 48		41,472000	"11"	"11"	"11"	"01"
GE		41,667000	"00"	"11"	"00"	"01"
STM-1 / OC 3	16/15 on transmitting side	41,472000	"10"	"01"	"10"	"11"
STM-4 / OC 12		41,472000	"01"	"01"	"01"	"11"
STM-16 / OC 48		41,472000	"11"	"01"	"11"	"11"
GE		41,667000	"00"	"01"	"00"	"11"
STM-1 / OC 3	16/15 on transmitting side and receiving side	41,472000	"10"	"11"	"10"	"11"
STM-4 / OC 12		41,472000	"01"	"11"	"01"	"11"
STM-16 / OC 48		41,472000	"11"	"11"	"11"	"11"
GE		41,667000	"00"	"11"	"00"	"11"
STM-1 / OC 3	Standard bit rates with programmable 32/31 overhead.	40,134194	"10"	"10"	"10"	"10"
STM-4 / OC 12		40,134194	"01"	"10"	"01"	"10"
STM-16 / OC 48		40,134194	"11"	"10"	"11"	"10"
GE		40,322581	"00"	"10"	"00"	"10"

Standard Bit Rate	"Wrap" fraction	VCXO Centre Frequency [MHz]	GD16556 select pin settings RSEL1/2	MSEL1/2	GD16557 select pin settings RSEL1/2	MSEL1/2
STM-1 / OC 3	32/31 on receiving side	40,134194	"10"	"11"	"10"	"10"
STM-4 / OC 12		40,134194	"01"	"11"	"01"	"10"
STM-16 / OC 48		40,134194	"11"	"11"	"11"	"10"
GE		40,322581	"00"	"11"	"00"	"10"
STM-1 / OC 3	32/31 on transmitting side	40,134194	"10"	"10"	"10"	"11"
STM-4 / OC 12		40,134194	"01"	"10"	"01"	"11"
STM-16 / OC 48		40,134194	"11"	"10"	"11"	"11"
GE		40,322581	"00"	"10"	"00"	"11"
STM-1 / OC 3	32/31 on transmitting side and receiving side	40,134194	"10"	"11"	"10"	"11"
STM-4 / OC 12		40,134194	"01"	"11"	"01"	"11"
STM-16 / OC 48		40,134194	"11"	"11"	"11"	"11"
GE		40,322581	"00"	"11"	"00"	"11"

Table 1: Valid combinations of VCXO centre frequency and clock generator divider settings for the transponder system shown on Figure 1.

Note on reading the table.

For the explanation below please refer to Figure 22.

Standard bit rates is understood as STM-1 / OC3, STM-4 / OC12, STM-16 / OC48 and Gigabit Ethernet (1.25 Gbit/s)

Reading the table is illustrated by the following example. Consider the wrap fraction 15/14. In this case the system must be equipped with two VCXOs. The first VCXO centre frequency equals 44,434286 MHz (SDH/SONET traffic) and the second VCXO centre frequency equals 44,642857 MHz (GE traffic). When the system receives and transmits data at standard bit rates the system settings is read from the row "Standard bit rates with programmable 15/14 overhead". If the system receives data at rates increased by 15/14 and transmits data at standard bit rates the system settings is read from the row "15/14 on receiving side". If the system receives standard bit rates and transmits data at a rate increased by 15/14 the system settings is read from the row 15/14 on transmitting side. Finally, if the system receives and transmits at data rates increased by 15/14 the system settings are read from the row "15/14 on transmitting side and receiving side".

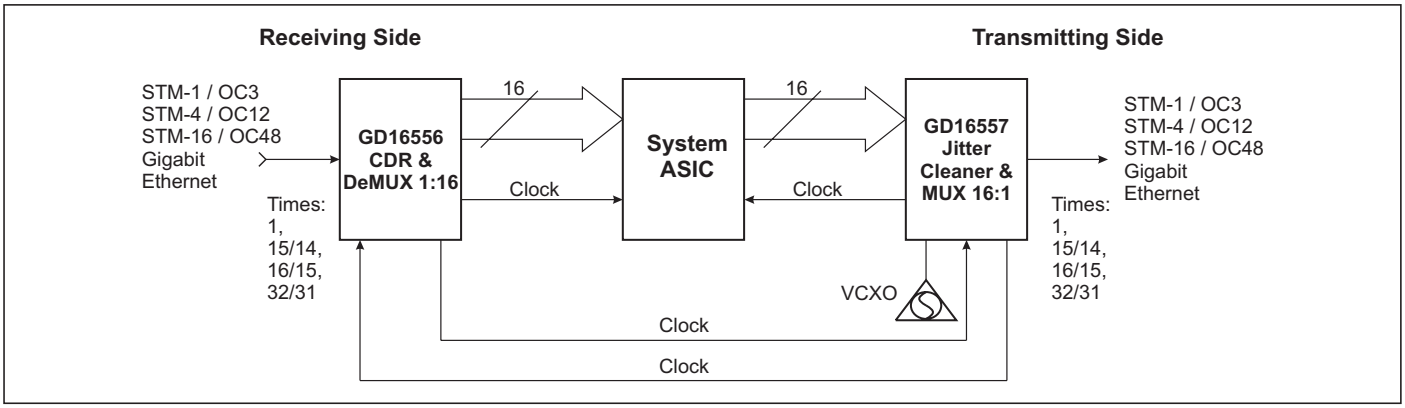


Figure 22.*Definition of receiving and transmitting side with respect to Table 1.*

Pin List GD16556 - Receiver (continued on next page)

Mnemonic:	Pin No.:	Pin Type:	Description:
DI, DIN	16, 14	ANALOG input	Differential AC or DC coupled data inputs to the Limiting Amplifier. Pins DI/DIN may be swapped with pins DIREF/DIREFN respectively.
DIREF, DIREFN	17, 13	Termination	Termination for DI and DIN. Refer to Figure 12 and 13 for termination.
BP, BPN	8, 7	CML output	Differential. CDR bypass data output. Terminated with 50 Ω to VDD on-chip.
BPEN	20	LVTTL input	Enables CDR bypass data output when logic “0". The pin is supplied with a 16 kΩ pull-up resistor.
LB, LBN	69, 70	CML output	Differential. Loop-back data output. Terminated with 50 Ω to VDD on-chip.
LBCK, LBCKN	71, 72	CML output	Differential. Loop-back clock output. Terminated with 50 Ω to VDD on-chip.
LBEN	6	LVTTL input	Loop-back enable. This pin enables the loop-back clock and data outputs when logic ”0". The pin is supplied with a 16 kΩ pull-up resistor.
RSEL1, RSEL2	90, 91	LVTTL input	Rate select pins. The pins are supplied with a 16 kΩ pull-up resistor. RSEL1 RSEL2 1.250 Gbit/s 0 0 622 Mbit/s 0 1 155 Mbit/s 1 0 2.488 Gbit/s (default) 1 1
MSEL1, MSEL2	4, 5	LVTTL input	Select for 15/14, 16/15 and 32/31 overhead bit rates. These pins select the divide ratio tuning the on-chip VCO frequency. The pins are supplied with a 16 kΩ pull-up resistor. Divide by MSEL1 MSEL2 56 0 0 60 0 1 62 1 0 64 (default) 1 1 Refer to Table 1 on page 11 for configuration in transponder applic.
DO0 DO0N DO1 DO1N DO2 DO2N DO3 DO3N DO4 DO4N DO5 DO5N DO6 DO6N DO7 DO7N DO8 DO8N DO9 DO9N DO10 DO10N DO11 DO11N DO12 DO12N DO13 DO13N DO14 DO14N DO15 DO15N	67, 66 65, 64 63, 62 61, 60 59, 58 57, 56 55, 54 53, 52 49, 48 47, 46 45, 44 43, 42 41, 40 39, 38 37, 36 35, 34	LVDS output *.	Differential. Data output. The differential output impedance is 100 Ω. The LVDS output must be terminated with an 100 Ω impedance DC-path between the differential output.
CKO, CKON	74, 75	LVDS output *.	Differential. Recovered clock output. The differential output impedance is 100 Ω. The LVDS output must be terminated with an 100 Ω impedance DC-path between the differential output.
CKREFA, CKREFAN	87, 86	LVDS input *.	Differential. CDR reference clock. In transponder systems CKREFA or CKREFB should be connected to the output signal RECCK from the GD16557 device. The input impedance is 100 Ω differential. (100 Ω on-chip termination resistor).

Mnemonic:	Pin No.:	Pin Type:	Description:
CKREFB, CKREFBN	81, 80	LVDS input *.	Differential. CDR reference clock. In transponder systems CKREFA or CKREFB should be connected to the output signal RECCK from the GD16557 device. The input impedance is 100 Ω differential. (100 Ω on-chip termination resistor).
CKRSEL	83	LVTTL input	Reference input clock select pin. The pin is supplied with a 16 kΩ pull-up resistor. “1”: Selects CKREFA, CKREFAN “0”: Selects CKREFB, CKREFBN.
CDRSEL	73	LVTTL input	Lock-select for CDR setup. The pin is supplied with a 16 kΩ pull-up resistor. “0" selects Manual Phase Freq. detector “1" selects Auto-lock, 500 ppm (default)
TCK	95	LVPECL input	Leave open for normal operation. Only used at DC test.
SELTCK	94	LVTTL input	Test-clock select. Connect to VDD for normal operation. Only used for test purposes.
LD_SEL	23	LVTTL input	Select of count. “0” Double the time that LOCKDET remains high. “1” Normal mode (default).
SBER0, SBER1	21, 22	LVTTL input	BER select inputs. SBER0 SBER1 BER-level 0 0 0.5×10^{-3} 0 1 1×10^{-3} 1 0 2×10^{-3} 1 1 4×10^{-3}
LOCK	79	PCMOS output	A high level indicates that the PLL is locked to the incoming serial data. A low level indicates out of lock. When the GD16556 cannot acquire lock to the serial data this signal switches between ”0" and “1"
BC_DET	28	PCMOS output	Bit consecutive detect output (logic High).
LOS_DET	29	PCMOS output	Loss Of Signal detect (alarm = logic High) output.
LOCKDET	30	PCMOS output	Valid data loss detect (alarm) output. Asserted when the divided VCO frequency deviates more than 500 ppm from reference frequency, or BC_DET is asserted.
FCK, FCKN	77, 76	LVDS output *.	Differential. Forward reference clock for transmitter in transponder system. In transponder systems connect this pin to the input CKI on the GD16557 device. The differential output impedance is 100 Ω. The LVDS output must be terminated with an 100 Ω impedance DC-path between the differential output.
VCTL	99	ANALOG input	VCO control voltage pin.
OUCHP	92	PCMOS output	Charge pump output to be connected to loop-filter.
VDD	2, 9, 18, 25, 26, 27, 78, 84, 85, 89, 93	PWR	+3.3 V Positive power supply for core logic and I/O
VDDV	1	PWR	+3.3 V Positive supply for VCO. To be connected to the loop-filter.
VDDL	10, 11	PWR	+3.3 V Positive supply for Limiting Amplifier.
VDDO	33, 50, 68	PWR	+3.3 V Positive supply for Outputs.
VDDP	98	PWR	+3.3 V Positive supply for Charge Pump.
VEE	3, 19, 24, 31, 32, 51, 82, 88, 96	PWR	0 V Ground. The heat sink must be connected to VEE by a soldered connections.
VEEL	12, 15	PWR	0 V for Limiting Amplifier.
VEEP	97	PWR	0 V for Charge Pump.
VEEV	100	PWR	0 V Ground for VCO.
Heat sink			Connected to VEE by soldering.

Note: * indicates that the pin is available as **LVPECL I/O**. Please refer to LVPECL characteristics and Figures 6 and 7 .

End of GD16556 Pin List

Package Pinout - GD16556

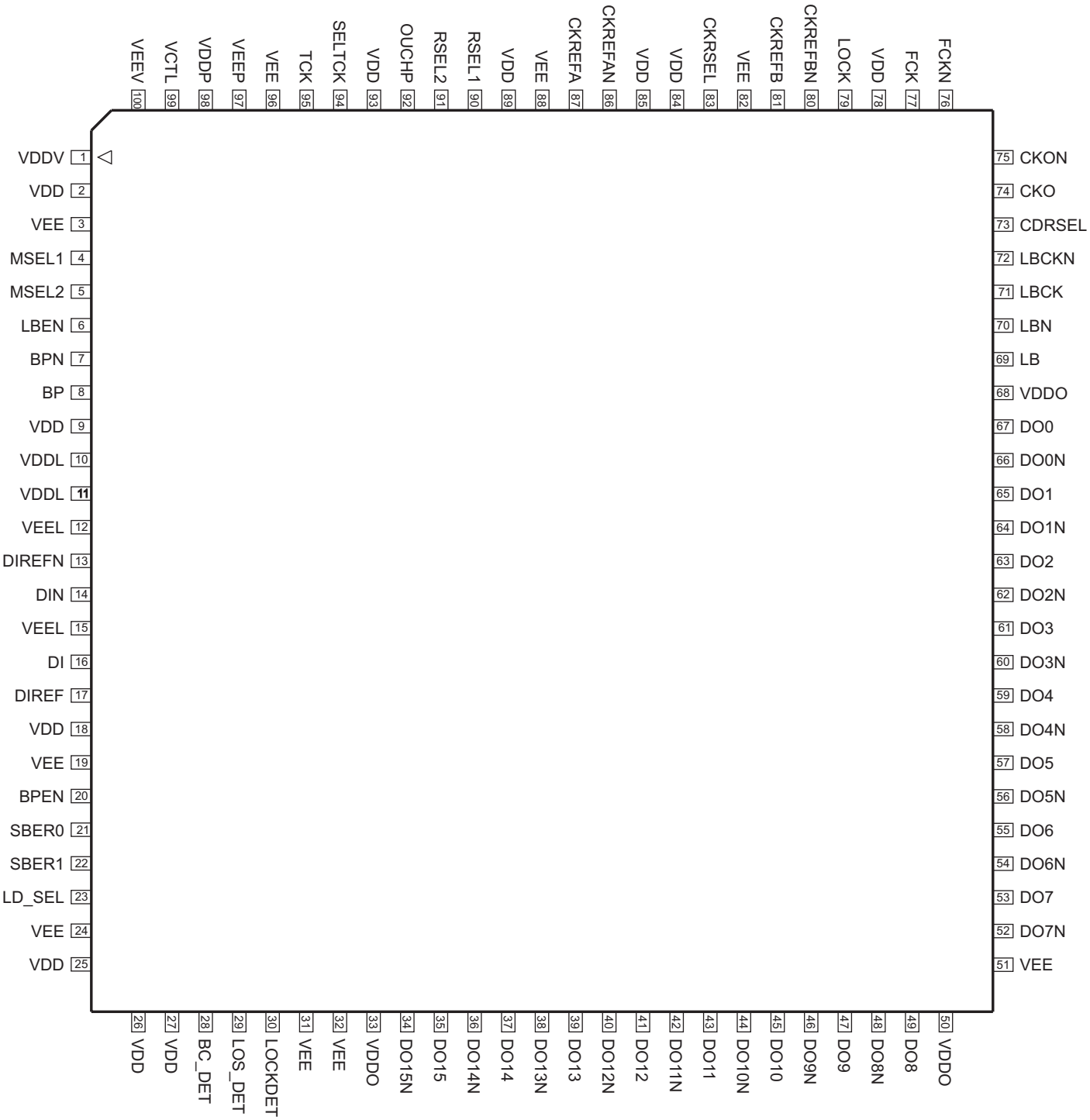


Figure 23.*Package pinout, 100 pin. Top view.*

Pin List GD16557 - Transmitter (continued on next page)

Mnemonic:	Pin no.:	Pin type:	Description:
DI0 DI0N DI1 DI1N DI2 DI2N DI3 DI3N DI4 DI4N DI5 DI5N DI6 DI6N DI7 DI7N DI8 DI8N DI9 DI9N DI10 DI10N DI11 DI11N DI12 DI12N DI13 DI13N DI14 DI14N DI15 DI15N	34, 35 36, 37 38, 39 40, 41 42, 43 44, 45 46, 47 48, 49 52, 53 54, 55 56, 57 58, 59 60, 61 62, 63 64, 65 66, 67	LVDS input *.	Differential data inputs. The input impedance is 100 Ω differential. (Terminated on-chip with 100 Ω resistor).
CKI, CKIN	75, 74	LVDS input. *.	Differential reference clock input. In transponder systems this input should be connected to the output FCK from the receiver device GD16556. The input impedance is 100 Ω differential. (Terminated on-chip with 100 Ω resistor).
XCK1, XCK1N XCK2, XCK2N	78, 77 83, 82	LVPECL input.	Differential clock input. To be used for VCXO clock.
VCXOSEL	85	LVTTL input.	VCXO select. ”1" (default) selects XCK1, XCK1N and “0" selects XCK2, XCK2N. The pin is supplied with a 16 kΩ pull-up resistor.
BP, BPN	17, 19	CML input.	Differential. When in bypass mode data is input through these pins. Terminated with 50 Ω to VCMLT1.
BPEN	2	LVTTL input.	Bypass enable. When logic ”0" then data is input from BN, BP. The pin is supplied with a 16 kΩ pull-up resistor. When this signal is logic “0” the VCO is disabled.
PHA1, PHA2	4, 5	LVTTL input.	Phase adjust. Adjusts the phase between the counter clock CNTCK and the input data. The pin is supplied with a 16 kΩ pull-up resistor. 0° PHA1=0 PHA2=0 180° PHA1=0 PHA2=1 90° PHA1=1 PHA2=0 270° (default) PHA1=1 PHA2=1
RSEL1, RSEL2	6, 7	LVTTL input.	Rate select pins. The pins are supplied with a 16 kΩ pull-up resistor. 1.250 Gbit/s RSEL1=0 RSEL2=0 622 Mbit/s RSEL1=0 RSEL2=1 155 Mbit/s RSEL1=1 RSEL2=0 2.488 Gbit/s (default) RSEL1=1 RSEL2=1
LB, LBN	27, 29	CML input	Differential. Data signal input for loop-back operation. Terminated with 50 Ω to VCMLT2.
LBEN	25	LVTTL input.	Loop-back select. When logic “0" then outputs DO, DON and CKO, CKON are fed from LB, LBN and LBCK, LBCKN. When this signal is logic “0” the VCO is disabled.
LBCK, LBCKN	21, 23	CML input.	Differential. Clock signal input for loop-back operation. Terminated with 50 Ω to VCMLT3.
VCK, VCKN	87, 86	LVPECL input.	Differential. External clock input for Phase Frequency Detector. To be used when operating without jitter-clean up (i.e. without double PLL).
VSEL	84	LVTTL input.	Input select for Phase Frequency Detector. The pin is supplied with a 16 kΩ pull-up resistor. “0" selects VCKI, VCKIN “1" (default) selects XCK1/XCK2

Mnemonic:	Pin no.:	Pin type:	Description:
VCTL	99	ANALOG input.	Voltage Control pin for VCO. Connect the VCO loop-filter to this pin.
VCXOCHAP	89	PCMOS output.	Connect the VCXO loop-filter to this pin. This output will source current when the VCXO increases the frequency and sink current when the VCXO decreases the frequency. Otherwise the output tristates (high impedance).
VCOCHAP	98	PCMOS output.	Charge Pump output for VCO. Connect the VCO loop-filter to this pin. The loop-filter should be terminated to VDDA. This output will sink current when the VCO increases the frequency and source current when the VCO decreases the frequency. Otherwise the output tristates (high impedance).
DO, DON	13, 15	CML output	Differential. High speed serial data output. Terminated with 50 Ω to VDD on-chip.
CKO, CKON	11, 9	CML output	Differential. High speed clock output. Terminated with 50 Ω to VDD on-chip.
CNTCK, CNTCKN	31, 32	LVDS output *	Differential. Counter clock for input data. Output impedance is 100 Ω differential. The LVDS output must be terminated with an 100 Ω impedance DC-path between the differential output.
RECCK, RECCKN	71, 70	LVDS output *	Differential. Reference clock output for CDR device GD16556. To be used in transponder systems only. In transponder systems connect this output to the GD16556 input CKREF. Output impedance is 100 Ω differential. The LVDS output must be terminated with an 100 Ω impedance DC-path between the differential output.
MSEL1, MSEL2	81, 80	LVTTL input	Select for 15/14, 16/15 and 32/31 overhead bit rates. These pins select the divide ratio tuning the on-chip VCO frequency. The pins are supplied with a 16 kΩ pull-up resistor. Divide by MSEL1 MSEL2 56 0 0 60 0 1 62 1 0 64 (default) 1 1 Refer to Table 1 on page 11 for configuration in transponder applic.
CKTST	96	LVPECL input	Test clock input. To be used for test purposes only.
TSTMODE	95	LVTTL input	Test mode select pin. To be used for test purposes only. The pin is supplied with a 16 kΩ pull-up resistor. A logic “0" selects test mode. When not connected the signal defaults to a logic ”1".
LOCK1, LOCK2	91, 93	PCMOS output	PLL lock-detect signals. LOCK1 monitors the VCXO based PLL and LOCK2 monitors the VCO based PLL. A logic “1" indicates no lock and a logic ”0" indicates lock. Connect these pins to a 10 nF capacitance.
LOCK1A, LOCK2A	90, 92	LVTTL output	Buffered lock detect signal.
VCMLT1 VCMLT2 VCMLT3	18 22 28	Termination	CML input termination pin. Connect these pins to the positive supply. Refer to Figure 9.
VDD	8, 10, 14, 20, 30, 33, 51, 69, 73, 76, 88, 94	PWR	+3.3 V Power supply for core and I/O
VDDA	100	PWR	+3.3 V Power supply for VCO. To be connected to the loop-filter.
VEE	3, 12, 16, 24, 26, 50, 68, 72, 79, 97	PWR	0 V Ground. The heat sink must be connected to VEE by a soldered connection.
VEEA	1	PWR	0 V Ground for VCO.
Heat sink			Connected to VEE by soldering.

Note: * indicates that the pin is available as **LVPECL I/O**. Please refer to LVPECL characteristics and Figures 6 and 7.

End of GD16557 Pin List.

Package Pinout - GD16557

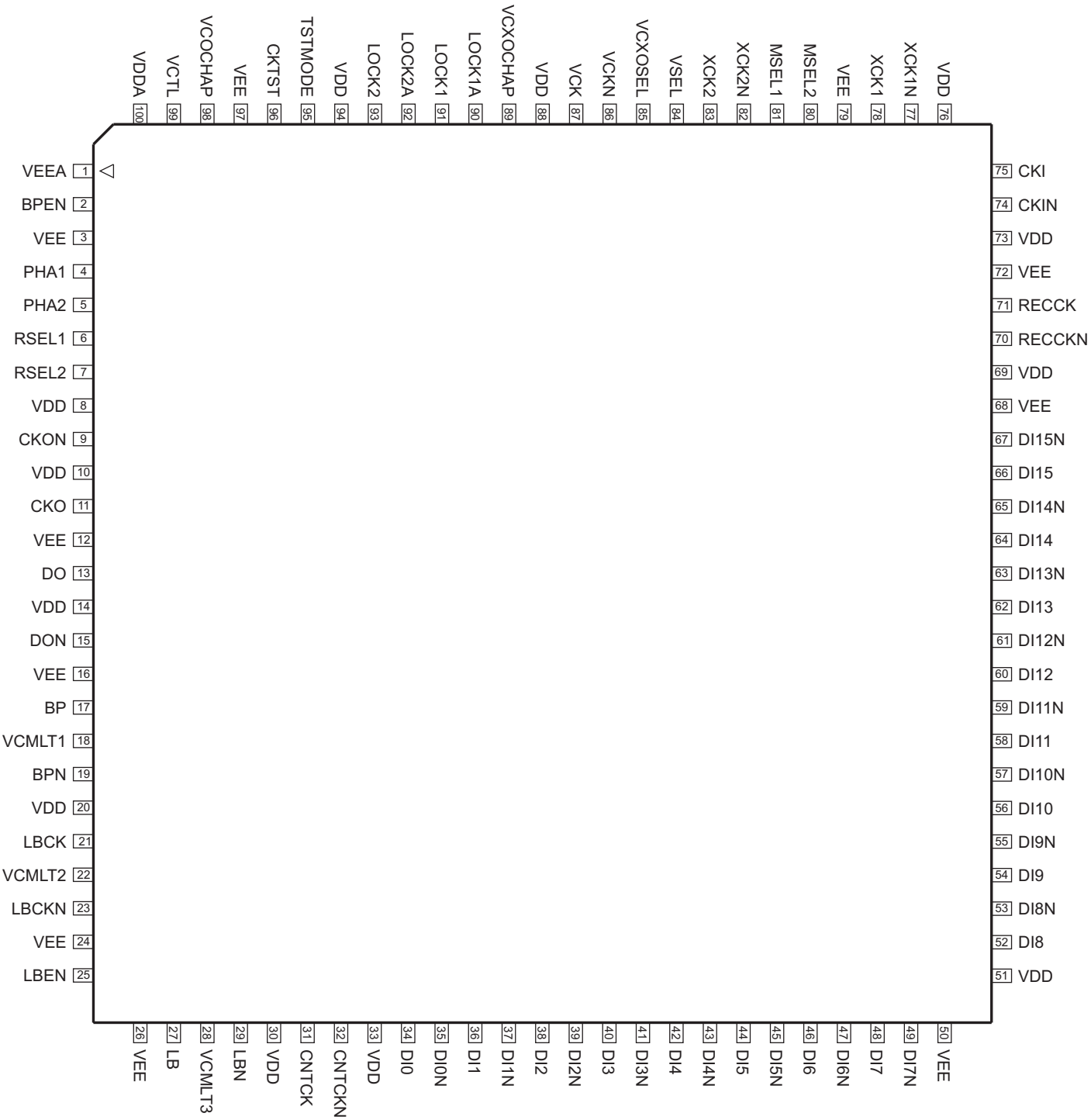


Figure 24.*Package Pinout, 100 pin. Top view.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table refer to $V_{EE.}$
All output signal currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$V_{DD,}$ V_{DDA}	Power supply		-0.5		6	V
V_I	Applied voltage (all inputs)		-0.5		V_{DD} +0.5	V
V_O	Applied voltage (all outputs)		-0.5		V_{DD} +0.5	V
$V_{IO\ ESD}$	Static Discharge Voltage	HBM, Note 1			500	V
		CDM, Note 2			50	V
$I_{I\ LVPECL}$	LVPECL input current		-1		1	mA
$I_{O\ LVPECL}$	LVPECL output source current				50	mA
$I_{O,\ LVDS}$	LVDS output current				25	mA
$I_{OO,\ LVTTL}$	LVTTL output source current				24	mA
$I_{OI,\ LVTTL}$	LVTTL output sink current				-24	mA
$I_{O,\ PCMOS}$	Charge pump output source and sink current		-250		250	μA
T_O	Operating temperature	Junction	-40		+125	°C
T_S	Storage temperature		-65		+125	°C

Note 1: Human Body Model: MIL 883D 3015.7 standard.
Note 2: Charge Device Model.: JESD2-C101 standard.

Thermal Characteristics

The heatsink must soldered to the board. In this case the junction to case thermal resistance is worst case 20°C / W (two layer board, low conductivity). The junction temperature is not to exceed 125°C.

DC Chararacteristics

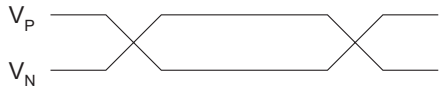
T_{CASE} = -5 °C to +75 °C (For /ECL version T_{CASE} = -5 °C to +90 °C).
All voltages in the table are referred to V_{EE} .
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Common

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply voltage		+3.1	+3.3	+3.5	V
V_{DD}	Supply voltage (only valid for /ECL version)		+3.1	+3.3	+3.6	V
$I_{DD,GD16556}$	Supply current GD16556	Note 1		390		mA
$I_{DD,GD16557}$	Supply current GD16557	Note 1		390		mA
$P_{GD16556}$	Power dissipation GD16556	Note 1		1.3		W
$P_{GD16557}$	Power dissipation GD16557	Note 1		1.3		W
$V_{ICM, LVPECL}$	LVPECL input common mode voltage		V_{DD} -1.5		V_{DD} -1.1	V
$V_{ODIFF, LVPECL}$	LVPECL input differential voltage		0.250		1.3	V
$V_{IH, LVTTL}$	LVTTL input HI voltage	Note 3, 4	2.0		V_{DD}	V
$V_{IL, LVTTL}$	LVTTL input LO voltage	Note 3, 4	0.0		0.8	V
$I_{IH, LVTTL}$	LVTTL input HI current	Note 3, 4			200	µA
$I_{IL, LVTTL}$	LVTTL input LO current	Note 3, 4	-500			µA
$V_{OH, LVTTL}$	LVTTL output HI voltage	I_{OH} = 3 mA, Note 4	2.1			V
$V_{OL, LVTTL}$	LVTTL output LO voltage	I_{OL} = -1 mA, Note 4	0		0.5	V
I_{VCTL}	VCTL leakage current	$V_{EE} < V_{VCTL} < V_{DD}$	-30			µA
$V_{ICM, LVDS}$	LVDS input common mode voltage	Note 4, 5	1.0		*2.1*	V
$V_{IDIFF, LVDS}$	LVDS input differential voltage	Note 4, 5	0.2		1.1	V
$I_{I, LVDS}$	LVDS input current	Note 4			16	mA
$V_{0CM, LVDS}$	LVDS output common mode voltage	Note 2, 4, 10		1.2		V
$V_{ODIFF, LVDS}$	LVDS output differential voltage	Note 2, 4, 10		300		mV
R_{LVDS}	LVDS input termination resistor		70		130	Ω
$V_{OH\ LVPECL}$	LVPECL output HI voltage		V_{DD} -1.02		V_{DD}-0.89	V
$V_{OL\ LVPECL}$	LVPECL output LO voltage		V_{DD}-2.00		V_{DD}-1.60	V
$V_{ODIFF,LVPECL}$	LVPECL differential output voltage	Note 7, 8, 9	0.6		1.3	V
$I_{OH, PCMOS}$	Charge pump output source current			100		µA
$I_{OL, PCMOS}$	Charge pump output sink current			-100		µA
$V_{OH, PCMOS}$	Charge pump output high saturation voltage (outputs VCOCHAP and VCXOCHAP)	Note 6		V_{DD}-0.3		V
$V_{OL, PCMOS}$	Charge pump output low saturation voltage (outputs VCOCHAP and VCXOCHAP)	Note 6		V_{EE} +0.3		V
$V_{OH, CML}$	CML HI voltage	Note 4		V_{DD}		V
$V_{OL, CML}$	CML LO voltage	Note 4		V_{DD} -0.5		V
$I_{OH, CML}$	CML HI current	Note 4		0		mA
$I_{OL, CML}$	CML LO current	Note 4		-20		mA
R_{CML}	CML input and output termination resistor	Note 4	35		65	Ω

Note 1: Supply currents are estimates based on advance studies. The maximum current consumed by GD16556 and GD16557 equals 1.3 times the typical value. Current delivered to external loads is not included in the power estimate.
Note 2: 100 Ω load.

Note 3: All LVTTL inputs are provided with an internal pull-up resistor R_{LVTTL} = 16 kΩ connected to V_{DD} giving a default logic “1" when not connected.
Note 4: Under the condition of typical supply voltage (3.3 V).
Note 5: The LVDS input is LVPECL compatible.
Note 6: Assuming a pure capacitive load.
Note 7: Definition of common mode voltage: $V_{CM} = (V_p + V_N)/2$.
Note 8: Definition of differential voltage: $V_{DIF} = V_P - V_N$



Note 9: R_{load} = 50 Ω to V_{DD} -2.0 V.
Note 10: A DC-path with impedance of 100 Ω must be provided between the differential outputs. Please refer to Figure 5.

AC Characteristics - General

T_{CASE} = -5 °C to +75 °C (For /ECL version T_{CASE} = -5 °C to +90 °C).

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$t_{R,\ LVDS}$	LVDS rise time	Note 1		500		ps
$t_{F,\ LVDS}$	LVDS fall time	Note 1		500		ps
$t_{R,\ LVPECL}$	LVPECL rise time	Note 3			450	ps
$t_{F,\ LVPECL}$	LVPECL fall time	Note 3			450	ps
$t_{R,\ LVTTL}$	LVTTL rise time	Note 2			1	ns
$t_{F,\ LVTTL}$	LVTTL fall time	Note 2			1	ns
F_{VCO}	VCO frequency				2.7	GHz
K_{VCO}	VCO gain constant			-250		MHz/V

Note 1: 20% - 80%, R_{LOAD} = 100 Ω.
Note 2: 20% - 80%, Z_{LOAD} = 10 pF. Rise and fall times are approximate 2 ns with 20 pF load.
Note 3: 20% - 80% differential.

AC Characteristics - GD16556

T_{CASE} = -5 °C to +75 °C (For /ECL version T_{CASE} = -5 °C to +90 °C).

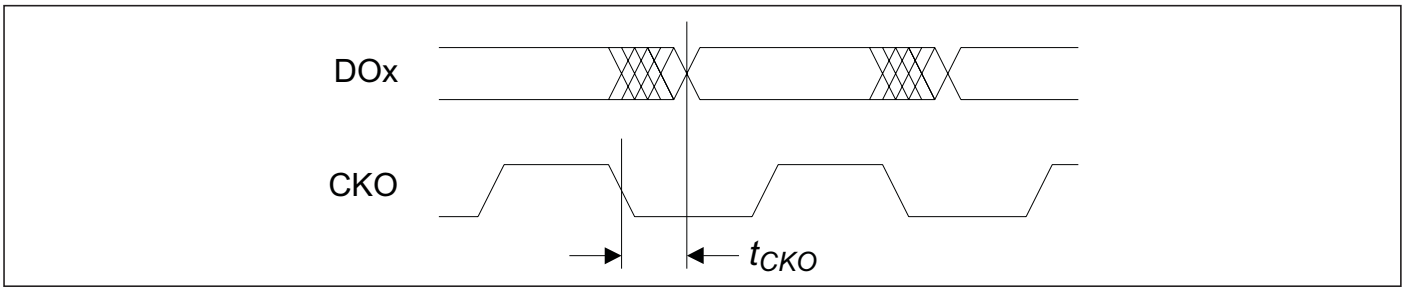


Figure 25.*Low-speed Output Timing.*

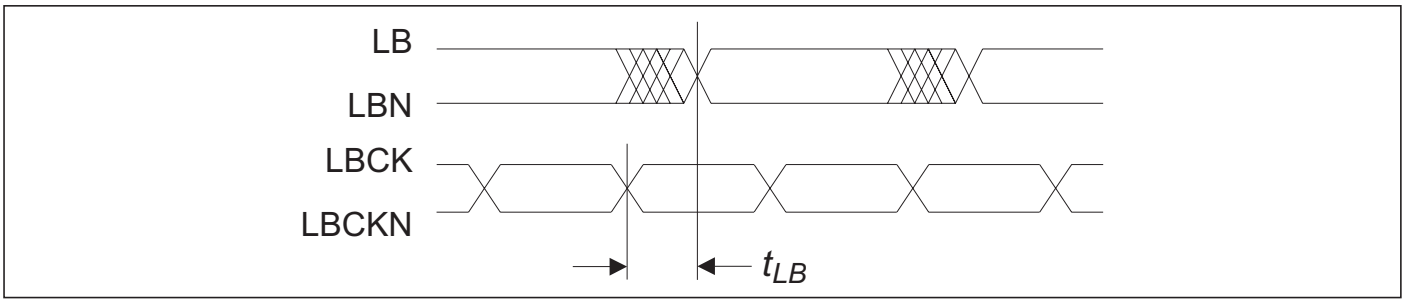


Figure 26.*Loop-back Timing.*

Symbol:	**Characteristic:**	**Conditions:**	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
$J_{TRANSFER}$	Jitter transfer	Note 1			0.1	dB
$J_{TRAN.\ Loop\text{-}back}$	Jitter transfer	@3R loop-back	Refer to Figure 27			
$J_{TOL.\ Loop\text{-}back}$	Jitter tolerance	@3R loop-back	Refer to Figure 28			
S_{LIA}	Linear Input Amplifier sensitivity (differential)	BER = 1E-10		5	8	mV
CID	Consecutive Identical Digits (Number of bits without transitions)			2000		
$t_{ACQUISITION}$	Acquisition time	Transition density=0.5		50		µs
t_{CKO}	Output phase delay		0	0.3	0.65	ns
t_{LB}	Loop-back output phase delay			84		ps
L_{LOS_DET}	LOS_DET low to high	BER above preset level			26	µs
	LOS_DET high to low	BER below preset level	131		316	µs
$F_{LBCK/N}$	Maximum frequency of LBCK, LBCKN		2.67	5		GHz
$F_{LB/N}$	Maximum frequency of LB, LBN		2.67	5		Gbit/s
$F_{BP/N}$	Maximum frequency of BP, BPN		3	5		Gbit/s

Note 1: This figure applies when the GD16556 is used in non-transponder systems. **In this type of application it may be necessary to adjust the loop-filter depending on the bit-rate to achieve the jitter-transfer and jitter tolerance** (This implies that true on-the-fly operation between bit-rates is not possible). The recommended loop-filter(s) is to be used. Customer input is required with respect to jitter-transfer in transponder systems.

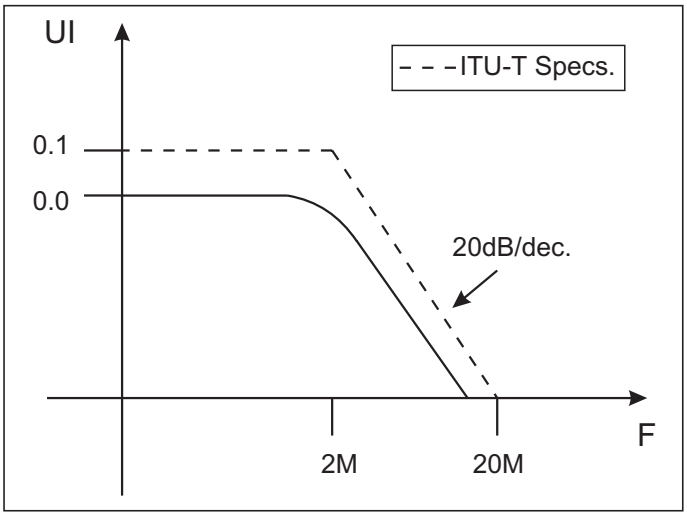


Figure 27.*Jitter Transfer*

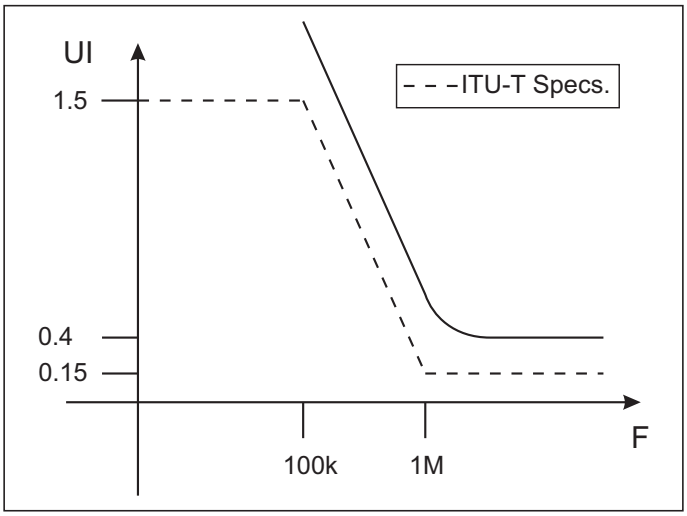


Figure 28.*Jitter Tolerance with 2 dB Power Penalty @ BER = 1E-10*

AC Characteristics - GD16557

T_{CASE} = -5 °C to +75 °C (For /ECL version T_{CASE} = -5 °C to +90 °C).

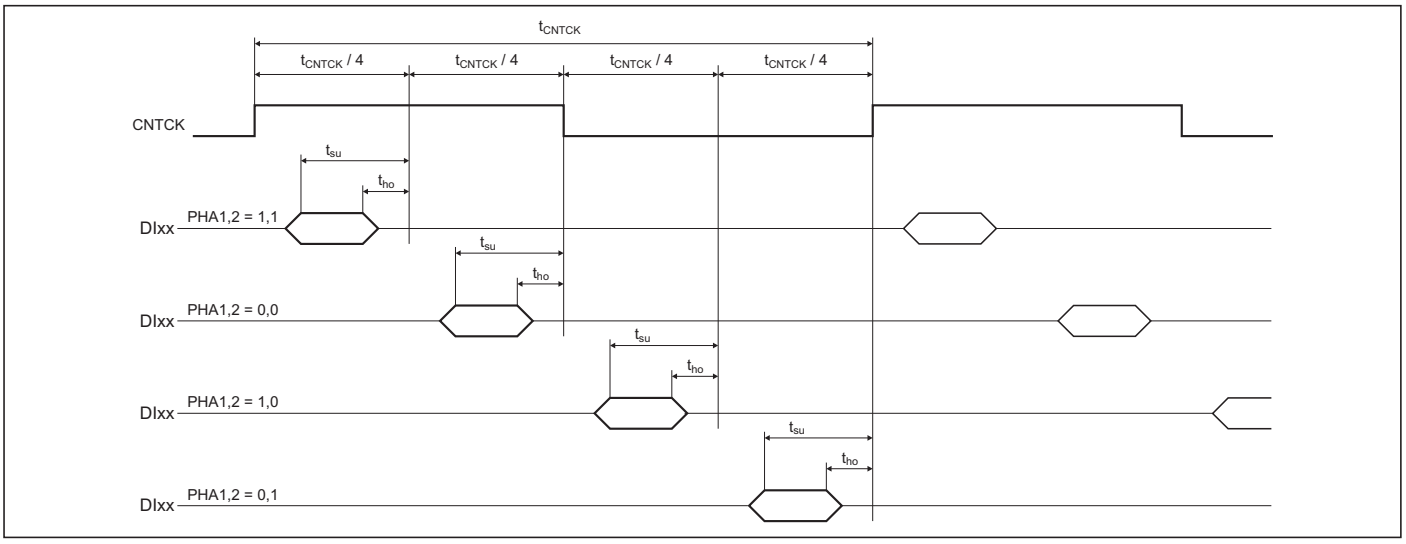


Figure 29.*Low-speed input timing.*

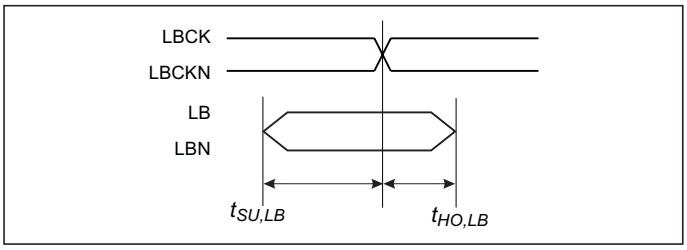


Figure 30.*Loop-back timing.*

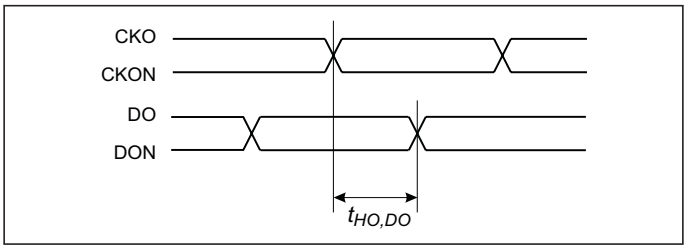
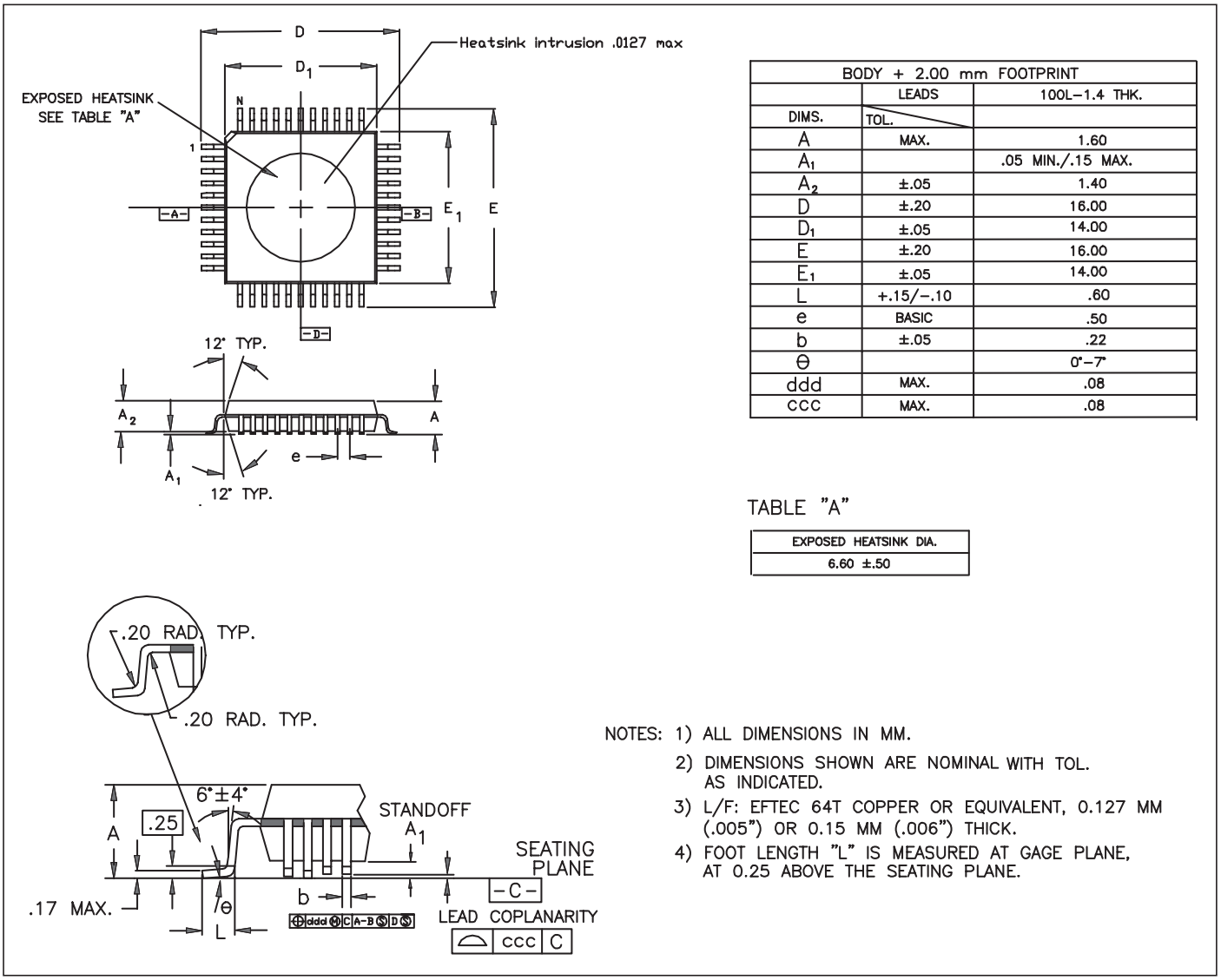


Figure 31.*High-speed clock/data timing*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
t_{SU}	DIx setup time			2000		ps
t_{HO}	DIx hold time			500		ps
$t_{HO,DO}$	High-speed data hold time		30	50	80	ps
$t_{SU,LB}$	Loop-back input setup time		50	30		ps
$t_{HO,LB}$	Loop-back input hold time			30		ps
t_{BP}	Bypass propagation delay			250	400	ps
$J_{GENERATION}$	Jitter generation			5	8	mUI_{RMS}
$J_{TRANSFER}$	Jitter transfer				0.1	dB
$F_{CKO/N}$	Maximum frequency of CKO, CKON		2.67			GHz
$F_{DO/N}$	Maximum frequency of DO, DON		2.67			Gbit/s
$F_{LBCK/N}$	Maximum frequency of LBCK, LBCKN		2.67	5		GHz
$F_{LB/N}$	Maximum frequency of LB, LBN		2.67	5		Gbit/s
$F_{BP/N}$	Maximum frequency of BP, BPN		3	5		Gbit/s
$R_{DUTY-CYCLE}$	Reference clock duty cycle (signals VCK/XCK1/XCK2/CKI)			50/50		%
$t_{LOCK1A/2A}$	Lock detect acquisition time (signals LOCK1A and LOCK2A)			200		µs

Package Outline



BODY + 2.00 mm FOOTPRINT		
	LEADS	100L–1.4 THK.
DIMS. / TOL.		
A	MAX.	1.60
A_1		.05 MIN./.15 MAX.
A_2	±.05	1.40
D	±.20	16.00
D_1	±.05	14.00
E	±.20	16.00
E_1	±.05	14.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

TABLE "A"

EXPOSED HEATSINK DIA.
6.60 ±.50

NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

Figure 32.*100 pin TQFP-EDQUAD. All dimensions are in mm.*

Device Marking

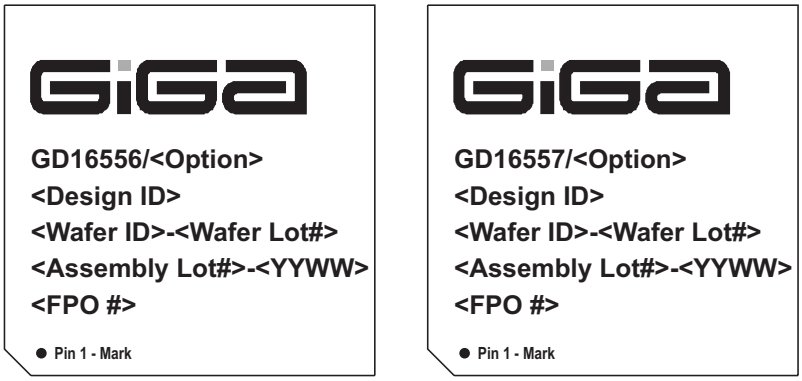


Figure 33.*Device marking. Top view.*

External References

ITU-T G.825 (3/93) : The control of jitter and wander within digital networks based on SDH.
ITU-T G.958 (11/94) : Digital line system based on the SDH for use on optical fibre channels.
MIL Std.883 (3/89) : Method 3015, Human Body Model.

Ordering Information

To order, please specify as shown below.

Product Name:	Description:	Package:	Case Temperature Range:
GD16556-100BA	Receiver with LVDS I/O	100 pin TQFP-EDQUAD	-5...+75 °C
GD16556/ECL-100BA	Receiver with LVPECL I/O	100 pin TQFP-EDQUAD	-5...+90 °C
GD16557-100BA	Transmitter with LVDS I/O	100 pin TQFP-EDQUAD	-5...+75 °C
GD16557/ECL-100BA	Transmitter with LVPECL I/O	100 pin TQFP-EDQUAD	-5...+90 °C

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