SIEMENS

ICs for Communications

Multipoint Switching and Conferencing Unit - Attenuation MUSAC-A

PEB 2445 Version 1.2

Data Sheet 02.96

PEB 2445 **Revision History:**		**Current Version: 02.96**
Previous Version: Digital Switching and Conferencing IC's Data Book 01.94		
Page (in Version 01.94)	Page (in new Version)	Subjects (major changes since last revision)
220	11	Version 1.2
220	11	P-DIP-40 package not further available
224, 227, 243	16, 19, 36	Motorola Mode not available
249	40	Figure (Initializing the … 4096-kHz Device Clock) corrected
–	56	Abs. Max. Ratings: I_{LPD} defintion
	59	$t_{WD\ min.}$ = 20 ns
	59	$t_{s\ min.}$ = 15 ns
	60	$t_{SS8\ min.}$ = 20 ns, $t_{SH4\ max.} = t_{CP4} - 10\ ns + t_{CP4H}$
–	60	$t_{SPL\ min.}$ = 100 ns added
–	66	Appendix: Design sheets added

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1 Overview

A Complete Family of Efficient Solutions

If the issue is digital switching and conferencing, the solution is flexibility, capacity, and economy.

Siemens Semiconductor offers the most economical answer to all conceivable applications in this field. Our complete family of switching network devices satisfies even the most rigorous switching demands.

A Complete Family of Efficient Solutions

Take our **MTSC (Memory Time Switch CMOS) PEB 2045** with a switching capability of 512 incoming PCM channels to 256 outgoing PCM channels. It has the perfect size to economically build medium sized switches. The design of a non-blocking switch for 512 PCM channels is possible with a simple parallel configuration with a second MTSC.

If you need a non-blocking switch for up to 256 channels, we offer a smaller version of the MTSC, the **MTSS (Memory Time Switch Small) PEB 2046**. And the **MTSL (Memory Time Switch Large) PEB 2047**, the largest in our family, is capable of switching 1024 PCM channels.

Siemens also supplies the best solution for conferencing, our **MUSAC (Multipoint Switching and Conferencing Unit) PEB 2245** performs the complete switching functions of the MTSC, and offers a signal processor for handling up to 64 conferencing channels in any combination. The input and output channels can also be attenuated individually to achieve best transmission quality.

The **MUSAC-A (Multipoint Switching and Conferencing Unit) PEB 2445** is an upward compatible device to the MTSC and MUSAC. It offers in addition the attenuation and amplification of every time slot.

Pin compatible device allow simplicity in hardware and software design. To allow for more flexibility, the PCM data rate can be 2, 4, or 8 Mbit/s – configurable also for mixed use.

The figure below shows the general architecture of a digital exchange.

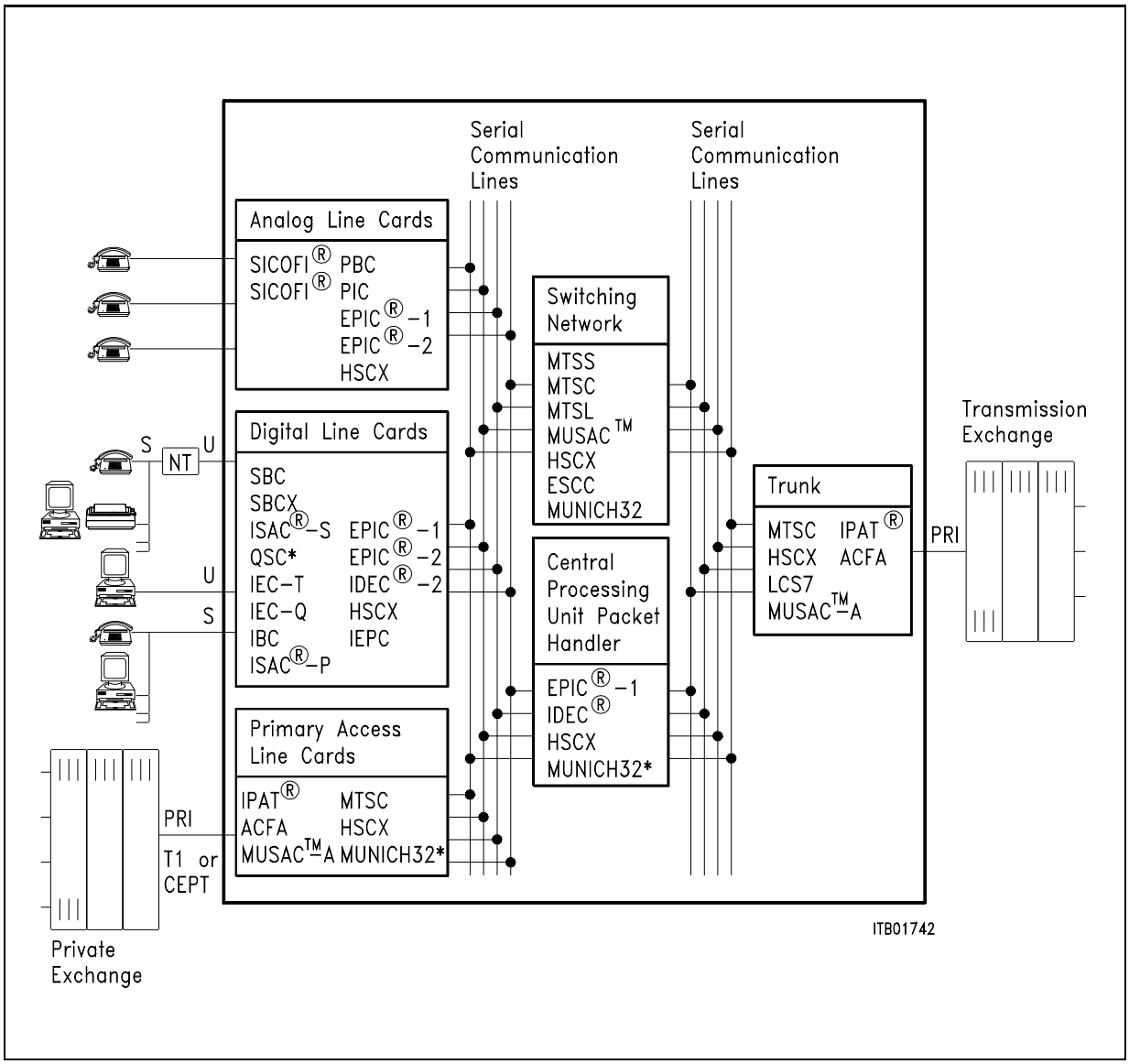


Figure 1
General Exchange Architecture

System Background

Digital exchanges put calls through by newly arranging the speech signals coded with 8-bit words (PCM time-slots). The code words are transmitted serially on PCM lines. The sampling frequency of 8 kHz produces PCM frames with a duration of 125 µs. The transmission rate on the line determines how many code words (speech channels) can be accommodated within a sampling period. With a data rate of 2048 kbit/s for example, there are 32 time-slots of 8 bits each. 4 lines with a data rate of 8192 kbit/s have a transmission capacity of 512 channels.

Overview

An overview on the complete switching and conferencing IC-family is shown in the following table:

Table 1
Complete Switching and Conferencing IC Family

	MTSC PEB 2045	MTSS PEB 2046	MTSL PEB 2047	MTSL 16 PEB 2047-16	MUSAC PEB 2245	MUSAC-A PEB 2445	EPIC-1 PEB 2055	EPIC-S PEB 2054
Switching capacity (time-slots)	512 × 256	256 × 256	1024 × 512	1024 × 1024	512 × 256	512 × 256	256 × 256	256 × 256
Input/output lines	‘16/8	‘8/8	‘16/8	‘16/8	‘16/8	‘16/8	‘8/8 SLD/IOM/ PCM	‘6/6 IOM/PCM
PCM-data rate (Mbit/s)	2/4/8 + mixed mode	2	2/4/8 + mixed mode	2/4/8/16 + mixed mode	2/4/8 + mixed mode	2/4/8 + mixed mode	up to 8	up to 8
Clock rate (MHz)	4.096 8.192	4.096 8.192	4.096 8.192	4.096/8.192 16.384	4.096 8.192	4.096 8.192	up to 8.192	up to 8.192
Conferencing					64 channels	64 channels		
Attenuation					64 channels 3/6/9 dB	all channels – 4 to 12 dB		
PRI/T1 mode	yes				yes	yes		
Fractional T1 data bundling			yes	yes			128-Kbit/s channel	128-Kbit/s channel
µC access			read	read			yes	yes
Multipoint switching					yes	yes		
Power (mW) max. consumption typ	50	50	100	170	100	100	50	50
Package	P-DIP-40 P-LCC-44	P-DIP-40 P-LCC-44	P-LCC-44	P-LCC-44	P-LCC-44	P-LCC-44	P-LCC-44	P-LCC-44

[1] in definition

Conferencing

An important task in PCM voice handling is conferencing. I.e. several subscribers of a digital PBX system would like to arrange a conference call. This task will be done in the central switching network. Modern switching IC like the MUSAC-A fulfill this important task in a cost effective way in the central switching unit. A powerful on chip Digital Signaling Processor handles this requirement.

Definite time-slots will be added together to one subscriber signal. In order to ensure an acceptable speech quality and reduce of echo and ‘singing’ problems, the input and output channels have to be attenuated individually. Additionally, input signals below a threshold programmable to different levels are disregarded. Another trick to lessen the risk of instability in multiparty conferences is to invert every second voice channel. Odd and even channels are substracted from one other.

Conferencing with the MUSAC™-A

Conferencing means that PCM data of several subscribers are processed such that each subscriber receives the contribution of the PCM data transmitted by all participants of the conference. Except the data transmitted by himself.

Each subscriber is qualified by an input channel which corresponds to a certain input line and time-slot of the MUSAC-A, and an output channel which corresponds to a certain output line and time-slot of the MUSAC-A.

The data flow through the MUSAC-A in case of conferencing is illustrated in **figure 2**.

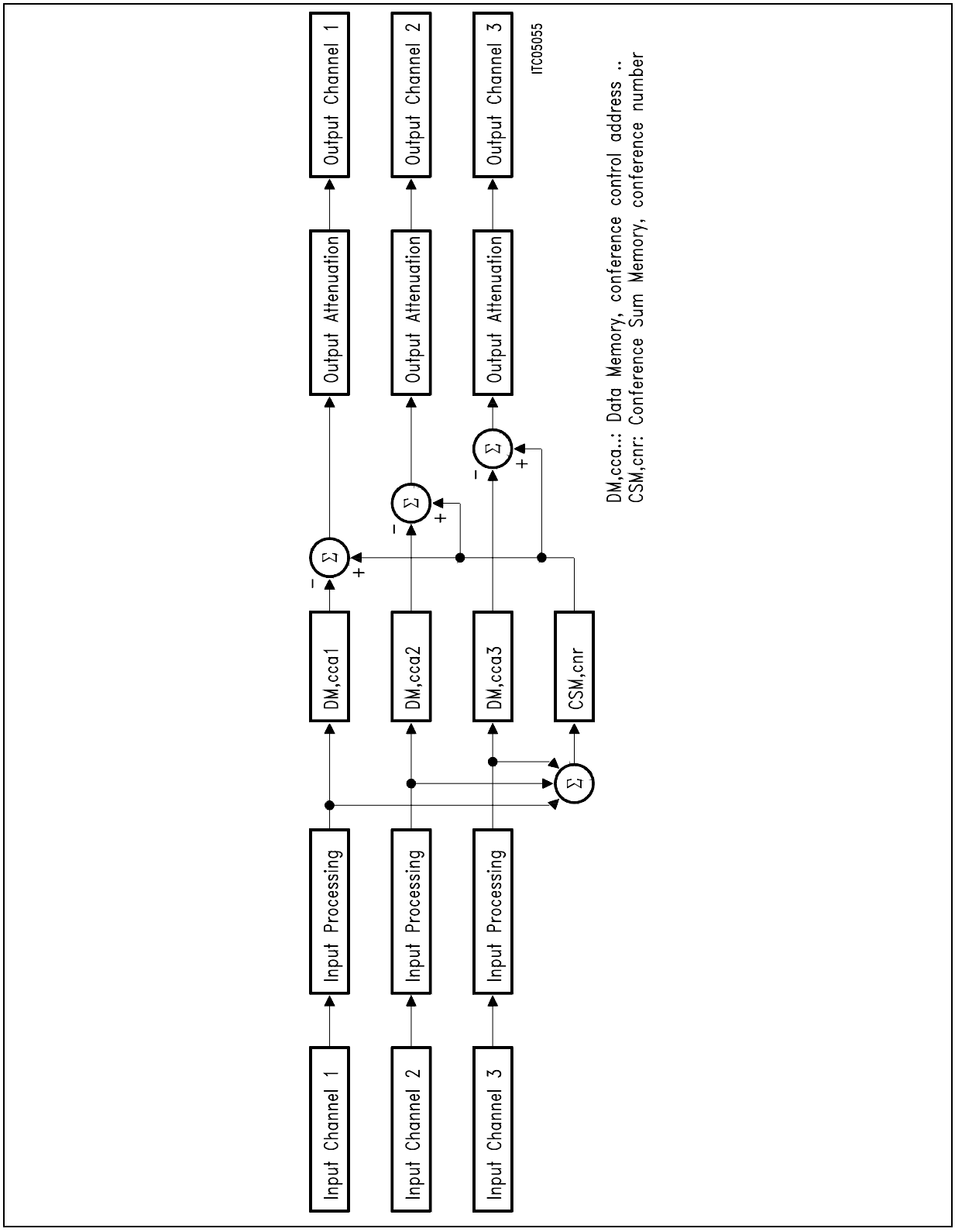


Figure 2
Data Flow through the MUSAC-A in Case of Conferencing

The PCM samples of each input channel first pass through an input processing stage. In this stage, an input attenuation level (0, 3, 6 or 9 dB) and a noise suppression threshold can be programmed individually for each channel. Following the input processing the PCM data is expanded according to the A- or μ-law encoding rules and written to the Data Memory (DM). Additionally the PCM data of each input channel is added to the Conference Sum Memory (CSM). The DM location (1 out of 64) is specified by the Conference Control Address (CCA) and the CSM location (1 out of 21) is specified by the conference number when writing to the Conference Control Memory (CCM).

The PCM data then passes through a substractor stage such that the resulting output channel for a given subscriber contains the contribution of all the other channels in the conference except its own. Finally the PCM data is forwarded to the output channel after PCM compression and an optional output attenuation of 3 dB.

Attenuation

Attenuation is a new requirement for PBX switching systems. The purpose is to avoid echo and noise problems on a PBX network for voice connections with access to the public network. Further a certain loudness rating on a definite point for different terminals and phones could be fixed (see **figure 3**).

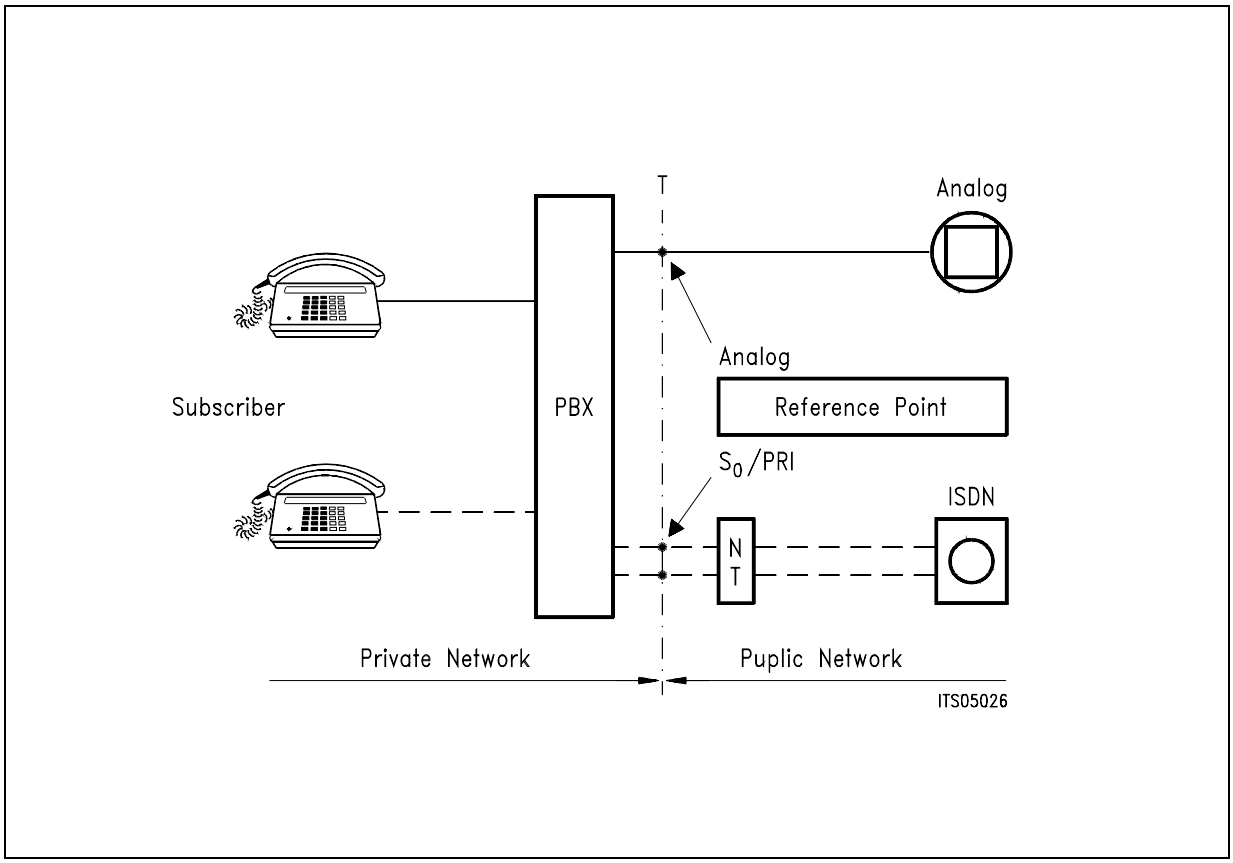


Figure 3

SIEMENS

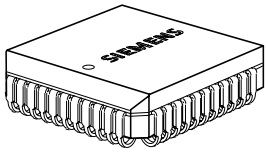
Multipoint Switching and Conferencing Unit - Attenuation
MUSAC™-A

PEB 2445

Version 1.2

CMOS IC

1.1 Features



P-LCC-44

Switching

- Time/space switch for 2048-, 4096- or 8192-kbit/s PCM systems
- Switching of up to 512 incoming PCM channels to up to 256 outgoing PCM channels
- 16 input and 8 output PCM lines
- Different kinds of modes (2048, 4096, 8192 kbit/s or mixed mode)
- Configurable for a 4096- and 8192-kHz device clock
- Tristate function for further expansion and tandem operation

Attenuation and Amplification

- Attenuation and amplification of every time-slot
- Attenuation range from 0 to 12 dB
- Amplification range from 0 to 4 dB

Type	Version	Ordering Code	Package
PEB 2445-N	V1.2	Q67100-H6298	P-LCC-44 (SMD)

Conference Mode

- Up to 64 conference channels in any combination
- Up to 21 independent conferences simultaneously (3 subscribers)
- Programmable attenuation (0/3/6/9 dB) on each input channel
- Programmable attenuation (0/3 dB) on each output channel
- Programmable PCM-level adaption (attenuation or amplification) of up to 64 channels
- Programmable noise suppression (four thresholds)
- Conference overflow handling
- Tone insertion capability
- A-law / µ-law compatible
- Compatible with all kinds of PCM-byte formats

Multipoint Switching

- Multiple independent LAN's within one PBX
- Multiplexing of up to 64 channels
- 64-kbit/s channels

General

- 8-bit µP interface
- Single + 5 V power supply
- Advanced low power CMOS technology
- TTL-compatible inputs/outputs
- Upward compatible to MTSC and MUSAC

General Description

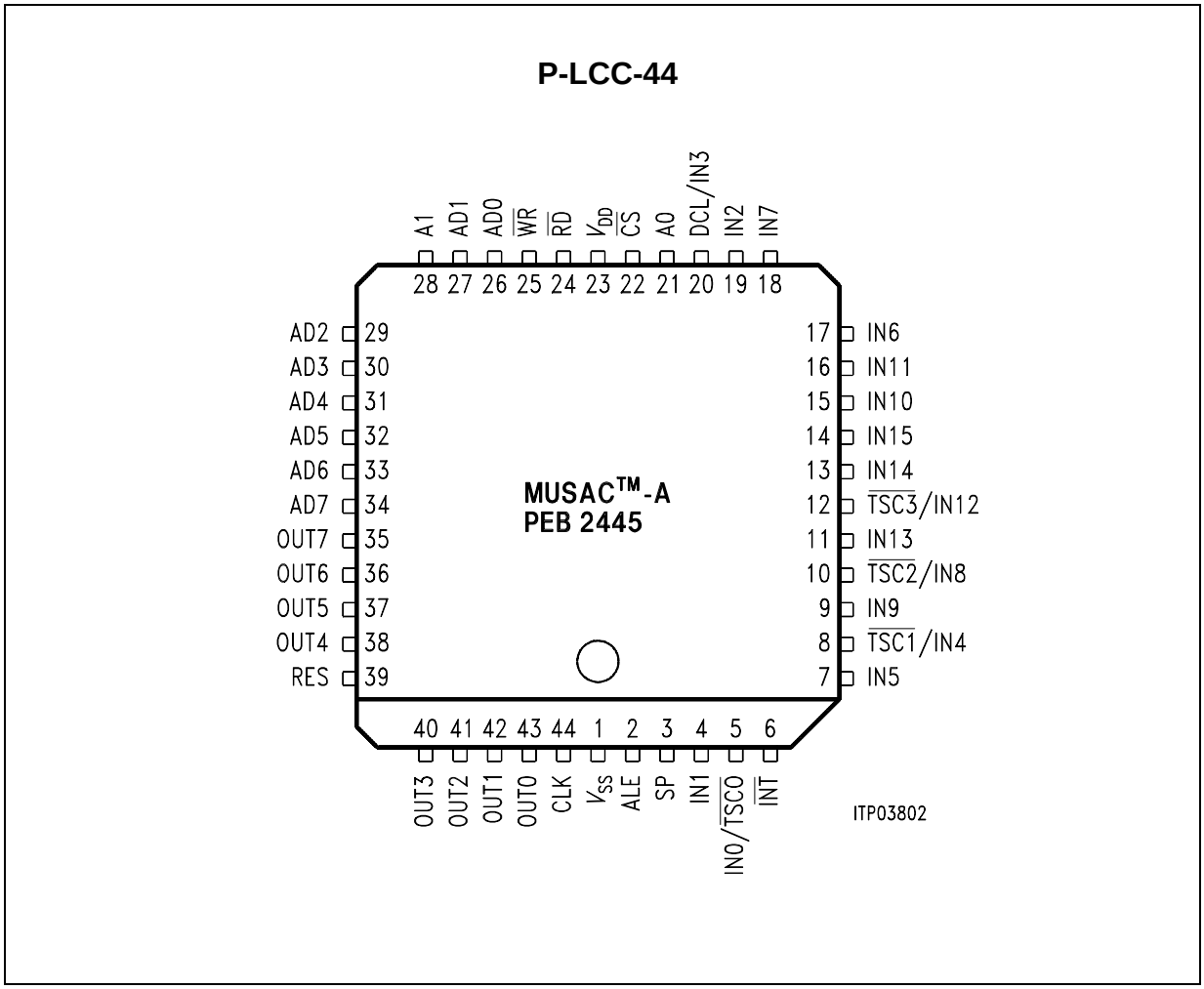
The MUSAC-A is an upward compatible device to the reliable components MTSC and MUSAC. Additionally to the standard MUSAC features switching and conferencing, the MUSAC-A supports enlarged attenuation functions.

Every time-slot is freely programmable in 1-dB step resolutions to an attenuation range from 0 to 12 dB and amplified from 0 to 4 dB.

With enlarged attenuation functions to every time-slot the MUSAC-A fulfills the ability for new requirements. I.e. different PBX terminals could be adapted to a certain reference point from the private network to the public network.

1.2 Pin Configuration

(top view)



1.3 Pin Definitions and Functions

Pin No. P-LCC	Symbol	Input (I) Output (O)	Function
1	V_{SS}	I	Ground (0 V)
6	$\overline{INT}$	OD open drain	**Interrupt Request:** The signal is activated when a conference overflow is detected. The microprocessor may determine the specific conference in overflow by reading the conference status register (CST). The interrupt is maskable. $\overline{INT}$ is an open drain output, thus a 'wired-or' combination of interrupt request outputs of several MUSAC-As is possible (a pull up resistor is necessary).
3	SP	I	**Synchronization Pulse:** The MUSAC-A is synchronized relative to the PCM system via this line.
4 7 9 11 13 14 15 16 17 18 19	IN1 IN5 IN9 IN13 IN14 IN15 IN10 IN11 IN6 IN7 IN2	I I I I I I I I I I I	**PCM-Input Ports:** Serial data is received at these lines at standard TTL levels.
5 8 10 12	IN0/$\overline{TSC0}$ IN4/$\overline{TSC1}$ IN8/$\overline{TSC2}$ IN12/$\overline{TSC3}$	I/O I/O I/O I/O	**PCM-Input Port / Tristate Control:** In standard configuration these pins are used as input lines, in primary access configuration they supply control signals for external devices.
20	IN3/DCL	I/O	**PCM-Input Port / Data Clock:** In standard configuration IN3 is the PCM-input line 3, in primary access configuration it provides a 2048-kHz data clock for the synchronous interface.
21 28	A0 A1	I I	**Address for Direct Register Access:** These pins are only active if a demultiplexed µP-interface mode is selected. If A1 is not connected it will be set to ground internally.

1.3 Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Symbol	Input (I) Output (O)	Function
22	$\overline{CS}$	I	**Chip Select:** A low level selects the MUSAC-A for a register access operation.
23	V_{DD}	I	**Supply Voltage:** 5 V ± 5 %
24	$\overline{RD}$	I	**Read:** This signal indicates a read operation and is internally sampled only if $\overline{CS}$ is active. The MUSAC-A puts data from the selected internal register on the data bus with the falling edge of $\overline{RD}$. $\overline{RD}$ is active low (Siemens/Intel bus mode).
25	$\overline{WR}$	I	**Write:** This signal initiates a write operation. The $\overline{WR}$ input is internally sampled only if $\overline{CS}$ is active. In this case the MUSAC-A loads an internal register with data from the data bus at the rising edge of $\overline{WR}$. $\overline{WR}$ is active low (Siemens/Intel bus mode).
2	ALE	I	**Address Latch Enable:** In the Intel type multiplexed µP-interface mode a logical high on this line indicates an address of a MUSAC-A internal register on the external address/data bus. In the Intel type demultiplexed. µP-interface mode this line is hardwired to V_{SS}, in the demultiplexed Motorola type µP-interface mode it should be connected to V_{DD}. If ALE is not connected it will be set to ground internally.
26 27 29 30 31 32 33 34	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus:** If the multiplexed address/data µP-interface bus mode is selected these pins transfer data and addresses between the µP and the MUSAC-A. If a demultiplexed mode is used, these bits interface with the system data bus.

1.3 Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Symbol	Input (I) Output (O)	Function
35 36 37 38 40 41 42 43	OUT7 OUT6 OUT5 OUT4 OUT3 OUT2 OUT1 OUT0	O O O O O O O O	**PCM-Output Port:** Serial data is sent by these lines at standard CMOS- or TTL levels. These pins can be tristated.
39	RES	I	**Reset:** A high signal on this input forces the MUSAC-A into reset state. The minimum pulse length is four clock periods. If this pin is not connected it will be set to ground internally.
44	CLK	I	**Clock:** 4096- or 8192-kHz device clock

1.4 Functional Symbols

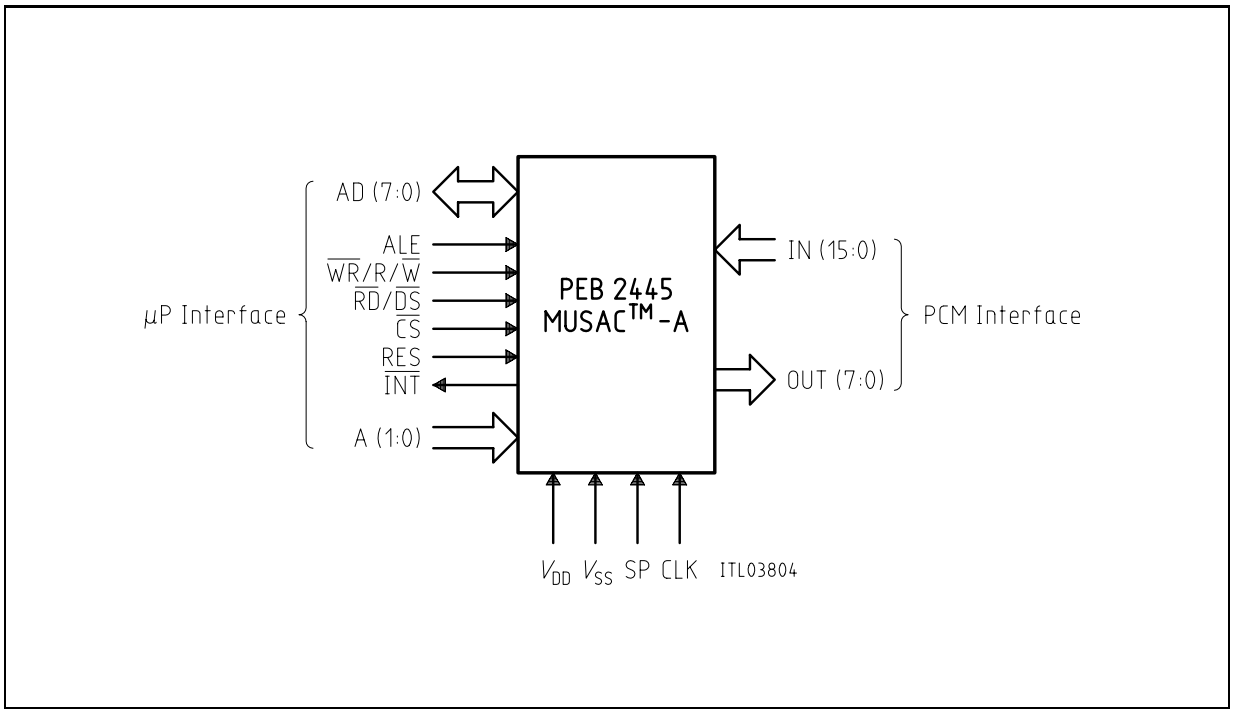


Figure 4
Functional Symbol for the Standard Configuration

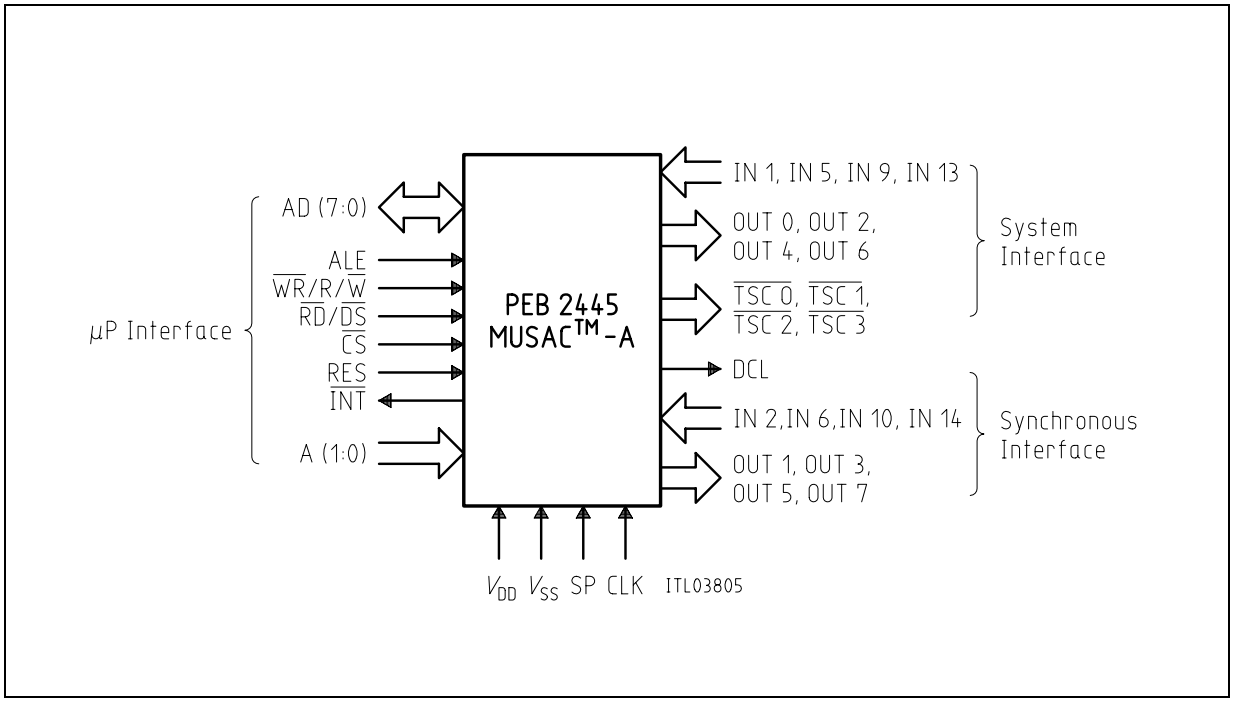


Figure 5
Functional Symbol for the Primary Access Configuration

1.5 Device Overview

The Multipoint Switching and Conferencing Unit (MUSAC-A) combines a time switch unit (MTSC) and a powerful signal processor on one chip. The MUSAC-A enhances the capabilities of a PBX by supporting teleconferencing and multipoint data communication over voiceband channels. Digital signal processing techniques are used to implement the conferencing algorithms. Up to 64 channels of the 512 incoming PCM channels may be manipulated by the signal processor and output to any of 256 outgoing PCM channels. All functions are programmed and controlled via an 8-bit standard µP interface (Intel type).

The MUSAC-A is fabricated using the advanced CMOS technology from SIEMENS and is mounted in a P-LCC-44 package. Inputs and outputs are TTL-compatible.

The PEB 2445 is pin and register compatible to the PEB 2045.

In addition, it includes the following features:

- Conference Unit
- Programmable attenuation for each output channel in the range of – 4 dB up to 12 dB.
- The attenuations of the outputs and the attenuations in the conference unit can be selected independent of one another.

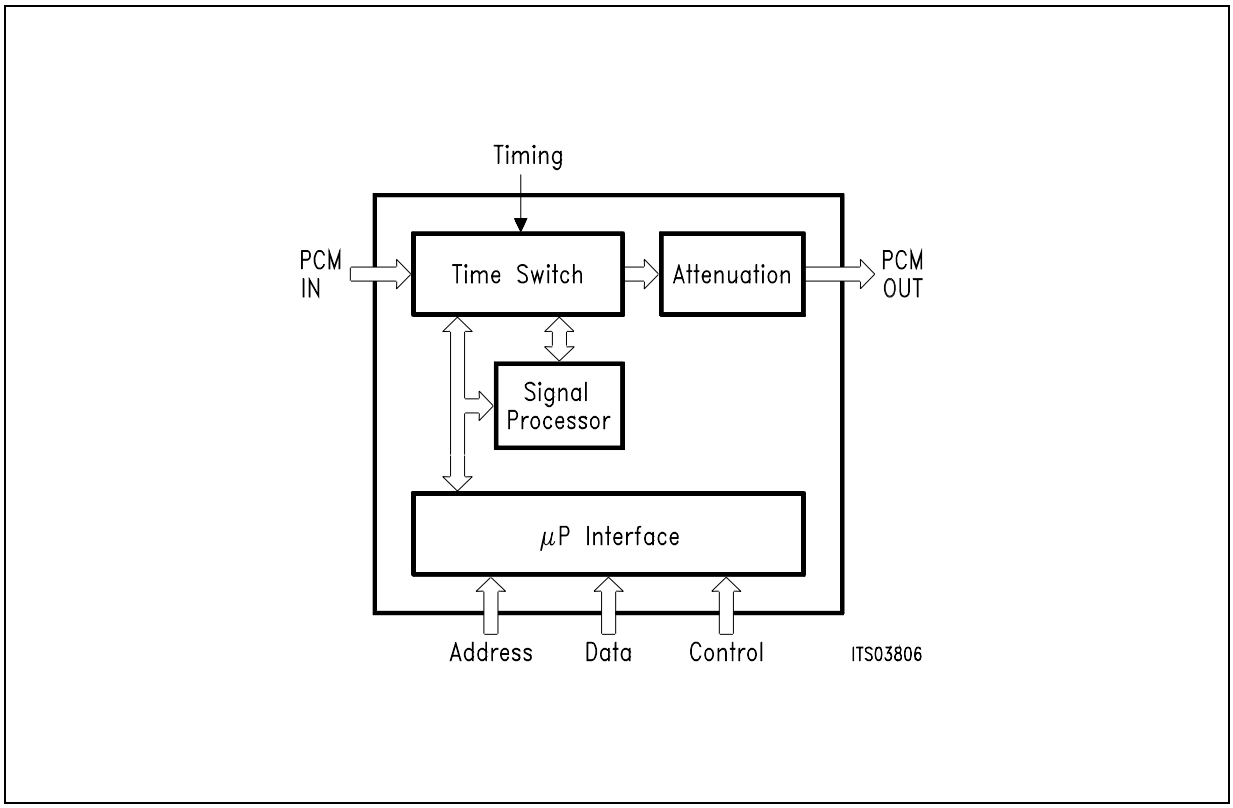


Figure 6
Block Diagram of the PEB 2445

1.6 System Integration

Conferencing

The MUSAC-A is designed to connect any of the 512 PCM-input channels to any of 256 output channels. Any input channel up to a total number of 64 can be handled in 21 independent conferences simultaneously. Any conference combination from 3 subscribers in 21 conferences up to 64 subscribers in only one conference is possible. In order to ensure an acceptable speech quality and to reduce echo and 'singing' problems, the input channels can be attenuated individually by 0, 3 dB, 6 dB or 9 dB and the output channels by 0 or 3 dB; additionally, input signals below a threshold programmable to four different levels are disregarded (see **chapter 4.5**).

To lessen the risk of instability in multiparty conferences the voice signal from every second channel can be inverted so that disturbance signals in odd and even channels are subtracted from one another.

If more capacity is needed, several devices can be connected. By connecting the 16 PCM-input lines in parallel to two MUSAC-As, a non-blocking switching matrix for 512 subscribers can be implemented: 128 input channels can be selected for up to 42 independent, simultaneous conferences. **Figure 7** shows such an arrangement. Due to the tristate capability of the MUSAC-A larger switches with conferencing capability can be easily formed.

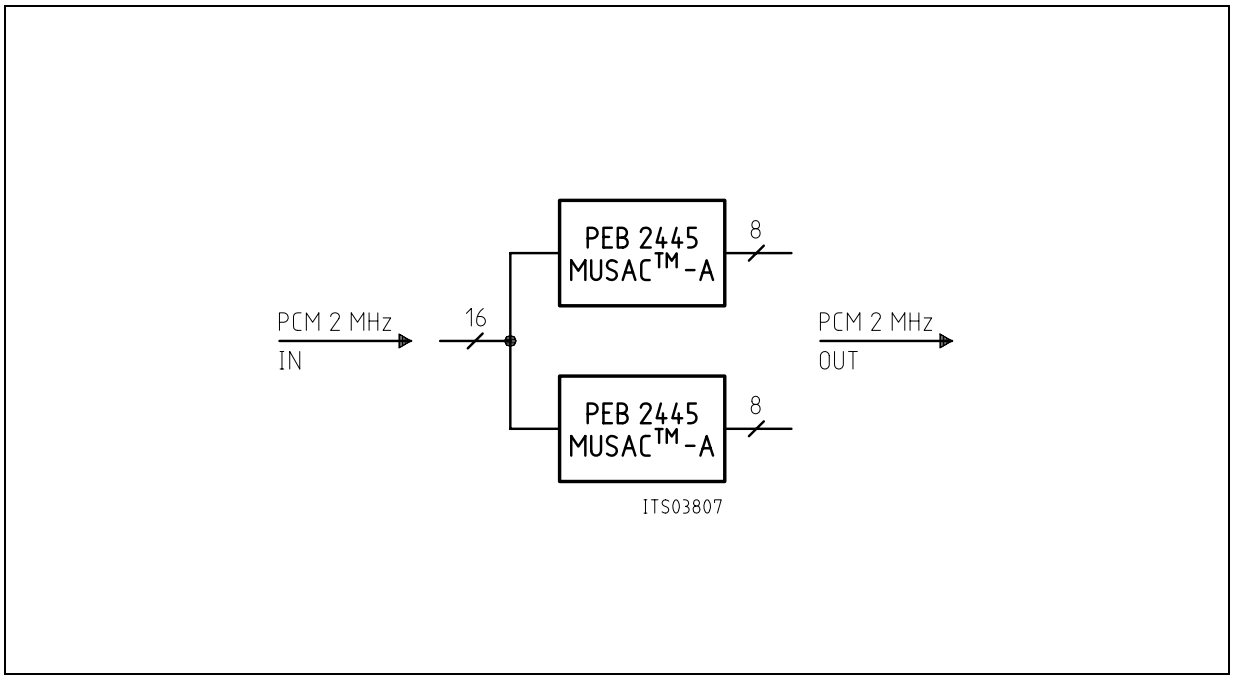


Figure 7
Memory Time Switch 16/16 for a Non-Blocking 512 Channel Switch with Conferencing Capability

Figure 8 shows the architecture of a primary access board with common channel signaling using four CMOS devices.

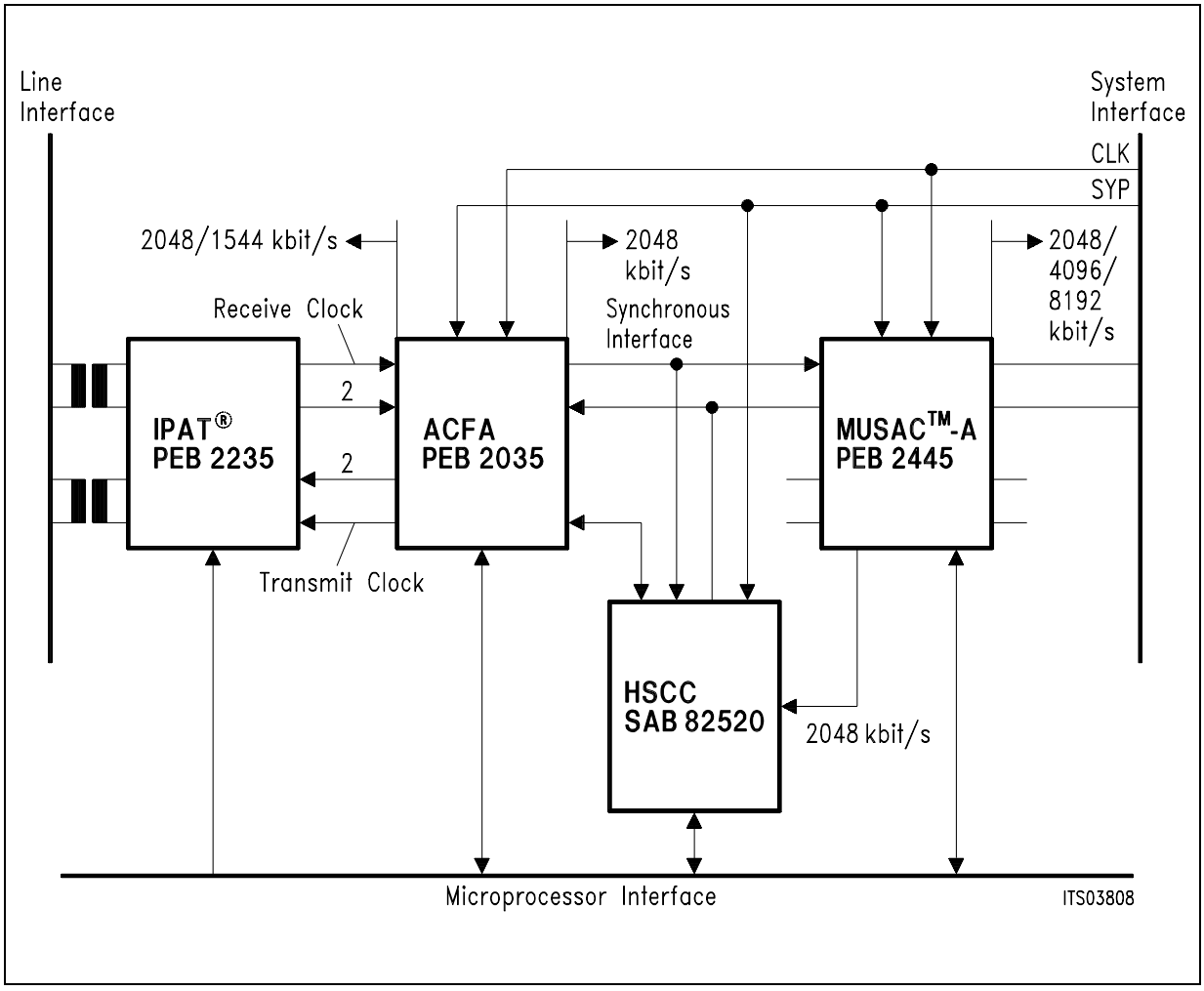


Figure 8
Architecture of a Primary Access Board

Multipoint Switching

In a multipoint configuration the communication between different stations is done by using a common media. In a PBX system this can be achieved by connecting all stations to one (or more) time-slots and transmitting the information back. Multipoint-switching is a special form of conferencing for data communication. In contrast to audio conferences terminals broadcast data to the MUSAC-A which are only ‘or-connected’. That is, at each bit time, the ‘conference sum’ is ‘1’ if the input of one or more terminals is ‘1’; otherwise, the result is ‘0’. A simple example of such a system using Siemens VLSI switching devices is shown in **figure 9**.

ISDN subscribers are connected via line cards and PCM highways to a multipoint switching matrix. The data from different terminals are summed up in the multipoint switching matrix and transmitted back to all stations. The switching matrix is build by using just one MUSAC-A. Every combination of subscribers may be switched to the same transport media (time-slot), in this way enabling a number of powerful multipoint communication systems.

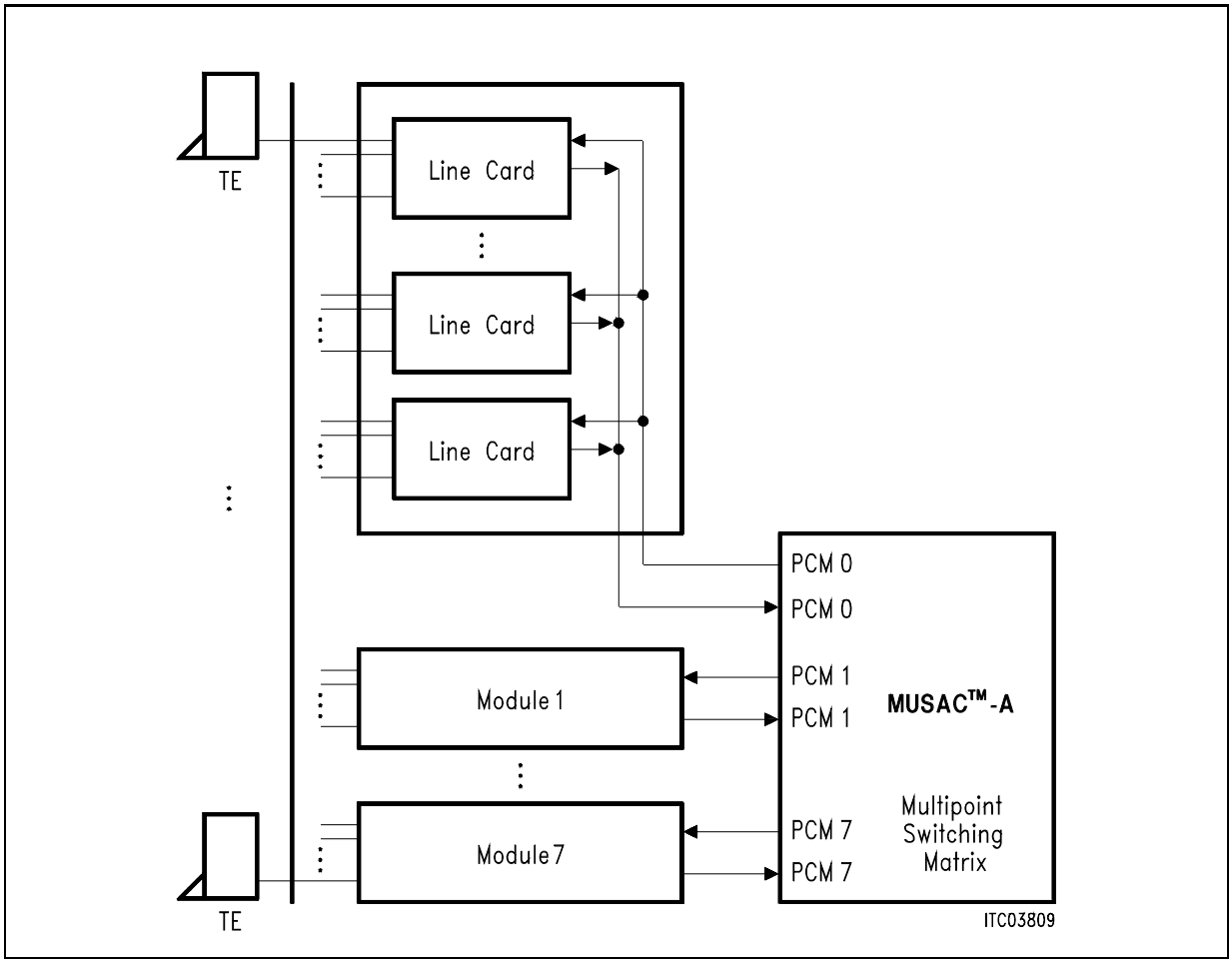


Figure 9
Multipoint System Configuration for ISDN Subscribers

In order to establish a multipoint-connection with more than 64 terminals, you can form a multistage arrangement, as shown in **figure 10**.

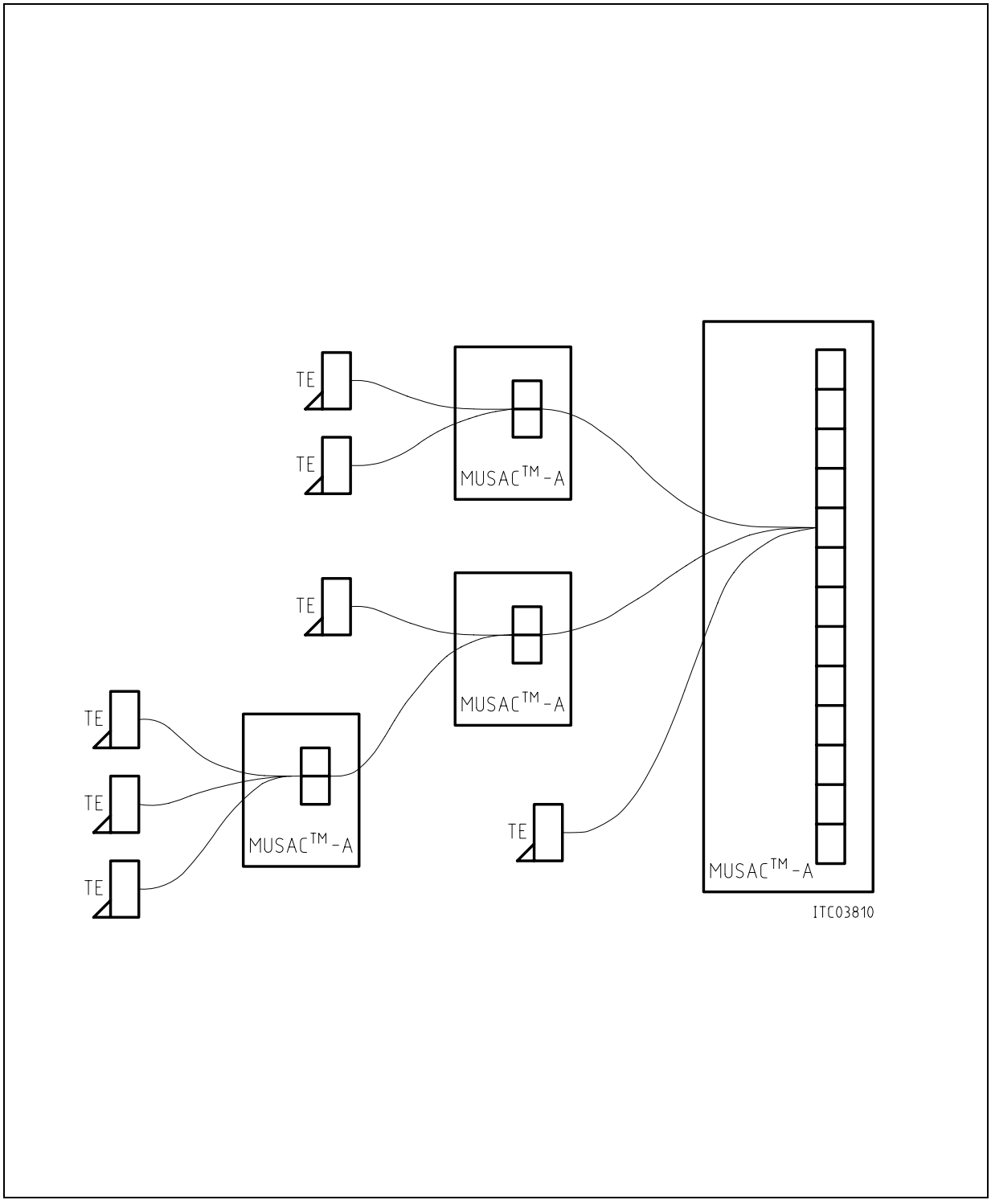


Figure 10
Multistage Arrangement

2 Functional Description

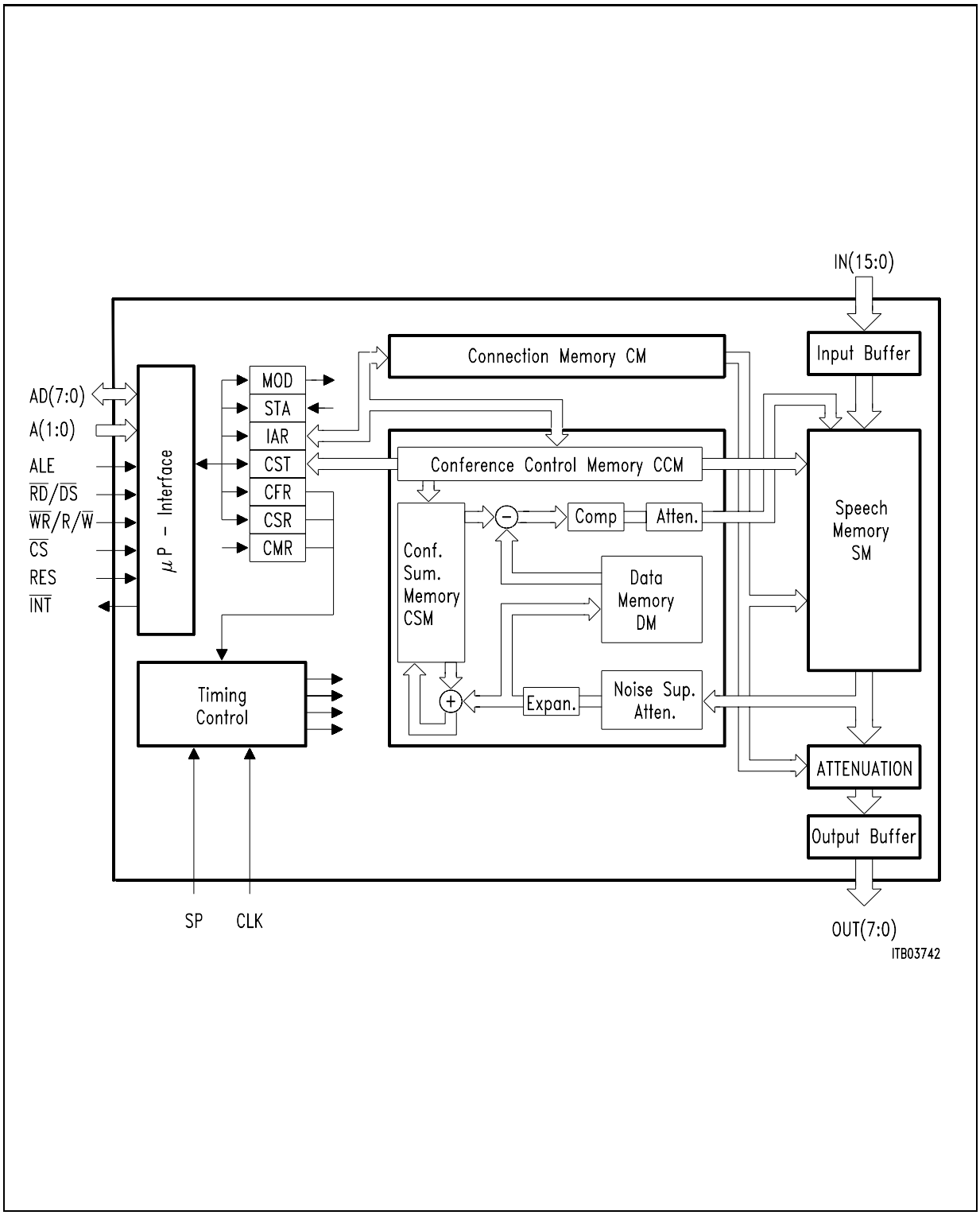


Figure 11
Detailed Block Diagram of the PEB 2445

2.1 Basic Functional Principles

The MUSAC-A is a memory time switch device for a PCM PBX system, offering a variety of additional features like multipoint switching, conference calls, programmable noise suppression and attenuation. The MUSAC-A works either in standard configuration for usual switching applications or in the primary access configuration, where it realizes, together with the PEB 2035 (ACFA) and the PEB 2235 (IPAT), the system interface for up to four primary multiplex access lines. In both configurations the conference and multipoint switching capability can be used.

The block diagram is shown in **figure 11**. The MUSAC-A is designed to connect any of 512 PCM- input channels to any of 256 output channels. Any input channel up to a total number of 64 can be handled in 21 independent conferences simultaneously. Any conference combination from 3 subscribers in 21 conferences up to 64 subscribers in only one conference is possible. Not more than 8 subscribers should be connected to a single conference, however, in order to ensure an acceptable speech quality. It can be improved by selecting an additional attenuation and activating the noise suppression: The input channels can be attenuated by 0, 3 dB, 6 dB or 9 dB and the output channels by 0 or 3 dB. Input signals below a threshold programmable to four different levels are disregarded.

The input information of a complete frame is stored in the on-chip 4-Kbit Speech Memory (SM). The incoming 512 channels of 8 bits each are written in sequence into fixed positions in the SM with a repetition rate of 8 kHz. Additionally, in the second half of the frame the 64 conference output channels of 8 bit each are written into the SM. The memory access is normally controlled by the input counter in the timing control block when writing into the SM but by the conference unit when writing the conference output channels. The read access is independent of the write access, so that both input and conference output channels can be read at any time.

For outputting, the Connection Memory (CM) is read in sequence. Each location in the CM points to a location in the Speech Memory. Before the byte in this SM location is read into the current output time-slot, it can be attenuated. The attenuation takes care of the compressed data format (A-law, μ-law). The attenuations for all 256-output channels are stored in the CM and can be chosen between – 4 dB (amplification) to 12 dB (attenuation). The read access of the CM is controlled by the output counter also contained in the timing control block. In addition, in the first half of the frame the input channels connected to a conference are read in sequence by the Conference Unit (CU).

All connections are set up by an external controller which programs the Connection Memory (CM) and the Conference Control Memory (CCM) using the microprocessor interface. The CM address corresponds to one particular output time-slot and line number. The contents of this CM-location points to a particular input time-slot and line number in the transparent mode. In the conference mode or multipoint switching mode it contains the conference address and points to a conference output location in the SM instead. The same conference address is used to access the CCM. The parameters

stored in the CCM include the input time-slot and line number, the associated conference number as well as the noise suppression thresholds and the attenuation levels. The conference number defines a unique location in the Conference Sum Memory (CSM) used to store the accumulated samples for each conference. The Conference Sum Memory is alternately loaded in the first half of the frame and unloaded in the following second half. In the first half the input samples are processed to implement the noise suppression, the expansion according to the European A-law or the US μ-law and the attenuation function. The Data Memory (DM) buffers these samples for output processing. The CSM is used to accumulate these samples and store the resulting sum. During output processing the input sample is retrieved from the Data Memory and the appropriate sum from the Conference Sum Memory for subtraction, so that the channel output signal contains the contribution of all the other channels in the conference except its own. After output attenuation and PCM compression, the data are written in the Speech Memory for output switching.

If one result of the subtractions exceeds the full scale value, a saturation appears and the MUSAC-A signals this conference overflow condition by an interrupt. The conference number of the conference in overflow is buffered in the Conference Status Register (CST) which can be retrieved by the external controller.

A tone to be inserted into a conference is handled as an additional conference subscriber using any input PCM channel (access to CCM) but without assigning an output time-slot (no access to CM).

Multipoint Switching is a special form of conferencing for data communication. In the multipoint switching mode several terminals are connected together. Normally only one should transmit at a time; its signal is distributed to the other terminals. For collision detection purposes all input signals are summed up to construct the output signal. In contrast to audio conferences terminals broadcast data to the MUSAC-A which are only ‘or-connected’. That is, at each bit time, the ‘conference sum’ is ‘1’ if the input of one or more terminals is ‘1’; otherwise, the result is ‘0’. The data memory, the subtractor, the linearization and attenuation are of no use in this mode. The general procedure is the same as for conferencing.

All attenuations of the PCM values are calculated by the following mechanism

1. Expansion according CCITT Rec. G. 711
2. Attenuation by
   lin. value $\times 2^{-(x/6)}$, x = Attenuation
3. Comparison according CCITT Rec. G. 711

These functions are implemented by a PLA/ROM.

The chip architecture makes it possible to decrease the delay between incoming and outgoing PCM channels. The processed input samples are transmitted either in the same frame or in the next frame at the latest.

Definitions

- The PEB 2445 works with either an 8192-kHz clock or a 4096-kHz clock. Henceforth, the respective clock periods are referred to as t_{CP8} and t_{CP4}.
- The bits of a time-slot are numbered 0 through 7. Bit 0 (MSB) of a time-slot is the first bit to be received or transmitted by the MUSAC-A, bit 7 (LSB) the last.

Preparation of the Input Data (Input Buffer)

The PEB 2445 works in 2048-, 4096- or 8192-kbit/s PCM systems. The frame frequency is 8000 Hz in all 3 types of systems. Therefore a frame consists of 32-, 64- or 128 time-slots of 1 byte each, respectively. In order to fill the speech memory, which has a fixed capacity of 512 channels, either 16-, 8- or 4 input lines are necessary, respectively. Thus, in 4- and 8-MHz systems only some of the 16 input lines can be used.

Moreover, the PEB 2445 can also work with two different input data rates simultaneously. In this case some of the PCM-input lines operate at one data rate, while others operate at another. **Table 2** states how many input lines are operating at the different data rates for all possible input data rate combinations. In the following they will be referred to as input modes.

The input mode the PEB 2445 is actually working in has to be programmed into the mode register, bits MI1, MI0, MO1, MO0. In **chapter 4.1** you will find a complete description which input line is connected to which system, for each of the input modes.

Table 2
Possible Input Modes

Input Modes				Type
16	×	2048	kbit/s	Single mode
8	×	4096	kbit/s	Single mode
4	×	8192	kbit/s	Single mode
2 × 8192	+	8 × 2048	kbit/s	Mixed mode
4 × 4096	+	8 × 2048	kbit/s	Mixed mode

The PEB 2445 runs with either a 4096- or a 8192-kHz device clock as selected with **CFR:CPS**. Data rates and clock frequencies may be combined freely. However, processing 8192-kbit/s data, an 8192-kHz clock must be supplied.

The preparation of the input data according to the selected input mode is made in the input buffer. It converts the serial data of a time-slot to parallel form.

In **standard configuration** time-slot 0 begins with the rising edge of the SP pulse as shown in upper half of **figure 12** denoted **CSR:(0000XXXX)**.

As can be seen there the beginning of a input time-slot is defined such, that the input lines have settled to a stable value, when the datum is actually sampled.

4096- and 8192-kbit/s data is sampled in the middle of the bit period at the falling edge of the respective data clock. 2048-kbit/s data is sampled after 3/4 of the according bit period, i.e. with the rising edge of the 4^{th} 8192-kHz clock cycle or the falling edge of the 2^{nd} 4096-kHz clock cycle of the considered bit period.

In the **primary access configuration** a different timing scheme may apply to the odd physical input lines. They are affected by the content of the clock shift register (**CSR**), which can be programmed via the µP interface (see **chapter 2.2**).

The clock shift register holds the information, how the frame structure is shifted in the primary access configuration. Its content defaults to 00_H after power up and is also set to this value, whenever the standard configuration is selected.

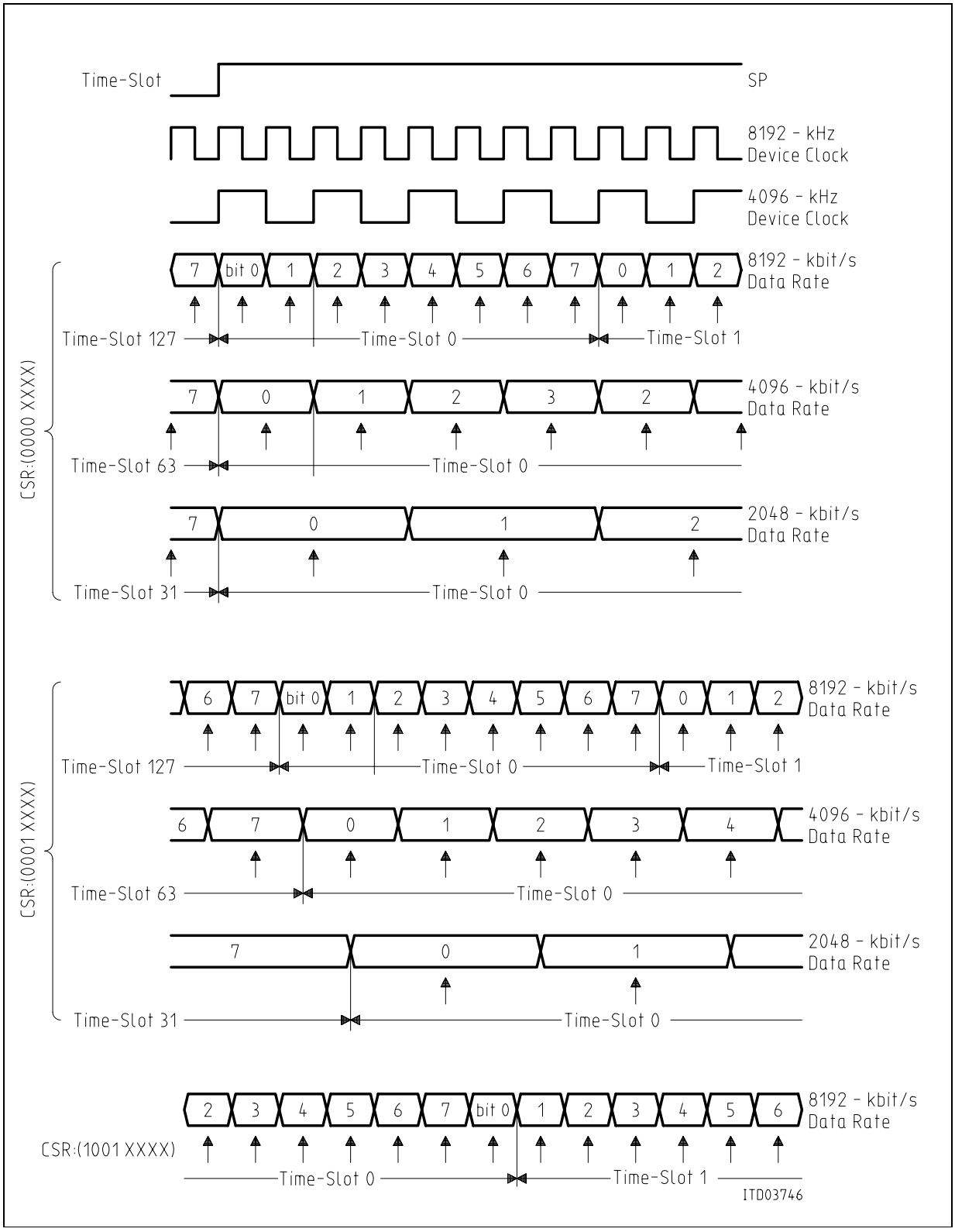


Figure 12
Latching Instant for Input Data

The four most significant bits of the clock shift register are of interest for the input lines. They only affect the odd input lines (see **chapter 4.6.2**): The frame structure can be advanced by the number of bit periods programmed to the RS2, RS1 and RS0 bits of the **CSR**. For example, programming the **CSR** with (1100XXXX) a new frame starts 6-bit periods before the rising edge of the SP pulse.

Selecting RRE to logical 1 the frame is delayed by half a bit period (see **figure 12**). The data is then sampled in the middle of the respective bit period for all data rates.

The last line of **figure 12** shows the sampling instants for the **CSR** entry (1001XXXX). Then the input frame is advanced by 4-bit periods and delayed by a half resulting in an 3 1/2-clock period advancement of the input frame. For further examples refer to **figure 20**.

Thus the frame structure may be selected to begin at any 1/2-bit period value between an resulting advancement of 7-bit periods and a resulting delay of 1/2 a bit period.

Setting **CSR** = $0X_H$ the same timing conditions apply to even and odd inputs. Then all system interface inputs are processed in the same way they are in the standard configuration.

Output Buffer

The output buffer rearranges the data read from the speech memory. It basically converts the parallel data to serial data. Depending on the validity bit the output buffer outputs the data or switches the line to high impedance. The most significant bits of the 256 words in the connection memory are interpreted as validity bits for the 256 possible output channels: A logical 0 enables the programmed connection, a logical 1 tristates the output.

The mode register (**MOD**) bits MI1, MI0, MO1 and MO0 control this process. The possible output modes are listed in **table 3**.

Table 3
Possible Output Modes

Output Modes				Type
8	×	2048	kbit/s	Single mode
4	×	4096	kbit/s	Single mode
2	×	8192	kbit/s	Single mode
1 × 8192	+	4 × 2048	kbit/s	Mixed mode
2 × 4096	+	4 × 2048	kbit/s	Mixed mode

Figure 13 shows when the single bits are output. In standard configuration they are clocked off at the rising clock edge at the beginning of the considered bit period. Time-slot 0 starts two t_{CP8} before the falling edge of the SP pulse.

In primary access configuration the even output lines are affected by the XS2, XS1, XS0 and XFE entries in the clock shift register. The output frame is synchronized with the rising edge of the SP signal.

Assuming a **CSR** entry $X0_H$ the output frame starts with the rising edge of the SP pulse. Programming the XS2, XS1 and XS0 bits with a value deviating from binary 000 the output frame is delayed by 8_D – $(XS2, XS1, XS0)_B$ bit periods. E.g, a **CSR** entry of (XXXX0010) delays the output frame by 7-bit periods relative to the rising SP-pulse edge.

Programming **CSR:(XXXXXXX1)** the output frame is delayed by another half a **device** clock period. In **figure 13** the outputting instants are shown for a device clock of 4096 and 8192 kHz and a **CSR:(XXXX0001)**.

The last line in **figure 13** shows an even 8192-kbit/s output line for the **CSR** entry (XXXX1101) and an 8192-kHz device clock. The output frame is delayed by 2 1/2-bit periods. For further examples refer to **figure 20**.

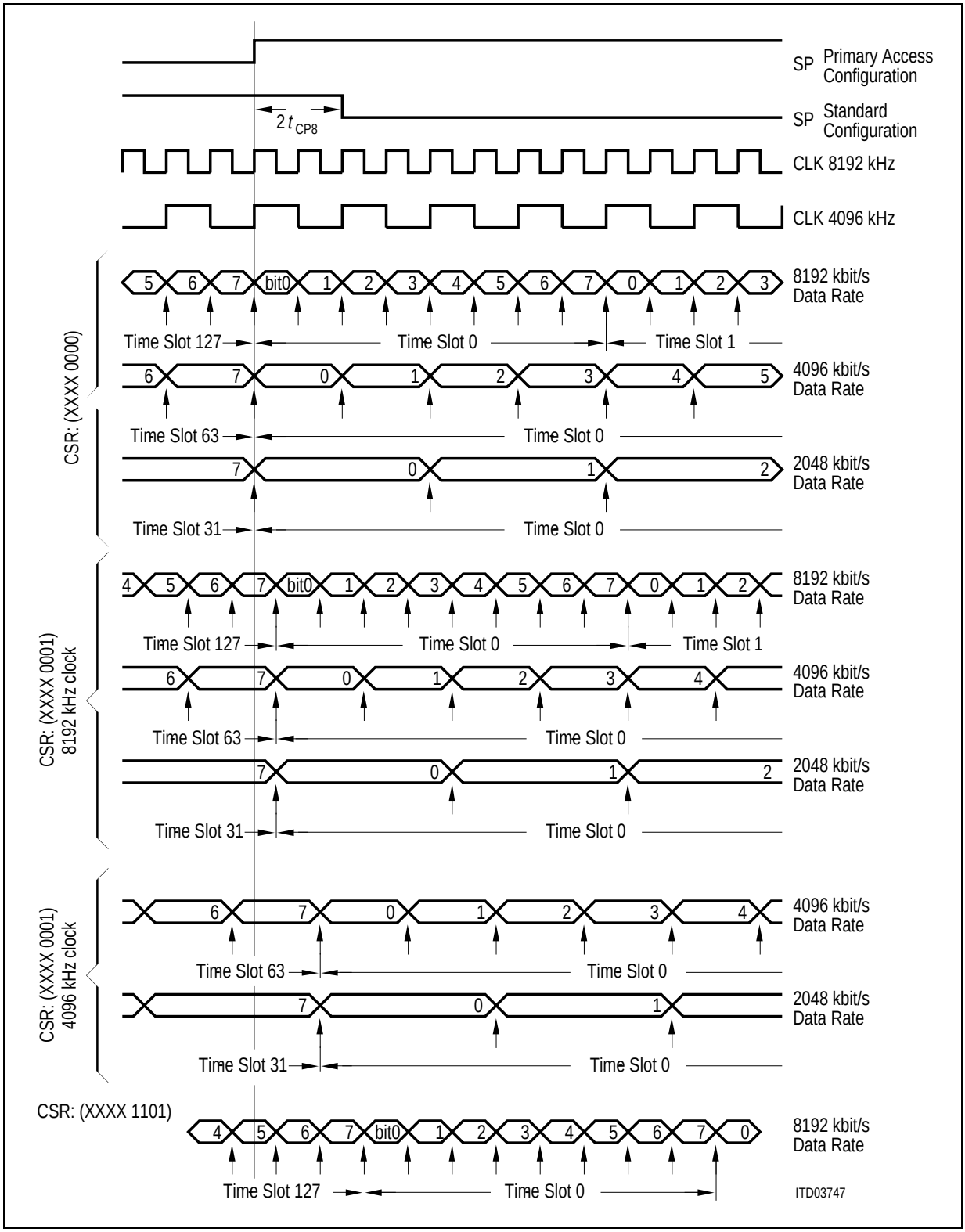


Figure 13
Clocking Off Instant of Output Data

Configuration Type

The MUSAC-A works either in the standard configuration for usual switching applications or in the primary access configuration. In these both configurations the conference and multipoint switching capability can be used.

Standard Configuration

A logical 1 in the **CFS** bit of the configuration register sets the PEB 2445 in standard mode (default after power up). All modes from **table 7** can be used. It has to be ensured that the data rate is not higher than the selected device clock (4096 or 8192 kHz).

In this application 512 channels per frame are written into the speech memory. Each one of them can be connected to any output channel.

Any output channel can be attenuated independently of each other.

According to **table 8** and **table 12** and depending on the selected mode the least significant bits of the connection memory address and data contain the logical pin numbers, the most significant bits the time-slot number of the output and input channels.

The following example explains the programming sequence.

Time-slot 7 of the incoming 8192-kbit/s input line IN 14 shall be connected to time-slot 6 of the output line OUT 5 of an 2048-kbit/s system. The attenuation for this connection should be 7 dB. According to **table 8** in 8192-kbit/s systems the input line IN 14 is the logical input line 2. Output line number and logical output number are identical to one another. According to **chapter 4.5** C3 … C0 is set to 7_H.

Therefore the following byte sequence on the address data bus has to be used to program the CM properly (see **table 12**):

01101100	(Control Byte)	or	01011100	(Control Byte)
00011110	(Data Byte)		00011110	(Data Byte)
00110101	(Address Byte)		00110101	(Address Byte)

The frame, for all input channels, starts with the rising edge of the SP signal. The frame for all output channels begins two t_{CP8} (with 8192-kHz device clock) or one t_{CP4} period (4096-kHz device clock) before the falling SP edge. The period of time between the rising and falling edge of the SP pulse should be

$$t_{SPH} = (2 + N \times 4)\, t_{CP8} \qquad (0 \le N \le 255)$$
$$= (1 + N \times 2)\, t_{CP4}$$

N is an user defined integer. By varying N, t_{SPH} can be varied in 2048-kHz clock period steps. For an example using N = 2 refer to **figure 14**.

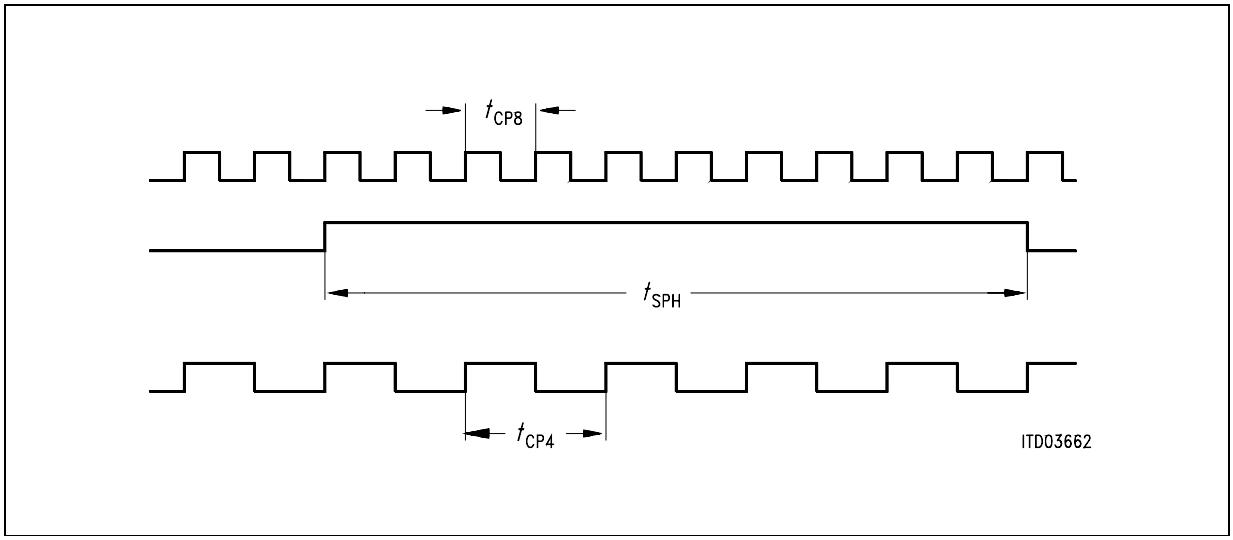


Figure 14
SP Duration for N = 2

Primary Access Configuration

A logical 0 in the **CFS** bit of the configuration register selects the PEB 2445 for primary access applications. In this case the MUSAC-A is an interface device connecting a standard PCM interface (system interface) with another PCM interface e.g. an intermediate interface for connections to primary loops (synchronous interface). For both a serial interface is provided.

The synchronous 2048-kbit/s interface consists of four input and four output lines with a bit rate of 2048-kbit/s. This interface can be used to connect the PEB 2445 to up to four primary trunk lines via coding/decoding devices with frame alignment function (e.g. PEB 2035 ACFA) and line transceivers with clock and data recovery (e.g. PEB 2235 IPAT) and to signaling processors (e.g. the SAB 82520 HSCC).

The system interface is not confined to one data rate but can operate at the full choice of the PEB 2445 data rates: 2048, 4096 and 8192 kbit/s. A clock shift in a range of 7 1/2 clock steps with half clock step resolution may be programmed independently for inputs and outputs.

The frame for all input- and output lines starts with the rising edge of the SP signal.

In the primary access mode the signals $\overline{TSC0}$, $\overline{TSC1}$, $\overline{TSC2}$ and $\overline{TSC3}$ indicate when the associated system interface output is valid. The signal DCL supplies a 2-MHz clock which can be used for other devices at the synchronous interface, e.g. the High Level Serial Communication Controller HSCC (SAB 82520).

In the primary access configuration only those modes which support at least 4 input and 4 output lines at 2048 kbit/s can be used. These are the modes MI1, MI0, MO1, MO0 = 0_H, A_H, F_H (see **table 7**). Programming the CM in the primary access configuration is described in **tables 8, 13 and 14**. The attenuations are programmed in the same way as in the standard configuration. The least significant 2 bits of the data byte and the least significant bit of the address byte determine the type of interface, the more significant bits define the logical line number and time-slot number.

According to **figure 15** in the primary access configuration the connection memory is usually programmed to switch the system and synchronous interface inputs to the synchronous and system interface outputs, respectively. However, it is also possible to connect the system interface inputs to the system interface outputs as well as the synchronous interface inputs to the synchronous interface outputs. This connection possibility allows for test loops at the system and the synchronous interfaces.

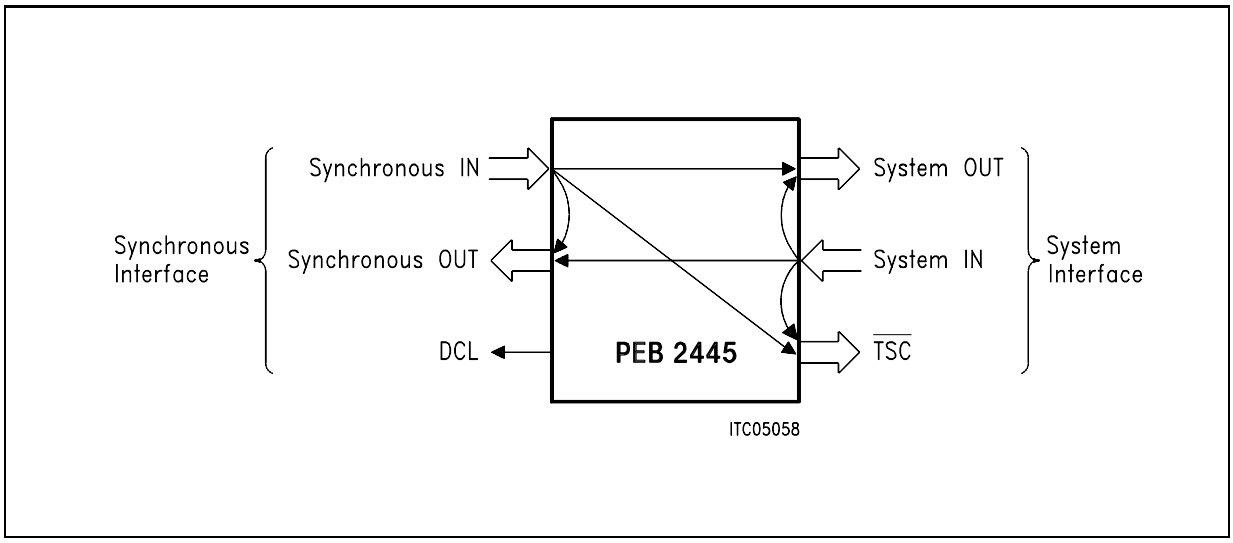


Figure 15
Connection Choices in the Primary Access Configuration

2.2 Microprocessor Interface and Registers

The MUSAC-A is programmed via the µP interface. It consists of the address data bus AD7 … AD0, the address bits A1 … A0, the Write ($\overline{WR}$), the Read ($\overline{RD}$), the Address Latch Enable (ALE), the Interrupt ($\overline{INT}$) and the Chip Select ($\overline{CS}$) signal, as shown in **figure 16**.

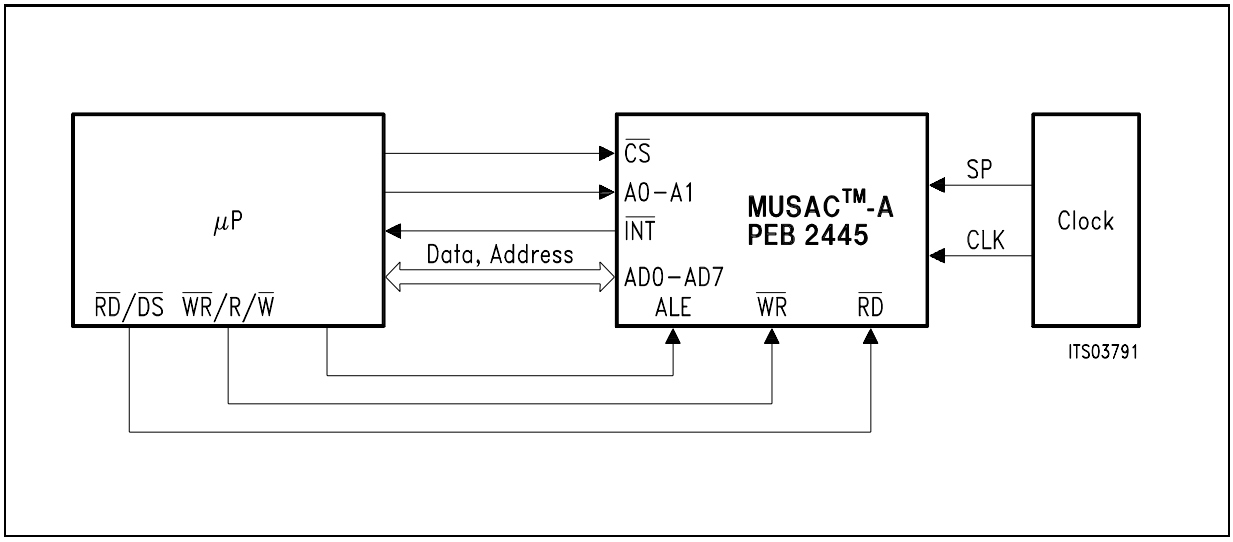


Figure 16
The MUSAC™-A Controlled by a Microprocessor

The standard 8-bit µP interface can communicate with Intel multiplexed/demultiplexed microprocessors. It gives access to the internal registers and to the control memories (Connection Memory, Conference Control Memory).

Table 4
µP-Interface Functions

ALE	Type of µP Interface	Bus Structure	Pin 24	Pin 25
Fixed to ground	Intel	demultiplexed	$\overline{RD}$	$\overline{WR}$
Switching	Intel	multiplexed	$\overline{RD}$	$\overline{WR}$

ALE is internally set to ground if it is not connected.

For a demultiplexed µP interface the address bits A1 and A0 are needed for addressing a register. For the µP-interface timing please refer to **chapter 5.3**.

Five directly addressable registers are provided:

- Mode register (MOD)
- Status register (STA)
- Conference Status register (CST)
- Conference Mask Register (CMR)
- Indirect Access Register (IAR)

Two other registers and the control memories are accessed by a simple three byte indirect access method:

- Configuration Register (CFR)
- Clock Shift Register (CSR)
- Connection Memory (CM)
- Conference Control Memory (CCM)

The status register (STA) and the conference status register (CST) are read-only-registers, the conference mask register (CMR) is a write-only-register; MOD, CFR, CSR, IAR and CM or CCM can be read or written. An indirect access scheme is used to access the CFR, CSR, CM or CCM using the indirect access register (IAR).

The following direct registers may be accessed:

Table 5
Addressing the Direct Registers

Address		Write Operation	Read Operation
Demultiplexed Mode A(1:0)	**Multiplexed Mode AD(7:0)**		
0_H	0_H	MOD	STA
1_H	2_H	IAR	IAR
2_H	4_H	CMR	CST
3_H	6_H	–	MOD

If A1 is not connected in the demultiplexed mode neither an access to the CMR, CST nor a read access to the MOD register is possible.

In this case A1 is fixed to ground internally.

Indirect access to the CFR, CSR, CM or CCM:

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR.

Bit 7							Bit 0	
C3	C2	K1	K0	C1	C0	D9	D8	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte determines whether the CFR, the CSR, the CM or the CCM shall be accessed, whether a write or read operation shall be performed and whether the first or the second memory access shall be executed. (To describe a conference two accesses to the CCM are necessary). The bits D7 … D0 contain the information which shall be written into the control memories or the indirect registers. In the case of programming the CM the output attenuation is included either in the control byte (transparent switch) or in the data bits (conference switch). The address byte indicates which one of the indirect registers shall be accessed or in which memory location the data shall be written. An exact definition is given in **chapter 4.5**.

Before an indirect access is started, the Z- and B bits of the status register must be 0. With the first instruction the Z bit is set (see **chapter 4.2**). After the third instruction the MUSAC-A accesses the memory location. This access requires maximally 900 ns. After the access is finished the Z bit is reset.

Figure 17 a) illustrates a write operation on the IAR.

It is possible to read or write the direct access registers while an indirect access is in progress. Thus a register may be read in the time intervals that separate the three sequential indirect access instructions. Also, the current indirect access may be aborted by setting the MOD:RI. One indirect register access has to be completed before the next one can be started.

To read the indirect registers or the CM two sequences of three instructions each have to be programmed. In the first sequence the MUSAC-A is instructed which register or CM address to read. The data transferred to the PEB 2445 in this first sequence is of no significance. With the first write instruction STA:Z is set. After the first 3 instructions the MUSAC-A needs 900 ns to write the result to the IAR. The status register bit Z is reset after maximally 900 ns. Then 3 read operations follow. Again, STA:Z is set with the first read instruction. The 3 instructions read 3 bytes from the IAR. **Figure 17 b)** shows this procedure. After the third read operation the PEB 2445 needs another 900 ns to reset the indirect access mechanism and the Z bit in the status register. In CCM read accesses three sequences of three instructions (two identical write sequences and one read sequence; see **figure 17 c)** are necessary.

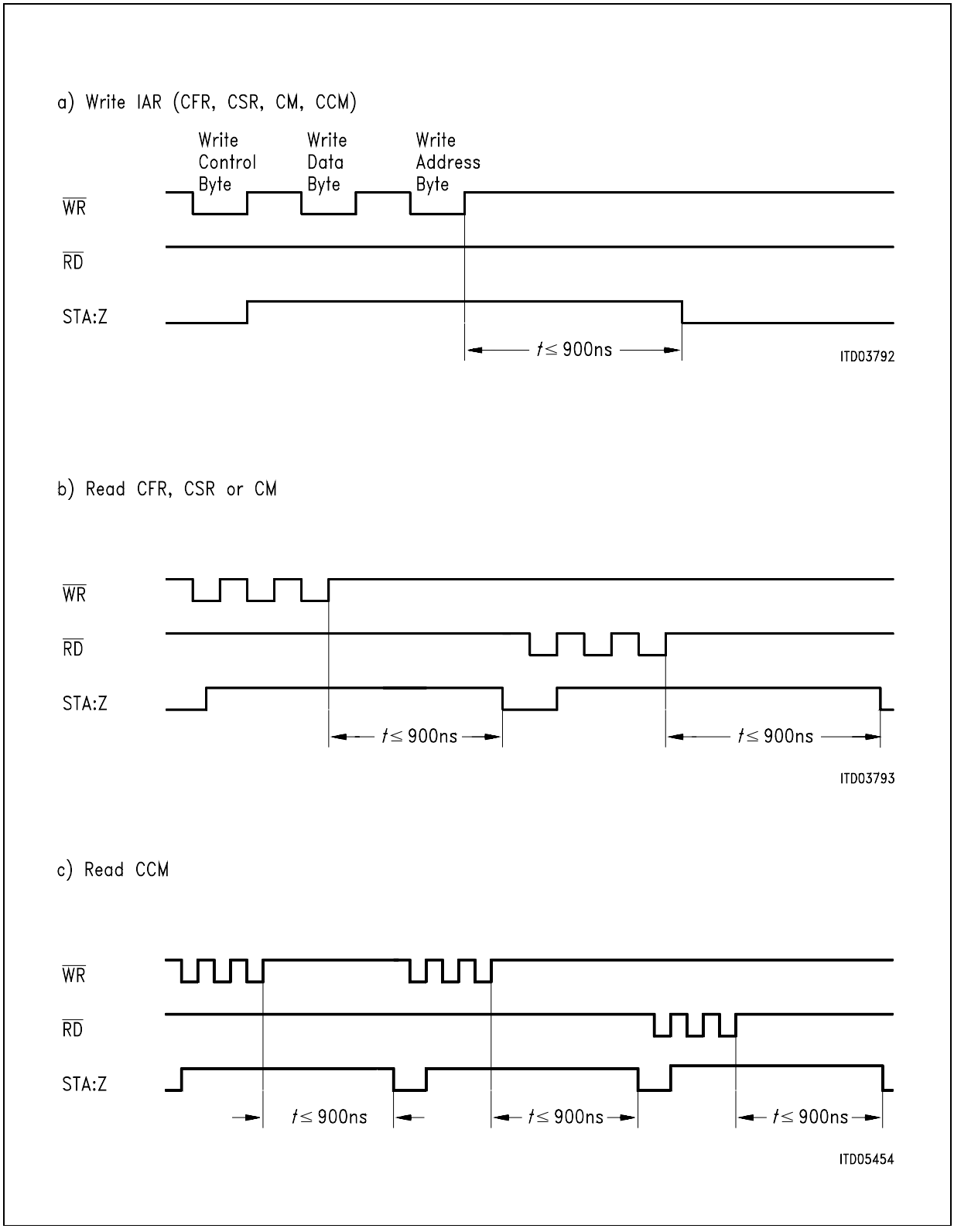


Figure 17
Timing Diagrams of IAR

3 Operational Description

3.1 Reset State

After a hardware reset (RES) or power up the MUSAC-A is set to its initial state. The MOD- and CFR register bits are all set to logical 1; the CSR-, CST- and CMR-register bits are set to logical 0. The STA register **B** bit is undefined, the **Z** bit contains logical 0.

3.2 Initialization Procedure

After reset a few internal signals and clocks need to be initialized. This is done with the initialization sequence. To give all signals and clocks a defined value only 4 SP pulses are necessary. The SP pulses may be of any length allowed in normal application, the time interval between the two SP pulses may be of any length down to 250 ns.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into MOD:RC. STA:B is set. The resulting CM reset is finished after max. 250 µs and is indicated by the status register B bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM-reset time longer than 250 µs.

After resetting the CM, all bits in the CM are reset to 0, except for the D9-bit, which is set to one, causing the output lines to be tristated.

To prepare the MUSAC-A for programming the CM and CCM, the RI bit in the mode register must be reset. Note that one mode register access can serve to reset both RC- and RI bits as well as configuring the chip (i.e. selecting operating mode etc.).

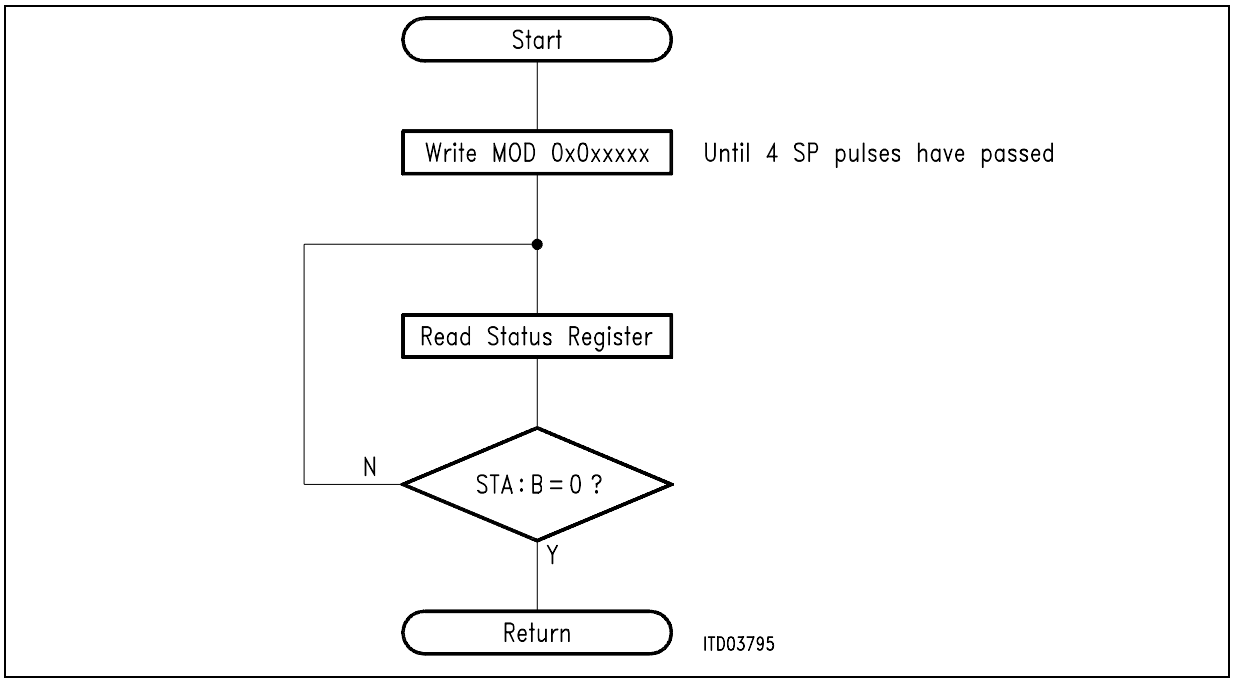


Figure 18
Initializing the PEB 2445 for a 8192-kHz Device Clock

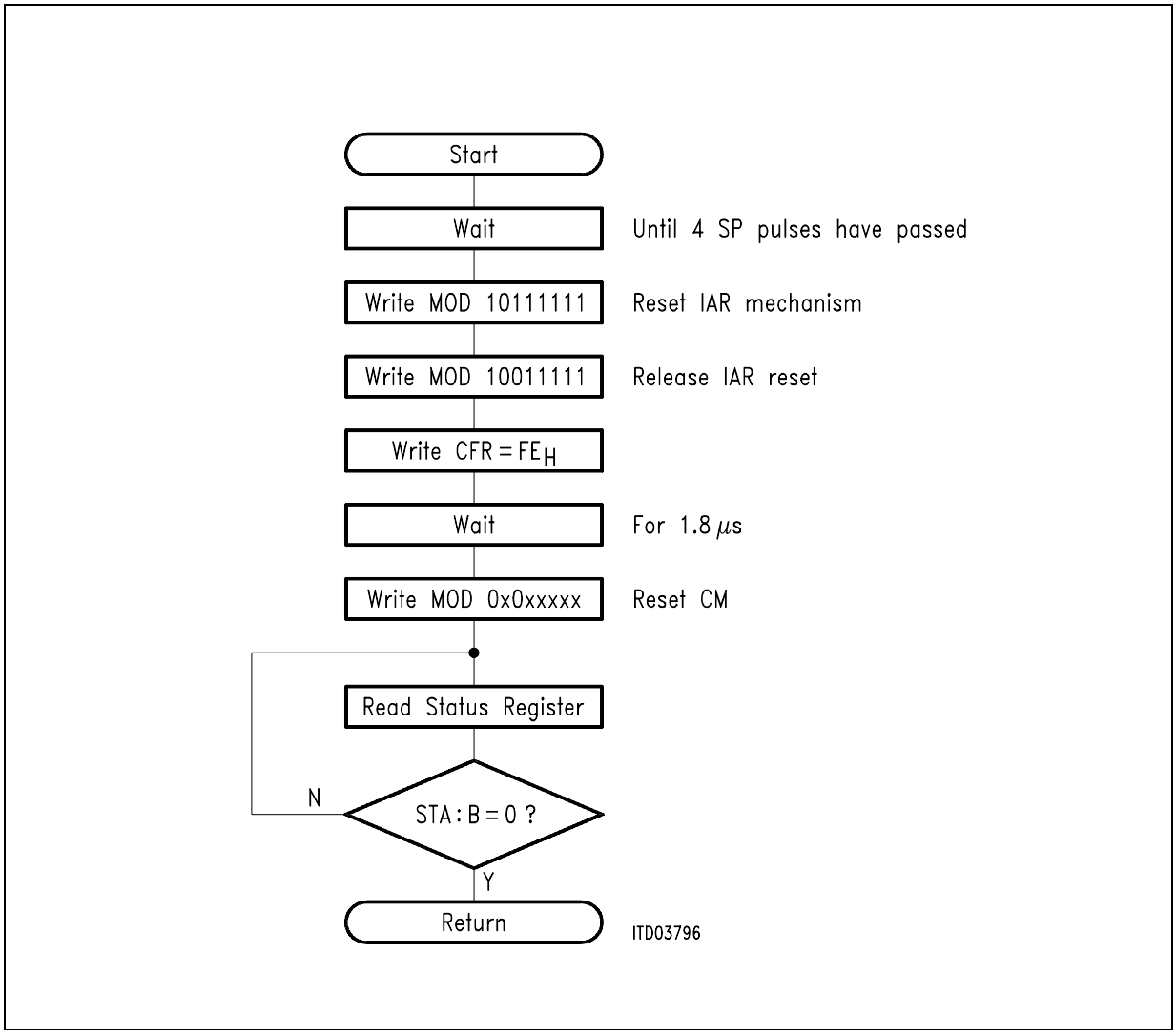


Figure 19
Initializing the PEB 2445 for a 4096-kHz Device Clock

3.3 Operation with a 4096-kHz Device Clock

In order for the MUSAC-A to operate with a 4096-kHz device clock the CPS bit in the CFR register needs to be reset. This has to be done before the CM reset and needs 1.8 µs. For a flow chart of this process refer to **figure 19**.

3.4 Standby Mode

With MOD:SB being logical 1 the MUSAC-A works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the SB bit is reset, the outputs are switched to low impedance for the programmed active channels and this MUSAC-A can take over from another device which has been recognized as being faulty.

4 Detailed Register Description

The following registers may be accessed:

Table 6
Addressing the Direct Registers

Address		Write Operation	Read Operation
Demultiplexed Mode A(1:0)	**Multiplexed Mode AD(7:0)**		
0_H	0_H	MOD	STA
1_H	2_H	IAR	IAR
2_H	4_H	CMR	CST
3_H	6_H	–	MOD

If A1 is not connected it is internally set to ground. In the demultiplexed mode neither an access to the CMR, CST nor a read access to the MOD register is possible.

The paragraphs in this section cover the registers in detail.

4.1 Mode Register (MOD)

Access in the multiplexed µP-interface mode: Write, address: 0_H read, address: 6_H

Access in the demultiplexed µP-interface mode: Write, address: 0_H read, address: 0_H

Reset value: BF_H

AD7							AD0
RC	**0**	**RI**	**SB**	**MI1**	**MI0**	**MO1**	**MO0**

RC **Reset Connection** memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time STA:B is set. The maximum time for resetting is 250 µs.

RI **Reset Indirect** access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB **Stand By**; By selecting SB = 1 all PCM outputs are tristated. The connection memory works normally. The MUSAC-A can be activated immediately by resetting SB.

MI1/0
MO1/0 **Input/Output** operation **Mode**; these bits define the bit rate of the input and output lines. The bitrates are given in **table 7**, the corresponding pin functions in **table 8** (standard configuration).

Table 7
Input/Output Operating Modes

MI1	MI0	MO1	MO0	Input Mode		Output Mode	
0	0	0	0	16 × 2	Mbit/s	8 × 2	Mbit/s[2)]
0	0	0	1	16 × 2	Mbit/s	2 × 8	Mbit/s
0	0	1	0	16 × 2	Mbit/s	4 × 2 / 1 × 8	Mbit/s
0	1	0	0	4 × 8	Mbit/s	8 × 2	Mbit/s
0	1	0	1	4 × 8	Mbit/s	2 × 8	Mbit/s
0	1	1	0	4 × 8	Mbit/s	4 × 2 / 1 × 8	Mbit/s
1	0	0	0	2 × 8 / 8 × 2	Mbit/s	8 × 2	Mbit/s
1	0	0	1	2 × 8 / 8 × 2	Mbit/s	2 × 8	Mbit/s
1	0	1	0	2 × 8 / 8 × 2	Mbit/s	4 × 2 / 1 × 8	Mbit/s[2)]
0	0	1	1	8 × 4	Mbit/s	4 × 4	Mbit/s
0	1	1	1	4 × 8	Mbit/s	4 × 4	Mbit/s
1	1	1	1	4 × 4 / 8 × 2	Mbit/s	4 × 2 / 2 × 4	Mbit/s[2)]
1	0	1	1	8 × 4	Mbit/s	2 × 8	Mbit/s
1	1	0	1	16 × 8	Mbit/s	2 × 8	Mbit/s[1)]
1	1	0	0	unused		unused	
1	1	1	0	unused		unused	

[1)] for space switch application only; the conference or multipoint switching capability cannot be used in this operating mode

[2)] can also be used for primary access configuration

Note: In the mixed modes the first bit rate refers to the odd line numbers, the second one to the even line numbers.

Input Pin Arrangement

Table 8
Input and Output Pin Arrangement for the Standard Configuration

Pin No.	16 × 8 Mbit/s 16 × 2 Mbit/s	4 × 8 Mbit/s	8 × 2 + 2 × 8 Mbit/s	8 × 4 Mbit/s	8 × 2 + 4 × 4 Mbit/s
4	IN1				
5	IN0		IN0		IN0
7	IN5				
8	IN4		IN4		IN4
9	IN9			IN1	IN1
10	IN8		IN8	IN0	IN8
11	IN13	IN1	IN1	IN5	IN5
12	IN12	IN0	IN12	IN4	IN12
13	IN14	IN2	IN14	IN6	IN14
14	IN15	IN3	IN3	IN7	IN7
15	IN10		IN10	IN2	IN10
16	IN11			IN3	IN3
17	IN6		IN6		IN6
18	IN7				
19	IN2		IN2		IN2
20	IN3				

Note: The input line numbers shown are the logical line numbers to be used for programming the connection memory and the conference control memory. In the case of 16 input lines the logical line numbers are identical to the pin names.

Output Pin Arrangement

Pin No.	8 × 2 Mbit/s	2 × 8 Mbit/s	4 × 2 + 1 × 8 Mbit/s	4 × 4 Mbit/s	4 × 2 + 2 × 4 Mbit/s
35	OUT7		OUT7		OUT7
36	OUT6				
37	OUT5		OUT5		OUT5
38	OUT4				
40	OUT3		OUT3	OUT3	OUT3
41	OUT2			OUT2	OUT2
42	OUT1	OUT1	OUT1	OUT1	OUT1
43	OUT0	OUT0	OUT0	OUT0	OUT0

Note: The logical output line numbers shown above are identical to the pin names.

Table 9
Input, Output and Tristate Pin Arrangement for the Primary Access Configuration

	Pin No.	System Interface Mode			
Pin Name	**P-LCC**	**2 MHz**	**4 MHz**	**8 MHz**	
$\overline{TSC0}$ $\overline{TSC1}$ $\overline{TSC2}$ $\overline{TSC3}$	5 8 10 12	$\overline{TSC0}$ $\overline{TSC1}$ $\overline{TSC2}$ $\overline{TSC3}$	$\overline{TSC0}$ $\overline{TSC1}$	$\overline{TSC0}$	System interface tristate control signals, clock shift programmable
OUT0 OUT2 OUT4 OUT6	43 41 38 36	OUT0 OUT1 OUT2 OUT3	OUT0 OUT1	OUT0	System interface outputs, clock shift programmable
IN13 IN9 IN5 IN1	11 9 7 4	IN3 IN2 IN1 IN0	IN1 IN0	IN0	System interface inputs, clock shift programmable
OUT1 OUT3 OUT5 OUT7	42 40 37 35	OUT0 OUT1 OUT2 OUT3	OUT0 OUT1 OUT2 OUT3	OUT0 OUT1 OUT2 OUT3	Synchronous 2-MHz interface outputs
IN14 IN10 IN6 IN2	13 15 17 19	IN3 IN2 IN1 IN0	IN3 IN2 IN1 IN0	IN3 IN2 IN1 IN0	Synchronous 2-MHz interface inputs
Mode		0000	1111	1010	MI1, MI0, MO1, MO0

Note: The input, output and tristate control line numbers shown in the center columns of this table are logical line numbers. The corresponding pin names are listed in the left most column.

4.2 Status Register (STA)

Access in the multiplexed µP-interface mode: Read, address: 0_H
Access in the demultiplexed µP-interface mode: Read, address: 0_H

AD7							AD0
B	**Z**	**X**	**X**	**VN3**	**VN2**	**VN1**	**VN0**

X don't care

B **Busy:** The chip is busy resetting the connection memory (B = 1). B is undefined after power up and logical 0 after the device initialization. The three byte indirect access register is not accessible.

Note: The maximum time for resetting is 250 µs.

Z Incomplete instruction; a three byte indirect instruction is not completed (Z = 1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting MOD:RI or resetting MOD:RC.

VN (3:0) Version Number according to the table below:

VN3	VN2	VN1	VN0	Device Versions
1	0	0	0	A1
1	0	0	1	V 1.2

4.3 Conference Status Register (CST)

Access in the multiplexed µP-interface mode: Read, address: 4_H
Access in the demultiplexed µP-interface mode: Read, address: 2_H

Reset value: 00_H

AD7							AD0
X	**IR**	**COV**	**CN4**	**CN3**	**CN2**	**CN1**	**CN0**

X don't care

IR **Initialization Request**. The connection memory and the conference control memory may have lost data (IR = 1). The IR bit is set after power failure or inappropriate clocking and is reset by reading CST.

COV **Conference Overflow** (overflow ⇒ logical 1)

CN4 … CN0 **Conference Number** of the conference in overflow

4.4 Conference Mask Register (CMR)

Access in the multiplexed µP-interface mode: Write, address: 4_H
Access in the demultiplexed µP-interface mode: Write, address: 2_H

Reset value: 00_H

AD7							AD0
0	**IR**	**COV**	**0**	**0**	**0**	**0**	**0**

A logical 1 disables the corresponding interrupt.

IR **Initialization Request** mask; the initialization request is masked (IR = 1)

COV **Conference Overflow** mask; the conference overflow is masked (COV = 1)

4.5 Indirect Access Register (IAR)

Access in the multiplexed µP-interface mode: Read/write, address: 2_H
Access in the demultiplexed µP-interface mode: Read/write, address: 1_H

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR.

Bit 7							Bit 0	
C3	C2	K1	K0	C1	C0	D9	D8	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

K1, K0 control the indirect access according to the following table
C3 – C0 additional programming bits

K1, K0	C3 – C0	D8	Type of Access
00	X_H	–	Read CM
10/01	0_H, 2_H 4_H – F_H	–	Write CM: transp. switch, att. value programmable with C3 … C0
	1_H, 3_H	–	Write CM: conf. switch, att. value programmable with D8 – D6
11	4_H	–	Write CCM, first access
	6_H	–	Read CCM, first access
	8_H	–	Write CCM, second access
	A_H	–	Read CCM, second access
	0_H	0	Write indirect register
	0_H	1	Read indirect register

X = don’t care; – is not needed to define type of access

Attenuation

Table 10
Transparent Switching

C3 … C0	Attenuation
0_H	0 dB
A_H	1 dB
2_H	2 dB
B_H	3 dB
4_H	4 dB
5_H	5 dB
6_H	6 dB
7_H	7 dB
8_H	8 dB
9_H	10 dB
F_H	12 dB
E_H	– 2 dB
D_H	– 3 dB
C_H	– 4 dB

Table 11
Conference Switching

C3 … C0	D8 – D6	Attenuation
1_H	0_H	0 dB
	1_H[1)]	–
	2_H	2 dB
	3_H[1)]	–
	4_H	4 dB
	5_H	5 dB
	6_H	6 dB
	7_H	7 dB
3_H	0_H	8 dB
	1_H	10 dB
	2_H	1 dB
	3_H	3 dB
	4_H	– 4 dB
	5_H	– 3 dB
	6_H	– 2 dB
	7_H	12 dB

[1)] may not select

Access to CM

	Transparent Switching (i.e. the MUSAC-A works exactly like a MTSC)
	C3 … C0 = 0_H, 2_H, 4_H – F_H
D9	Validity bit: A logical 0 enables the programmed connection, a logical 1 tristates the outputs
D8 … **D0**	Logical line and time-slot number of the inputs
IA7… **IA0**	Logical line and time-slot number of the outputs
C3 … **C0, D9** – **D0**	Is written to the CM address IA7 – IA0
	Conference switching or multipoint switching mode C3 … C0 = 1_H, 3_H
D9	Validity bit: A logical 0 enables the programmed connection, a logical 1 tristates the outputs
D8 … **D6**	Output attenuation
D5 … **D0**	Conference control address
IA7 … **IA0**	Logical line and time-slot number of the outputs
C3 … **C0, D9** – **D0**	Is written to the CM address IA7 – IA0. D5 – D0 contain the address which points to the appropriate CCM location.

D8 – D0 and IA7 – IA0 contain the information for the logical line and time-slot numbers of the programmed connection, D8 – D0 for the inputs, IA7 – IA0 for the outputs. **Table 12** shows the programming of these bits for standard configuration, **table 13 and 14** for the primary access configuration.

Standard Configuration

Table 12
Time-Slot and Line Programming for Standard Configuration

Standard configuration, all modes except space switch mode					
2-Mbit/s input lines	Bit Bit Bit	D3 D8 D9	to to	D0 D4	Logical line number Time-slot number Validity bit
4-Mbit/s input lines	Bit Bit Bit	D2 D8 D9	to to	D0 D3	Logical line number Time-slot number Validity bit
8-Mbit/s input lines	Bit Bit Bit	D1 D8 D9	to to	D0 D2	Logical line number Time-slot number Validity bit
2-Mbit/s output lines	Bit Bit	IA2 IA7	to to	IA0 IA3	Line number Time-slot number
4-Mbit/s output lines	Bit Bit	IA1 IA7	to to	IA0 IA2	Line number Time-slot number
8-Mbit/s output lines	Bit Bit	IA0 IA7	to	IA1	Line number Time-slot number

Primary Access Configuration

Table 13
Time-Slot and Line Programming for the Primary Access Configuration

2-Mbit/s input lines	Bit	D1	to	D0	Interface select in
	Bit	D3	to	D2	Line number
	Bit	D8	to	D4	Time-slot number
	Bit	D9			Validity bit
4-Mbit/s input lines	Bit	D1	to	D0	Fixed to 01 (system interface)
	Bit	D2			time slot number
	Bit	D8	to	D3	Time-slot number
	Bit	D9			Validity bit
8-Mbit/s input lines	Bit	D1	to	D0	Fixed to 01 (system interface)
	Bit	D8	to	D2	Time slot number
	Bit	D9			Validity bit
2-Mbit/s output lines	Bit	IA0			Interface select out
	Bit	IA2	to	IA1	Line number
	Bit	IA7	to	IA3	Time-slot number
4-Mbit/s output lines	Bit	IA0			Fixed to 0 (system interface)
	Bit	IA1			Line number
	Bit	IA7	to	IA2	Time-slot number
8-Mbit/s output lines	Bit	IA0			Fixed to 0 (system interface)
	Bit	IA7	to	IA1	Time-slot number

The interface select bits have to be programmed as shown in the following table:

Table 14
Interface Selection Bits

	System Interface	Synchronous 2-MHz Interface
Input lines	01	10
Output lines	0	1

Access 1 to CCM

C3 … **C0** Logical 4_H, 6_H

D9 Inversion bit: In a multiparty conference there is some risk of instability due to reflections at the hybrid. If these reflections are not cancelled, they will be summed up in the conference sum and will be transmitted to the subscriber, where again they could be reflected. In very big conferences (>> 4 subscribers) this behaviour could result in an instability.
To avoid this the PEB 2445 has the ability to invert every second conference channel, which has no audible influence on the speech quality. By this the noise due to reflections is compensated to a high degree.
The feature can also be applied to reduce noise due to line impedence mismatch.

D8 … **D0** Logical line and time-slot number of the inputs (see **table 12, 13 and 14**)

IA7/IA6 Logical 0

IA5 … **IA0** Conference control address

Access 2 to CCM

C3 … **C0** Logical 8_H, A_H

D9/D8 Noise suppression threshold

D7/D6 Input attenuation level

D5 Output attenuation level

Note: D7, D6, D5 are only relevant to conference mode; in the multipoint switching mode these bits must be logical 0.

D4 … **D0** Conference number: 21 independent simultaneous conferences are possible. By using the conference number $1F_H$ an attenuation or noise suppression can be inserted in a channel without conferencing.

IA7/IA6 Logical 0

IA5 … **IA0** Conference control address

Table 15

D9	D8	Noise Suppression Threshold
0	0	No noise suppression
0	1	Fifth step, first segment
1	0	Ninth step, first segment
1	1	Sixteenth step, first segment

Table 16

D7	D6	Input Attenuation Level
0	0	0 dB
0	1	3 dB
1	0	6 dB
1	1	9 dB

Table 17

D5	Output Attenuation Level
0	0 dB
1	3 dB

Note: The sequence of programming (access 1, access 2) is important.

4.6 Indirect Registers

4.6.1 Configuration Register (CFR)

Access: Read or write at address FE_H

Reset value: FF_H

AD7							AD0
1	**1**	**CUA2**	**CUA1**	**CUA0**	**FS**	**CFS**	**CPS**

CPS **Clock Period Select:** Device clock is set to 8192 kHz (logical 1) or 4096 kHz (logical 0).

CFS **Configuration Select:** The MUSAC-A works either in the primary access configuration (CFS = 0) or in the standard configuration (CFS = 1).

FS **Function Select:**
FS = 0: Multipoint switching
FS = 1: Conferencing

CUA0 … **CUA2** PCM encoding law and PCM-byte format

CUA0	**Encoding Law**
1	A-law
0	µ-law

CUA2	**CUA1**	**PCM-Byte Format**
0	0	No bits inverted
0	1	Even bits inverted
1	0	Odd bits inverted
1	1	All bits inverted

4.6.2 Clock Shift Register (CSR)

Access: Read or write at address FF_H

Reset value: 00_H

AD7							AD0
RS2	**RS1**	**RS0**	**RRE**	**XS2**	**XS1**	**XS0**	**XFE**

RS2 …**RS0** **Receive** clock **Shift**, bits 2 – 0. The received data stream is shifted in bit period steps.

RRE **Receive** with **Rising Edge**. The data is sampled with the falling (RRE = 0) or rising edge (RRE = 1) of the data equivalent clock.

XS0 …**XS2** **Transmit** clock **Shift**, bits 2 – 0. The transmitted data stream is shifted.

XFE **Transmit** with **Falling Edge**; data is transmitted with the rising (XFE = 0) or falling edge (XFE = 1) of the device clock.

Data stream manipulation according to these register entries only affects the system interface and only in the primary access configuration. The frame structure can be moved relative to the SP slope by up to 7 clock periods in half clock period steps. This register can hold non-zero values only for a CFR:CFS value of logical 0.

Identical non-zero entries for RS2 – RS0 and XS2 – XS0 as well as identical RRE and XFE generate an output time-slot structure which is 1 time-slot late relative to the input time-slot structure.

Identical 000 entries for RS2 – RS0 and XS2 – XS0 as well as RRE and XFE being logical 0 cause the input and output frames to coincide in time.

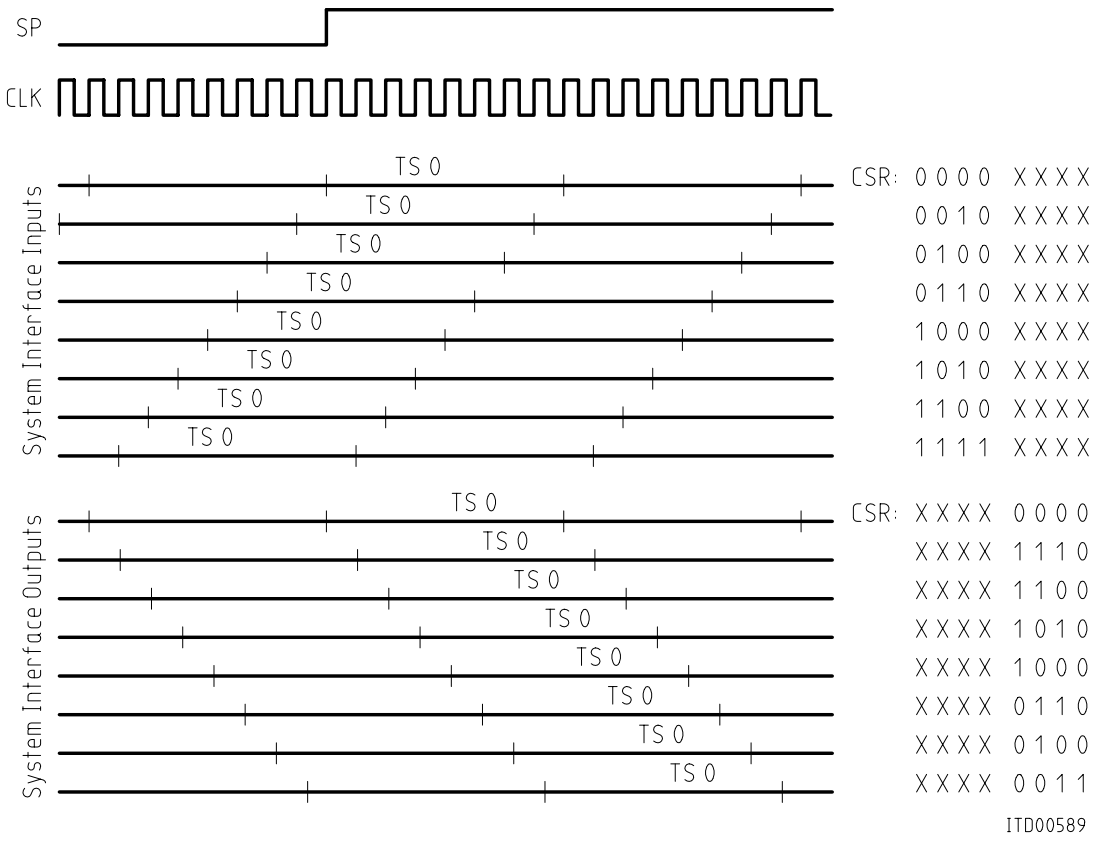


Figure 20
Clock Shifting

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	7	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.1 DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.0 2.7	V_{DD} + 0.4 V_{DD} + 0.4		CLK and $\overline{WR}$ only
L-output voltage		V_{OL}		0.45	V	I_{OL} = 2 mA
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Power supply current	operational CLK = 4 MHz CLK = 8 MHz	 I_{CC} I_{CC}		 5 10	 mA mA	 V_{DD} = 5 V, Inputs at 0 V or V_{DD}, no output loads
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V
Input leakage current at inputs with internal pull-down		I_{LPD}		700	µA	0 V < V_{IN} < V_{DD} to 0 V RES, ALE, A0, A1 only

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

5.2 Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
Output capacitance	C_{OUT}		15	pF
I/O	$C_{I/O}$		20	pF

5.3 AC-Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven to 2.4 V for a logical ‘1’ and to 0.4 V for a logical ‘0’.
Timing measurements are made at 2.0 V for a logical ‘1’ and at 0.8 V for a logical ‘0’.
The AC-testing input/output wave forms are shown below.

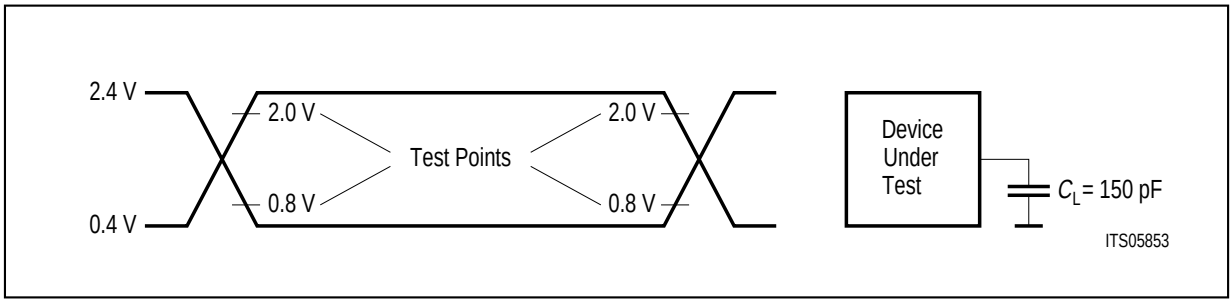


Figure 21
I/O-Wave Form for AC-Test

5.3.1 Microprocessor Interface Timing

5.3.1.1 Intel Bus Mode

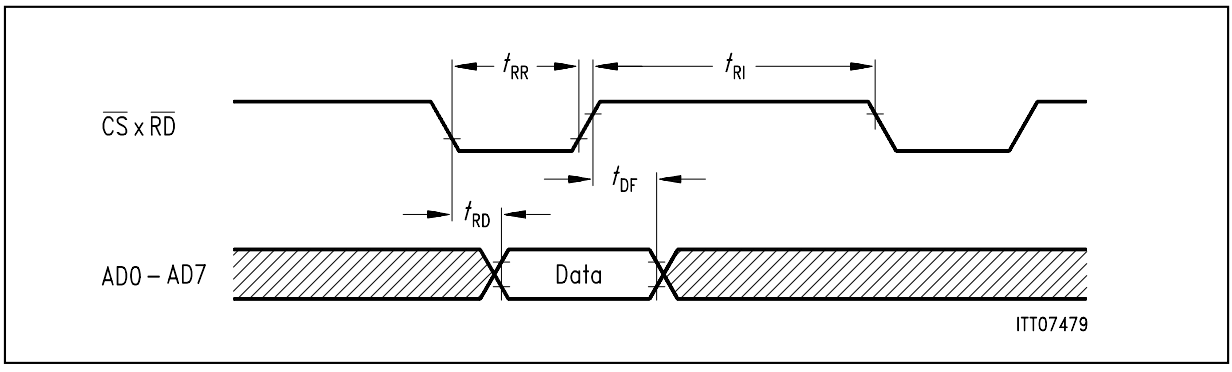


Figure 22
µP Read Cycle

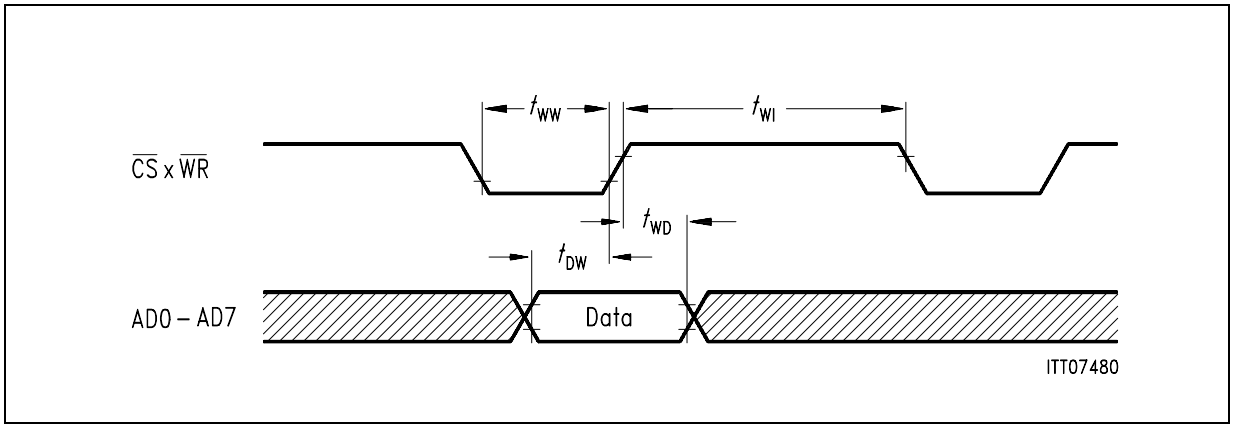


Figure 23
µP Write Cycle

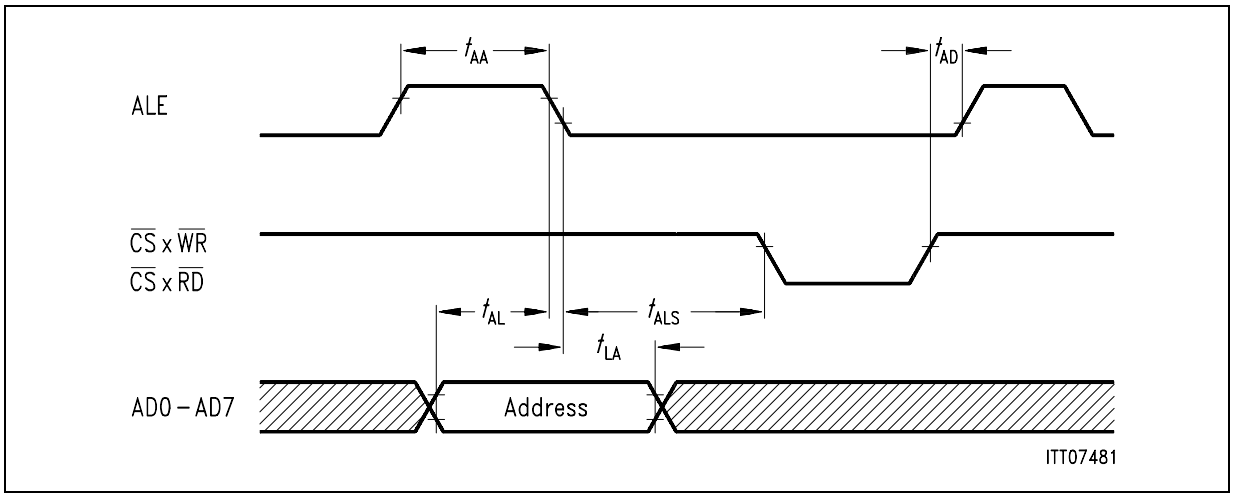


Figure 24
Multiplexed Address Timing

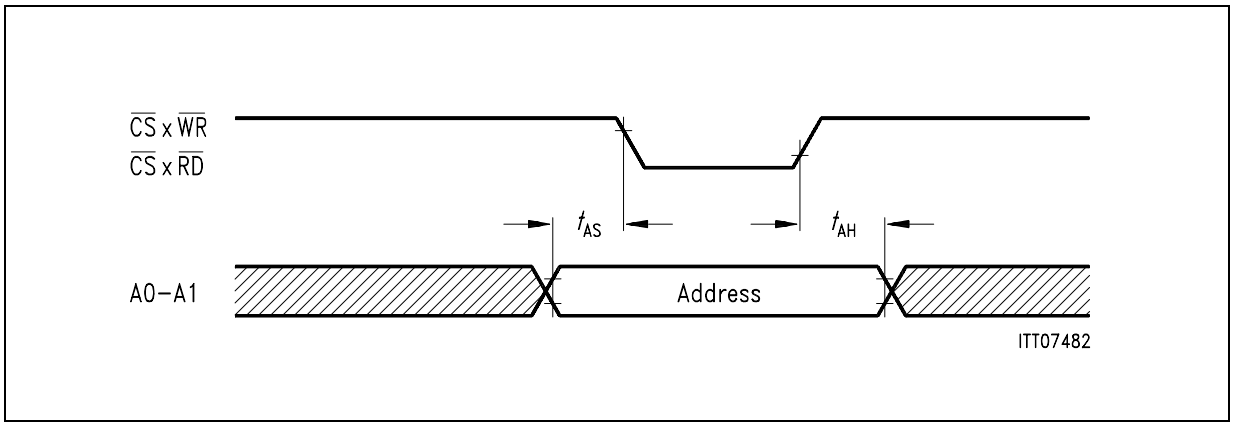


Figure 25
Non-multiplexed Address Timing

Table 18
Microprocessor Interface Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
ALE pulse width	t_{AA}	50	–	ns	–
Address setup time to ALE	t_{AL}	20	–	ns	–
Address hold time from ALE	t_{LA}	10	–	ns	–
Address latch setup time to $\overline{WR}$, RD	t_{ALS}	0	–	ns	–
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10	–	ns	–
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20	–	ns	–
ALE pulse delay	t_{AD}	15	–	ns	–
$\overline{RD}$ pulse width	t_{RR}	110	–	ns	–
Data output delay from $\overline{RD}$	t_{RD}	–	110	ns	–
Data float from $\overline{RD}$	t_{DF}	–	25	ns	–
$\overline{RD}$ control interval	t_{RI}	70	–	ns	–
$\overline{WR}$ pulse width	t_{WW}	60	–	ns	–
Data setup time to $\overline{WR}$ + $\overline{CS}$	t_{DW}	35		ns	–
Data hold time from $\overline{WR}$ + $\overline{CS}$	t_{WD}	20	–	ns	–
$\overline{WR}$ control interval	t_{WI}	70	–	ns	–

5.3.2 PCM Interface Timing

Table 19
PCM Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM input setup	t_S	15	–	ns
PCM input hold	t_H	30	–	ns
Output Delay	t_D	–	45	ns
Tristate Delay	t_T	–	66	ns

5.3.3 Clock and Synchronization Timing

Table 20
PCM Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock period 8 MHz high	t_{CP8H}	40	–	ns
Clock period 8 MHz low	t_{CP8L}	48	–	ns
Clock period 8 MHz	t_{CP8}	120	–	ns
Synchronization pulse setup 8 MHz	t_{SS8}	20	$t_{CP8} - 20$	ns
Synchronization pulse delay 8 MHz	t_{SH8}	0	$t_{CP8} - 20$	ns
Clock period 4 MHz high	t_{CP4H}	90	–	ns
Clock period 4 MHz low	t_{CP4L}	90	–	ns
Clock period 4 MHz	t_{CP4}	240	–	ns
Synchronization pulse setup 4 MHz	t_{SS4}	20	$t_{CP4} - 30$	ns
Synchronization pulse delay 4 MHz	t_{SH4}	30	$t_{CP4} - 10 + t_{CP4H}$	ns
Data clock delay	t_{DCD}	–	100	ns
Synchronization pulse low	t_{SPL}	100	–	ns

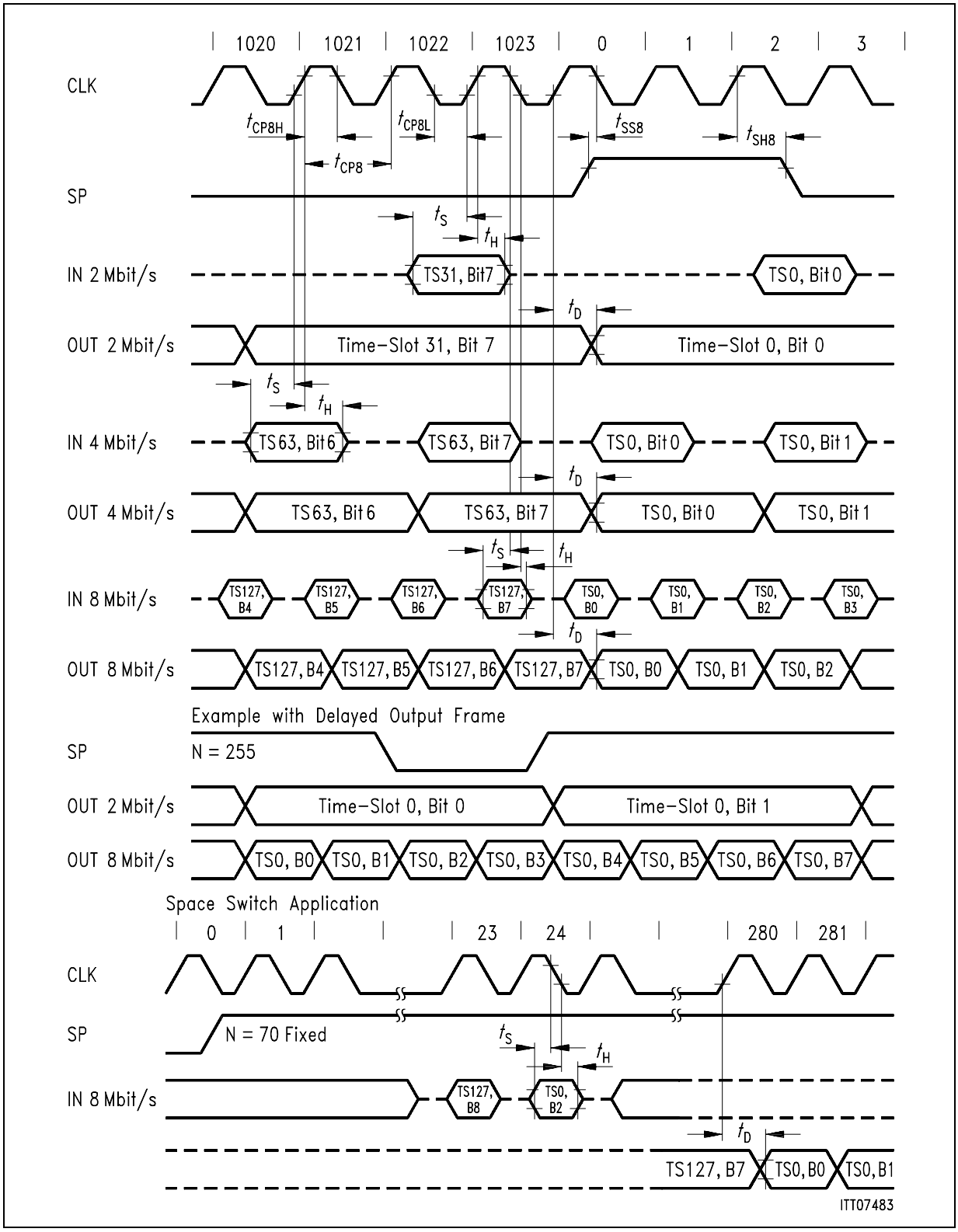


Figure 26
PCM Line Timing in Standard Configuration with a 8 MHz Device Clock

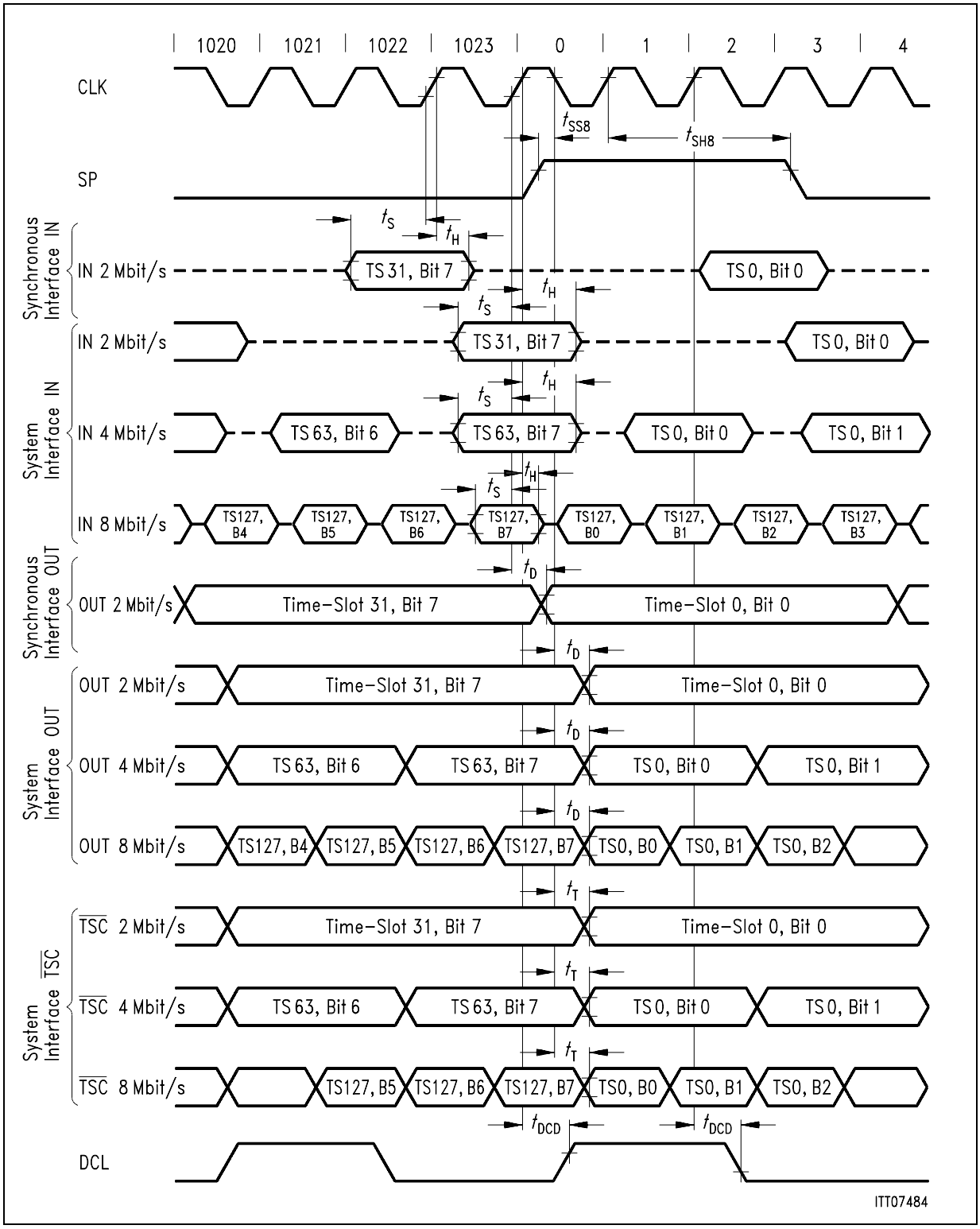


Figure 27
PCM Line Timing in Primary Access Configuration with a 8 MHz Device Clock and a CSR Entry (00010001)

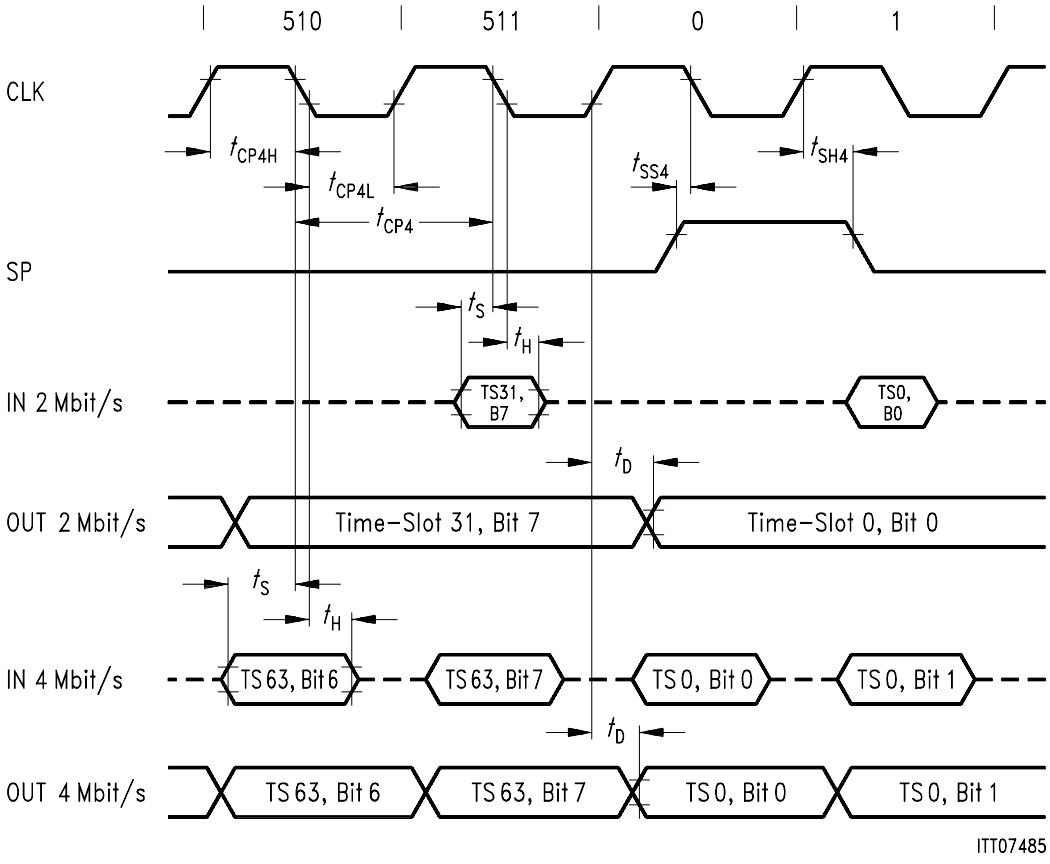


Figure 28
PCM Line Timing in Standard Configuration with a 4 MHz Device Clock

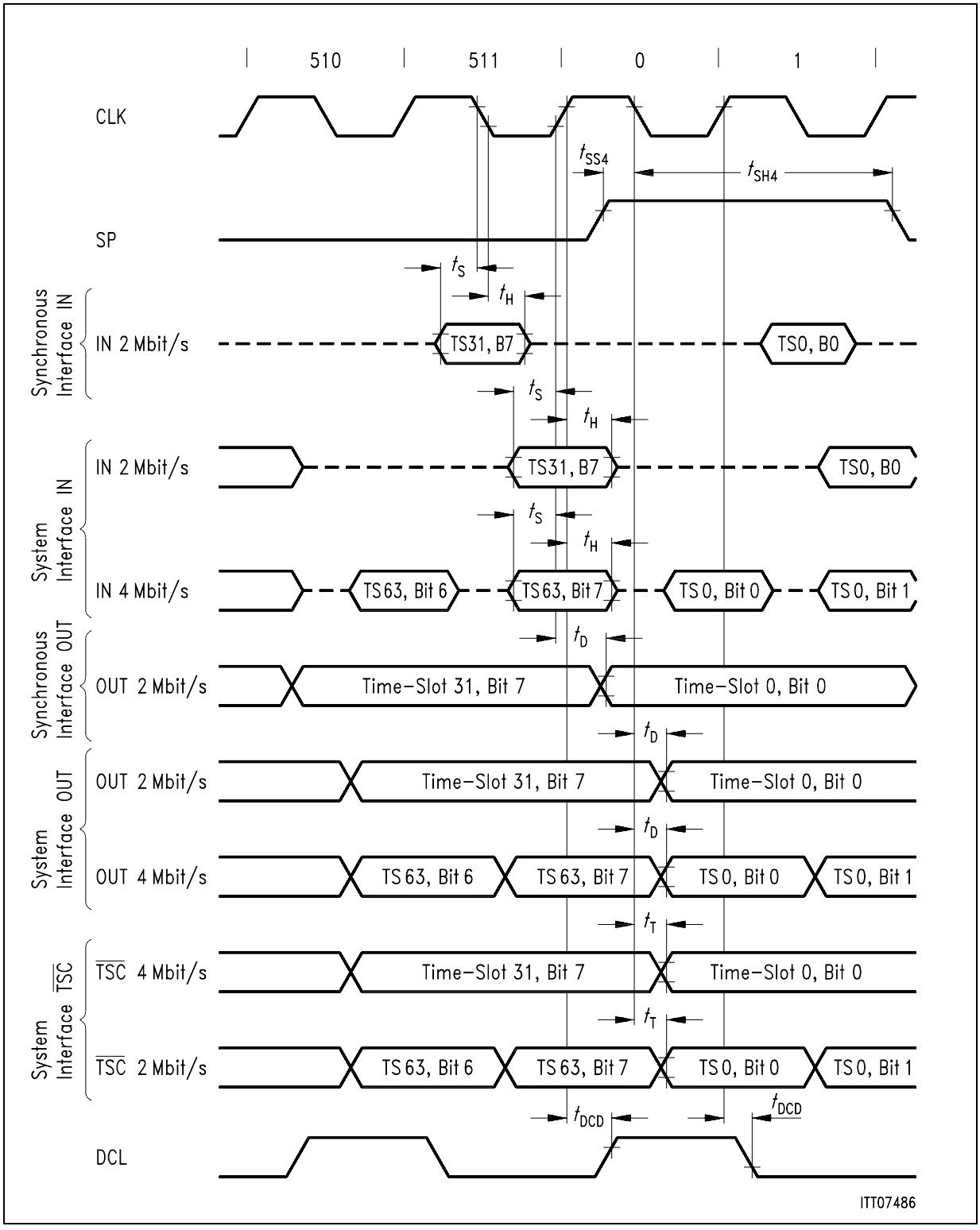
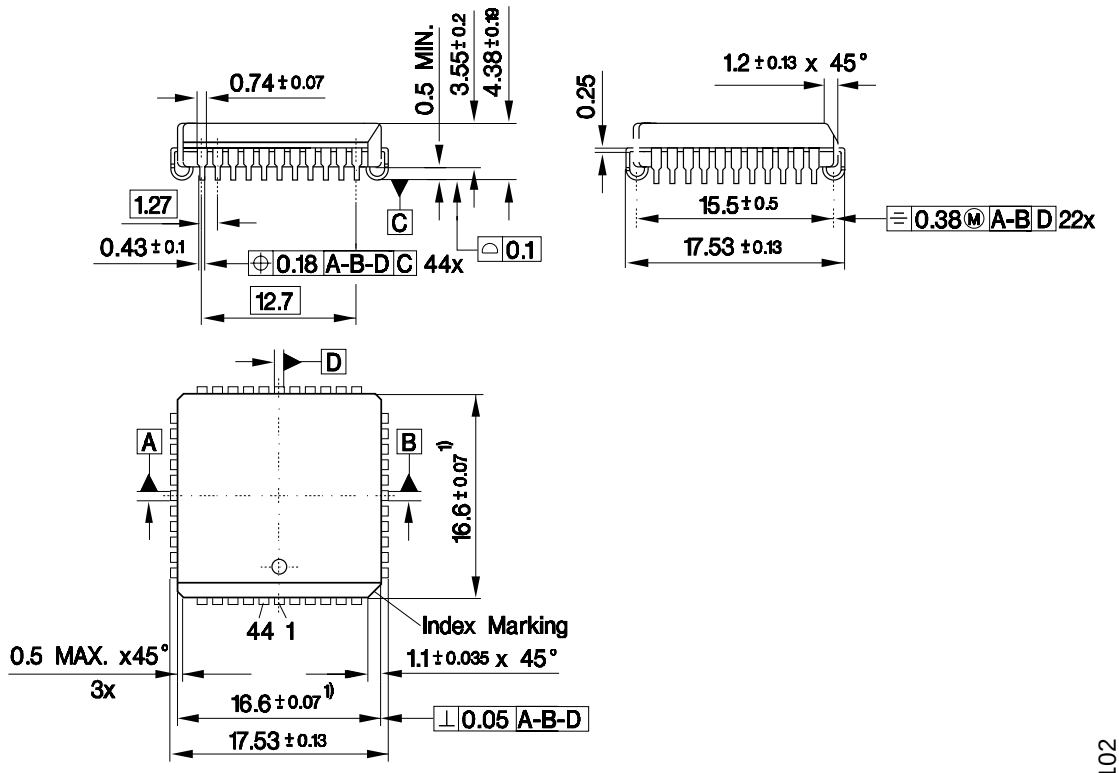


Figure 29
PCM Line Timing in Primary Access Configuration with a 4 MHz Device Clock and a CSR Entry (00010001)

6 Package Outlines

P-LCC-44 (SMD)
(Plastic Leaded Chip Carrier)



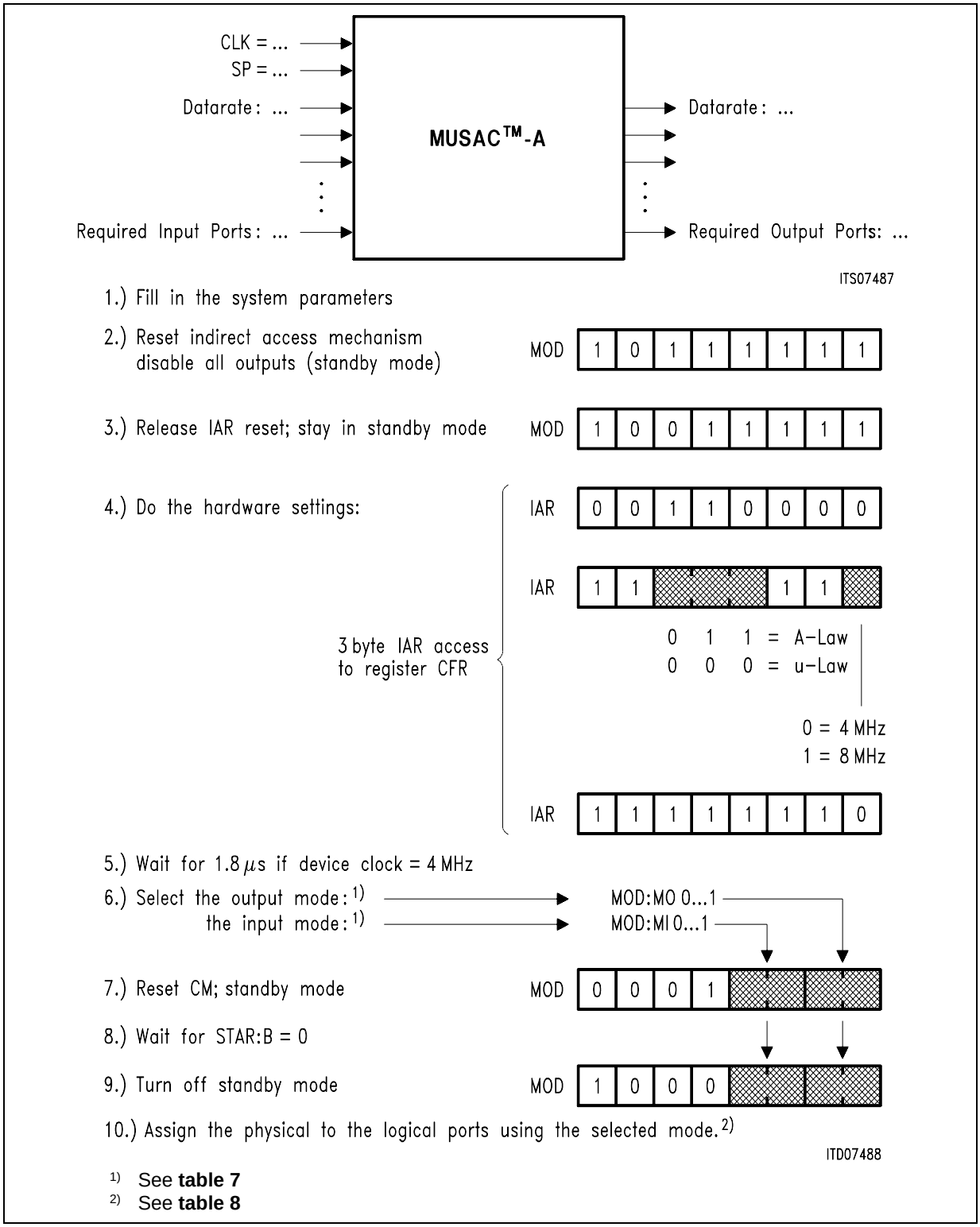
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

MD = Surface Mounted Device

Dimensions in mm

7 Appendix

7.1 Initialization for Conferencing in a PBX



1) See **table 7**
2) See **table 8**

7.2 Programming a Conference in a PBX

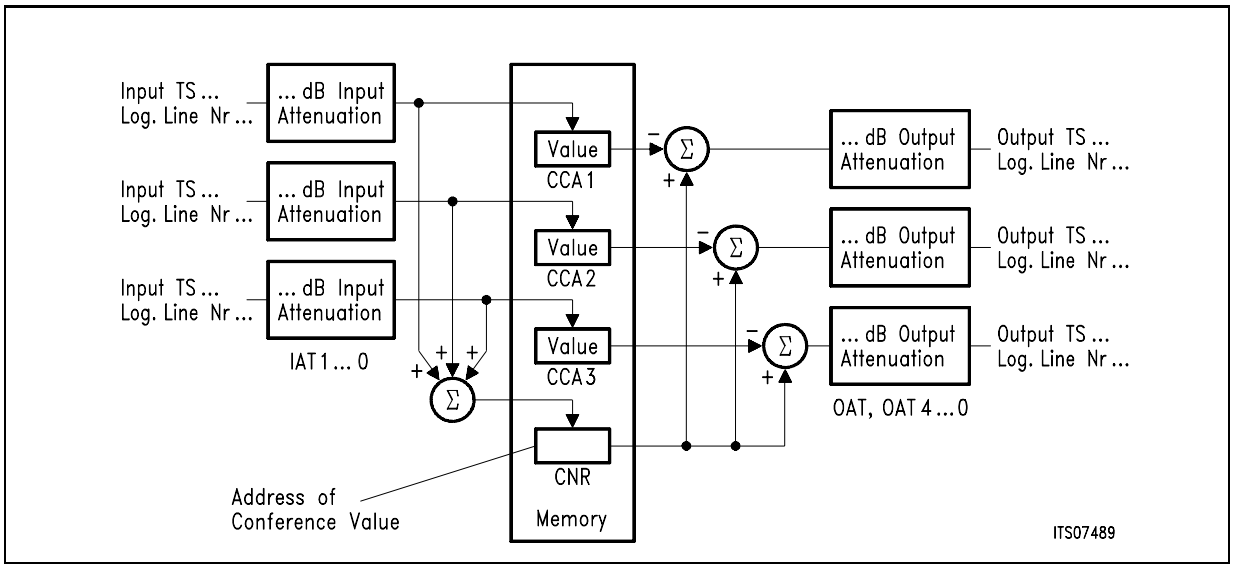


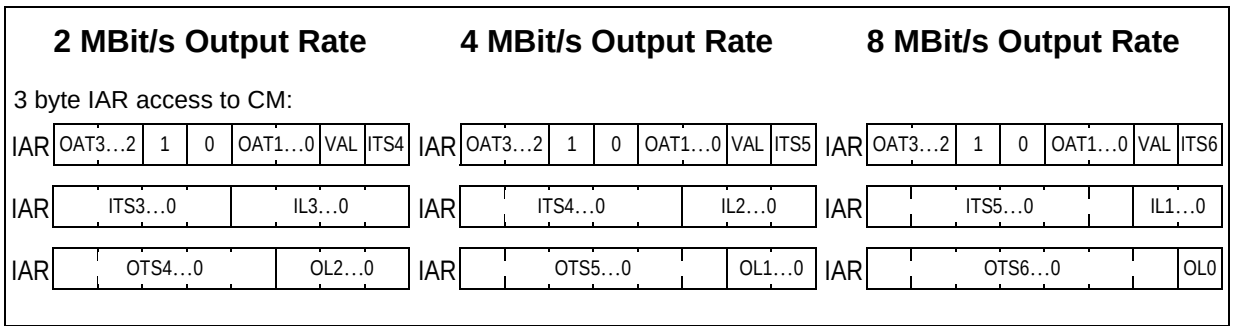
Figure 30

Table 21

Procedure for each Conference	Bits in IAR	Values for Subscribers		
		TE 'A'	TE 'B'	TE 'C'
1. Make a list of the conference subscribers				
2. Determine the input time slot Determine the logical input port	ITS6 … 0 L3 … 0			
3. Determine the output time slot Determine the logical output port	OTS6 … 0 OL2 … 0			
4. Find an unused conference number	CNR4 … 0			
5. Assign an unused conference control address to every conference input	CCA5 … 0			
6. Fix the input attenuation	IAT1 … 0			
7. Fix the output attenuation	OAT, OAT4 … 0			
8. Fix the noise suppression threshold	NOI1 … 0			
9. Insert the determined values in the corresponding bit positions of the 'MUSAC-A Work Sheet' (see **chapter 7.3** and **7.4**). Write the 9 bytes to the CM and CCM using the three byte IAR access.				

7.3 Programming Procedure for Switching TS's

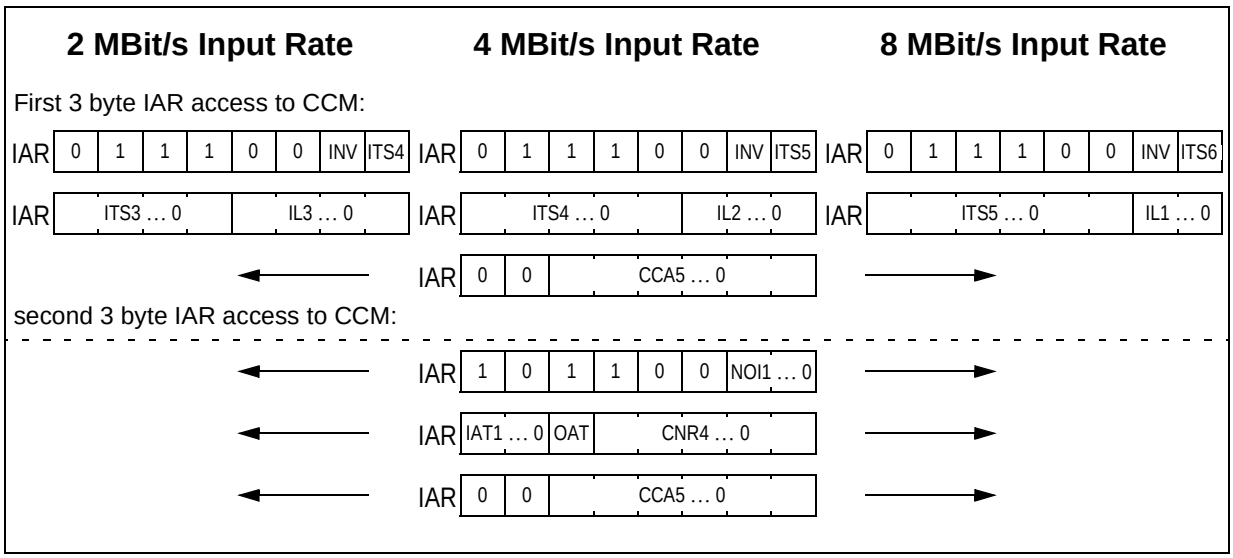
– Select a column for input and output rate
– Fill in the values of the bits
– Write the 3 bytes (from top to bottom) to register IAR

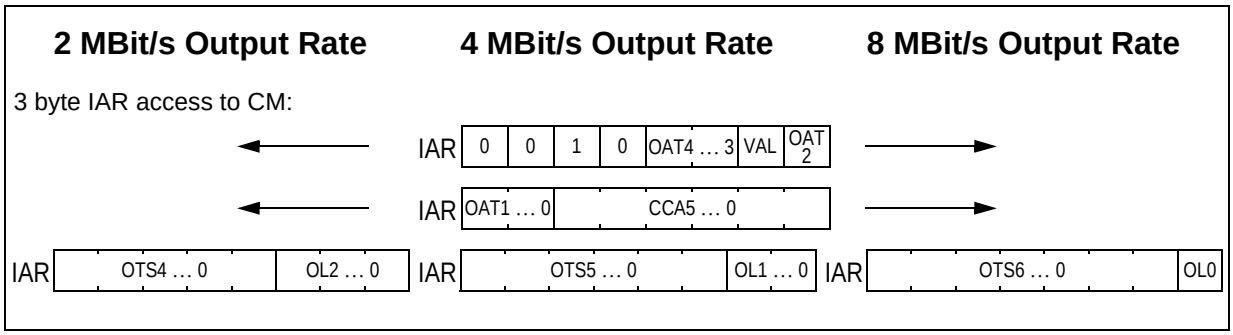


ITS6 … **0** **IL0** … **3**	Input time slot number Logical input line number
VAL	**Validity:** output enabled (= 0) output disabled (= 1)
OTS6 … **0**	Output time slot
OL2 … **0**	Logical output line number
OAT3 … **0**	**Output attenuation:** 0_H = 0 dB A_H = 1 dB 2_H = 2 dB B_H = 3 dB 4_H = 4 dB 5_H = 5 dB 6_H = 6 dB 7_H = 7 dB 8_H = 8 dB 9_H = 10 dB F_H = 12 dB E_H = – 2 dB D_H = – 3 dB C_H = – 4 dB

7.4 Programming Procedure for a PBX Conference

– Select a column for input and output rate
– Fill in the values of the bits by aid of **chapter 7.1** and **7.2**
– Write the 9 bytes (from top to bottom) to register IAR





INV	PCM data inverted (= 1) or not (= 0)
ITS6 … **0**	Input time slot number
IL0 … **3**	Logical input line number
CCA5 … **0**	Conference control address
NOI1 … **0**	**Noise suppression threshold:** 00 = no noise suppression 01 = 5th step, first segment 10 = 9th step, first segment 11 = 16th step, first segment
IAT1 … **0**	**Input attenuation:** 00 = 0 dB 01 = 3 dB 10 = 6 dB 11 = 9 dB
CNR4 … **0**	Conference number
VAL	**Validity:** output enabled (= 0) output disabled (= 1)
OTS6 … **0**	Output time slot
OL2 … **0**	Logical output line number
OAT	**Output attenuation:** 0 = 0 dB, 1 = 3 dB
OAT4 … **0**	**Output attenuation:** 01000 = 0 dB 11010 = 1 dB 01010 = 2 dB 11011 = 3 dB 01100 = 4 dB 01101 = 5 dB 01110 = 6 dB 01111 = 7 dB 11000 = 8 dB 11001 = 10 dB 11111 = 12 dB 11100 = – 4 dB 11101 = – 3 dB 11110 = – 2 dB **other bit combinations not allowed!**