# ADF7010 RF Transmitter Evaluation Board

## EVAL-ADF7010EB1

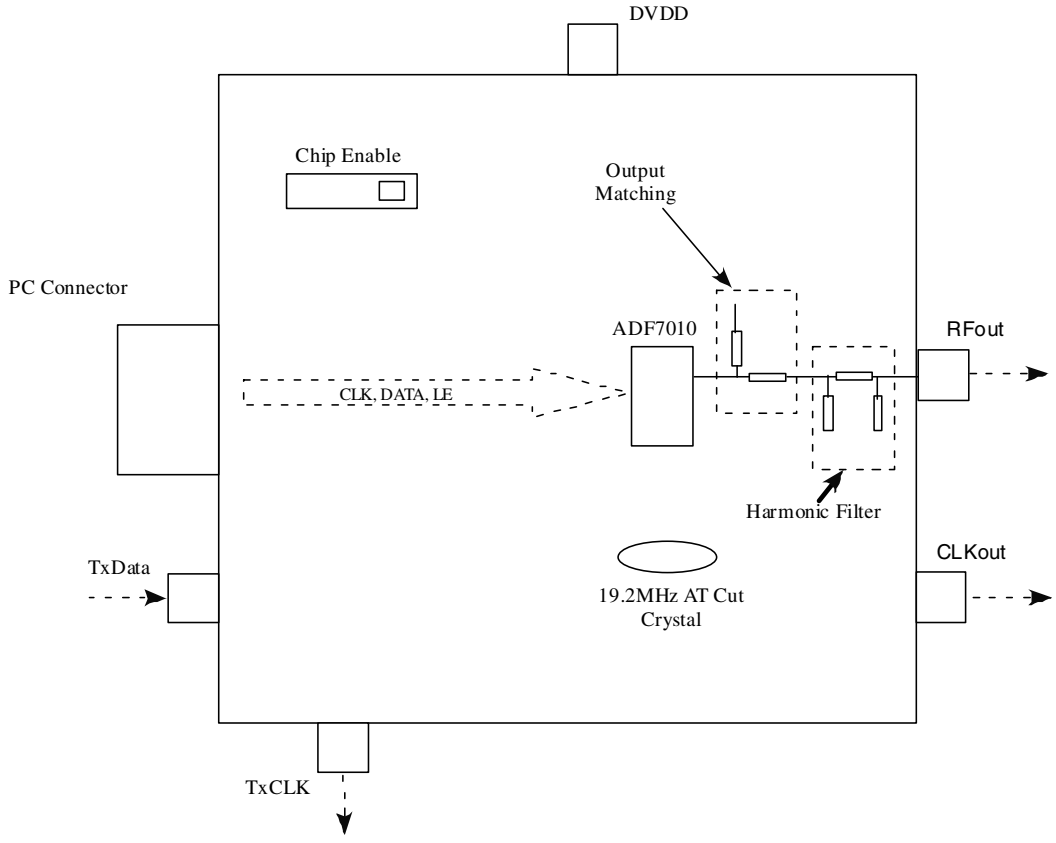
### FEATURES

**ADF7010 ISM band transmitter.**
**Software programmable modulation modes of FSK, ASK and OOK.**
**Loop Filter set-up for operation at 19.2 kbits/s**
**Free SIMPLL loop filter software available for design and simulation of filter**
**On board 19.2MHz crystal - No external reference needed**
**Programmable CLKout frequency and output power**
**Software is Windows 95/98/2000/ME/XP compatible**

### GENERAL DESCRIPTION

The ADF7010 is an ISM band transmitter capable of FSK, GFSK, ASK and OOK modulation in the ISM bands. The evaluation board contains all the components required for wireless data transfer, including loop filter, output matching, and SMA components. The loop filter software allows the user to design and change the loop filter components.

### BLOCK DIAGRAM

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**Hardware Description**

The evaluation board comes with a cable for connecting to the printer port of a PC. The silk screen and cable diagram for the evaluation board are shown below. The board schematic are shown on page 3

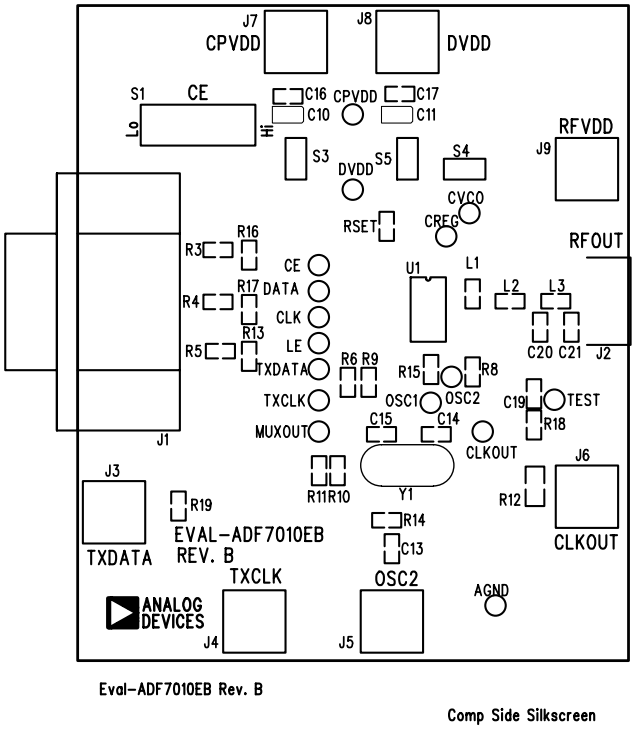



*Figure 1. Evaluation Board Silkscreen*

The ADF7010 should be supplied with an external supply of 2.3V to 3.6V. There is an on-board 19.2 MHz AT crystal from FOX. The crystal combined with 33pF shunt capacitors provide the low cost frequency reference for the PLL. The loop filter is designed for use with a 19.2MHz PFD frequency. This means that the R divide should be set to 1. The N-divide should be set to whatever factor is required to multiply the 19.2MHz PFD frequency up to the required output frequency.

The necessary SMA connectors are included to interface the part to the measurement instrument. (Normally a spectrum analyzer). **Care should be taken to ensure that no DC level exists at the RFout SMA - DC into the front of measurement equipment will damage the input. There is a 150pF ac coupling capacitor at the output.**

The parallel port has 5V voltage levels, so there is a voltage divider to bring this down to levels acceptable to the ADF7010.

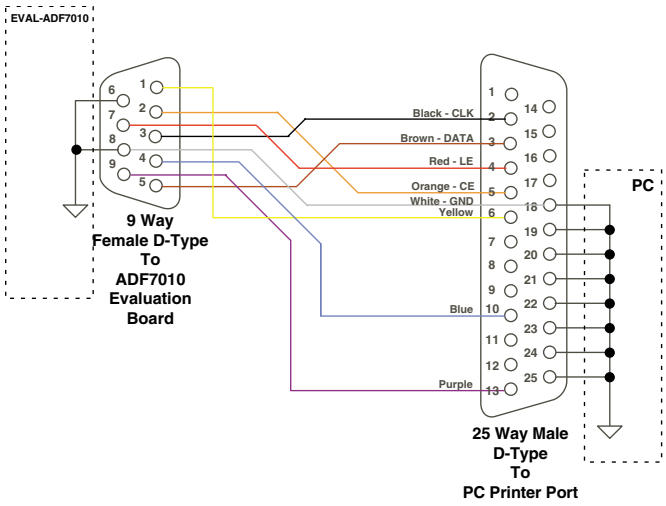



*Figure 2. PC Cable Diagram*

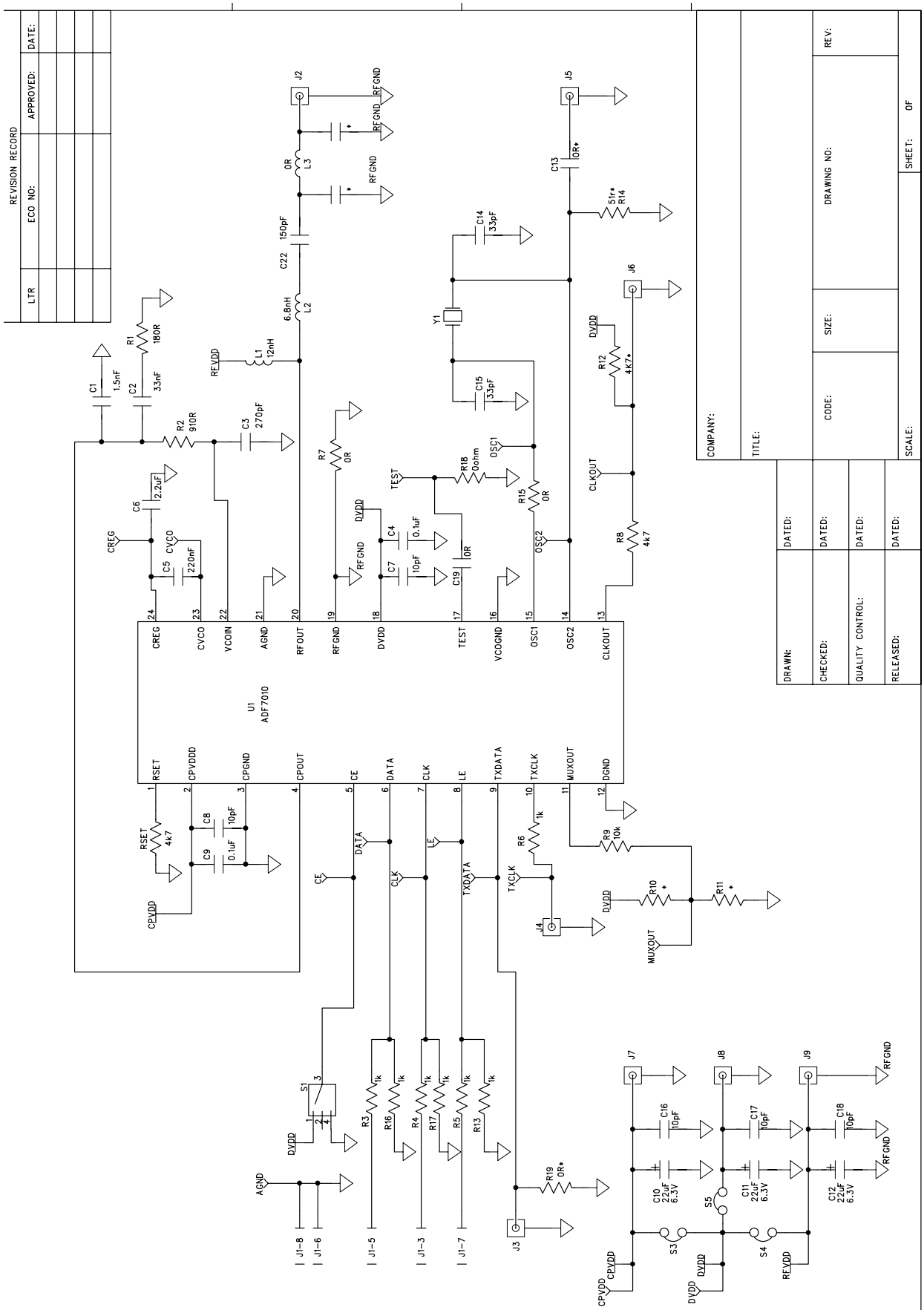



*Figure 3. Evaluation Board Circuit Diagram (Page 1)*

**Software Description**

The ADF7010 software comes on an installation CD. Hit the start button and choose run. Select D:\setup.exe - This will run the Installshield setup utility. Choose the directory you wish to install into and proceed.
Once the program is setup run ADF7010.exe to run the program. The window shown below should appear - you will need a screen resolution of **1024 x 768** to use the program.

You should start by setting up the output frequency. Click the '915.3MHz' to bring you to the PLL sub-menu.Type in the output frequency, desired PFD frequency (default 19.2MHz), and the crystal frequency (default = 19.2MHz) used and hit the 'calculate' button. The prescaler can be chosen by clicking the '4/5'. The blue toggle buttons allow the user to change between two settings. The green and red toggle buttons turn a feature on or off.

The charge pump current and power down should be set next. To move to the charge pump current sub-menu click on the '2.02mA' setting in blue. Within the charge pump menu you can choose to set the Rset resistor and the charge pump current. The default value for Rset on your eval board is 4.7k. This is an external resistor and will change the available charge pump settings. You will have to adjust the loop filter for any changes to the charge pump current setting, as this will change the stability of the filter. You can use ADIsimPLL to model these effects.

Click on the drop-down box to select the modulation. To see the part in PLL mode you should select ASK. This will allow the user to evaluate phase noise, reference spurs and output power levels available. The initial offset in the crystal will cause the absolute output frequency to be off. This error can be calibrated out using the fractional-N registers.

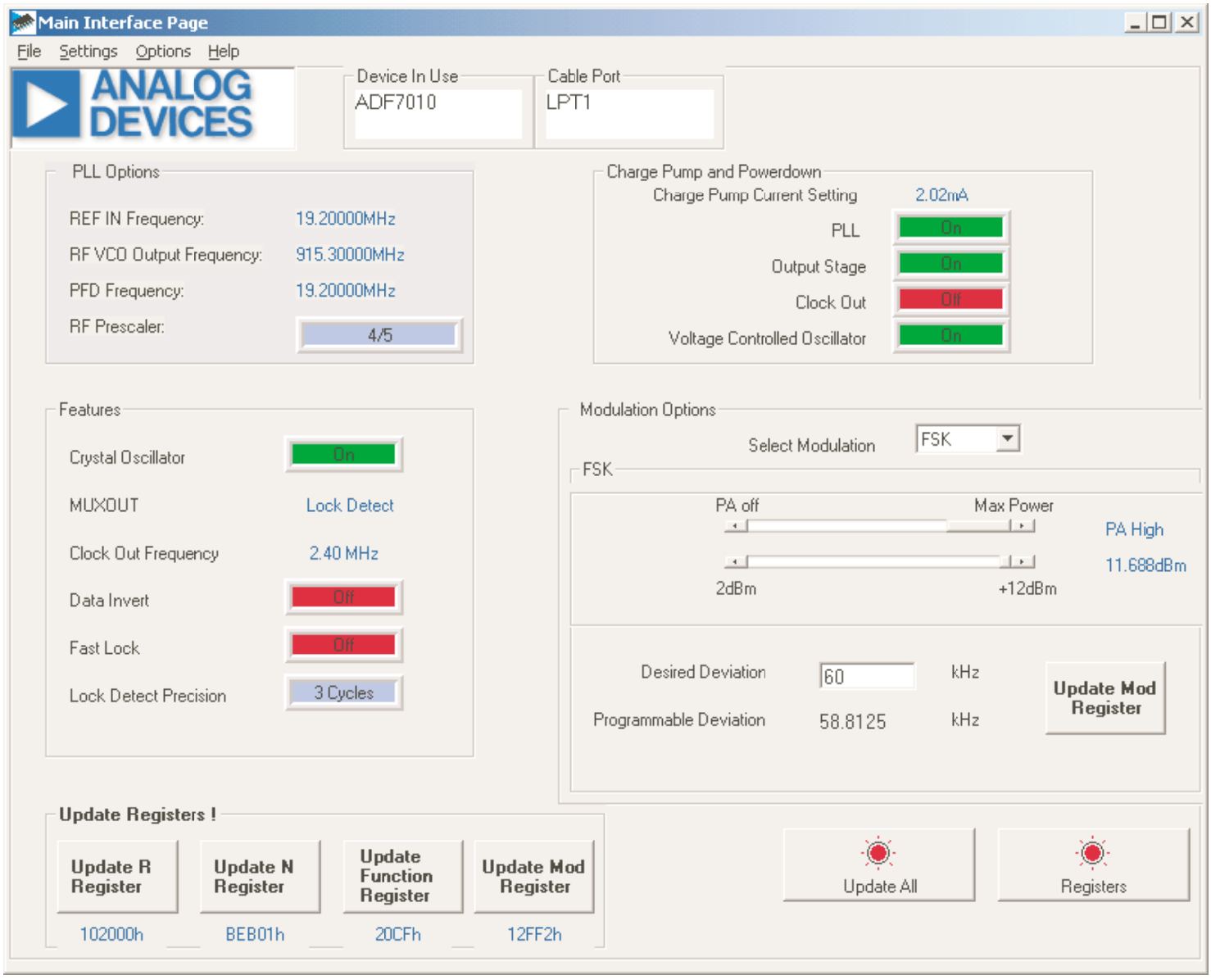



*Figure 4 Software Front Panel Display*

## GETTING STARTED WITH THE ADF7010

The evaluation performed will be specific to each application, but this section will enable to user to familiarise themselves with the features of the ADF7010.

### Initial Set-up

The board will be set-up will RFVdd and CPVdd tied to the DVDD supply. Set this to 3V, and use a current meter to monitor the supply current. With Chip Enable (low) the part will be set to its default condition as goverened by the values preset internally in the registers. There will be no current drawn. Once CE is brought high the part will become active and approximately 0.8mA is drawn.

| | |
|---|---|
| Crystal Oscillator circuit | ON |
| CLKout | ON |
| CLKout Divide | 16 ( 8 x 2) |
| PLL | OFF |
| PA | OFF |
| Data Invert | OFF |
| MuxOUT | Regulator Ready |

For the user, this means that there will be a signal at 19.2MHz / 16 at the CLKout pin, and also that the crystal oscillator is running.

### Programming the ADF7010

Programming is accomplished using the parallel port of the PC. The interface is SPI compatible, and the LPT1 levels are divided down to make them compatible with the lower Vdd of the transmitter. The programming lines are pulled low internally once programming has been completed. This is important as the parallel port can source current to the part if it's 'high' voltage is at a higher level than the Vdd of the ADF7010.

### Setting the output frequency

The output frequency is set by the PFD (Phase Frequency Detector) frequency x by the N divider value. The default setting for the PFD is 19.2MHz. This is accomplished by setting the R-divider to 1. The N value is comprised of an integer and fractional part. The output frequency is -

$$\text{PFD frequency} \times \left(\text{Int} + \frac{(2^3 \times \text{Fractional}) + \text{Error}}{2^{15}}\right)$$

So 19.2MHz * (47 + 2752 / 2^15) = 915.3MHz
In this case the integer register contains 47 and the Fractional register is set to 2752.

### Test Procedure for the ADF7010

Use a supply of 3V to power the part. Monitor the current using an ammeter.

1. Set CE high using the switch. Ensure that all jumpers on the board are tied together. The current drawn should be <1uA. This is the standby current.

2. Monitor the CLKout pin using a scope. The output frequency once CE is high is 19.2MHz / 16. This is the power-up default. The crystal is oscillating and the CLKout feature is working.

3. Set the output frequency to the desired frequency using the evalutation software. Hit the calculate and load now buttons to see what N and R values are written and to load the ADF7010 N and R registers.

4. Return to the main menu. Select OOK modulation, and set Data Invert to 1. This will put the part in PLL mode with the output power selectable by changing the power level. Update the Modulation and Function register.

5. Examine the output using a spectrum analyser. The output should be locked to the programmed output frequency (There will be some error associated with the crystal). You can change the output level by adjusting the output power in the OOK window.

6. Re-Enter the 'set frequency' menu and change the output frequency and verify it covers your required frequency range.

7. Phase Noise and Spurious
The ADF7010 can operate in both in integer and fractional PLL modes. When the part is in ASK or OOK mode and the fraction is zero then the part is in integer mode and the sigma-delta is powered down.

In FSK and ASK (with F >0) the sigma delta is on and the output can be changed in steps of PFD/2^12. To measure the spurious set the Marker to peak search and locate the carrier. Using the marker delta function on the spectrum analyser set the next highest peak. In integer mode the spurious components will be at Carrier + Fpfd, Carrier + 2Fpfd, etc. In fractional mode the spurs will be at pfd * fraction and its harmonics. e.g. If the fractional register is 2048, and the fraction is 1/2, then there will be a fractional spur at Fpfd / 2. The loop filter will significantly attenuate fractional spurs, that are at a frequency many times the loop BW, away from the carrier.

It is for this reason that 19.2MHz is chosen as the crystal reference as it allows most channel spacings (30kHz, 40kHz, 100kHz,400kHz) to be divided into it easily. This results in bigger fractions, and spurious that are well attenuated by the loop filter.

The phase noise is measured by moving to a 10kHz span on the spectrum analyser, and setting the marker delta at 2kHz. Turn marker noise on. A typical measurment for 0dBm output power is -80dBc/Hz. Increased output

power will result in an increased noise floor. Typical phase noise at +9.6dBm is -73dBc/Hz.

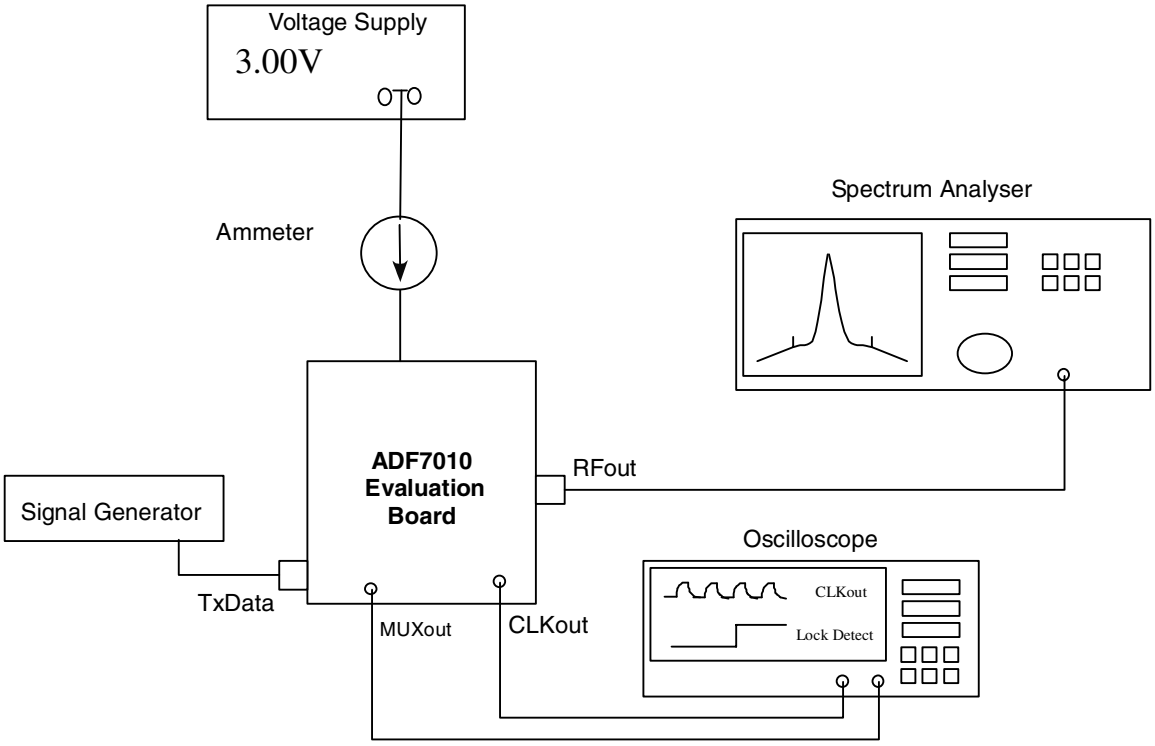



*Figure 4. Evaluation Board Test Setup*

**MUXout feature**

The MUXout feature is very useful in the debug and system use of the ADF7010. It allows access to internal sections of the IC such as the R-divider and N-divider outputs. The R-divider/2 can be used to check that the crystal oscillator is working, and that the R-divider is dividing the crystal frequency down to the Fpfd as expected. For the evaluation board, the crystal is chosen as 19.2MHz and the PFD is at 19.2 MHz. The R-divider/2 output will look like a 9.6MHz square wave. When the PLL is locked, the N-divider output will be in phase and at the same frequency as the R-divider. This can be verified by setting the MUXout to N-divider / 2. The result should be a 9.6MHz square wave.

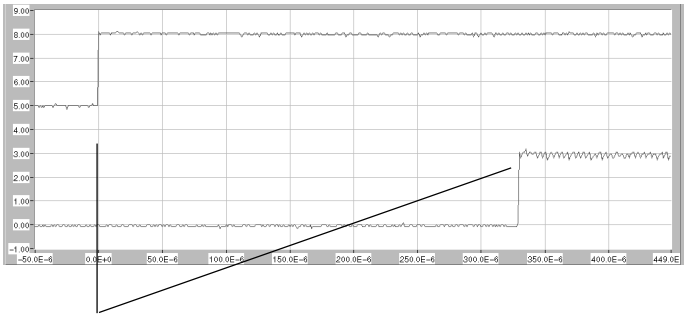
*Regulator Ready* - The ADF7010 goes into complete powerdown when Chip Enable (CE) is brought low. The values in the registers are lost and the serial interface is disabled. When CE is brought high there is a delay before the regulator voltage settles to the correct level (2.2V). By default the MUXout is set to regulator ready. When CE is brought high the MicroController must wait until the regulator ready (reg_ready) signal is high (at MUXout) before the ADF7010 can be programmed.

The part is initialised by programming each of the 4 registers. Usually, MUXout is set to *Lock Detect* (Digital). There is a delay associated with the VCO being enabled and also the loop has to settle to the output frequency as defined by the N and R-registers. Once the part is locked to the correct frequency the Lock Detect signal goes high. *It is therefore a good idea to wait for Lock Detect signal to go high before enabling the output stage to ensure there are no unwanted tranmissions at incorrect frequencies while the PLL is attempting to lock.*

**Start-up Procedure**

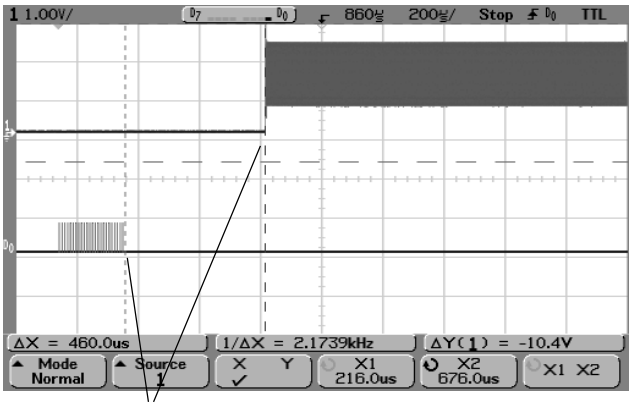
There is specified start-up time/sequence from the CE going high to the ADF7010 being ready to transmit

1. The regulator works at a nominal voltage of 2.2V. It supplies the reference voltage to the serial interface and most blocks of the tranmitter. Due to the large Creg capacitor, there is a settling transient associated with this. Before the part can be programmed the regulator voltage must have settled. This can be monitored by the default condition on MUXout (reg_ready).



*Regulator start-up time = 300us, Vdd = 3V, Creg = 4.7uF*

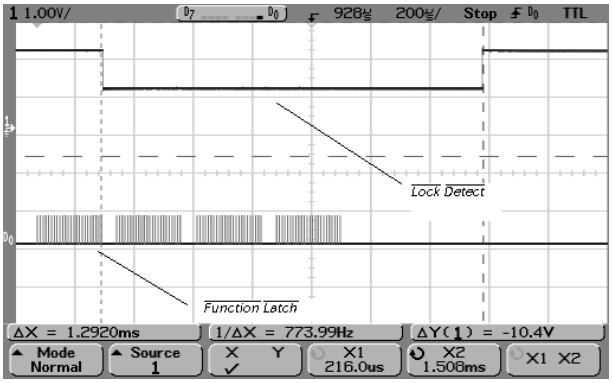
The crystal oscillator (enabled by default) needs to power up. This is determined by the Q of the crystal, and the supply voltage. A CLKout signal will appear at Fcrystal / 16 at the CLKout pin, once the oscillation has reached sufficient threshold to trigger the R-divider.




*Crystal start-up time = 460us, Vdd = 3V, Xtal AT 19.2MHz.*

2. The PLL and VCO also have an associated power-up time.Once the VCO is active (70us approximately), the PLL will attempt to lock. This will occur when the N-divider output and the R-divider output are at frequency and phase locked at the PFD (Phase Frequency Detector). The ADF7010 features a Digital Lock Detect which goes high at MUXout when the PLL is locked.

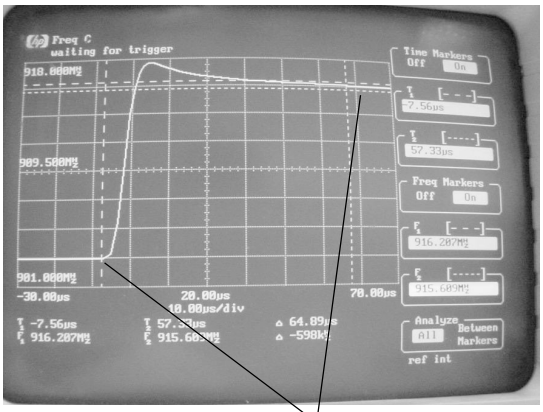
The total start-up time is typically 1.2ms for 3V operation with a 40kHz loop BW.



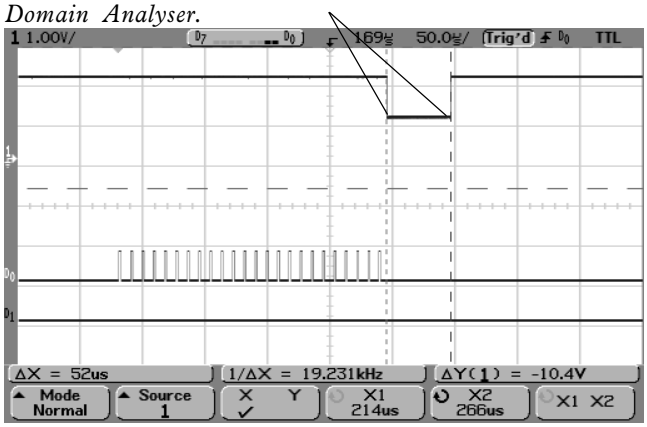

*Start-up time for ADF7010 from Function Latch being programmed to Lock Detect going high, Vdd = 3V*

The Lock Detect should be monitored then to determine when it is OK to transmit. However there is a delay between the Lock Detect and when the PLL is locked to 1ppm.

This is shown below for a 12.4MHz jump. The Lock Detect shows a locked PLL at 42us. The actual lock time to 1ppm is 50% more than this. This can be used as a rule of thumb for frequency to frequency lock. For a start-up locked condition it is relatively much less.




*The lock time as given by the Digital Lock Detect from MUXout shows a 40us jump time for a 12MHz jump. The actual lock time is 65us as shown from the Modulation Domain Analyser.*



**Designing Loop Filters with ADIsimPLL**

The design of a loop filter for a PLL based transmitter is crucial to its performance. For an FSK based system it determines how quickly the jump from frequency 1 to frequency 2 can be made. In a frequency hopping system it determines how much time is 'wasted' when jumping from one hopping frequency to another. Often we use as wide a bandwidth as possible while still meeting FCC regulations. A good 'rule-of-thumb' is 5 to10 times the datarate. (e.g. 19.2kbits/s datarate requires a 100kHz Loop BW).

For an ASK based system, there will be some 'pulling' of the VCO when a significant output level changes occurs when the data transitions between a mark and a space. To minimise this, a wide loop BW (300kHz) should be designed even for lower datarates, to pull the output frequency back to the correct value quickly.

ADIsimPLL can be found on the Evaluation CD. This allows simple accuarate design of loop filters with real components in several configurations. The next version will have several additonal functions for ADF7010 users.

**EXAMPLE DESIGN**

FSK based frequency hopping system
Designed to meet FCC 15.247

| | |
|---|---|
| Datarate | 19.2kbits/s |
| Crystal | 19.2MHz AT |
| Requires | 50 Hopping Channels |

The 'rule-of-thumb' of loop filter BW points being 5-10 times the datarate.

| | |
|---|---|
| Desired Loop BW | 100kHz |

Increasing the phase margin damps the response and so reduces the overshoot resulting in a better FSK spectrum.

| | |
|---|---|
| Desired phase margin | 60 degrees |

The charge pump current should be set to 2.02mA to optimise noise performance. Normally the effects are negligible. Some users may wish to set the charge pump current to ICPmax / 2, so they can switch the current to ICPmax when jumping from one frequency to another to temperoraily increase the loop BW and reduce settling time. The gains are not significant.

| | |
|---|---|
| Icp | 2.02mA |

The PFD frequency should be chosen to be a max. There are 2 good reasons for this. The bigger the PFD frequency - the less the multiplication factor (N) to the output frequency. Since phase noise is multiplied up by 20 log N, doubling the N will degrade phase noise by 3dB's.
The 2nd reason is to minimise integer boundary spurs. Integer boundary spurs are created when the fractional value is either near zero or near the max F. These spurs in-band are typically of the order of -25dBc. By avoiding fractions near integers, the spurious are reduced to < 45dBc at 1MHz offset with a 100kHz loop filter. Higher PFD frequencies create fewer of these integer channels in the desired band, therefore reduce the occurances of integer boundary spurs.

| | |
|---|---|
| PFD frequency | 19.2MHz |

The VCO on the ADF7010 is internal. The tuning sensitivity plots (Kv) are shown in the datasheet. As the Kv increases so does the loop BW. A Kv of 80MHz/V at 915MHz is typical.

| | |
|---|---|
| Kv | 80MHz/V |

Designing the loop filter - ADIsimPLL

Run ADIsimPLL
1) Select 'Create a new PLL design'
2) Choose Output Frequency in the desired range.

| | |
|---|---|
| Min Frequency | 902MHz |
| Max Frequency | 928MHz |

Channel spacing is 400kHz (50 x 400kHz = 20MHz)

3) Select Fractional-N - Use the default Frac-N which is the ADF4252_RF

Select Fractionality = 48

4) Select custom VCO and set Kv = 80MHz/V

5) Select custom reference (crystal) = 19.2MHz

6) Use the next key to select the loop filter with an extra RC for spurious attenuation. This is a 3rd order integrator and is ideal for Frac-N designs.

7) Click Finish to see the simulation

8) On the left hand side of page, expand the chip and make Rset = 5.6k. Icp = 2.1mA which is close to our actual Icp.

9) Expand the loop filter section. Set the Loop BW to 100kHz. Set the phase margin to 60 degrees.

10) Click on 'Tools' on the top menu and 'Build' to generate the loop filter from real capacitor and resistor values.

**Using GFSK on the ADF7010**

What is GFSK ? GFSK stands for Gaussian Frequency Shift Keying, and it represents a filtered form of frequency shift keying. The data to be modulated to RF is pre-filtered digitally using an Finite Impulse Response (FIR) filter. The filtered data is then used to modulate the sigma-delta fractional-N, to generate sprectrally-efficient FSK.

FSK consists of a series of sharp transitions in frequency as the data is switched one level to the other. The sharp switching will generate higher frequency components at the output resulting in a wider output spectrum.

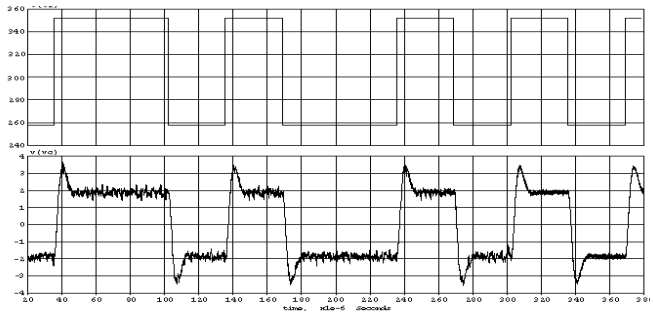


*Figure 5. FSK Modulation shown on a modulation domain analyzer. The sharp data transitions results in frequency overshoot as the PLL jumps from one frequency to another.*

With GFSK the sharp transitions are replaced with 3 smooth steps. The result is a gradual change in frequency. As a result the higher frequency components are reduced and the spectrum occupied is reduced significantly.

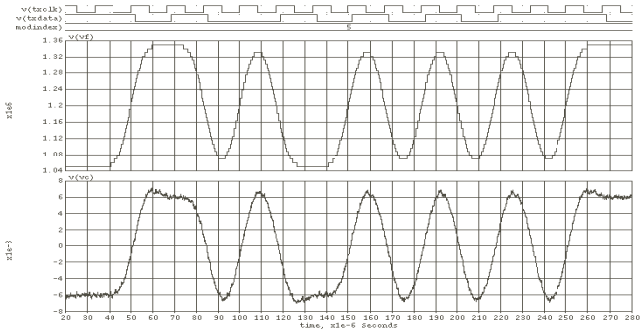


*Figure 6. GFSK Modulation of the same data signal is shown. The upper signal represents the pre-filtered data which is fed to the sigma delta modulator. The output observed on the modulation domain analyzer(lower signal) shows almost no overshoot.*

GFSK is useful where the spectral occupancy is crucial. It requires some extra design work, as the data most be clocked into the ADF7010 at a constant rate.

The bits designated for GFSK are in the modulation register. To decide on what these should be set to, the following are required

Frequency Deviation - The deviation between the carrier and a high, or half the distance between a zero or a one frequency.

Data Rate -

The following formulas are use to find m (modulation control (MC1 to MC3)), divider factor (D1 to D7) and Index Counter (IC1 and IC2).

$$\text{GFSK Deviation (Hz)} = \frac{2^m \times F_{PFD}}{2^{12}}$$

where m is the mod control, bits MC1 to MC3

$$\text{Data Rate (bits/s)} = \frac{F_{PFD}}{\text{Divider factor x Index counter}}$$

| Example | |
|---|---|
| Data Rate(desired) | 19.2kbits/s |
| Deviation (desired) | 19.2kHz |
| PFD Frequency | 19.2MHz |

m is approximately 2, which yields a deviation of 18.75kHz. Setting the Index counter to 16 and the divider to 64 gives a datarate allowable of 18.75kbits/s. The datarates are not as desired but this example shows the limitation of GFSK, where exact datarates can only be obtained by supplying a particular crystal frequency. The TxCLK features provides a clock at this rate (18.75kHz), which a microcontroller can use to clock the data into the ADF7010.

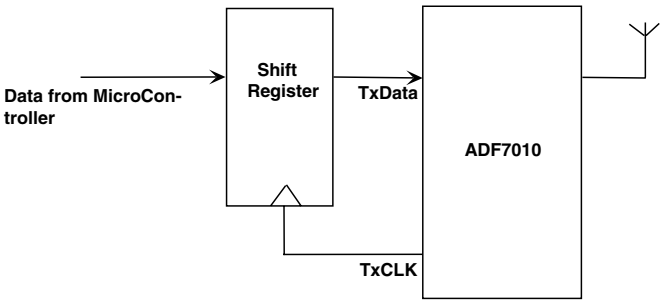



*Figure 7. In a case where it is difficult for the microcontroller to generate the exact datarate for GFSK, the ADF7010 can send a clock at the datarate back to the micro.*

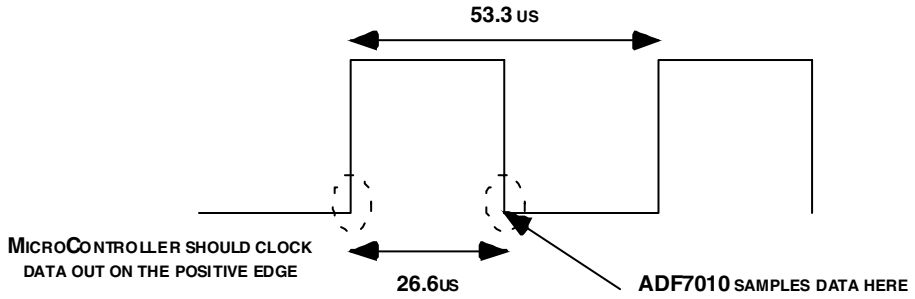



*Figure 8. TxCLK signal provided at 18.75kHz. The micro or shift register should use the positive edge to clock the data from its buffer to the TxData pin of the ADF7010. The delay allowed is 26.6us in this case at the 7010 will sample on the negative edge of the signal.*

**Table 1. Bill of Materials for the EVAL-ADF7010 Eval Board**

| | | | | | |
|---|---|---|---|---|---|
| 1 | ADF7010 | U1 | TSSOP24 | | SUPPLIED |
| 1 | CON-DB9HM | J1 | DB9-HM | 150-750 | |
| 1 | EDGE SMA | J2 | SMA_CARD_EDGE_RF | J502-ND | Digi-key |
| 4 | SMA | J3 J4 J6 J8 | SMA | | Pasternack PE4118 |
| 3 | SMA | J5 J7 J9 | SMA | | DO NOT INSERT |
| 1 | 19.2MHz Crystal | Y1 | HC49 | | SUPPLIED |
| | SW-SP3T-SLIDE,??? | S1 | SW-SP3T-SLIDE | 733-659 | |
| 3 | JUMPER | S3-S5 | SIP-2P | 511-705 | |
| 3 | Shorting link | S3-S5 | | 528-456 | |
| 16 | TESTPOINT | AGND DVDD CPVDD CREG CE DATA CLK LE TEST TXDATA TXCLK MUXOUT CVCO OSC1 OSC2 CLKOUT | TESTPOINT | 240-333 | |
| 1 | IND,12UH | L1 | Coilcraft 603CS_12NX_BC | | |
| 1 | IND,6.8UH | L2 | Coilcraft 603CS_6N8X_BC | | |
| | | | | | |
| 7 | RES,1K | R3-R6 R13 R16 R17 | 603 | 612-480 | |
| 5 | RES 0R | R7 R15 R18 C19 L3 | 603 | 772-227 | |
| 1 | RES,0R | R19 | 603 | 772-227 | DO NOT INSERT |
| 2 | RES,4K7 | RSET R8 | 603 | 612-560 | |
| 1 | RES,10K | R9 | 603 | 612-601 | |
| 2 | RES,10K | R10 R11 | 603 | 612-601 | DO NOT INSERT |
| 1 | RES,4K7 | R12 | 805 | 613-174 | DO NOT INSERT |
| 1 | RES,51R | R14 | 603 | | DO NOT INSERT |
| | | | | | |
| 2 | CAP,100NF | C4 C13 | 603 | 432-210 | |
| 1 | 220nF | C5 | 603 | 335-2020 | |
| 1 | CAP,4.7UF | C6 | 603 | 317-275 | |
| 4 | CAP,10PF | C7 C16-18 | 603 | 499-110 | |
| 1 | CAP,10PF | C8 | 805 | 499-158 | |
| 1 | 220pF | C22 | 603 | 722-133 | |
| 2 | 33pF | C14 C15 | 603 | 722-029 | |
| 1 | CAP,0.1UF | C9 | 805 | 499-687 | |
| 3 | CAP+,22UF | C10-C12 | CAP\TAJ_A | 197-038 | |
| 1 | CAP,1NF | C13 | 603 | | DO NOT INSERT |
| 2 | CAP | C20 C21 | 603 | | DO NOT INSERT |
| 4 | Stick-on Feet | Each Corner | 3M | FEC 148-922 | |
| | | | | | |
| | | LOOP FILTER COMPONENTS | | | |
| | | | | | |
| 1 | 1.5nF | C1 | 603 | 722-182 | |
| 1 | 33nF | C2 | 603 | 431-953 | |
| 1 | 270pF | C3 | 603 | 301-9627 | |
| 1 | 180R | R1 | 603 | 612-406 | |
| 1 | 910R | R2 | 603 | 612-649 | |