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**OCTAL BUS SWITCH** 

### **FEATURES:**

- Bus switches provide zero delay paths
- Low switch on-resistance
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Hot insertion capability
- Very low power dissipation
- Available in QSOP, SOIC, SSOP, and TSSOP Packages

### **DESCRIPTION:**

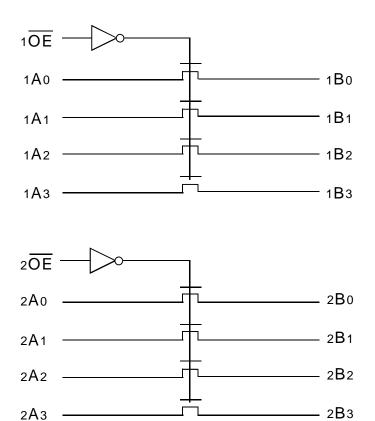
The FST3244 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

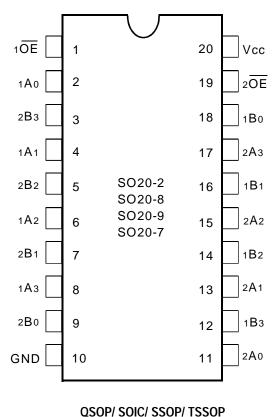
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST3244 is an octal TTL-compatible bus switch. The  $\overline{OE}$  pins provide output enable control for all 8 bits. This device is pin-compatible with and functionally similar to the FCT244T.

**PIN CONFIGURATION** 

## FUNCTIONAL BLOCK DIAGRAM





TOP VIEW

#### INDUSTRIAL TEMPERATURE RANGE

#### **APRIL 2001**

#### ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	–0.5 to +7	V
Tstg	Storage Temperature	-65 to +150	°C
Ιουτ	Maximum Continuous Channel Current	128	mA

#### NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Vcc, Control, and Switch terminals.

#### CAPACITANCE (1)

Symbol	Parameter	Conditions <sup>(2)</sup>	Тур.	Unit
CIN	Control Input Capacitance		8	pF
Ci/o	Switch Input/Output Capacitance	Switch Off	13	pF

NOTES:

1. Capacitance is characterized but not tested.

2. TA =  $25^{\circ}$ C, f = 1MHz, VIN = 0V, VOUT = 0V

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: TA =  $-40^{\circ}$ C to  $+85^{\circ}$ C, Vcc =  $5.0V \pm 5\%$ 

Symbol	Parameter	Те	st Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vih	Control Input HIGH Voltage	Guaranteed Logic H	Guaranteed Logic HIGH Level		—	_	V
VIL	Control Input LOW Voltage	Guaranteed Logic L	Guaranteed Logic LOW Level		—	0.8	V
Ін	Control Input HIGH Current	Vcc = Max.	VI = VCC	—	—	±1	μA
lı.	Control Input LOW Current		VI = GND	_	—	±1	
Іоzн	Current during	Vcc = Max., Vo = 0	Vcc = Max., Vo = 0 to 5V		_	±1	μA
Iozl	Bus Switch DISCONNECT			_	_	±1	
Vik	Clamp Diode Voltage	Vcc = Min., IIN = -18mA		_	-0.7	-1.2	V
IOFF	Switch Power Off Leakage	Vcc = 0V, VIN or Vo $\leq 5.5$ V		_	_	±1	μA
Icc	Quiescent Power Supply Current	Vcc = Max., VIN = G	ND or Vcc	_	0.1	3	μA

## **BUS SWITCH IMPEDANCE OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified: Operating Conditions: TA =  $-40^{\circ}$ C to  $+85^{\circ}$ C, VCC =  $5.0V \pm 5\%$ 

Symbol	Parameter	Test Conditions	Min.	Тур. <sup>(1)</sup>	Max.	Unit
Ron	Switch CONNECT Resistance, A to B <sup>(2)</sup>	Vcc = Min., VIN = 0V		5	7	Ω
		Ion = 30mA				
		Vcc = Min., VIN = 2.4V	Ι	10	15	
		Ion = 15mA				
los	Short Circuit Current, A to B <sup>(3)</sup>	$A(B) = 0V, B(A) = V_{CC}$	100	_		mA

#### NOTES:

1. Typical values are at Vcc = 5.0V, +25°C ambient.

3. Not more than one output should be shorted at one time. Duration of the test should not esceed one second.

# **PIN DESCRIPTION**

Pin Names	Description
xOE	Output Enable Inputs (Active LOW)
хАх	A Port Bits
хВх	B Port Bits

# FUNCTION TABLE (1)

1 <mark>0E</mark>	2 <mark>0E</mark>	Description
Н	Н	Disconnect
L	Н	Connect 1A to 1B
Н	L	Connect 2A to 2B
L	L	Connect 1A to 1B and 2A to 2B

**NOTE:** 1. H = HIGH

EST LINK

L = LOW

<sup>2.</sup> The voltage drop between the indicated ports divided by the current through the switch.

## **POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test C	onditions <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Unit
Δlcc	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = Max.$ $V_{IN} = 3.4V^{(3)}$		-	0.5	1.5	mA
Ісср	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open 1 Enable Pin Toggling 50% Duty Cycle	VIN = VCC VIN = GND	_	120	160	μΑ/ MHz/ Enable
Ic	Total Power Supply Current <sup>(6)</sup>	Vcc = Max. Outputs Open 2 Enable Pins Toggling	VIN = VCC VIN = GND	-	2.4	3.2	mA
		fi = 10MHz 50% Duty Cycle	VIN = 3.4 VIN = GND	-	2.9	4.7	

#### NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at Vcc = 5.0V, +25°C ambient.

3. Per TTL driven input (VIN = 3.4V). All other inputs at Vcc or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. CPD = ICCD/VCC

CPD = Power Dissipation Capacitance

6. IC = IQUIESCENT + INPUTS + IDYNAMIC

 $IC = ICC + \Delta ICC DHNT + ICCD (fiN)$ 

Icc = Quiescent Current

 $\Delta$ Icc = Power Supply Current for a TTL High Input (VIN = 3.4V)

DH = Duty Cycle for TTL Inputs High

 $N\tau$  = Number of TTL Inputs at DH

Icco = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

fi = Input Frequency

N = Number of Switches Toggling at fi

All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: Operating Conditions: TA = -40°C to +85°C, Vcc = 5.0V ±5%

Symbol	Description	Min. <sup>(2)</sup>	Тур.	Max.	Unit
<b>t</b> PLH	Data Propagation Delay	_	_	0.25	ns
<b>t</b> PHL	A to B, B to A <sup>(2)</sup>				
tрzн	Switch CONNECT Delay	1.5	_	6.5	ns
tPZL	xOE to A or B				
tрнz	Switch DISCONNECT Delay	1.5	_	5.5	ns
tPLZ	xOE to A or B				
Qci	Charge Injection During Switch DISCONNECT,	_	1.5	_	рС
	$x\overline{OE}$ to A or B <sup>(3)</sup>				

NOTES:

1. See test circuit and waveforms.

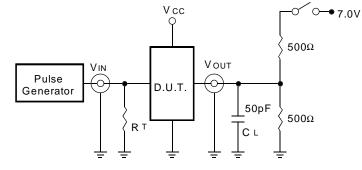
2. The bus switch contributes no propagation delay other than the RC delay of the load interacting with the RC of the switch.

3. IQcII is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers.

IQDCII is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge Injection is reduced becasue the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

### **TEST CIRCUITS AND WAVEFORMS**

#### **TEST CIRCUITS FOR ALL OUTPUTS**



#### **SWITCH POSITION**

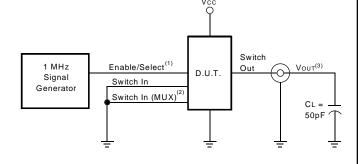
Test	Switch
Open Drain	
Disable Low	Closed
Enable Low	
All Other Tests	Open
	FCT LINK

#### **DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

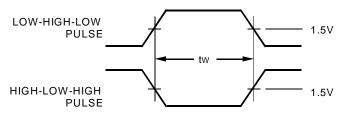
## **CHARGE INJECTION**



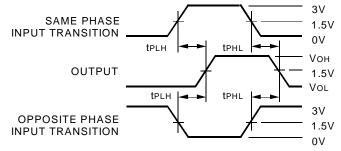
#### NOTES:

- Select is used with multiplexers for measuring IQDCII during multiplexer select. During all other tests Enable is used.
- 2. Used with multiplexers to measure IQDCII only.
- 3. Charge Injection =  $\Delta$ Vout CL, with Enable toggling for IQcII or Select toggling for IQDCII.  $\Delta$ Vout is the change in Vout and is measured with a 10M $\Omega$  probe.

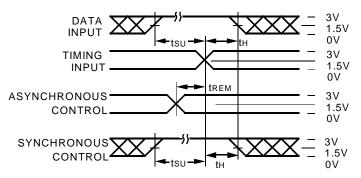
#### **PULSE WIDTH**



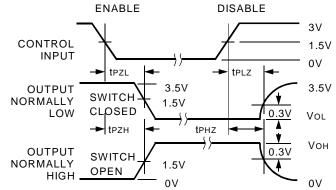
# **PROPAGATION DELAY**



# SET-UP, HOLD, AND RELEASE TIMES



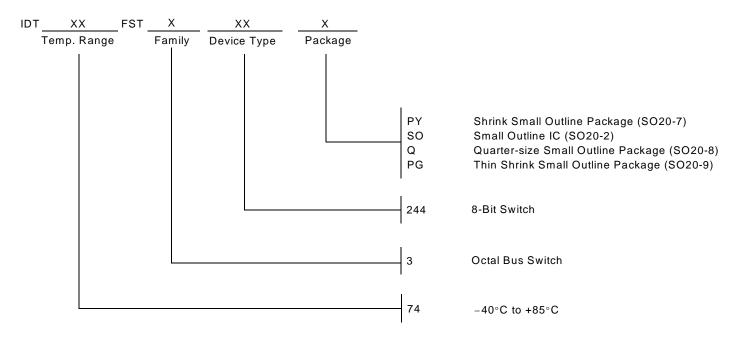
# **ENABLE AND DISABLE TIMES**



#### NOTES:

- 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- 2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz; tF  $\leq$  2.5ns; tR  $\leq$  2.5ns

## **ORDERING INFORMATION**





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