

DATA SHEET

CBT3244

Octal bus switch with quad output enables

Product specification
Supersedes data of 1998 Dec 8

2000 Jun 19

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CBT3244

FEATURES

- Standard '244-type pinout
- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), thin shrink small outline (TSSOP)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3244 device is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and high-impedance state exists between the two ports.

The CBT3244 is characterized for operation from -40°C to 85°C .

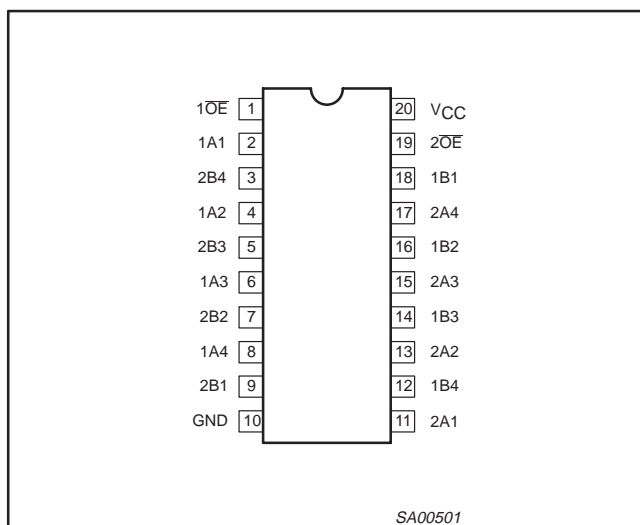
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$		ns
$C_{\text{IO(OFF)}}$	Pin capacitance (OFF state)	$V_O = 3\text{V}$ or 0V	6	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$		μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
20-Pin Plastic TSSOP Type I	-40°C to 85°C	CBT3244 PW DH	SOT360-1
20-Pin Plastic SSOP Type I	-40°C to 85°C	CBT3244 PW DB	SOT339-1
20-Pin Plastic SO Type I	-40°C to 85°C	CBT3244 PW D	SOT163-1

PIN CONFIGURATION



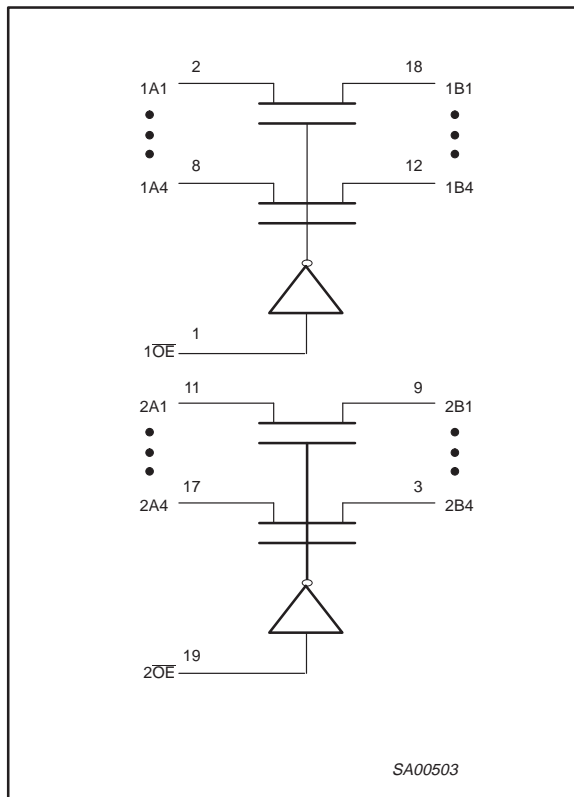
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 19	$1\overline{OE}, 2\overline{OE}$	Output enable
2, 4, 6, 8	1A1–1A4	Inputs
11, 13, 15, 17	2A1–2A4	Inputs
18, 16, 14, 12	1B1–1B4	Outputs
9, 7, 5, 3	2B1–2B4	Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

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LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
1OE	2OE	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level
 L = Low voltage level
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +7	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
T _{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T _{amb} = -40°C to +85°C			
			Min	Typ ¹	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _I = -18mA			-1.2	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V			±5	μA
I _{CC}	Quiescent supply current ²	V _{CC} = 5.5V; I _O = 0, V _I = V _{CC} or GND			50	μA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V, one input at 3.4V, other inputs at V _{CC} or GND			3.5	mA
C _I	Control pins	V _I = 3V or 0, \overline{OE} = V _{CC}		3		pF
C _{IO(OFF)}	Power-off leakage current	V _O = 3V or 0		6		pF
r _{on} ³	On-resistance	V _{CC} = 4.5V; V _I = 0V; I _I = 64mA		5	7	Ω
		V _{CC} = 4.5V; V _I = 0V; I _I = 30mA		5	7	
		V _{CC} = 4.5V; V _I = 0V; I _I = 15mA		10	15	

NOTES:

- All typical values are at V_{CC} = 5V, T_{amb} = 25°C
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

GND = 0V; t_R; C_L = 50pF

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	74CBT3244		UNIT
				T _{amb} = -40°C to +85°C V _{CC} = +5.0V ±0.5V		
				Min	Max	
t _{pd}	Propagation delay ¹	A or B	B or A		.25	ns
t _{en}	Output enable time to High and Low level	OE	A or B	1.0	8.9	ns
t _{dis}	Output disable time from High and Low level	OE	A or B	1.0	7.4	ns

NOTE:

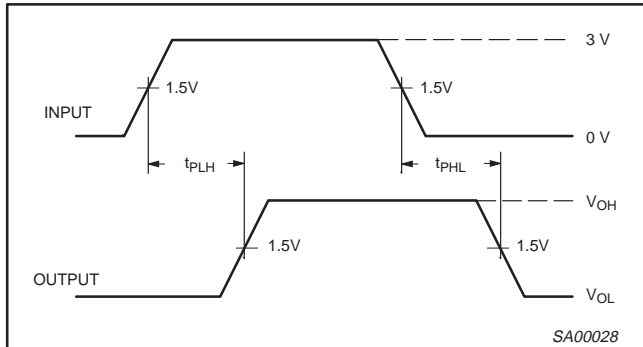
- This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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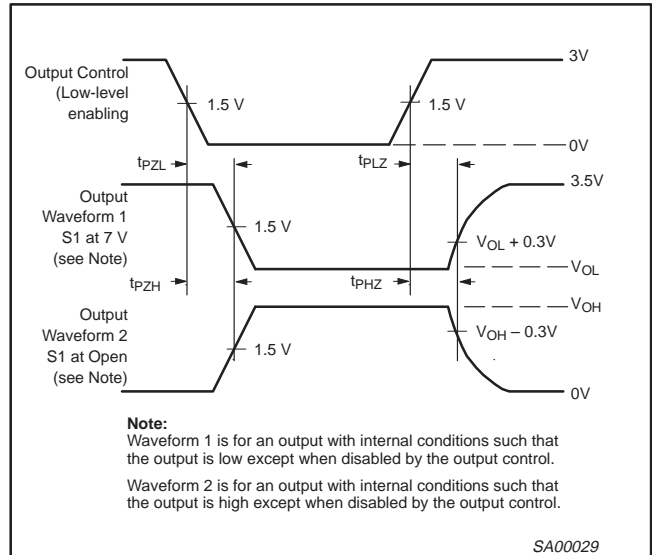
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AC WAVEFORMS

$V_M = 1.5V, V_{IN} = GND \text{ to } 3.0V$



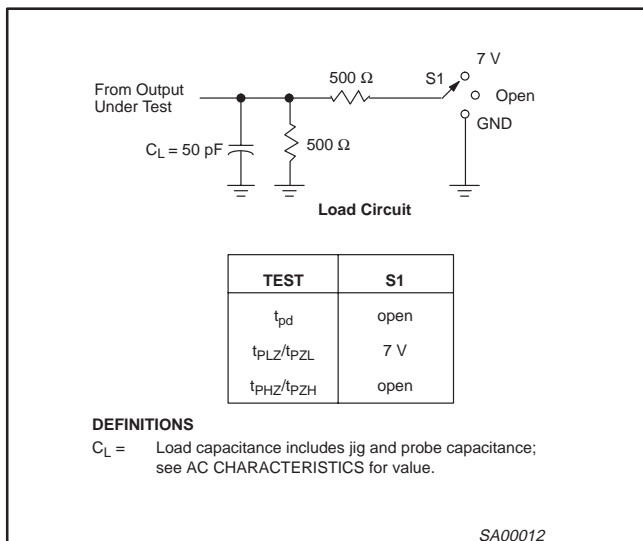
Waveform 1. Input to Output Propagation Delays



Note:
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



NOTES:

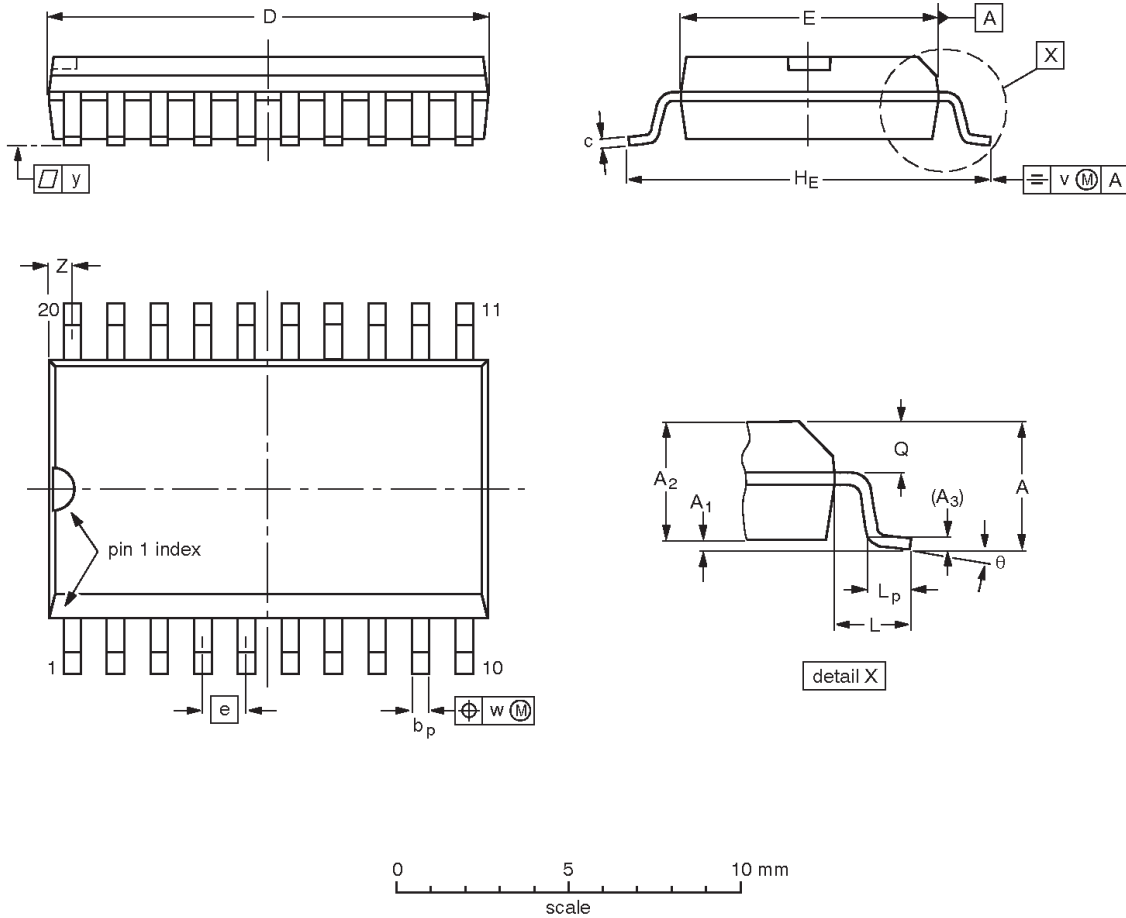
1. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz, Z_O = 50 \Omega, t_r \leq 2.5 ns, t_f \leq 2.5 ns.$
2. The outputs are measured one at a time with one transition per measurement.

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

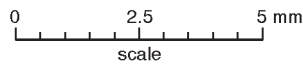
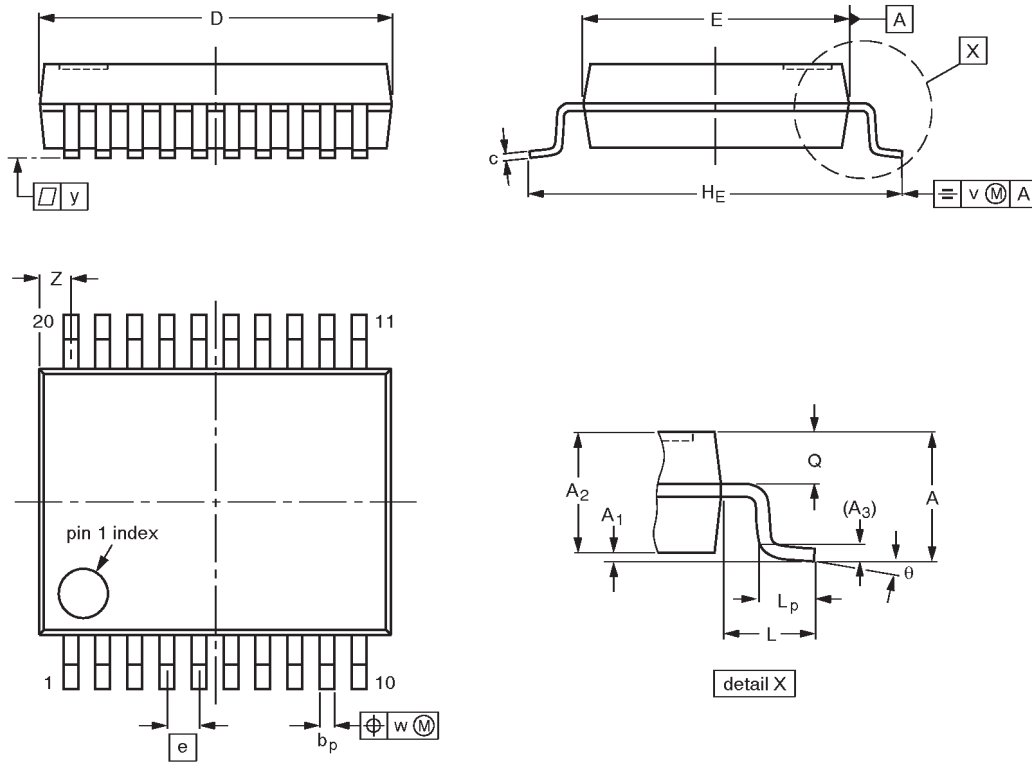
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

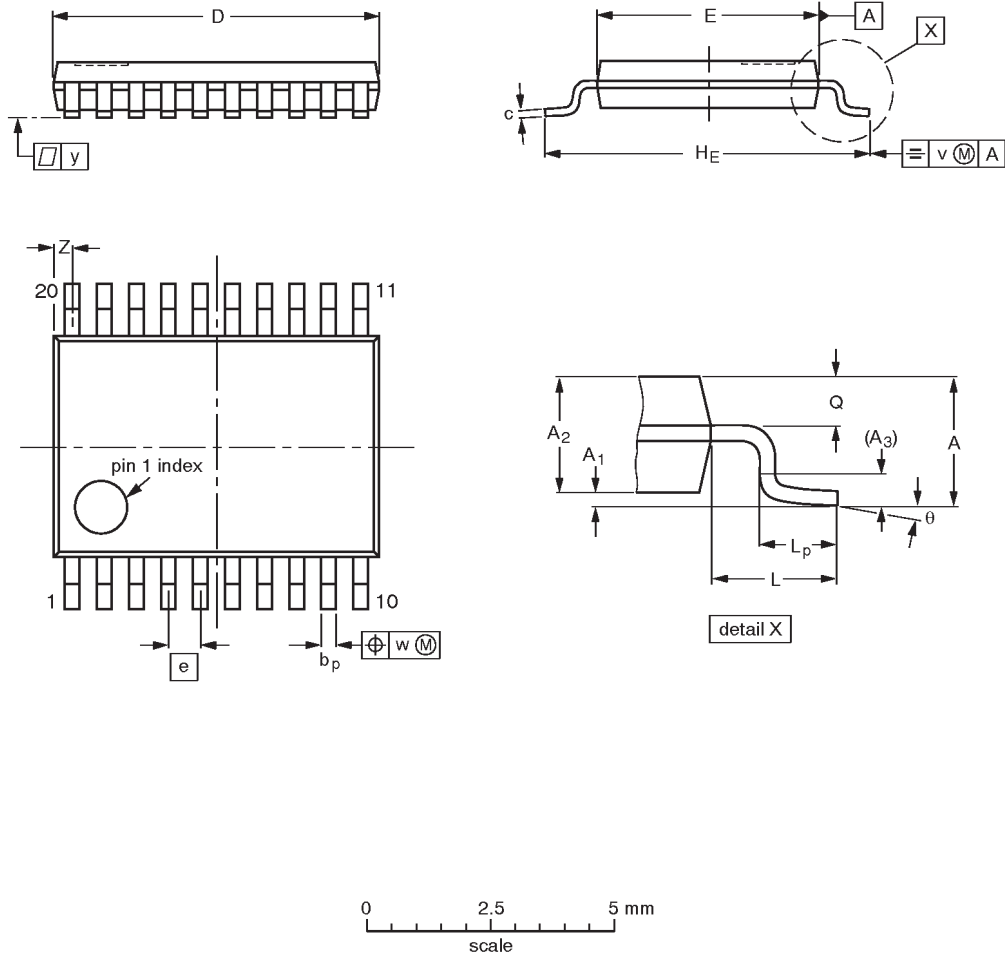
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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