National Semiconductor

November 1994

54F/74F169
4-Stage Synchronous Bidirectional Counter

General Description

The 'F169 is a fully synchronous 4-stage up/down counter. The 'F169 is a modulo-16 binary counter. Features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

Features

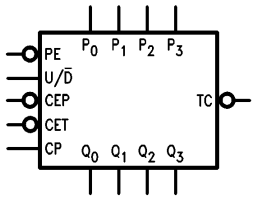
- Asynchronous counting and loading
- Built-in lookahead carry capability
- Presettable for programmable operation

Commercial	Military	Package Number	Package Description
74F169PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F169DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F169SC (Note 1)		M16A	16-Lead (0.150″ Wide) Molded Small Outline, JEDEC
74F169SJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB.

Logic Symbols



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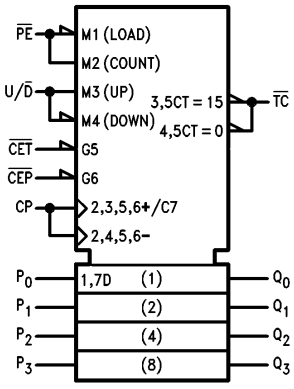
IEEE/IEC
'F169



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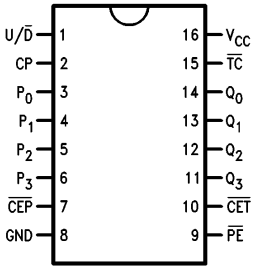
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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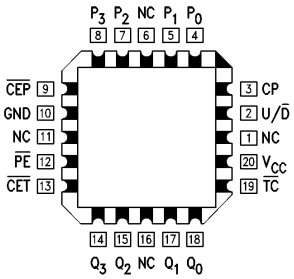
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 μA/ −0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/2.0	20 μA/ −1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ −0.6 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 μA/ −0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 μA/ −0.6 mA
U/$\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 μA/ −0.6 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	−1 mA/20 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	50/33.3	−1 mA/20 mA

Functional Description

The 'F169 uses edge-triggered J-K type flip-flops and has no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 for the 'F169 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

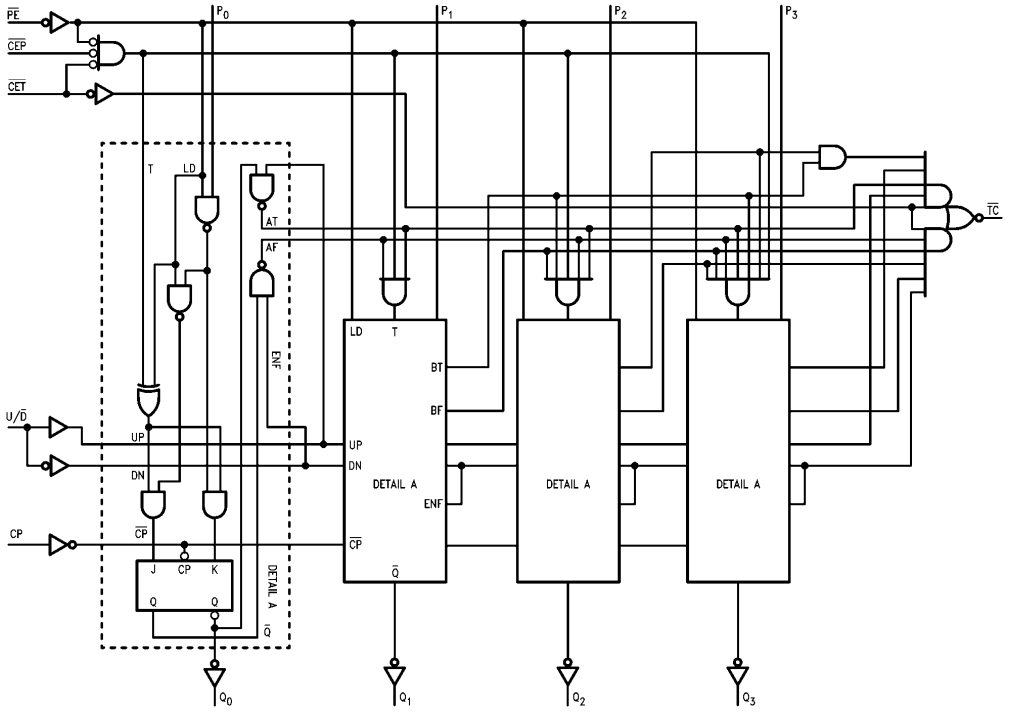
1) Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$

2) Up: ('F169): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet$ (Up) $\bullet \overline{CET}$

3) Down: $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet$ (Down) $\bullet \overline{CET}$

Logic Diagram

'F169



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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

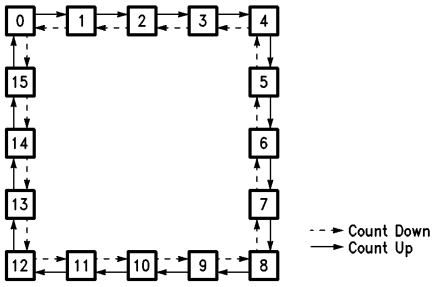
Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram

'F169



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 74F 10% V_{CC} 74F 5% V_{CC}	2.5 2.5 2.7			V	Min	I_{OH} = −1 mA I_{OH} = −1 mA I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC} 74F 10% V_{CC}			0.5 0.5	V	Min	I_{OL} = 20 mA I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6 −1.2	mA	Max	V_{IN} = 0.5V (except $\overline{CET}$) V_{IN} = 0.5V ($\overline{CET}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCL}	Power Supply Current			35	52	mA	Max	V_O = LOW

’F169

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} =$ Mil $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	90			60		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	12.0 16.0	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.5 4.0	12.0 8.5	15.5 12.5	5.5 4.0	20.0 15.0	5.5 4.0	17.5 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	4.5 8.5	6.5 11.0	2.5 2.5	9.0 12.0	2.5 2.5	7.0 12.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 8.0	11.5 12.0	3.5 4.0	16.0 14.0	3.5 4.0	12.5 13.0	ns

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		4.5 4.5		4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	7.0 5.0		8.0 8.0		8.0 6.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0.5		0 1.0		0 0.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0		10.0 10.0		9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	1.0 0		1.0 0		1.0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	11.0 7.0		14.0 12.0		12.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0		0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 7.0		6.0 9.0		4.5 8.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 169 S C X

Temperature Range Family
- 74F = Commercial
- 54F = Military

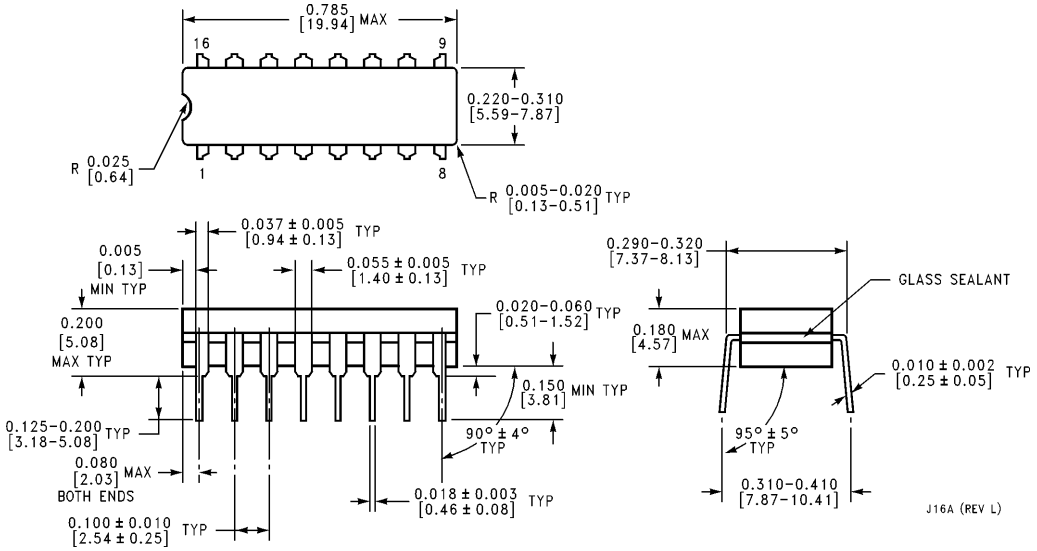
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- S = Small Outline Package SOIC JEDEC
- SJ = Small Outline SOIC EIAJ

Temperature Range
- C = Commercial (0°C to +70°C)
- M = Military (−55°C to +125°C)

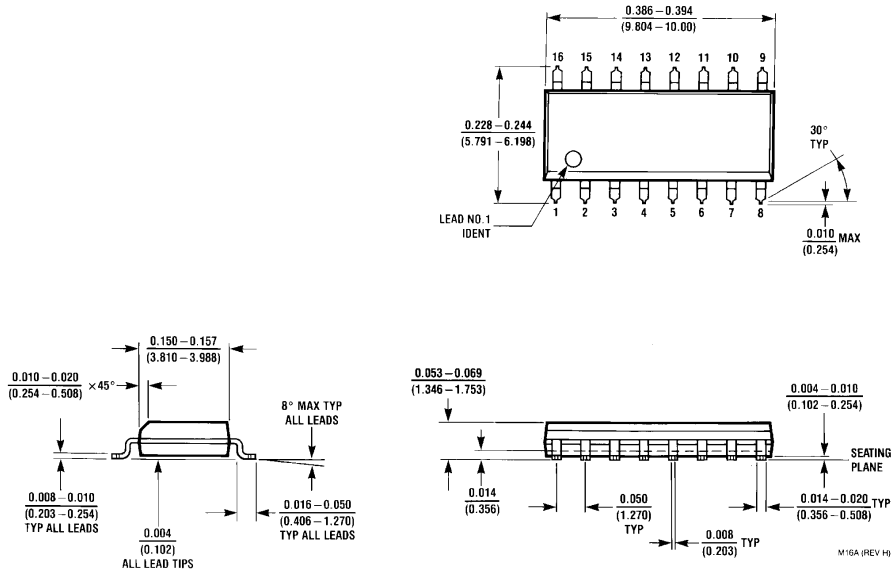
Special Variations
- X = Devices shipped in 13″ reels
- QB = Military grade device with environmental and burn-in processing shipped in tubes

Physical Dimensions inches (millimeters)

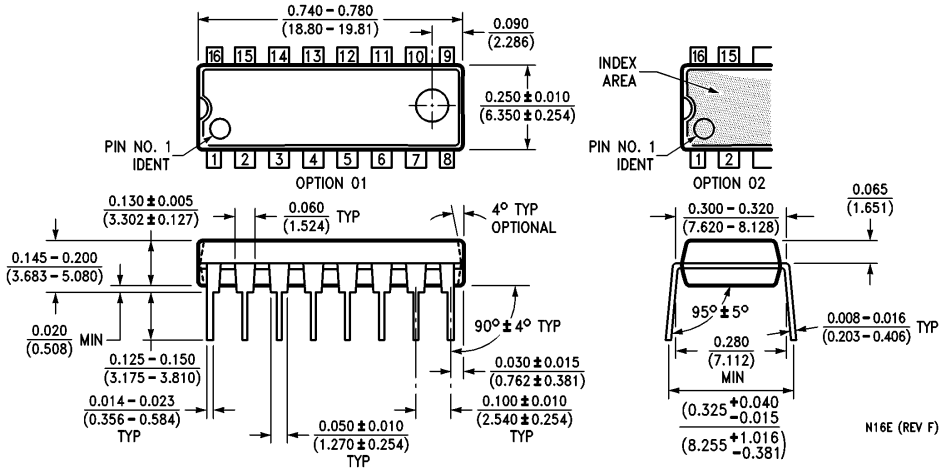


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

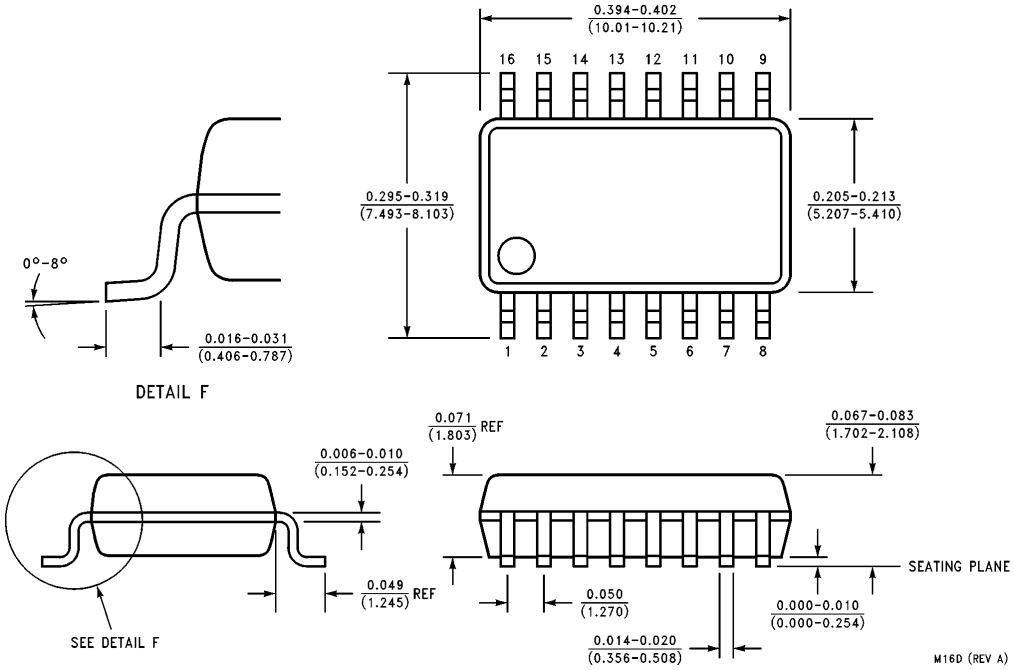


16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A



16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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