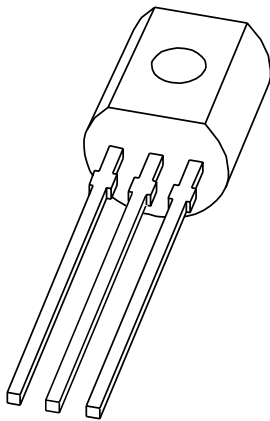


DATA SHEET



MPSA64 PNP Darlington transistor

Product specification
Supersedes data of 1999 Apr 27

2004 Oct 11

PNP Darlington transistor

MPSA64

FEATURES

- Low current (max. 500 mA)
- Low voltage (max. 30 V)
- High DC current gain (min. 10000).

APPLICATIONS

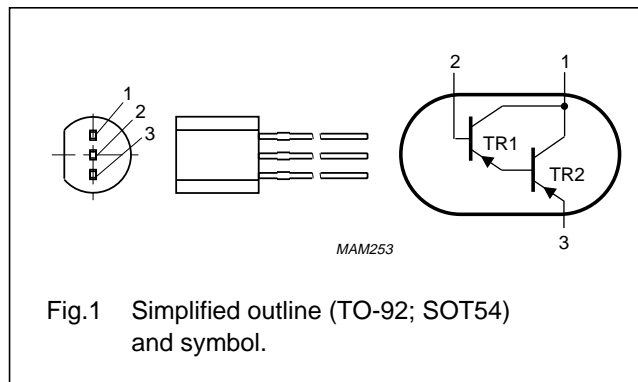
- High gain amplification.

DESCRIPTION

PNP Darlington transistor in a TO-92; SOT54 plastic package. NPN complement: MPSA14.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
MPSA64	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–30	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0$ V	–	–30	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
I_C	collector current (DC)		–	–500	mA
I_{CM}	peak collector current		–	–1	A
I_B	base current (DC)		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

PNP Darlington transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	250	K/W

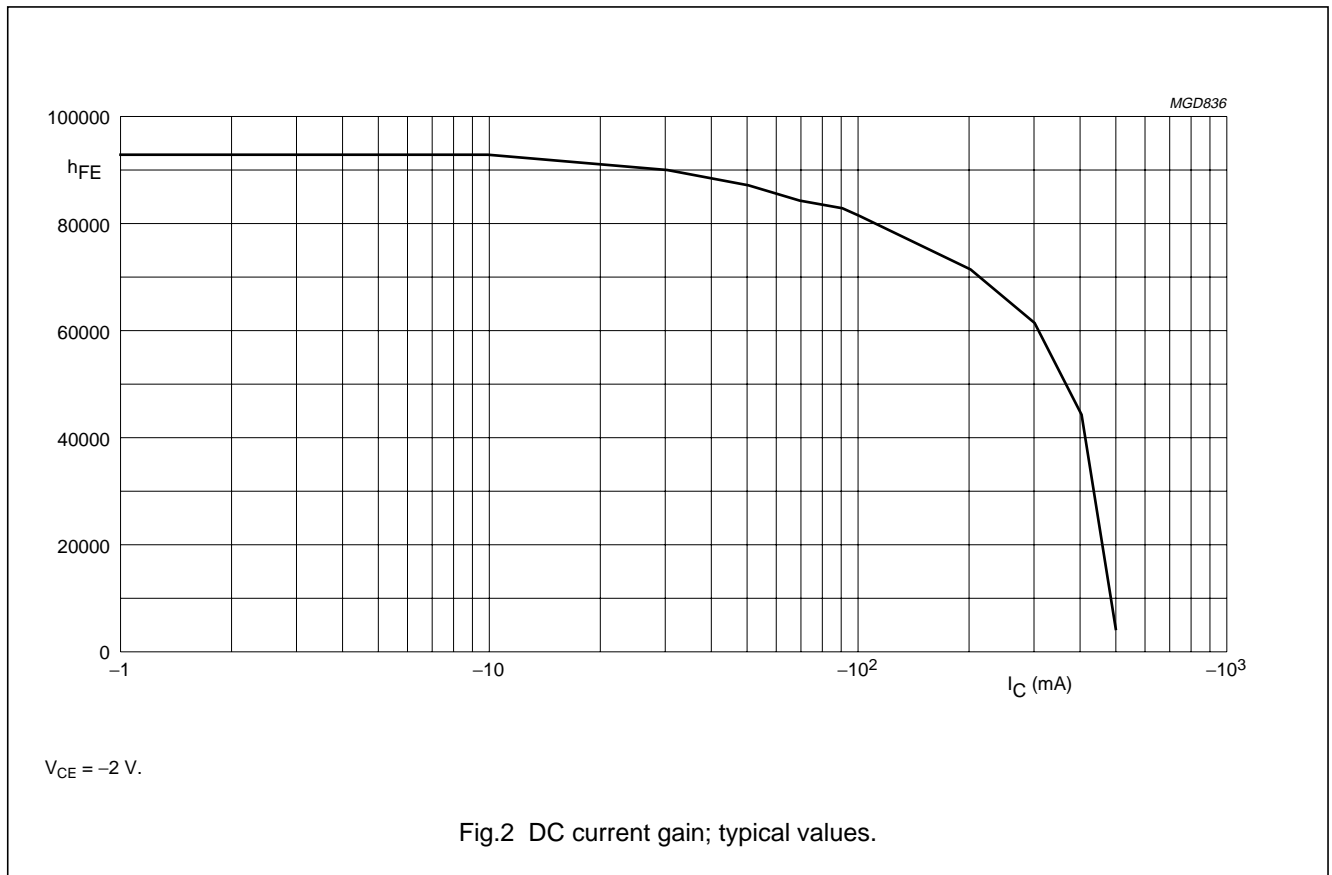
Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0\text{ A}$	-	-100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -10\text{ V}; I_C = 0\text{ A}$	-	-100	nA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}; I_C = -10\text{ mA}; \text{ see Fig.2}$	10000	-	
		$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}; \text{ see Fig.2}$	20000	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -0.1\text{ mA}$	-	-1.5	V
V_{BEsat}	base-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -0.1\text{ mA}$	-	-1.5	V
V_{BEon}	base-emitter on-state voltage	$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}$	-	-2	V
f_T	transition frequency	$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}; f = 100\text{ MHz}$	125	-	MHz



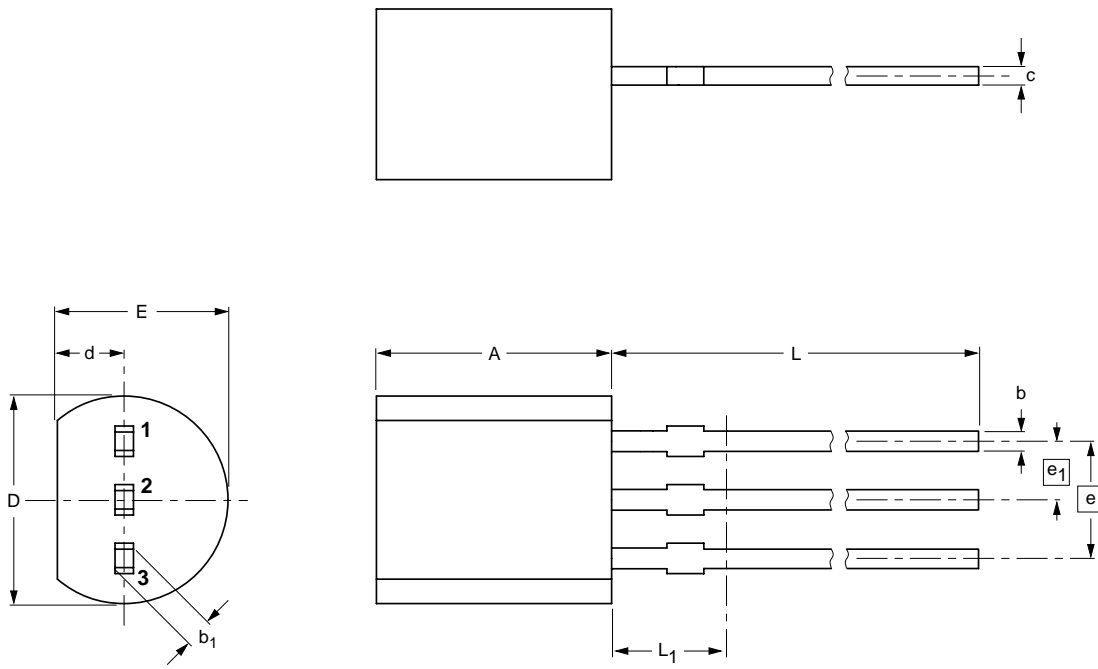
PNP Darlington transistor

MPSA64

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		97-02-28 04-06-28

PNP Darlington transistor

MPSA64

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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