REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add B, S, Q, and V test limits Change to one part-one part number format. Add ground bounce and latch-up immunity tests. Add 10.1 substitution statements. Editorial changes throughout.	92-07-10	Monica L. Poelking
B	Changes in accordance with NOR 5962-R082-93. – tjr	93-02-26	Monica L. Poelking
C	Changes in accordance with NOR 5962-R373-97. – cfs	97-07-08	Monica L. Poelking
D	Add device type 02. Add vendor CAGE F8859. Add case outlines X and Z. Add radiation features for device type 01. Update boilerplate to MIL-PRF-38535 requirements. - jak	02-09-24	Thomas M. Hess
E	Add radiation features for device type 02 in section 1.5. Update the boilerplate to include radiation hardness assured requirements for device type 02. Editorial changes throughout. – jak	05-03-18	Thomas M. Hess

The original first page of this drawing has been replaced.

REV																			
SHEET																			
REV	D	D	D	D	D	E	E	E	E	E	E	D							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS	REV	E	D	E	E	E	D	D	E	E	E	E	E	E	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Tim H. Noh

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Wm J. Johnson

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89-05-18

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL POSITIVE EDGED-TRIGGERED D-TYPE FLIP-FLOP WITH THREE STATE OUTPUTS AND TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

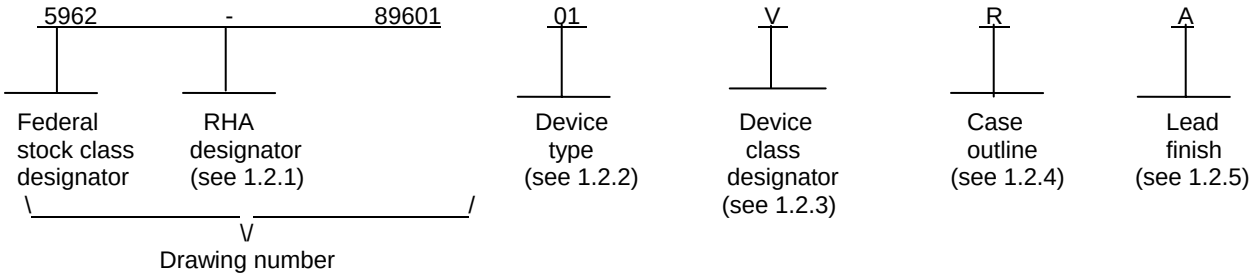
SIZE	CAGE CODE	
A	**67268**	**5962-89601**

SHEET 1 OF 26

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes M, B and Q) and space application (device classes S and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.



1.2.1 RHA designator. Device classes B, S, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT574	Octal posititve-edge triggered D-type flip-flop with three-state outputs and TTL compatible inputs
02	54ACT574	Octal posititve-edge triggered D-type flip-flop with three-state outputs and TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
B, S, Q, or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
X	See figure 1	20	Flat pack
Z	GDFP1-G20	20	Flat pack with gullwing
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	±20 mA
DC output current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±200 mA 3/
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds):	
Case outline X	+260°C
All other case outlines except case X	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}) (V_{CC} = 4.5 V and 5.5 V)	0.8 V
Minimum high level input voltage (V_{IH}) (V_{CC} = 4.5 V and 5.5 V)	2.0 V
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall rate ($\Delta t/\Delta V$) maximum:	
V_{CC} = 4.5 V	10 ns/V
V_{CC} = 5.5 V	8 ns/V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	24 mA

1.5 Radiation features.

Device type 01:	
Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	100 Krads (Si)
Single Event Latch-up (SEL)	≥ 120 MeV-cm^2/mg
Device type 02:	
Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 krads (Si)
Single Event Latch-up (SEL)	≥ 93 MeV-cm^2/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} or GND pins.
4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA/JEDEC Standard No. 78 - IC Latch-Up Test

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes B, S, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes B, S, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes B, S, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes B, S, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes B, S, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that effects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

3.11 Substitution. Substitution data shall be as indicated in the appendix herein.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
High level output voltage 3006	V_{OH1} 6/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	4.5 V	1, 2, 3	4.4		V
	V_{OH2} 7/ 8/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$		All All	5.5 V	1, 2, 3	5.4		
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$	M	01 B, S, Q, V		1	5.4		
			D				5.4		
			P, L, R				5.4		
	V_{OH3} 7/ 8/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$		All All	4.5 V	1, 2, 3	3.7		
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$	M	01 B, S, Q, V		1	3.7		
			D				3.7		
			P, L, R				3.7		
	V_{OH4} 6/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All All	5.5 V	1, 2, 3	4.7		
	V_{OH5} 7/ 8/ 9/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$		All All	5.5 V	1, 2, 3	3.85		
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$	M	01 B, S, Q, V		1	3.85		
			D				3.85		
			P, L, R				3.85		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Low level output voltage 3007	V_{OL1} 6/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All All	4.5 V	1, 2, 3		0.1	V
	V_{OL2} 7/ 8/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All All	5.5 V	1, 2, 3		0.1	
			M	01 B, S, Q, V		1		0.1	
			D					0.1	
			P, L, R					0.1	
	V_{OL3} 7/ 8/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$		All B, S, Q, V	4.5 V	1, 3		0.4	
						2		0.5	
				All M		1		0.4	
						2, 3		0.5	
			M	01 B, S, Q, V		1		0.4	
			D					0.4	
			P, L, R					0.4	
	V_{OL4} 6/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$		All B, S, Q, V	5.5 V	1, 3		0.4	
						2		0.5	
				All M		1		0.4	
						2, 3		0.5	
	V_{OL5} 7/ 8/ 9/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ mA$		All All	5.5 V	1, 2, 3		1.65	
			M	01 B, S, Q, V		1		1.65	
			D					1.65	
			P, L, R					1.65	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Three-state output leakage current high 3021	I_{OZH} 7/ 8/ 10/	$\overline{OE} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = 5.5\ V$		All	5.5 V	1		0.5	µA
				B, S, Q, V		2		10.0	
				All		1		0.5	
				M		2, 3		10.0	
			M	01 B, S, Q, V		1		25.0	
			D					25.0	
			P, L, R					25.0	
			M, D, P, L, R, F	02 Q, V				5.0	
Three-state output leakage current low 3020	I_{OZL} 7/ 8/ 10/	$\overline{OE} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = GND$		All	5.5 V	1		-0.5	µA
				B, S, Q, V		2		-10.0	
				All		1		-0.5	
				M		2, 3		-10.0	
			M	01 B, S, Q, V		1		-25.0	
			D					-25.0	
			P, L, R					-25.0	
			M, D, P, L, R, F	02 Q, V				-5.0	
Positive input clamp voltage 3022	V_{IC+} 7/ 8/	For input under test, $I_{IN} = 1\ mA$		All B, S, Q, V	GND	1	0.4	1.5	V
			M	01 B, S, Q, V		1	0.4	1.5	
			D				0.4	1.5	
			P, L, R				0.4	1.5	
Negative input clamp voltage 3022	V_{IC-} 7/ 8/	For input under test, $I_{IN} = -1\ mA$		All B, S, Q, V	Open	1	-0.4	-1.5	V
			M	01 B, S, Q, V		1	-0.4	-1.5	
			D				-0.4	-1.5	
			P, L, R				-0.4	-1.5	
Input current high 3010	I_{IH} 7/ 8/	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		0.1	µA
						2		1.0	
				All		1		0.1	
				M		2, 3		1.0	
			M	01 B, S, Q, V		1		0.1	
			D					0.1	
			P, L, R					0.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Input current low 3009	I_{IL} 7/ 8/	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1		-0.1	µA
				B, S, Q, V		2		-1.0	
				All		1		-0.1	
				M		2, 3		-1.0	
			M	01		1		-0.1	
			D	B, S, Q, V				-0.1	
			P, L, R					-0.1	
Control input capacitance 3012	C_{IN}	See 4.4.1b T_C = +25°C		All	GND	4		10.0	pF
				All					
Output capacitance 3012	C_{OUT} 10/	See 4.4.1b T_C = +25°C		All	5.5 V	4		15.0	pF
				All					
Power dissipation capacitance	C_{PD} 11/	See 4.4.1b T_C = +25°C		All	5.0 V	4		55.0	pF
				All					
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 7/ 8/ 12/	For input under test, $V_{IN} = V_{CC}$ - 2.1 V For all other inputs, $V_{IN} = V_{CC}$ or GND		01	5.5 V	3		1.6	mA
				B, S, Q, V		1, 2		1.0	
				02		1, 2, 3		1.6	
				Q, V					
				All		1, 2, 3		1.6	
				M					
			M	01		1		1.6	
			D	B, S, Q, V				1.6	
			P, L, R					3.5	
Quiescent supply current output high 3005	I_{CCH} 7/ 8/	$\overline{OE}$ = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1		2.0	µA
				B, S, Q, V		2		40.0	
				All		1		8.0	
				M		2, 3		160.0	
			M	01		1		100.0	
			D	B, S, Q, V				1.0	mA
			P, L, R					3.5	
			M, D, P, L, R, F 13/	02 Q, V				50.0	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Quiescent supply current output low 3005	I_{CCL} 7/ 8/	$\overline{OE}$ = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		2.0	µA
						2		40.0	
				All M		1		8.0	
						2, 3		160.0	
			M	01 B, S, Q, V		1		100.0	
			D					1.0	mA
			P, L, R					3.5	
			M, D, P, L, R, F 13/	02 Q, V				50.0	µA
Quiescent supply current outputs three-state 3005	I_{CCZ} 7/ 8/	$\overline{OE} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		2.0	µA
						2		40.0	
				All M		1		8.0	
						2, 3		160.0	
			M	01 B, S, Q, V		1		100.0	
			D					1.0	mA
			P, L, R					3.5	
			M, D, P, L, R, F 13/	02 Q, V				50.0	µA
Low level ground bounce noise	V_{GBL} 13/ 14/	V_{LD} = 2.5 V I_{OL} = +24 mA See figure 5		All B, S, Q, V	4.5 V	4		2000	mV
High level ground bounce noise	V_{GBH} 13/ 14/	V_{LD} = 2.5 V I_{OH} = -24 mA See figure 5		All B, S, Q, V	4.5 V	4		2000	mV
Latch-up input/ output over-voltage	I_{CC} (O/V1) 15/	$t_w \ge 100$ µs $t_{cool} \ge t_w$ 5 µs $\le t_r \le$ 5 ms 5 µs $\le t_f \le$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V V_{over} = 10.5 V		All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 15/	$t_w \ge 100$ µs $t_{cool} \ge t_w$ 5 µs $\le t_r \le$ 5 ms 5 µs $\le t_f \le$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V $I_{trigger}$ = +120 mA		All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 15/	$t_w \ge 100$ µs $t_{cool} \ge t_w$ 5 µs $\le t_r \le$ 5 ms 5 µs $\le t_f \le$ 5 ms V_{test} = 6.0 V V_{CCQ} = 5.5 V $I_{trigger}$ = -120 mA		All B, S, Q, V	5.5 V	2		200	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Latch-up supply over-voltage	I_{CC} (O/V2) 15/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$		All B, S, Q, V	5.5 V	2		100	mA
Truth table test output voltage 3014	7/ 8/ 16/	$V_{IL} = 0.40\ V$ $V_{IH} = 2.40\ V$ Verify output V_{OUT} See 4.4.1e		All All	4.5 V	7, 8	L	H	
				All M	5.5 V	7, 8	L	H	
			M	01 B, S, Q, V	4.5 V	7	L	H	
			D				L	H	
			P, L, R				L	H	
Propagation delay time, clock to output, CP to On 3003	t_{PHL}, t_{PLH} 7/ 8/ 17/ 18/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 6		All B, S, Q, V	4.5 V	9, 11	1.0	11.0	ns
						10	1.0	13.5	
				All M		9	1.0	11.0	
						10, 11	1.0	13.5	
			M	01 B, S, Q, V		9	1.0	11.0	
			D				1.0	11.0	
			P, L, R				1.0	11.0	
Propagation delay time, output enable, OE to On 3003	t_{PZH}, t_{PZL} 7/ 8/ 17/ 18/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 6		All B, S, Q, V	4.5 V	9, 11	1.0	9.5	ns
						10	1.0	11.0	
				All M		9	1.0	9.5	
						10, 11	1.0	11.0	
			M	01 B, S, Q, V		9	1.0	9.5	
			D				1.0	9.5	
			P, L, R				1.0	9.5	
Propagation delay time, output disable, OE to On 3003	t_{PHZ}, t_{PLZ} 7/ 8/ 17/ 18/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 6		All B, S, Q, V	4.5 V	9, 11	1.0	10.5	ns
						10	1.0	12.0	
				All M		9	1.0	10.5	
						10, 11	1.0	12.0	
			M	01 B, S, Q, V		9	1.0	10.5	
			D				1.0	10.5	
			P, L, R				1.0	10.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type 4/ and device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Maximum operating frequency	f_{MAX}	C_L = 50 pF minimum R_L = 500Ω See figure 6 See 4.4.1f	All B, S, Q, V	4.5 V	9, 11	100		MHz
					10	70		
			All M		9	95		
					10, 11	70		
Input set-up time, Dn (high and low) to CP	t_s	C_L = 50 pF minimum R_L = 500Ω See figure 6 See 4.4.1g	All All	4.5 V	9	3.5		ns
					10, 11	3.5		
Input hold time, Dn (high and low) to CP	t_h	C_L = 50 pF minimum R_L = 500Ω See figure 6 See 4.4.1g	All B, S, Q, V	4.5 V	9, 10	1.5		ns
					11	2.0		
			All M	4.5 V	9	1.5		ns
					10, 11	2.0		
Clock pulse width (high and low)	t_W	C_L = 50 pF minimum R_L = 500Ω See figure 6 See 4.4.1g	All All	4.5 V	9	5.0		ns
					10, 11	5.0		

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.

c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 are tested at all levels M, D, P, L, and R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in table I.

RHA parts for device type 02 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table I.

4/ The word "All" in the device type and device class column, means non-RHA limits for all device types and classes. Where M, D, P, L, R, and/or F in the conditions column are postirradiation limits for those device types and classes specified in the device type and device class column.

TABLE I. Electrical performance characteristics - Continued.

5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

6/ For device classes B, S, Q, and V, this test is guaranteed, if not tested, to the limits specified in table I.

7/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.

8/ When performing post irradiation electrical measurements for RHA level, T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.

9/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

10/ Three-state output conditions are required.

11/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S, n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.

12/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits are equal to the number of inputs at a high TTL input level times the ΔI_{CC} maximum limit and the preferred method and limits are guaranteed.

13/ The maximum limit for this parameter at 100 krads (si) is 2.0 µA.

14/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} minimum = ±24 mA for example) and 50pF of load capacitance (see figure 5). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f$ = 3.5 ±1.5 ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

15/ When used in synchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2,000 mV can be a possible problem.

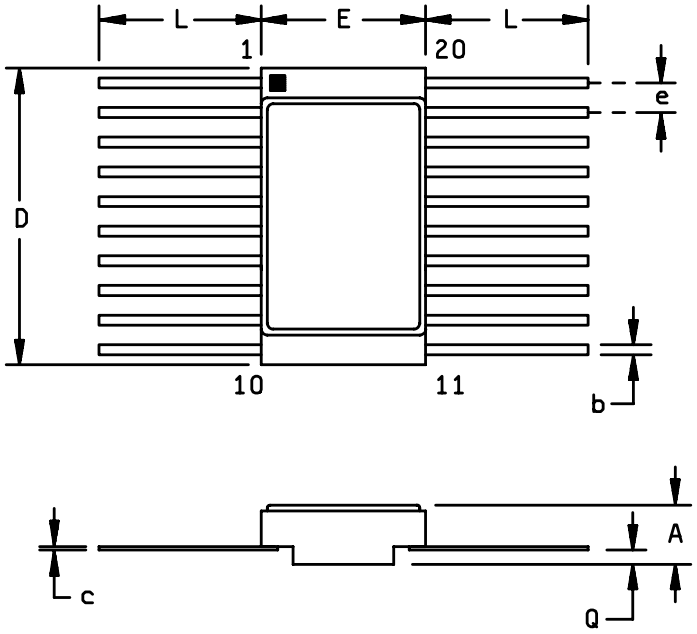
16/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ±5 percent.

17/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated. Functional tests at V_{CC} = 4.5 V are worst case for RHA specified devices.

18/ Device classes B, S, Q, and V are tested at V_{CC} = 4.5 V at T_C = +125°C for sample testing and at V_{CC} = 4.5 V at T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested. See 4.4.1d.

19/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

Case X



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.045	.085	1.14	2.16
b	.015	.019	0.38	0.48
c	.003	.006	0.076	0.152
D	.505	.515	12.83	13.08
E	.275	.285	6.99	7.24
e	.045	.055	1.14	1.40
L	.250	.370	6.35	9.39
Q	.010	---	0.25	---
N	20		20	

FIGURE 1. Case outline.

Device types	All
Case oultines	R, S X, Z and 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	GND
11	CP
12	O7
13	O6
14	O5
15	O4
16	O3
17	O2
18	O1
19	O0
20	V_{CC}

Terminal descriptions	
Terminal symbol	Description
$\overline{OE}$	Output enable inputs (active low)
CP	Clock pulse input
Dn (n = 0 to7)	Data inputs
On (n = 0 to 7)	Data outputs

FIGURE 2. Terminal connections.

Inputs			Output
$\overline{OE}$	Dn	CP	On
L	L	↑	L
L	H	↑	H
L	X	*	On_0
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high transition of the clock
↓ = High-to-low transition of the clock
Z = High impedance
* = CP at H or L or ↓
On_0 = The value of On after the most recent positive transition of CP

FIGURE 3. Truth table.

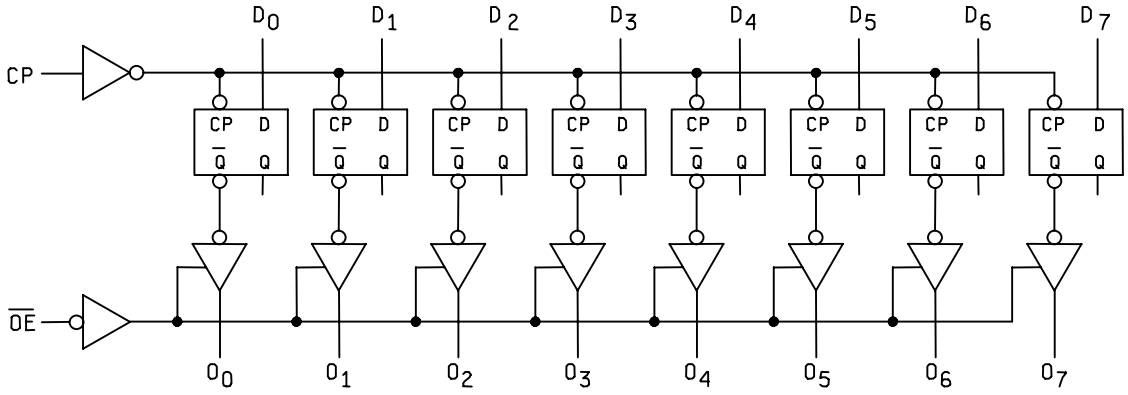
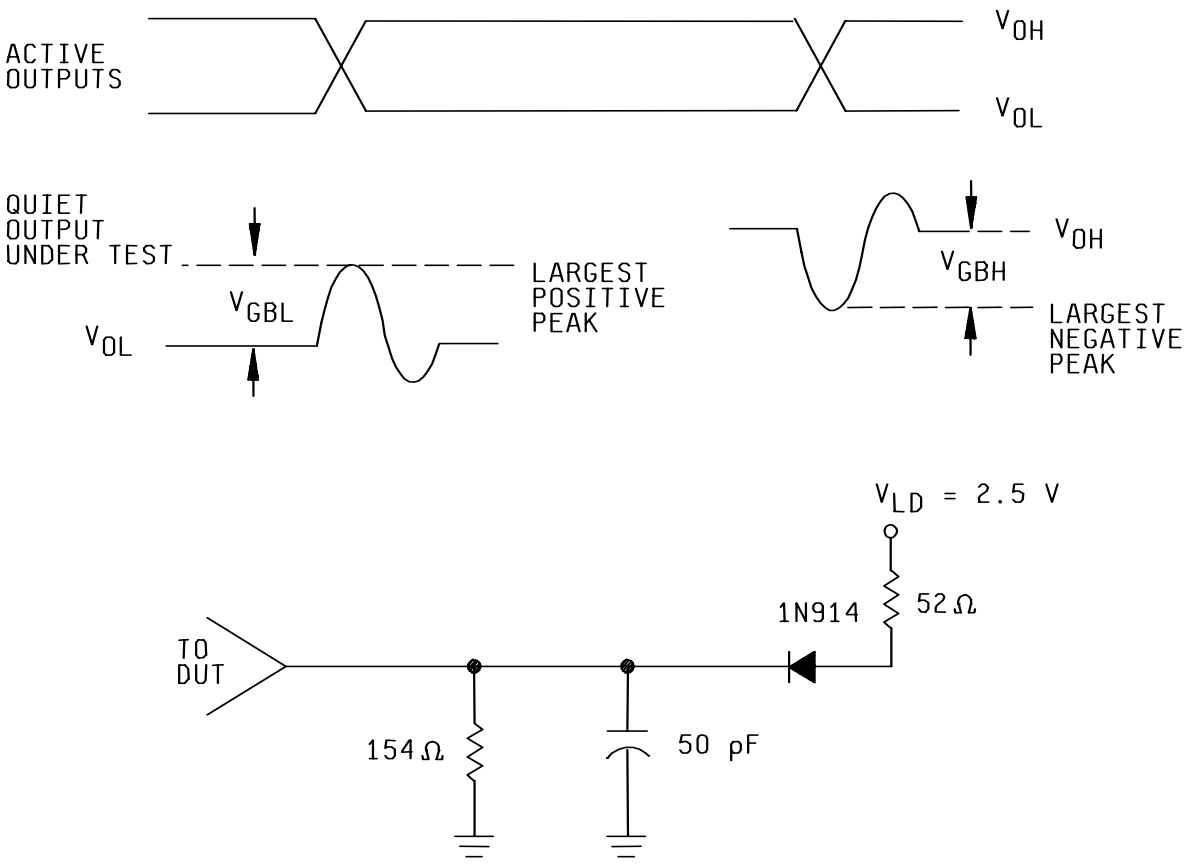


FIGURE 4. Logic diagram.



NOTE: Resistor and capacitor tolerances = ±10%.

FIGURE 5. Ground bounce waveforms and test circuit.

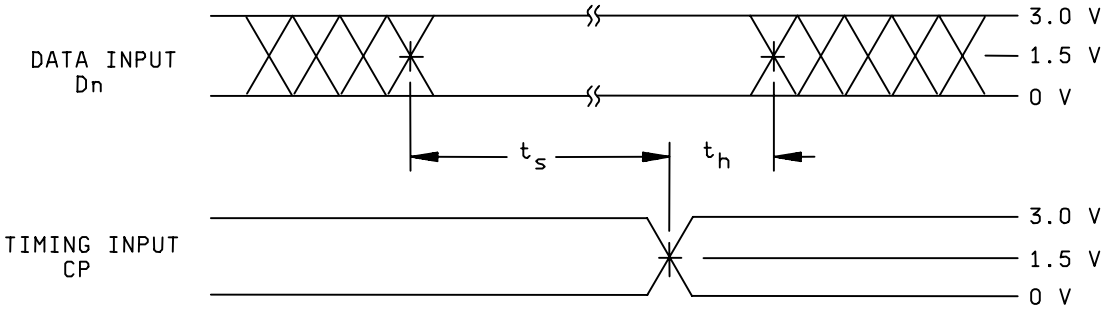
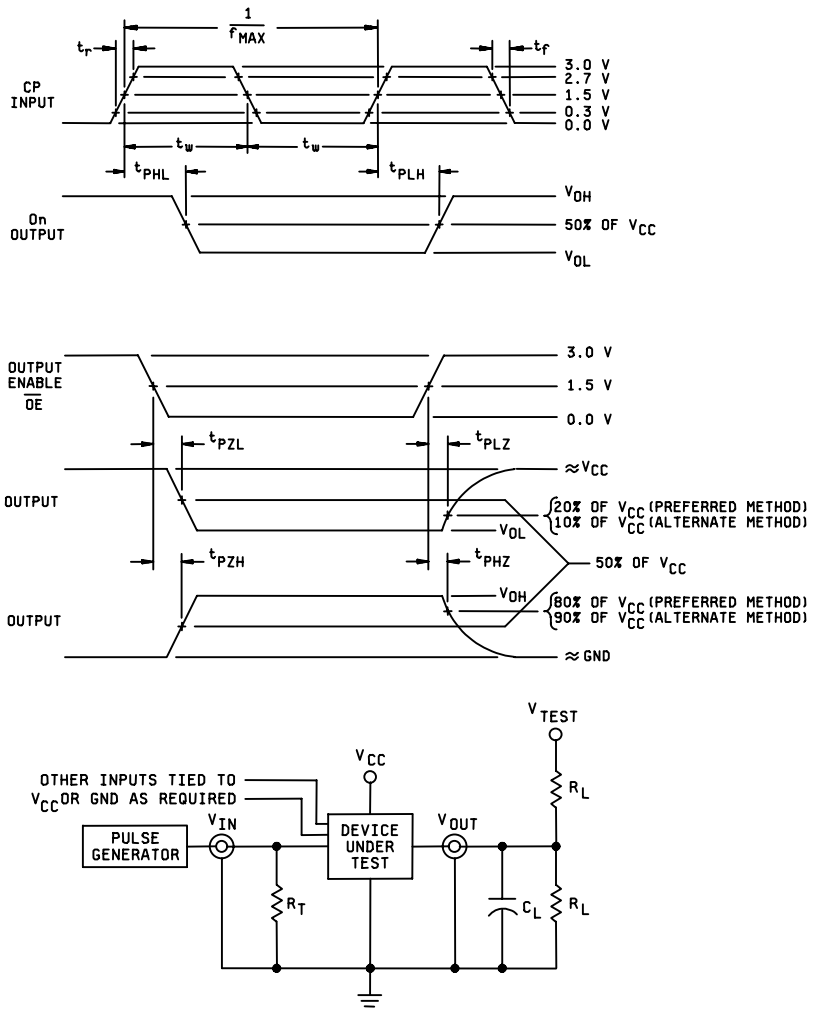


FIGURE 6. Switching waveforms and test circuit.



NOTES:

1. Preferred method:
   When measuring t_{PHZ} and t_{PZH}: V_{TEST}= GND
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PLH} and t_{PHL}: V_{TEST} = open
   Alternate method:
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open
2. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. Outputs are measured one at a time with one output per measurement.

FIGURE 6. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes B, S, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A

4.2 Screening. For device classes B, S, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 requirements of table II herein.

(4) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

(5) Unless otherwise specified in the QM plan for static burn-in, device classes B and S, test condition A of test method 1015 of MIL-STD-883; the test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

(a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC}. Outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors R1 are optional on open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(c) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(6) Unless otherwise specified in the QM plan for dynamic burn-in, device classes B and S, test condition D of test method 1015 of MIL-STD-883, the following shall apply:

(a) Input resistors = 220Ω to 2 kΩ ±20 percent.

(b) Output resistors = 220Ω ±20 percent.

(c) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(d) The output enable control pin(s) shall be connected through the resistors in parallel to V_{CC}. The clock input (CP) shall be connected through a resistor to a clock pulse (CP1). All other inputs shall be connected through the resistors in parallel to a common clock pulse (CP2), as applicable. Outputs shall be connected through the resistors to $V_{CC}/2$ ±0.5 V.

(e) CP1, CP2 = 25 kHz to 1 MHz square wave; $f_{CP1} = f_{CP2}/2$; duty cycle = 50 percent ±15 percent; V_{IH} = 4.5 V to V_{CC}; V_{IL} = 0 V ±0.5 V; t_r, $t_f \leq 100$ ns.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes B, S, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V or S beyond the requirements of device class Q or B shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S or V devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B or Q devices shall be in accordance with MIL-PRF-38535, for static burn-in. Dynamic burn-in is not required.

d. The PDA for class M devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in and dynamic burn-in.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup I, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection for device classes B, S, Q, and V. Qualification inspection for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up and ground bounce tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground bounce tests, test all applicable pins on five devices with zero failures.

c. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device classes B, S, Q, and V, subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes B, S, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

f. For device classes B, S, Q, and V, f_{MAX} shall be measured only for initial qualification and after process or design changes which may affect the device frequency. Test all applicable pins on 22 devices with zero failures.

g. For device classes B, S, Q, and V, t_s, t_h, and t_W shall be guaranteed, if not tested, to the limits specified in table I.

TABLE II. Electrical test requirements.

Test requirements	Subgroups 1/ (in accordance with MIL-STD-883, method 5005, table I)	Subgroups 1/ (in accordance with MIL-PRF-38535, table III)			
	Device class M	Device 2/ class B	Device 2/ class S	Device class Q	Device class V
Interim electrical parameters, method 5004 (see 4.2)		1	1	1	1
Static burn-in I, method 1015 (see 4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)			1 5/		1 5/
Static burn-in II, method 1015 (see 4.2.1a)	3/	Required 6/	Required 4/	Required 6/	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)		1 2/ 5/	1 2/ 5/	1 2/ 5/	1 2/ 5/
Dynamic burn-in I, method 1015 (see 4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)			1 5/		1 5/
Final electrical parameters, method 5004	1, 2, 3, 7, 8, 9 2/	1, 2, 7, 9 2/ 6/	1, 2, 7, 9 2/	1, 2, 3, 7, 8, 9, 10, 11 2/ 6/	1, 2, 3, 7,8, 9, 10, 11 2/
Group A test requirements, method 5005 (see 4.4.1)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters, method 5005 (see 4.4.2)			1, 2, 3, 7, 8, 9, 10, 11 5/		
Group C end-point electrical parameters, method 5005 (see 4.4.3)	1, 2, 3	1, 2 5/		1, 2, 3 5/	1, 2, 3, 7, 8, 9, 10, 11 5/
Group D end-point electrical parameters, method 5005 (see 4.4.4)	1, 2, 3	1, 2	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters, method 5005 (see 4.4.5)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

TABLE II. Electrical test requirements – Continued.

2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).

3/ The burn-in shall meet the requirements of 4.2.1a herein.

4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters the read-and-record requirements are for delta measurements only.

5/ Delta limits shall be required only on table I, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table III.

6/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table II).

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}	01	±100 nA 2/
	I_{CCZ}	02	±300 nA
Supply current delta	ΔI_{CC}	02	±0.4 mA
Input current low level	I_{IL}	02	±20 nA
Input current high level	I_{IH}	02	±20 nA
Output voltage low level (I_{OL} = 24 mA, V_{CC} = 5.5 V)	V_{OL}	02	±0.04 V
Output voltage high level (I_{OH} = -24 mA, V_{CC} = 5.5 V)	V_{OH}	02	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ Guaranteed, if not tested.

4.4.2 Group B inspection. When applicable, the group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained be the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes B, S, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes B, S, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, B, S, Q, and V for levels M, D, P, L, R, and F, shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Device type 01:

(1) Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20% and all outputs are open.

(2) Inputs tested low, V_{CC} = 5.5 V dc +5 %, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20% and all outputs are open.

b. Device type 02:

(1) Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.5.1.1 Accelerated aging test. Accelerated aging shall be performed on classes M, B, S, Q, and V devices requiring an RHA level greater that 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes B, S, Q, and V. Sources of supply for device classes B, S, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A

A.1 SCOPE

A.1.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. For new designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing designs prior to the date of this document the new PIN can be used in lieu of the old PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

A.2 APPLICATION DOCUMENTS

This section is not applicable to this appendix.

A.3 SUBSTITUTION DATA

New PIN	Old PIN
5962-8960101MRA	5962-8960101RA
5962-8960101MSA	5962-8960101SA
5962-8960101M2A	5962-89601012A

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-03-18

Approved sources of supply for SMD 5962-89601 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8960101RA	3/	54ACT574
5962-8960101SA	3/	54ACT574FMQB
5962-89601012A	3/	54ACT574LMQB
5962-8960101MRA	27014	54ACT574DMQB
5962-8960101MSA	27014	54ACT574FMQB
5962-8960101M2A	27014	54ACT574LMQB
5962-8960101BRA	3/	54ACT574
5962-8960101BSA	27014	JM54ACT574BSA
5962-8960101B2A	27014	JM54ACT574B2A
5962-8960101SRA	3/	54ACT574
5962-8960101SSA	3/	54ACT574
5962-8960101S2A	3/	54ACT574
5962R8960101SZA	27014	JM54ACT574SZA-R
5962R8960101BRA	27014	JM54ACT574BRA-R
5962R8960101BSA	27014	JM54ACT574BSA-R
5962R8960101B2A	27014	JM54ACT574B2A-R
5962R8960101SRA	27014	JM54ACT574SRA-R
5962R8960101SSA	27014	JM54ACT574SSA-R
5962R8960101S2A	27014	JM54ACT574S2A-R
5962-8960102QXA	F8859	54ACT574K02Q
5962-8960102QXC	F8859	54ACT574K01Q
5962-8960102VXA	F8859	54ACT574K02V
5962-8960102VXC	F8859	54ACT574K01V
5962F8960102QXA	F8859	RHFACT574K02Q
5962F8960102QXC	F8859	RHFACT574K01Q
5962F8960102VXA	F8859	RHFACT574K02V
5962F8960102VXC	F8859	RHFACT574K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
F8859	ST Microlelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.