INCH-POUND
MIL-M-38510/2G
8 February 2005
SUPERSEDING
MIL-M-38510/2E
24 December 1974

MIL-M-0038510/2F (USAF) 24 OCTOBER 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

- 1. SCOPE
- 1.1 <u>Scope.</u> This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outlines/lead finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).
 - 1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.
 - 1.2.1 <u>Device types.</u> The device types are as follows:

Device type	<u>Circuit</u>
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop, no preset
03	Dual J-K master-slave flip-flop, no preset
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop
06	Single edge-triggered J-K flip-flop
07	Dual D-type edge-triggered flip-flop, buffered output

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil

AMSC N/A FSC 5962

1.2.3 <u>Case outlines</u>. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
Α	GDFP5-F14 or CDFP6-F14	14	Flat pack
В	GDFP4-F14	14	Flat pack
С	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.3 Absolute maximum ratings.

Supply voltage rangeInput voltage range	
Storage temperature range	
Maximum power dissipation, (P _D)	
flip-flop, <u>1</u> /	. 110 mW <u>1</u> /
Lead temperature (soldering, 10 seconds)	. 300°C
Thermal resistance, junction to case (θ _{JC}):	. 0.09°C/mW for flat packs
	0.08°C/mW for dual-in-line pack
Junction temperature (T _J)	. 175°C

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	
	5.5 V dc maximum
Minimum high-level input voltage (V _{IH})	2.0 V dc
Maximum low-level input voltage (V _{IL})	0.8 V dc
Normalized fanout (each output) 2/	10 maximum
Case operating temperature range (T _C)	-55 °C to +125 °C
Input set up time:	
Device type 01, 02, 03 and 04,	≥ clock pulse width
Device type 05, 06, and 07	20 ns
Input hold time	
Device types 01, 02, 03 and 04	0 ns
Device type 05, 06 and 07	5 ns

2. APPLICABLE DOCUMENTS

2.1 <u>General</u>. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration

^{2/} Device will fanout in both high and low levels to the specified number of I_{IL1}/I_{IH1} inputs of the same device type as that being tested.

2.2 Government documents.

2.2.1 <u>Specifications and Standards</u>. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 <u>Order of precedence.</u> In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Qualification</u>. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).
- 3.2 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
- 3.3 <u>Design, construction, and physical dimensions.</u> The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
- 3.3.1 <u>Terminal connections and logic diagrams</u>. The terminal connections and logic diagrams shall be as specified on figures 1.
 - 3.3.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.
- 3.3.3 <u>Schematic circuits.</u> The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.
 - 3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.
- 3.4 <u>Lead material and finish.</u> The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).
- 3.5 <u>Electrical performance characteristics</u>. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.
- 3.6 <u>Electrical test requirements</u>. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III. Subgroups 7 and 8 testing requires only a summary of attributes data.
 - 3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 9/	Device	Lim	nits	Units
			Type	Min	Max	
High-level output voltage	V _{OH}	V _{CC} =4.5 V	All	2.4		Volts
		I _{OH} = -400 μA				
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}, I_{OL} = 16 \text{ mA}$	_			Volts
Input clamp voltage	V _{IC}	$V_{CC} = 4.5 \text{ V}, I_{IC} = -12 \text{ mA}$ $T_{C} = 25^{\circ}\text{C}$	All		-1.5	Volts
Low-level input current	I_{IL1}	$V_{CC} = 5.5 \text{ V}$	01, 02, 03, 04,	-0.7	-1.6	mA
		$V_{IN} = 0.4 \text{ V } \underline{1}/$				
		.,				mA
Low-level input current	I _{IL2}	V _{CC} = 5.5 V		-1.4	-3.2	mA
		$V_{IN} = 0.4 \text{ V } \underline{2}/$		1.0	2.2	A
Low lovel input current		V _{CC} = 5.5 V	* *			mA m ^
Low-level input current	I _{IL3}		01, 02, 03, 04	-0.7	-3.2	mA
High-level input current	I _{IH1}	$V_{IN} = 0.4 \text{ V} \underline{6}/$ $V_{CC} = 5.5 \text{ V}$	ΔΙΙ		40	μА
riigii-ieveriiiput current	"IH1	$V_{IN} = 2.4 \text{ V} \frac{5}{4}$	All		40	μΑ
High-level input current	I _{IH2}	V _{CC} = 5.5 V	All		100	μА
ringir level in par carrent	·Inz		7			μιν
High-level input current	I _{IH3}	$V_{IN} = 5.5 \text{ V} \underline{5}/$ $V_{CC} = 5.5 \text{ V}$	All 11/		80	μА
3		$V_{IN} = 2.4 \ V \ 3/$	_			
High-level input current	I _{IH4}	$V_{CC} = 5.5 \text{ V}$	All		200	μА
		$V_{IN} = 5.5 \text{ V} \frac{3}{7}$ $V_{CC} = 5.5 \text{ V}$				
High-level input current	I _{IH5}	$V_{CC} = 5.5 \text{ V}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	μΑ		
		$V_{IN} = 2.4 \text{ V } \frac{7}{8}$,		120	μΑ
High-level input current	I _{IH6}	$V_{CC} = 5.5 \text{ V}$	05, 07		300	μΑ
		$V_{IN} = 5.5 \text{ V} \underline{8}/$ $V_{CC} = 5.5 \text{ V}$				·
Short-circuit output current	los	$V_{CC} = 5.5 \text{ V}$ $V_{IN} = 0.4/$	All	-20	-57	mA
Supply current per device	I _{cc}	$V_{IN} = 0$ <u>4/</u> $V_{CC} = 5.5$ V	01		20	mA
,		V _{IN} = 5 V	02, 03, 04		40	
			05, 06, 07		30	
Maximum clock frequency 10/	f _{MAX}		01, 02, 03	10		MHz
· , _			04, 05, 07			
				15		
Propagation delay to high logic level	t _{PLH}		01, 02, 03, 04,	5	39	ns
(clear or preset to output)						
		$V_{CC} = 5 \text{ V}$				
Propagation delay to low logic level	t _{PHL}	$V_{CC} = 5$ V CL = 50 pF minimum		5	50	ns
(clear or preset to output)		$RL = 390\Omega \pm 5\%$			00	
		NE = 33022 ± 370				
Decreasion delevite high legic level	_	4				
Propagation delay to high logic level (clock to output)	t _{PLH}					ns
(Glock to output)				S S	39	
	1			5	31	
Propagation delay to low logic level	t _{PHL}	1	06	5	62	ns
(clock to output)	YPHL		01, 02, 03, 04,	5	50	110
(05			
	1		07	5	39	

^{1/} Input condition – J or K for device types 01, 02, 03, 04, 06, and preset or D for device types 05 and 07, and clock, clear or preset for device type 06.

^{2/} Input condition – Clock for device types 01, 02, 03 and 04, and clear or clock for device types 05 and 07.

^{3/} Input condition – Clear or preset for device types 01, 02, 03, 04, 05, 06 and 07 and clock for device types 05 and 07.

^{4/} No more than one output should be shorted at a time.

^{5/} Input condition – J or K for device types 01, 02, 03, 04, 06, and D for device types 05 and 07, and clock for device type 06.

^{6/} Input condition – Clear or preset for device types 01, 02, 03 and 04.

^{7/} Input condition – Clock for device types 01, 02, 03 and 04.

- 8/ Input condition Clear for device types 05 and 07.
- 9/ See table III for complete terminal conditions.
- 10/ Minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- $\underline{11}$ / For device types 02 and 03, limits are 0 to 120 μ A.

TABLE II. Electrical test requirements.

	Subgroups	(see table III)
MIL-PRF-38535	Class S	Class B
test requirements	devices	devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 8, 9	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7 9
Group B test when using the method 5005 QCI option	1, 2, 3,	N/A
Group C end-point electrical parameters	1, 2, 3,	1, 2, 3
Additional electrical subgroups for Group C periodic inspections	N/A	10, 11
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

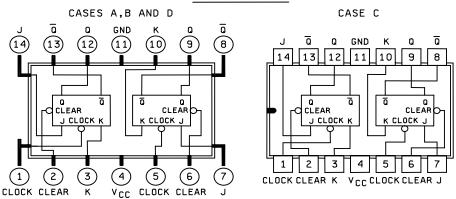
^{*}PDA applies to subgroup 1.

4. VERIFICATION

- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.
- 4.2 <u>Screening.</u> Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
 - a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
 - c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.
 - 4.3 <u>Qualification inspection.</u> Qualification inspection shall be in accordance with MIL-PRF-38535.
- 4.4 <u>Technology Conformance inspection (TCI).</u> Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

- 4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, and 6 shall be omitted.
 - 4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.
- 4.4.3 <u>Group C inspection.</u> Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burnin test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- 4.4.4 <u>Group D inspection.</u> Group D inspection shall be in accordance with table V of MIL-PRF-38535. Endpoint electrical parameters shall be as specified in table II herein.
 - 4.5 Methods of inspection. Methods of inspection shall be specified and as follows:
- 4.5.1 <u>Voltage and current.</u> All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

DEVICE TYPE 01 CASE C CASES A,B AND D (13)(11)VCC PRESETCLOCK K3 K2 (10)(12)(9) (8) 14 13 12 11 10 PRESET 2 [] 3 (1) (2) (3) (4) (5) K1 CLOCK PRESET V_{CC} CLEAR 6 NC NC CLEAR J1 J2 DEVICE TYPE 02 CASES A,B AND D CASE C

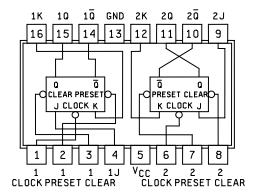


CASE C VCC CLEAR CLOCK K CLEAR CLOCK J 14 13 12 11 10 9 8 J CLOCK K CLOCK J CLEAR G G G 1 2 3 4 5 6 7

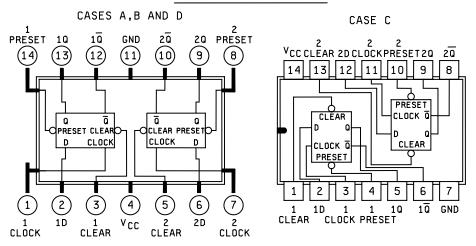
DEVICE TYPE 03

FIGURE 1. Logic diagram and terminal connections.

DEVICE TYPE 04 CASES E AND F



DEVICE TYPES 05 AND 07



DEVICE TYPE 06

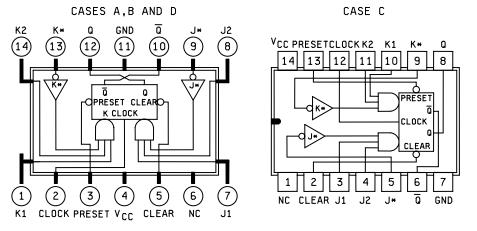


FIGURE 1. Logic diagram and terminal connections – Continued.

Device type 01

Truth table						
t	t _n + 1					
J	J K					
L	L	Q_n				
L	Н	L				
Н	L	Н				
Н	Н	\overline{Q}_n				

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level Preset and clear are independent of clock and dominate

regardless of the state of clock or J of K inputs.

NOTES:
$$1. J = J1 \bullet J2 \bullet J3$$

3. t_n = Bit time before clock pulse.

4. $t_n + 1$ = Bit time after clock pulse.

Device type 02 and 03

Truth table each flip-flop							
t _n t _n +							
J	J K						
L	L L						
L	L H						
Н	L	Н					
Н	Н	Q _n					

Positive logic: Low input to clear sets Q to low-level

Clear is independent of clock and dominate regardless of the state of clock or J or K inputs.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

FIGURE 2. Truth tables.

Device type 04

Truth table each flip-flop							
t	t _n + 1						
J	J K						
L	L L						
L	L H						
Н	H L						
Н	Н	$\overline{\overline{Q}}_n$					

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate regardless of the state of clock or J of K inputs.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

Device type 05 and 07

Truth table each flip-flop							
t _n t _n + 1							
INPUT D	OUTPUT Q	OUTPUT Q					
L	L	Н					
Н	Н	L					

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate

regardless of the state of clock or D input.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

FIGURE 2. <u>Truth tables</u> – Continued.

Device type 06

Truth table							
t	t _n + 1						
J	J K						
L	Qn						
L	L H						
Н	H L						
Н	Н	$\overline{\overline{Q}}_n$					

Positive logic: Low input to preset sets Q to high-level

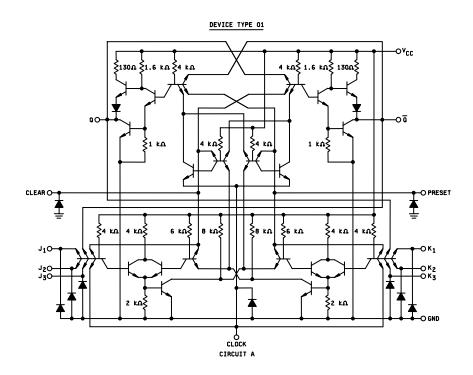
Low input to clear sets Q to low-level Preset or clear function can occur only When clock input is low.

NOTES: 1. J = J1 • J2 • $\overline{J^*}$

2. K = K1 • K2 • K*

- 3. t_n = Bit time before clock pulse.
- 4. $t_n + 1$ = Bit time after clock pulse.
- 5. If inputs J* or K* are not used must be grounded.

FIGURE 2. <u>Truth tables</u> – Continued.



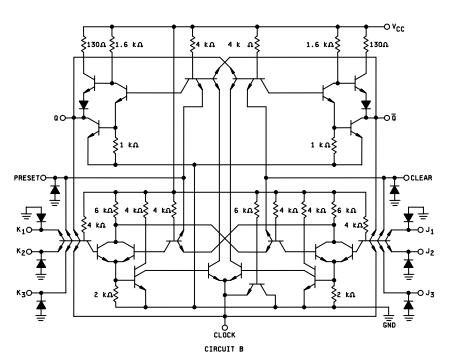


FIGURE 3. Schematic circuits.

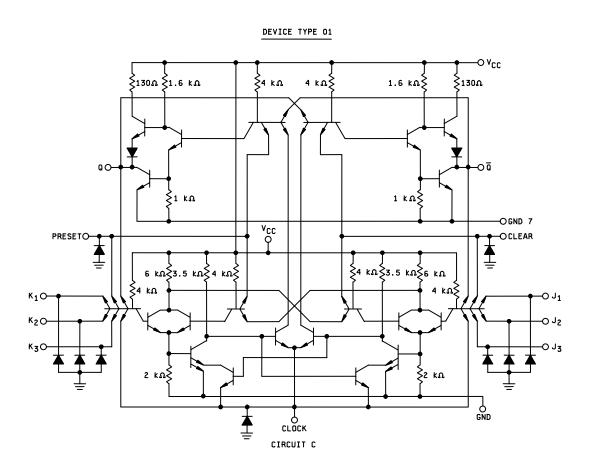


FIGURE 3. <u>Schematic circuits</u> – Continued.

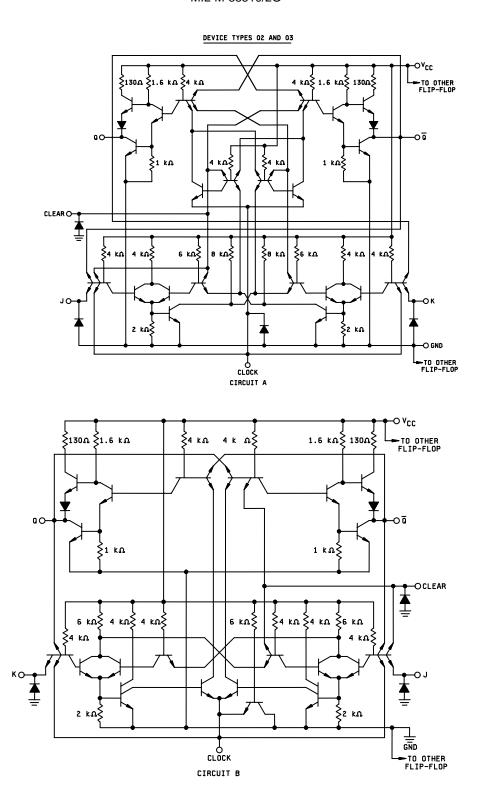
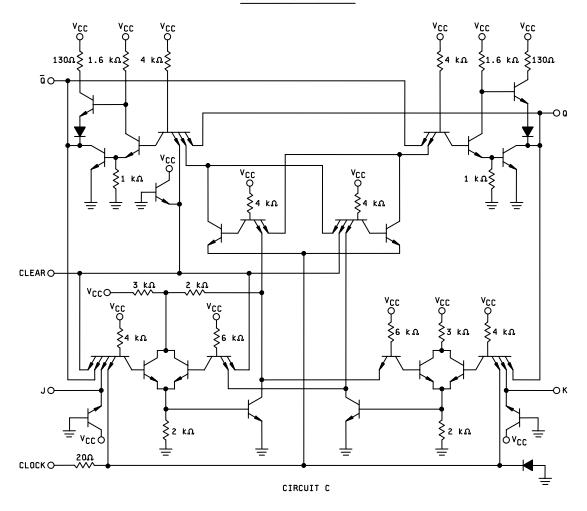


FIGURE 3. Schematic circuits - Continued.

DEVICE TYPES 02 AND 03



- 1. Circuits A, B, and C are the only acceptable variations for device types 02 and 03.
- 2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

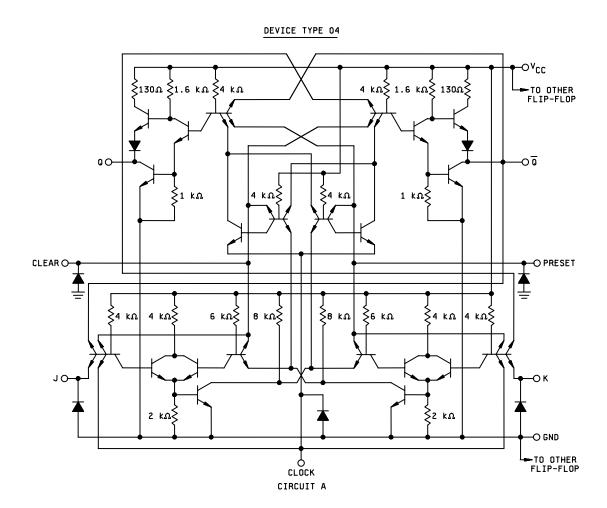


FIGURE 3. <u>Schematic circuits</u> – Continued.

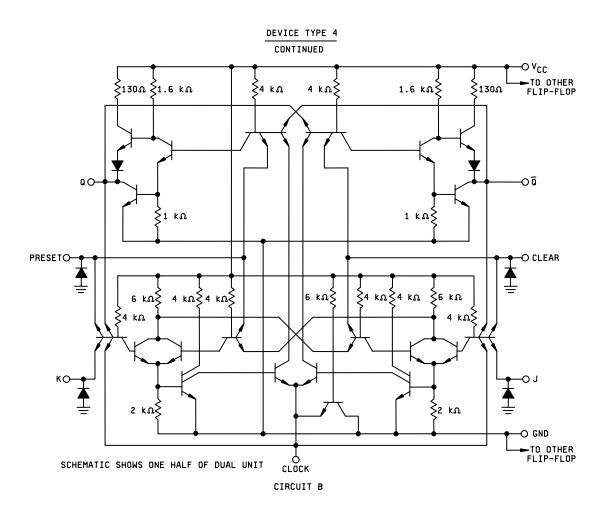
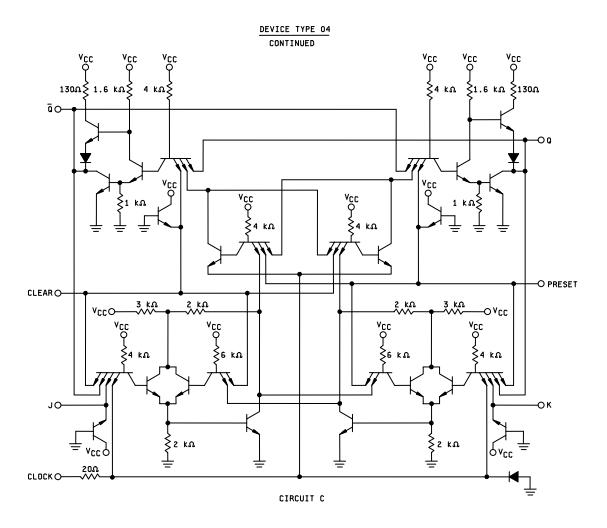
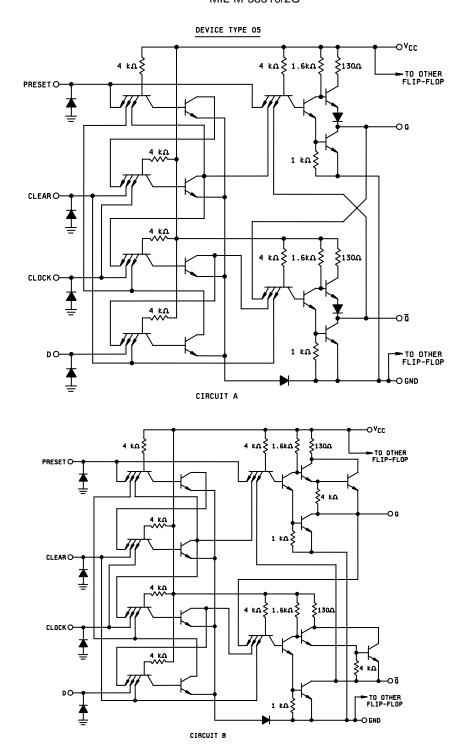


FIGURE 3. <u>Schematic circuits</u> – Continued.



- 1. Circuits A, B and C are the only acceptable variation for device type 04.
- 2. All resistance values shown are nominal.

FIGURE 3. <u>Schematic circuits</u> – Continued.



- Circuits A, B, and C are the only acceptable variations for device type 05. All resistance values shown are nominal.
- 2.

FIGURE 3. Schematic circuits - Continued.

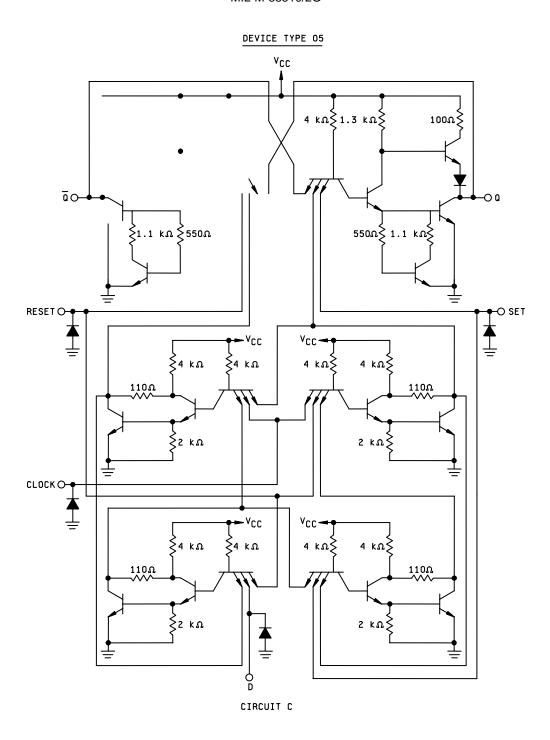
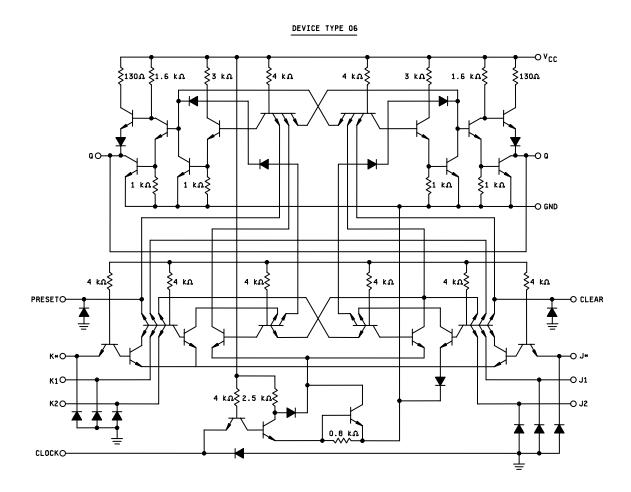
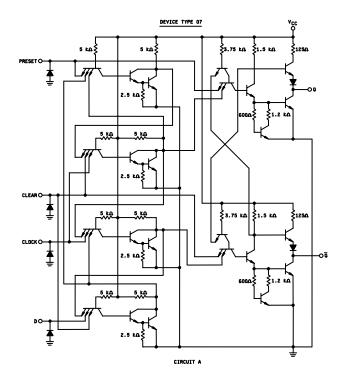


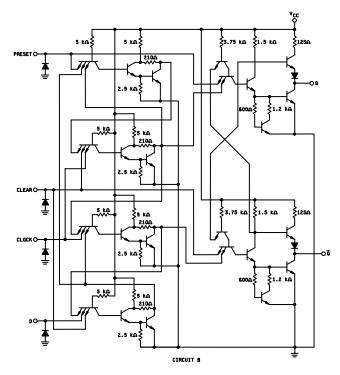
FIGURE 3. <u>Schematic circuits</u> – Continued.



NOTE: All resistance values shown are nominal.

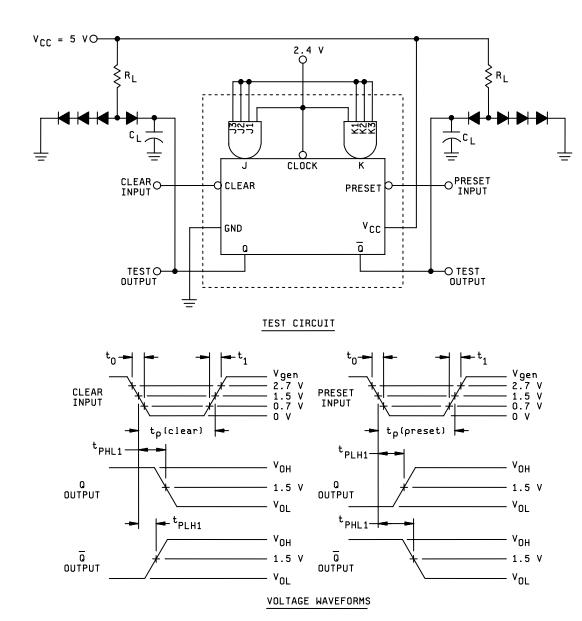
FIGURE 3. <u>Schematic circuits</u> – Continued.





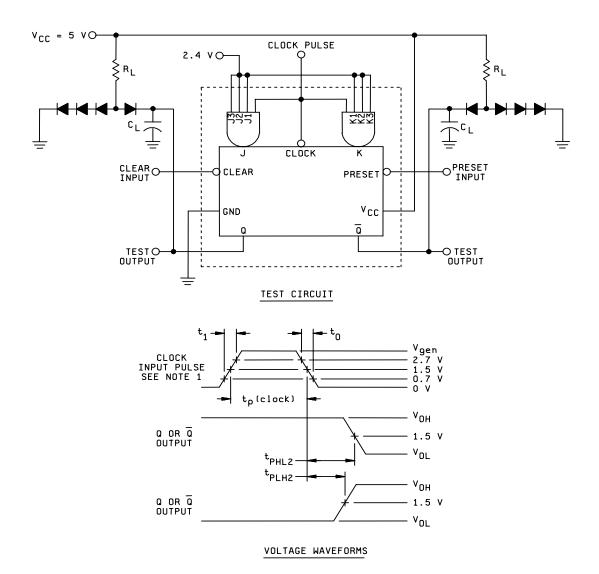
- Circuits A and B are the only acceptable variations for device type 07.
 All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.



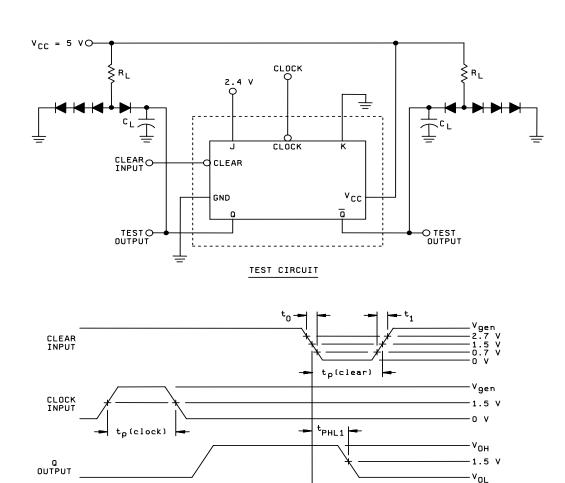
- 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
- 2. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(clear) = t_p(preset) = 30 \text{ ns}$, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
- 3. $C_L = 50$ pF, minimum (C_L includes probe and jig capacitance).
- 4. $R_L = 390\Omega \pm 5\%$.
- 5. All diodes are 1N3064, or equivalent.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 4. Clear and preset switching test circuit and waveforms for device type 01.



- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
- 2. $J = J1 \cdot J2 \cdot J3$; and $K = K1 \cdot K2 \cdot K3$
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF minimum } (C_L \text{ includes probe and jig capacitance}).$
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 5. Synchronous switching test circuit for device type 01.



VOLTAGE WAVEFORMS

t_{PLH1}

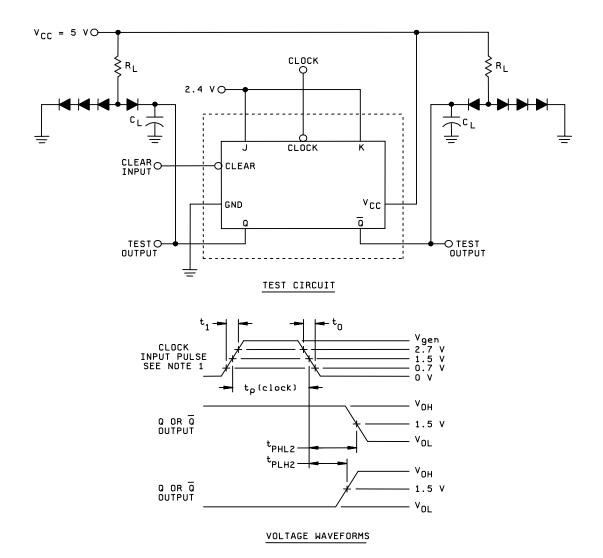
٧он 1.5 V

· V_{OL}

NOTES:

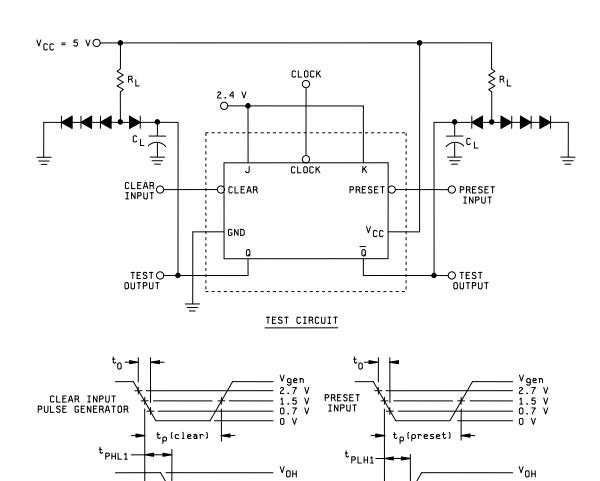
- Clear inputs dominate regardless of the state of clock or J-K inputs. Clear input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(\text{clear}) = 30 \text{ ns}$, PRR = 1 MHz.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50$ pF, minimum (C_L includes probe and jig capacitance).
- 5. $R_L = 390\Omega \pm 5\%$.
- 6. Clock input pulse characteristics: $V_{gen} = 3 \text{ V}, t_p \text{ (clock)} \ge 25 \text{ ns}, PRR = 1 \text{ MHz}.$

FIGURE 6. Clear switching test circuit and waveforms for device types 02 and 03.



- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0\leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0\leq 10$ ns, t_p (clock) = 20 ns, and PRR = 10 MHz for subgroups 9, 10, and 11.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF minimum (including jig and probe capacitance).
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 7. Synchronous switching test circuit for device type 02 and 03.



VOLTAGE WAVEFORMS

 v_{OL}

 v_{OH}

 v_{OL}

1.5 V

Q OUTPUT

OUTPUT

^tPHL1-

1.5 V

 v_{OL}

۷он

VOL

1.5 V

NOTES:

1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.

t_{PLH1}

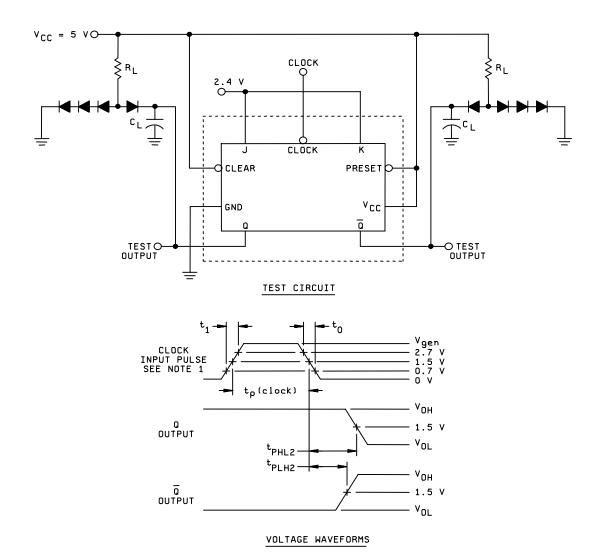
- 2. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(clear) = t_p(preset) = 30 \text{ ns}$, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
- 3. $C_L = 50$ pF, minimum (including jig and probe capacitance).
- 4. $R_L = 390\Omega \pm 5\%$.
- 5. All diodes are 1N3064, or equivalent.

OUTPUT

Q OUTPUT

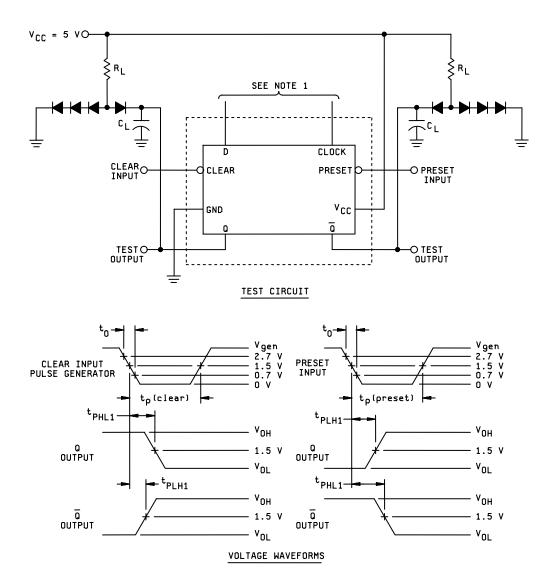
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 8. Clear and preset switching test circuit and waveforms for device type 04.



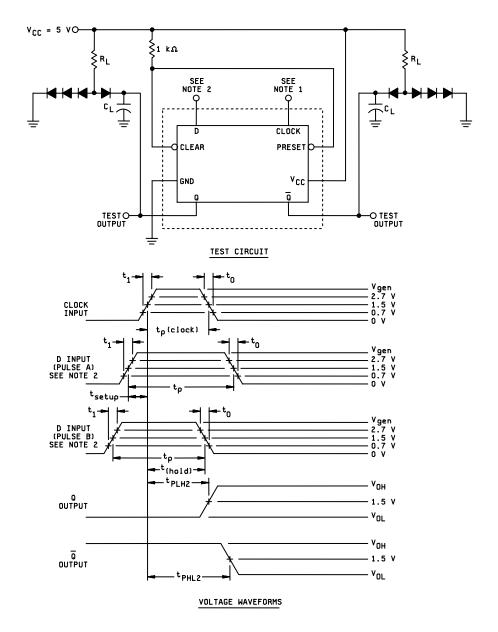
- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50 \text{ pF minimum (including jig and probe capacitance)}$.
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 9. Synchronous switching test circuit for device type 04.



- 1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
- 2. All diodes are 1N3064, or equivalent.
- 3. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_o \le 7 \text{ ns}$, t_p (clear) = t_p (preset) = 35 ns, and PRR = 1 MHz.
- 4. C_L = 50 pF, minimum (including jig and probe capacitance).
- 5. $R_L = 390\Omega \pm 5\%$.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 10. Clear and preset switching test circuit and waveforms for device types 05 and 07.



- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 \le 10 \text{ ns}$, t_p (clock) = 30 ns, and PRR = 1 MHz. When testing f_{MAX} , PRR = see table III.
- 2. D input (pulse A) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 \le 10$ ns, $t_{SETUP}=25$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 < 7$ ns, $t_{hold}=6$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF minimum (including jig and probe capacitance)}$.
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 11. Synchronous switching test circuit (high level data) for device types 05 and 07.

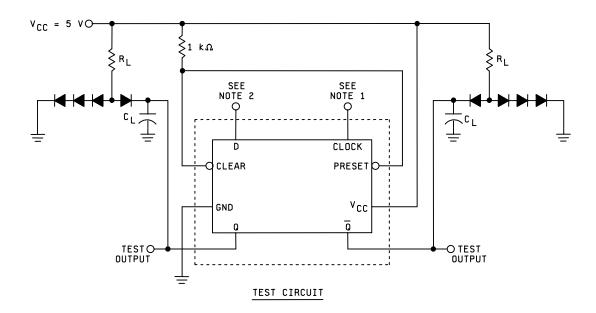
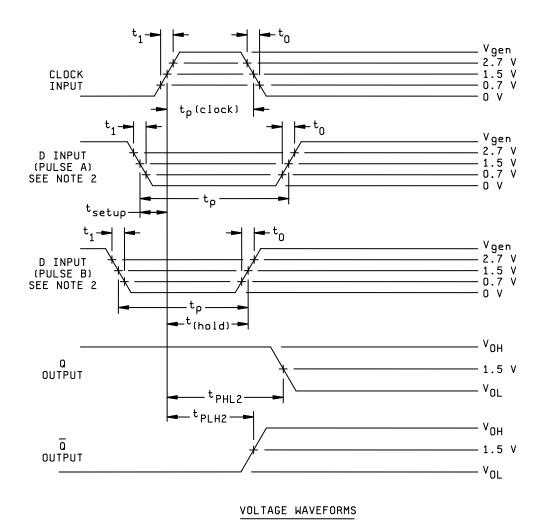
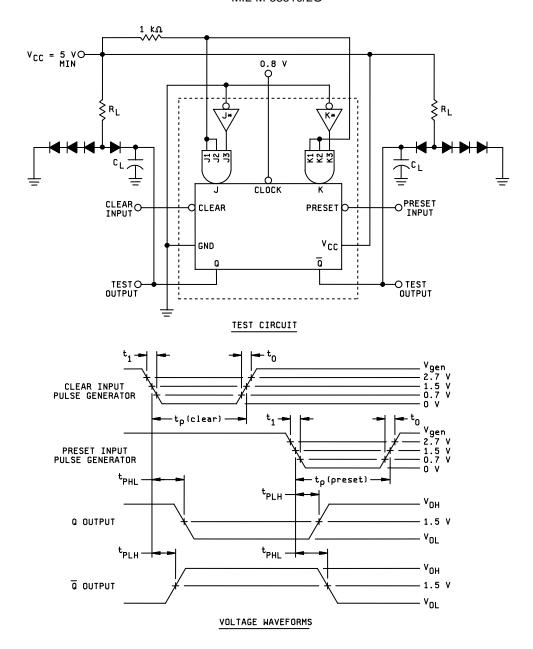


FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07.



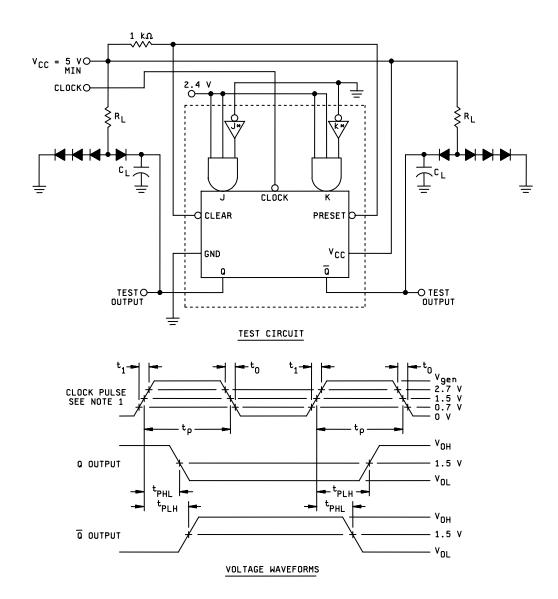
- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 < 10 \text{ ns}$, t_p (clock) = 30 ns, and PRR = 1 MHz.
- 2. D input (pulse A) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 \le 10$ ns, $t_{SETUP}=25$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 < 10$ ns, $t_{hold}=6$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50$ pF minimum (including jig and probe capacitance).
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07 - Continued.



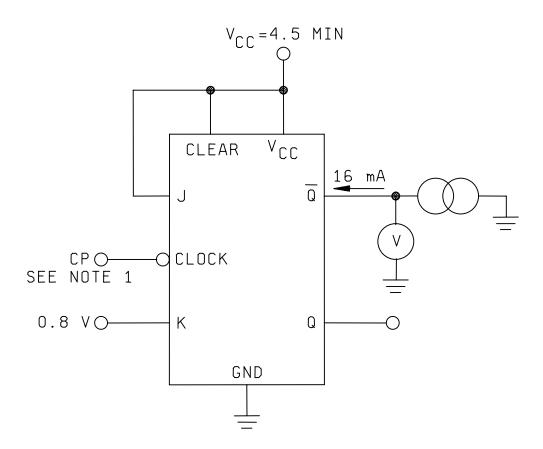
- 1. Preset or clear function can occur only when clock input is low. Gated inputs are inhibited.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF, minimum, including jig and probe capacitance.
- 4. Clear or preset input pulse characteristics: $V_{gen} = 3.0 \text{ V}$, $t_o = 5 \text{ ns}$, $t_1 \le 10 \text{ ns}$, $t_p = 25 \text{ ns}$.
- 5. $R_L = 390\Omega \pm 5\%$.

FIGURE 13. Clear and preset switching test circuit and waveforms for device types 06.



- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 = t_0 \le 10 \text{ ns}$, $t_p = 30 \text{ ns}$, and PRR = 1 MHz. When testing f_{MAX} , PRR = see table III.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50 \text{ pF}$ minimum including jig and probe capacitance.
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 14. Synchronous switching test circuit for device type 06.



- 1. Apply normal clock pulse, then sink -12 mA on the clock input.
- 2. The output \overline{Q} is measured after -12 mA is applied to the clock to insure it is still in the low state.

FIGURE 15. Input clamp voltage test circuit for device types 01, 02, 03, and 04 (circuit B).

TABLE III. Group A inspection for device type 01. 1/

Subgroup	Symbol	MIL-	Case A, B, D	11	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	
•		STD-883	Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11	Meas.			
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	ā	GND	Q	K2	K3	terminal	Min	Max	Unit
1 2/	V _{OH}	3006	1	0.8 V	Α		4.5 V			2.0 V	2.0 V	2.0 V			4 mA	0.8 V	0.8 V	Q	2.4		V
$T_C = 25^{\circ}C$	"	66	2	2.0 V	Α		"			0.8 V	0.8 V	0.8 V	4 mA	"		2.0 V	2.0 V	ā	66		
	ıı.	4	3			0.8 V		2.0 V							4 mA			Q	44		
	и	a	4			2.0 V	"	0.8 V					4 mA	"				ā	44		"
		0000	_	0.01/						0.01/	0.01/	0.01/			40.	0.01/	0.01/				
	V _{OL}	3007	5 6	2.0 V 0.8 V	A					0.8 V 2.0 V	0.8 V 2.0 V	0.8 V 2.0 V	16 mA		16 mA	2.0 V 0.8 V	2.0 V 0.8 V	Q —		0.4	
				0.6 V	A					2.0 V	2.0 V	2.0 V				0.6 V	0.6 V	ā			
"	"	44	7			0.8 V	"	2.0 V					16 mA	"				ā		**	"
"	"	44	8			2.0 V	"	0.8 V						"	16 mA			Q			"
"	V _{IC}	**	9				"			-12 mA				"				J1		-1.5	"
	"	44	10				"				-12 mA			"				J2		"	"
"	ű	ű	11				ii ii					-12 mA		"				J3		ii ii	"
		4	12	-12 mA			"							"				K1		"	
			13 14													-12 mA	-12 mA	K2 K3			
			15				"	-12 mA						- 4			-12 MA	Clear			
"		4	16			-12 mA		-12 IIIA										Preset			
	"		17		-12 mA	-12 111/4								"				Clock			
"	и	ш	17 CKT B	0.8 V	A*		"	4.5 V		4.5 V	4.5 V	4.5 V				0.8 V	0.8 V	Clock		0.5	"
**	I _{IL1}	3009	18	GND	4.5 V		5.5 V	В		0.4 V	4.5 V	4.5 V				GND	GND	J1	-0.7	-1.6	mA
"	ш	*	19	u	"		"	В		4.5 V	0.4 V	4.5 V		"		GND	GND	J2	ш	"	"
"	"	44	20	u				В		4.5 V	4.5 V	0.4 V		"		GND	GND	J3	44	"	"
	"	a	21	0.4 V	"	В				GND	GND	GND		"		4.5 V	4.5 V	K1	66	"	"
			22	4.5 V 4.5 V		В				GND	GND GND	GND				0.4 V 4.5 V	4.5 V 0.4 V	K2 K3		- "	
	I _{II 2}		23	4.5 V 4.5 V	0.4 V	B B	"			GND 4.5 V	4.5 V	GND 4.5 V				4.5 V 4.5 V	0.4 V 4.5 V	Clock	-1.4	-3.2	mA
44	I _{II 2}	м	25	4.5 V	0.4 V	ь		В		4.3 V	4.5 V	4.5 V		- 4		4.3 V	4.5 V	Clock	-1.4	-3.2	"
	I _{IL3}		26 CKT A		4.5 V	0.4 V	ш											Preset	-0.7	-1.6	ш
"	"ILO	4	26 CKT B	u		0.4 V					44					"		Preset	-1.4	-3.2	"
"	"		27 CKT A					0.4 V		"	44							Clear	-0.7	-1.6	"
"	и	a	27 CKT B	a a				0.4 V		"	a	44						Clear	-1.4	-3.2	
"	I _{IH1}	3010	28		GND		"	GND		2.4 V	GND	GND		"				J1		40	μА
	"	66	29				ii ii	GND		GND	2.4 V	GND		"				J2		"	"
			30	2.4 V		GND	"	GND		GND	GND	2.4 V				GND	ONE	J3			"
			31 32	GND		GND								- 4		2.4 V	GND GND	K1 K2			
44		м	33	GND		GND								- 4		GND	2.4 V	K3		ш	
	I _{IH2}	66	34	0.15		0.10	"	GND		5.5 V	GND	GND		44		0.10	2	J1		100	"
**	""		35				"	GND		GND	5.5 V	GND						J2		"	"
**			36				"	GND		GND	GND	5.5 V						J3		"	"
"	ш	*	37	5.5 V	"	GND	"							"		GND	GND	K1		"	"
"	"	**	38	GND		GND	"									5.5 V	GND	K2			"
"		4	39	GND	"	GND		0.417	ļ	ONE	O.U.D.	ON ID	1	"	ļ	GND	5.5 V	K3		"	"
-	IH3		40	4.5 V	A	0.417	"	2.4 V GND		GND	GND	GND	-			4.5 V GND	4.5 V	Clear	-	80	
	IH3	"	41 42	GND GND	A	2.4 V 5.5 V	"	GND		4.5 V 4.5 V	4.5 V 4.5 V	4.5 V 4.5 V	 			GND	GND GND	Preset	 	80 200	
	I _{IH4}		42	4.5 V	A	5.5 V	"	5.5 V		4.5 V GND	4.5 V GND	4.5 V GND	-	- 4		4.5 V	4.5 V	Preset Clear		200	
4	и		44	GND	5.5 V			GND		GND	GND	GND	 			GND	GND	Clock	 	"	
	и		45	GND	5.5 V	GND	ш	0.10		GND	GND	GND	1	4		GND	GND	Clock	l		
									1					1					1		

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. 1/ - Continued.

Subgroup	Symbol	MIL- STD-883	Case A, B, D Case C	9	12	3 13	4 14	5 2	6	7	8	9 5	10 6	11 7	12 8	13 10	14 11	Meas.	Т.	est limits	
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3		GND	Q Q	K2	K3	terminal	Min	Max	Ur
						1 10301			140				Ισ		3						U
1	I _{IH5}	3010	46 CKT A	GND	2.4 V		5.5 V	GND		GND	GND	GND		GND		GND	GND	Clock	-50	-700	ŀ
c = 25°C	"	44	46 CKT B		"		и	GND		"	66	"		"		"	er er	"	-200	-850	П
4	"	44	46 CKT C		"		и	GND		"	66	"		"		"	er er	"	-400	-1000	
4	"	44	47 CKT A		"	GND	и			"	66	"		"		"	er er	"	-50	-700	
	"	44	47 CKT B			GND	"			*	66	"					44	"	-200	-850	
	"	66	47 CKT C			GND				"	66			"		"	66	"	-400	-1000	
	Ios	3011	48	4.5 V	GND	GND	5.5 V			4.5 V	4.5 V	4.5 V				4.5 V	4.5 V	Q	-20	-57	r
"	Ios	3011	49	4.5 V	"		"	GND		4.5 V	4.5 V	4.5 V	GND	"		4.5 V	4.5 V	<u>_</u>	-20	-57	
"	Icc	3005	50	GND	"	GND	и			GND	GND	GND		"		GND	GND	V _{CC}		20	H
u	Icc	3005	51	GND	4	0.10	и	GND		GND	GND	GND		44		GND	GND	Vcc		20	
2			nditions and limits		roup 1 over	ont T 125	0C and 1/	tooto oro or	mitted					!				-00			_
3			nditions and limits	as for subg	group 1, exce	ept T _C = -55	°C and V _{IC}	tests are or	nitted.	В	В	В	Н 2/	CND	1.2/	В	В	T All		Uarl	
7 <u>2</u> / <u>4</u> Γ _C = 25°C		1	52 53	B B	B B	A B	4.5 V	B A	B B	B B	B B	B B	H <u>3</u> /	GND "	L <u>3/</u> H	B B	B B	All output		H or L shown 3	.,
C = 25°C			54	В	В	A	и	A	В	В	В	В	- L	"	H	A	A	output "	as	" "	
			55	В	A	A	u	A	В	В	В	В	i		Н	A	A			44	
			56	В	В	A		A	В	В	В	В	- t		H	A	A			"	_
			57	A	В	A		A	В	В	В	В	ì		H	В	A			"	
			58	A	A	A	и	A	В	В	В	В	Ĺ	**	H	В	A	*		44	_
			59	A	В	A	ш	A	В	В	В	В	- i		H	В	A	"		44	_
			60	A	В	A	ш	A	В	В	В	В	Ĺ		Н	A	В	"		44	_
			61	A	A	A	и	A	В	В	В	В	Ĺ		H	A	В	"		"	_
			62	A	В	A	и	A	В	В	В	В	Ĺ		H	A	В	"		44	
44			63	A	В	A	ш	В	В	В	В	В	Н	44	Ĺ	A	В	"		44	_
"			64	В	В	A	"	A	В	В	A	A	Н		Ē	В	В	"		"	
"			65	В	A	Α	и	A	В	В	A	Α	Н		L	В	В	"		44	
"			66	В	В	A		A	В	В	A	Α	Ι	**	L	В	В	**		a	
			67	В	В	Α	ш	A	В	Α	В	Α	Н		L	В	В	"		44	
"			68	В	A	Α	"	A	В	Α	В	Α	Н	"	L	В	В	"		"	
"			69	В	В	Α	"	A	В	Α	В	Α	Н	"	L	В	В	"		"	
			70	В	В	Α	и	A	В	Α	Α	В	Н	"	L	В	В	"		44	
			71	В	Α	Α	u	Α	В	Α	Α	В	Ι	"	L	В	В	"		44	
			72	В	В	Α		Α	В	Α	Α	В	Н		L	В	В	"		"	
			73	Α	В	Α	"	Α	В	Α	Α	Α	Η		L	Α	Α	"		"	
			74	A	A	Α	и	A	В	Α	A	A	Н	"	L	A	A	"		44	
"			75	Α	В	A	ш	A	В	Α	A	A	L	"	Н	Α	A	"		"	
			76	Α	Α	Α	u	Α	В	Α	A	Α	L	"	Н	Α	Α	"		"	
			77	A	В	Α	u u	A	В	A	A	A	Н	"	L	A	A	"			
			78	A	В	A		В	В	A	A	A	Н		L	A	A	"		-	
			79	A	A	A		В	В	A	A	A	Н		Ļ	A	A				
"			80	A	В	A		В	В	A	A	A	Н		L	A	A			"	
			81	A	В	В		В	В	A	A	A	H		H	A	A		-		
			82	A	A	В	u u	В	В	A	A	A	H		H	A	A				
			83	A	В	В		В	В	A	A	A	H		H	A	A		 		
			84	A	A	В		A	В	A	A	A	L		Н	A	A		ļ		_
			85 86	A B	A	A		A A	B B	A A	A A	A A	L		H	A	A		 		
		1	86 87	В	A	A		A	В	B B	A	A	L		H	A	A				
"		1	88	B	B	A		A	В	В	A	A	H		П .	A	A		-		_
			89	A	A	A	и	A	В	A	A	A	H	"		A	A			4	—
		1	69	A	A	A		A	В	A	A	A	П		L	A	A				

TABLE III. Group A inspection for device type 01. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	s
		STD-883	Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11	Meas.			
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	ā	GND	Q	K2	K3	terminal	Min	Max	Unit
7 <u>2</u> / <u>4</u> /			91	В	Α	Α	4.5 V	Α	В	В	Α	Α	Н	GND	L	Α	Α	All		H or L	.1
$T_C = 25^{\circ}C$			92	В	В	Α	4.5 V	Α	В	В	Α	Α	L	GND	Н	Α	Α	output		As shown	3/
8 <u>2</u> / <u>4</u> /	Same tests	s, terminal co	nditions and limits	as for sub	group 7, ex	cept T _C = 12	25 and -55	°C.													
9	F _{MAX} <u>5</u> /	(Fig. 5)	93	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	Q	10		MHz
$T_C = 25^{\circ}C$	F _{MAX} <u>5</u> /	(Fig. 5)	94	"	IN	5.0 V		5.0 V			"		OUT					ā	10		MHz
44	t _{PLH1}	3003	95	"	2.4 V	J		IN			"		OUT	44				Clear to Q	5	25	ns
66	t _{PLH1}	(Fig. 4)	96	"	"	IN		J		и	"	ű		66	OUT	4	"	Preset to Q	es .	25	"
66	t _{PHL1}		97	"	"	J		IN		ш	"	ш		66	OUT	"	"	Clear to Q	66	40	44
66	t _{PHL1}	"	98	"		IN		J		"		"	OUT	66		"	"	Preset to Q	66	40	44
es .	t _{PLH2}	3003 (Fig 5	99	"	IN	5.0 V	и	5.0 V		и	44	a	OUT	86		4	"	Clock to Q	44	30	ns
er .	t _{PLH2}		100				ш	ш		"	44	и		44	OUT	a		Clock to Q	-	30	
44	t _{PHL2}	"	101		"	**				"	"	"	OUT	*		"	"	Clock to Q	-	40	"
es .	t _{PHL2}	*	102				ш	ш		"	44	и		44	OUT	a		Clock to Q		40	
10	F _{MAX} <u>5</u> /	(Fig 5)	103	"	"	44					"			44	OUT			Q	10		MHz
$T_C = 125^{\circ}C$	F _{MAX} <u>5</u> /	(Fig 5)	104	"	"	*							OUT	*		"	44	ā	10		MHz
66	t _{PLH1}	3003 (Fig. 4)	105	"	2.4 V	J	и	IN		"	"	и	OUT	84		*	"	Clear to Q	5	39	ns
a	t _{PLH1}	"	106	"	"	IN		J		"	"				OUT	*	"	Preset to Q		39	"
66	t _{PHL1}		107	"	"	J		IN		ш	"	ш			OUT	"	"	Clear to Q	66	50	44
66	t _{PHL1}	"	108	"	"	IN	"	J		"	"	"	OUT	66		"	"	Preset to Q	44	50	"
66	t _{PLH2}	(Fig 5)	109	"	IN	5.0 V	ű	5.0 V		и	"	ű	OUT	a		4	"	Clock to Q	a	39	ns
66	t _{PLH2}		110	"	"	66	"	и		"	"	"		66	OUT			Clock to Q	66	39	
66	t _{PHL2}	"	111	"	*	66	"	ű		"	"	ű	OUT	44				Clock to Q	**	50	"
66	t _{PHL2}		112	"	"	66	"	ш		ш		ш		66	OUT	"	"	Clock to Q	66	50	

NOTES:

- A = Normal clock pulse. B = Momentary GND, then 4.5 V. J = Input pulse t_p = 100 ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V
- *After clock pulse apply -12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15).

- 1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
 2/ Input voltages shown are: A= 2.0 volts minimum and B = 0.8 volts maximum.
 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double camparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
 4/ Tests shall be performed in sequence.
 5/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	
5· P	-,	STD-883	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas.			
		method	Test No.	Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	Q ₂	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	Unit
1	V _{OH}	3006	1	Α		0.8 V	4.5 V							GND	4 mA		2.0 V	q	2.4		V
$T_C = 25^{\circ}C$	"	66	2	Α		2.0 V								66		4 mA	0.8 V	Q 1	66		"
4	"	4	3		0.8 V		44							4		4 mA		Q 1	66		
"	"	66	4				44	Α		2.0 V		4 mA	0.8 V					Q2	66		"
"	"	66	5					Α		0.8 V	4 mA		2.0 V	66				Q 2	66		ii ii
"	ш	66	6				66		0.8 V		4 mA			66				Q 2	66		
	V _{OL}	3007	7	Α		2.0 V	44								16 mA		0.8 V	Q1		0.4	"
44	"	66	8	Α		0.8 V	66							66		16 mA	2.0 V	Q 1		44	
"	"		9		0.8 V		44								16 mA			Q1		"	"
"	ш	66	10				44	Α		0.8 V		16 mA	2.0 V	66				Q2			ш
"	"	66	11					Α		2.0 V	16 mA		0.8 V	66				Q 2		"	
"	ш	66	12				44		0.8 V			16 mA		44				Q2			"
	V _{IC}		13				ш							64			-12 mA	J1		-1.5	"
	"		14				4			-12 mA				66				J2			
			15			-12 mA												K1			
-			16		12 m A								-12 mA					K2 Clear 1			
-			17 18	-12 mA	-12 mA													Clock 1			
			18 CKT B	A*	4.5 V	0.8 V	ш										4.5 V	Clock 1		-0.5	
			19		1.0 1	0.0 1			-12 mA								1.0 1	Clear 2		-1.5	и
	и		20					-12 mA										Clock 2		-1.5	"
44	и		20 CKT B				66	A*	4.5 V	4.5 V			0.8 V					Clock 2		-0.5	
"	I _{IL1}	3009	21	5/	4.5 V	0.414	5.5 V							66			0.4 V	J1	-0.7	-1.6	mA "
-			22 23	<u>5</u> /	4.5 V	0.4 V	4	5/	4.5 V	0.4 V								K1 J2			
			24					5/	4.5 V	U.4 V			0.4 V					K2	66		
**	I _{II 2}		25	0.4 V	В	4.5 V			4.5 V				0.4 1				4.5 V	Clock 1	-1.4	-3.2	
	I _{II 2}	66	26				44	0.4 V	В	4.5 V			4.5 V					Clock 2	-1.4	-3.2	"
	I _{IL3}		27 CKT A, C	4.5 V	0.4 V		66										4.5 V	Clear 1	-0.7	-1.6	ш
44	u u	66	27 CKT B	4.5 V	0.4 V		44										4.5 V	Clear 1	-1.4	-3.2	"
	"	66	28 CKT A, C				"	4.5 V	0.4 V	4.5 V								Clear 2	-0.7	-1.6	
		3010	28 CKT B 29	GND	GND		5.5 V	4.5 V	0.4 V	4.5 V							2.4 V	Clear 2 J1	-1.4	-3.2 40	
	I _{IH1}	3010	30	GND	B	2.4 V	3.3 V										2.4 V	K1		40	μA
			31	GIND	ь	2.4 V	ш	GND	GND	2.4 V								J2		ш	ш
		44	32					GND	В	2.11			2.4 V					K2		ш	и
	I _{IH2}	ш	33	GND	GND												5.5 V	J1		100	
	"	66	34	GND	В	5.5 V	ш							44				K1		"	"
	"	66	35				ш	GND	GND	5.5 V				64				J2		"	"
	u u	66	36				ш	GND	В				5.5 V					K2			"
	I _{IH3} 7/	66	37	GND	E		66	OND		OND				44	-		GND	Clear 1		80	и
	I _{IH3} <u>7</u> / I _{IH4}	4	38 39	5.5 V	5.5 V	GND		GND	E	GND	-		-		 	-	GND	Clear 2 Clock 1	-	80 200	
	IH4	66	40	GND	5.5 V E	GIND	4		-	 	-				1		GND	Clock 1	1	200	
	u u	66	41	GIND			44	5.5 V	5.5 V	GND			GND				GIND	Clock 2			
**	и	66	42			l	44	GND	5.5 V	GND	-		OIND	66	1			Clear 2	l		
	I _{IH5}	44	43 CKT A, C	2.4 V	Е	GND		0.15	· ·	0.15					1		GND	Clock 1	-50	-700	ш
"	"	66	43 CKT B	2.4 V	2.4 V	GND	44								1		GND	Clock 1	-200	-850	
	"		44 CKT A, C				"	2.4 V	E	GND			GND					Clock 2	-50	-700	и
"	"	44	44 CKT B				"	2.4 V	2.4 V	GND			GND					Clock 2	-200	-850	"

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		1	Test limits	š
		STD-883	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas.			
		method	Test No.	Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	Q,	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	L
1	Ios	3011	45	2.4 V	GND	2.4 V	5.5 V							GND		GND	2.4 V	Q 1	-20	-57	r
_C = 25°C		3011**	46	A	4.5 V	0								44	GND		4.5 V	Q1			+
"		3011**	47	Α	4.5 V	U	66	GND	4.5 V	4.5 V		GND	0 V	44	GIND		4.5 V	Q2	"	66	+-
		3011	48				66	2.4 V	GND	2.4 V	GND	GIND	2.4 V	66					"	66	+
											OND							Q 2			
"	I _{cc}	3005	49	D	4.5 V	GND		D	4.5 V	4.5 V			GND	44			4.5 V	V _{CC}		40	_
2	Same test	s, terminal co	nditions and limits	as for subg	roup 1, exce	pt T _C = 12	5°C and V	IC tests are	omitted.												
3	Same test	s, terminal cor	nditions and limits	_																	
7 <u>2</u> / <u>4</u> /			50	В	В	В	4.5 V	В	В	Α	H <u>3</u> /	L <u>3</u> /	В	GND	L <u>3</u> /	H <u>3</u> /	Α	All		H or L	
_C = 25°C			51	Α	В	В	66	Α	В	Α	Н	L	В	44	L	Н	Α	output	a	s shown 3	<u>3</u> /
"			52	В	В	В		В	В	A	Н	L	В		L	Н	A	66			
"			53	В	В	A		В	В	A	Н	L	A		L	Н	A	44			
	 		54 55	A B	B B	A A		A B	B B	A	H	L	A A	44	L	H	A				_
			56	В		A		В		A A	H	L	A	44		H	A	66			_
			57	A	A A	A		A	A A	A	H	Ĺ	A	44		H	A			66	_
**			58	В	A	A	4	В	A	A	Ľ	H	A		H	L'	A			4	_
			59	A	A	Ä	44	A	A	A	Ĺ	H	A	44	H	Ĺ	A	66		ш	_
ii .			60	В	A	A	4	В	A	A	H	Ĺ	A		i.	H	A			44	_
"			61	A	A	A	66	A	A	A	Н	Ē	A	44	ī	Н	A	66		66	_
"			62	В	A	A	44	В	A	A	Ĺ	Н	A		H	Ĺ	A			ш	_
44			63	В	Α	В		В	A	В	L	Н	В	**	Н	L	В	44		44	_
"			64	Α	Α	В	66	Α	A	В	L	Н	В	44	Н	L	В			44	
"			65	В	Α	В	66	В	Α	В	L	Н	В	"	Н	L	В	44		66	
"			66	В	В	В	44	В	В	В	Н	L	В	4	L	Н	В	44		ш	
"			67	В	Α	В	44	В	A	В	Н	L	В	44	L	Н	В	44		66	
"			68	A	A	В	66	Α	A	В	Н	L	В	66	L	Н	В	66		66	
			69	В	Α	В		В	A	В	Н	L	В		L	Н	В				
-			70	В	A	В	66	В	A	A	Н	L	В		L	Н	A				_
			71 72	A B	A A	B B	-	A B	A A	A A	H	L H	B B		L H	H	A	-			_
"			73	В	A	A	44	В	A	В	L	Н	A	44	Н	L	В	44		66	_
			74	A	A	A	- 4	A	A	В	L	H	A	44	H	L	В				_
"			75	В	A	A	66	В	A	В	H	Ë	A	44	ï	H	В	44		44	_
44			76	A	В	A	44	A	В	A	Н	Ē	A		Ē	Н	A			ш	_
			77	Α	Α	Α	66	Α	A	Α	Н	L	Α	66	L	Н	Α	44		66	_
**			78	A	A	Α	44	A	A	В	Н	L	Α		L	Н	В			66	
44			79	Α	Α	В	44	Α	Α	В	Н	L	В	4	L	Н	В	44		44	
			80	В	Α	В	44	В	Α	В	L	Ι	В	44	Ι	L	В	66		66	
"			81	Α	Α	Α	66	Α	Α	Α	L	Н	Α	44	Н	L	Α	66		44	
			82	A	Α	В	66	A	A	A	L	Н	В	44	Н	L	Α	*		66	
"			83	A	A	В	4	A	A	В	L	H	В	4	H	L	В	4			
			84	В	A	В		В	A	В	Н	L	В		L	H	В				
	 		85	A	A	В	66	A	A	Α	H	L	В	66	L	H	A	66		44	_
	 		86	В	A	В		В	A	A	L	Н	В		Н	L	A				_
			87 88	A	A B	B B	-	A	A B	A A	L H	H L	B B		H	L H	A	-			_

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Ι	Test limit	te
Subgroup	Symbol	STD-883	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas.		1631 111111	3
		method	Test No.	Clock 1	Clear 1	K1	V _{cc}	Clock 2	Clear 2	J2	Q ₂	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	Unit
9	F _{MAX} 6/	(Fig 7)	89	IN		2.4 V	5.0 V							GND	OUT		2.4 V	Q ₁	10		MHz
$T_C = 25^{\circ}C$	"		90	IN		2.4 V								44		OUT	2.4 V	Q 1	66		
66	и		91				"	IN		2.4 V		OUT	2.4 V	"				Q_2	66		64
44	"	"	92				"	IN		2.4 V	OUT		2.4 V	"				Q 2	66		4
44	t _{PLH1}	3003	93	IN	IN	GND								44		OUT	2.4 V	Clear 1	5	25	66
		(Fig 6)																to Q 1			
66	t _{PLH1}		94					IN	IN	2.4 V	OUT		GND	"				Clear 2	66	25	4
																		to Q 2			
**	t _{PHL1}	"	95	IN	IN	GND	"							"	OUT		2.4 V	Clear 1 to Q1	66	40	46
66	t _{PHL1}	**	96					IN	IN	2.4 V		OUT	GND	"				Clear 2	66	40	66
4																		to Q2			
	t _{PLH2}	3003 (Fig 7)	97	IN	5.0 V	2.4 V									OUT		2.4 V	Clock 1 to Q1		30	
66	u	(1.9./	98	IN	5.0 V	2.4 V								"		OUT	2.4 V	Clock 1			- 44
																		to Q 1			
66	"		99					IN	5.0 V	2.4 V		OUT	2.4 V					Clock 2	66		
44			100					IN	5.0 V	2.4 V	OUT		2.4 V	"				to Q2 Clock 2	66		
			100					liv.	3.0 V	2.4 V	001		2.4 V					to Q 2			
84	t _{PHL2}		101	IN	5.0 V	2.4 V								**	OUT		2.4 V	Clock 1	66	40	
	*PFIL2																	to Q1			
*	"		102	IN	5.0 V	2.4 V										OUT	2.4 V	Clock 1	**		"
																		to Q 1			
			103					IN	5.0 V	2.4 V		OUT	2.4 V					Clock 2 to Q2			
66		**	104					IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2	66		66
																		to Q 2			
10	F _{MAX} 6/	(Fig 7)	105	IN		2.4 V	"							"	OUT		2.4 V	Q1	10		MHz
T _C = 125°C	"		106	IN		2.4 V								44		OUT	2.4 V	Q 1	66		"
44		**	107				"	IN		2.4 V		OUT	2.4 V	44				Q2	66		66
44	"	"	108				"	IN		2.4 V	OUT		2.4 V	"				Q 2	66		66
66	t _{PLH1}	3003	109	IN	IN	GND	"							"		OUT	2.4 V	Clear 1	5	39	ns
		(Fig 6)																to Q 1			
44	t _{PLH1}		110					IN	IN	2.4 V	OUT		GND	"				Clear 2	66	39	44
																		to Q 2			
*	t _{PHL1}		111	IN	IN	GND									OUT		2.4 V	Clear 1 to Q1	**	50	"
	t _{PHL1}		112					IN	IN	2.4 V		OUT	GND	"				Clear 2	66	50	66
		2000		181	5.01/	0.41/									OUT		0.41/	to Q2	64		L .
_	t _{PLH2}	3003 (Fig 7)	113	IN	5.0 V	2.4 V									OUT		2.4 V	Clock 1 to Q1	-	39	_
66	и	` " ′	114	IN	5.0 V	2.4 V								"		OUT	2.4 V	Clock 1	44	"	66
																		to Q 1			
64	"		115					IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2	66	"	66
66	u	44	116					IN	5.0 V	2.4 V	OUT		2.4 V					to Q2 Clock 2	66		66
									0.0 .		00.							to Q 2			
			l					1		1	l	1						2	1		

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL- STD-883	Case A, B, D Case C	1	2	3	4	5	6	7	8	9	10 10	11	12 12	13 13	14 14	Meas.		Test limit	3
		method	Test No.	Clock 1	Clear 1	K1	V _{cc}	Clock 2	Clear 2	J2	Q ₂	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	Unit
10 T _C = 125°C	t _{PHL2}	3003	117	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	Clock 1 to Q1	5	50	ns
66	"	"	118	IN	5.0 V	2.4 V	"							44		OUT	2.4 V	Clock 1 to Q 1	44	44	66
66	"	44	119				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	44	"	64
66	и	"	120				"	IN	5.0 V	2.4 V	OUT		2.4 V	44				Clock 2 to Q 2	66	"	
11	Same test	s. terminal cor	nditions and limits	as for subg	roup 10, exc	cept T _C = -55	°C.														

- NOTES:
 A = Normal clock pulse,
 B = Momentary GND, then 4.5 V.
 C = This note has been deleted.
 D = Momentary 4.5 V, then GND.
 E = Momentary 4.5 V, then GND.
 F = Momentary ground, then 5.5 V.
 J = This note has been deleted.
- * After clock pulse apply –12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15). ** Test time limit \leq 100 ms.

- 1/ Terminal conditions (pins not designated may be H \ge 2.0 V, or L \le 0.8 V, or open.) 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum. 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H \ge 1.5 V and L < 1.5 V when using a high speed checker single comparator. 4/ Tests shall be performed in sequence. 5/ Input shall be one normal clock pulse, then 4.5 V 6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall ge one-half of the input frequency. 7/ For CKT A, I_{RS} limits are 0 to 120 μ A.

TABLE III. Group A inspection for device type 03. 1/

Subgroup	Symbol	MIL-	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	
- 1	-	STD-883 method	Test No.	J1	Q ₁	Q1	K1	Q2	Q ₂	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{CC}	Meas. terminal	Min	Max	Un
1	V _{OH}	3006	1	2.0 V		4 mA	0.8 V			GND					Α		4.5 V	Q1	2.4		V
$T_C = 25^{\circ}C$	ű	44	2	0.8 V	4 mA		2.0 V			"					Α		a	Q 1			
66	и	44	3		4 mA					"						0.8 V	66	Q 1	"		٠.
er .		44	4					4 mA		"	2.0 V	Α		0.8 V				Q2	"		
66	u u	"	5						4 mA		0.8 V	A		2.0 V			66	Q 2	"		1
es .	u		6						4 mA				0.8 V					Q 2			

66	V _{OL}	3007	7	0.8 V		16 mA	2.0 V			"					Α		44	Q1		0.4	
66	"		8	2.0 V	16 mA		0.8 V			"					Α			Q 1			
66	и	"	9			16 mA				"						0.8 V	66	Q1		"	
66		"	10					16 mA		a	0.8 V	Α		2.0 V				Q2		44	
66		"	11						16 mA		2.0 V	Α		0.8 V			66	Q 2		"	
66			12					16 mA		44			0.8 V					Q2		44	+
66	V _{IC}		13	-12 mA						u							4	J1		-1.5	1
44	ii ii		14				-12 mA			"								K1		"	
44	ш		15								-12 mA						44	J2		"	
66	a a		16							*				-12 mA				K2		"	
44	ii ii		17													-12 mA	44	Clear 1		44	
66			18												-12 mA			Clock 1		"	
66			18 CKT B	4.5 V			0.8 V			"					A*	4.5 V	44	Clock 1		-0.5	
			19							"			-12 mA					Clear 2		-1.5	
			20									-12 mA		0.01/				Clock 2		-1.5	₩
			20 CKT B	0.417							4.5 V	A*	4.5 V	0.8 V		4 = 14		Clock 2		-0.5	+
-	I _{IL1}	3009	21 22	0.4 V			0.4 V								<u>5</u> /	4.5 V 4.5 V	5.5 V	J1 K1	-0.7	-1.6	n
66			23				0.4 V			"	0.4 V	5/	4.5 V		<u>5</u> /	4.5 V		J2	"	"	+
			24							u	0.4 V	5/	4.5 V	0.4 V			4	K2	u	44	+
66	I _{IL2}		25	4.5 V			4.5 V			"		3/	4.5 ¥	0.4 ¥	0.4 V	В	66	Clock 1	-1.25	-3.2	+-
44	I _{IL2}	44	26	7.5 V			4.5 V			"	4.5 V	0.4 V	В	4.5 V	0.4 V		44	Clock 2	-1.25	-3.2	
	I _{IL3}		27 CKT A, C	4.5 V						u	1.0 1	0.1 0		1.0 1	4.5 V	0.4 V	4	Clear 1	-0.7	-1.6	+
44	u u		27 CKT B	4.5 V						"					4.5 V	0.4 V	44	Clear 1	-1.4	-3.2	†
66		44	28 CKT A, C								4.5 V	4.5 V	0.4 V				44	Clear 2	-0.7	-1.6	
			28 CKT B							"	4.5 V	4.5 V	0.4 V				44	Clear 2	-1.4	-3.2	
a	l _{IH1}	3010	29	2.4 V						44					GND	GND		J1		40	ļ
44			30				2.4 V			*					GND	В	4	K1		"	
66		44	31							4	2.4 V	GND	GND				66	J2		"	
		"	32							"		GND	В	2.4 V			"	K2		"	
-	I _{IH2}		33	5.5 V						"					GND	GND	4	J1		100	
			34				5.5 V								GND	В	4	K1			
-			35								5.5 V	GND	GND	E E \/			-	J2 K2			-
66			36 37	GND								GND	В	5.5 V	GND	-	66	Clear 1			-
66	I _{IH3} <u>7/</u> I _{IH3} 7/		38	GND						"	GND	GND	Е		GND	Е		Clear 1		80 80	+-
4	I _{IH3} I/	**	39	GND			GND				GIND	GIND			5.5 V	GND	44	Clock 1	 	200	
66	I _{IH4}		40	GND			GIND								GND	F		Clear 1	 	200	
4			41	GIND						"	GND	5.5 V	GND	GND	CIND	-	44	Clock 2	 	44	
66		44	42							"	GND	GND	F	OILD			44	Clear 2			t-
66	I _{IH5}	44	43 CKT A. C	GND			GND				0.15	0.10			2.4 V	GND	44	Clock 1	-50	-700	
66	"IHS		43 CKT B	GND			GND			"					2.4 V	GND	66	Clock 1	-200	-850	1
			44 CKT A, C							"	GND	2.4 V	GND	GND			66	Clock 2	-50	-700	1
44			44 CKT B	1					1	"	GND	2.4 V	GND	GND	l	l	44	Clock 2	-80	-850	

Subgroup	Symbol	MIL-	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	is
9	,	STD-883 method	Test No.	J1	Q ₁	Q1	K1	Q2	Q ₂	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{CC}	Meas. terminal	Min	Max	Un
1	Ios	3011	45	2.4 V	GND		2.4 V			"					2.4 V	GND	5.5 V	Q 1	-20	-57	m
$T_C = 25^{\circ}C$	ш	3011 *	46	4.5 V	GND	GND	0 V			"					Α	4.5 V	66	Q1	"		
66	"	3011 *	47					GND	GND	"	4.5 V	Α	4.5 V	2.4 V			"	Q2	"		
		3011	48						GND		2.4 V	2.4 V	GND	0 V				Q 2			
ec .	Icc	3005	49	4.5 V			GND			"	4.5 V	D	4.5 V	GND	D	4.5 V	66	V _{CC}		40	
2	Same tests	s, terminal con	ditions and limits	as for subgi	roup 1, exce	ept T _C = 125	C and V _{IC} to	ests are om	itted.												
3	Same tests	s, terminal con	ditions and limits																		
7 <u>2</u> / <u>4</u>			50	A	H <u>3</u> /	L <u>3</u> /	В	L <u>3</u> /	H <u>3</u> /	GND	A	В	В	В	В	В	4.5 V	All		H or L	
T _C = 25°C			51	A	Н	L	В	L	Н	"	A	A	В	В	A	В	"	output "	а	s shown	<u>3</u> /
4			52	A	H	L_	В	L	H	"	A	В	В	В	В	В		4			
			53 54	A A	H H	L L	A A	L	H		A	B A	B B	A A	B A	B B			-		
a a			55	A	Н	L	A	L	Н		A	В	В	A	В	В	4				
66			56	A	H	È	A	ì	H		A	В	A	A	В	A		44			_
44			57	A	H	ī	A	Ĺ	H		A	Ā	A	A	Ā	A		"			_
44			58	A	L	Н	Α	Н	L		Α	В	Α	A	В	Α	44			44	_
66			59	Α	L	Η	Α	Н	L		Α	Α	Α	Α	Α	Α	66	44		a	
4			60	A	Н	L	A	L	Н	"	Α	В	A	A	В	A	u	"		"	
66			61	A	Н	L	A	L	Н	"	Α	A	A	A	A	Α	44	"		"	
4			62	Α	L	Н	A	Н	L	"	Α	В	A	A	В	Α	66	"		"	
			63	В	L	Н	В	Н	L	"	В	В	A	В	В	Α					
			64 65	B B	L L	H	B B	H	L		B B	A B	A A	B B	A B	A A					
			66	В	Н	L	В	L	H		В	В	В	В	В	В	4			"	
66			67	В	H	È	В	Ĺ	H	44	В	В	A	В	В	A	4	44		"	_
44			68	В	Н	ī	В	ī	H	"	В	A	A	В	A	A					
44			69	В	H	Ĺ	В	Ĺ	H	"	В	В	A	В	В	A	4	44			_
			70	A	Н	L	В	L	Н		Α	В	A	В	В	A				"	
4			71	Α	Н	L	В	L	Н		Α	Α	Α	В	Α	Α	66	44		a	
66			72	A	L	Н	В	Н	L	"	Α	В	Α	В	В	Α	e e	"		44	
66			73	В	L	Н	Α	Н	L	"	В	В	A	A	В	Α	4	"		"	
			74 75	В	L	Η.	A	Н.	L	"	В	A	A	A	A	A	4			- :-	
			76	B A	H	L L	A A	L	H H		B A	B A	A B	A A	B A	A B	66			"	
44	-		77	A	H	Ĺ	A	Ĺ	H	"	A	A	A	A	A	A	4				
44			78	В	H	È	A	ì	H	"	В	A	Ä	A	A	A	u				
44			79	В	H	Ē	В	Ĺ	H	"	В	A	A	В	A	A	ш	"			_
44			80	В	L	Н	В	Н	L	"	В	В	Α	В	В	Α	4	44			_
44			81	Α	L	Ι	Α	Н	L	"	Α	Α	Α	Α	Α	Α	u	"		"	
66			82	A	L	Н	В	Н	L	"	Α	A	Α	В	Α	A	es .	44		a	
			83	В	L	Н	В	Н	L	"	В	Α	A	В	Α	Α	e e	"			
4	1		84	В	Н	L	В	L	Н	"	В	В	A	В	В	A		"		"	
	1		85	A	Н	L	В	L	Н	"	A	A	A	В	A	A	**	"			
			86 87	A	L	Н	В	Н	L		A	В	A	В	В	A				- :-	
	1		88	A A	L H	Н	B B	Н	L H		A	A A	A B	B B	A	A B					

Subgroup	Symbol	MIL-	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	
		STD-883 method	Test No.	J1	Q ₁	Q1	K1	Q2	Q ₂	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{CC}	Meas. terminal	Min	Max	Ur
9	F _{MAX}	(Fig. 7) 6/	89	2.4 V		OUT	2.4 V			GND					IN	5.0 V	5.0 V	Q1	10		M
$T_C = 25^{\circ}C$			90	2.4 V	OUT		2.4 V			44					IN	5.0 V	"	Q ₁	4		64
66	и	66	91					OUT		44	2.4 V	IN	5.0 V	2.4 V				Q2	66		66
a	a.	er .	92						OUT	66	2.4 V	IN	5.0 V	2.4 V			ii ii	Q ₂	66		66
a	t _{PLH}	3003 (Fig. 6)	93	2.4 V	OUT		GND			44					Α	IN	ш	Cir 1 to Q 1	5	25	ns
44	t _{PLH}	"	94						OUT		2.4 V	Α	IN	GND			"	Clr 2 to Q 2	44	25	66
	t _{PHL}	ш	95	2.4 V		OUT	GND			4					Α	IN		Clr 1 to Q1	66	40	
44	t _{PHL}	66	96					OUT		ш	2.4 V	Α	IN	GND			u	Clr 2 to Q2	66	40	66
66	t _{PLH}	3003	97	2.4 V		OUT	2.4 V			44					IN	5.0 V	ű	Clk 1 to Q1	5	30	ns
44	"	(Fig. 7)	98	2.4 V	OUT		2.4 V			44					IN	5.0 V	"	Clk 1 to Q 1	66	-	44
	"		99					OUT		44	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2		44	66
66	"	66	100						OUT	66	2.4 V	IN	5.0 V	2.4 V			**	Clk 2 to Q 2	**	**	66
66	t _{PHL}	66	101	2.4 V		OUT	2.4 V			66					IN	5.0 V	"	Clk 1 to Q1		40	66
44	"	66	102	2.4 V	OUT		2.4 V			66					IN	5.0 V	"	Clk 1 to Q 1	66	66	**
44	"		103					OUT		66	2.4 V	IN	5.0 V	2.4 V			u u	Clk 2 to Q2		*	66
66	"	66	104						OUT	66	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q 2	66	66	66
10	F _{MAX}	(Fig. 7) 6/	105	2.4 V		OUT	2.4 V			66					IN	5.0 V	u u	Q1	10		MH
$T_C = 125^{\circ}C$	"	66	106	2.4 V	OUT		2.4 V			66					IN	5.0 V	"	Q ₁	66		66
66	"	66	107					OUT		66	2.4 V	IN	5.0 V	2.4 V			"	Q2			66
66		es	108						OUT	44	2.4 V	IN	5.0 V	2.4 V			"	Q ₂	44		66
66	t _{PLH}	3003 (Fig 6)	109	2.4 V	OUT		GND			44					Α	IN	u	Clr 1 to Q 1	5	39	ns
a	t _{PLH}	(1.90)	110						OUT	44	2.4 V	A	IN	GND				Clr 2 to Q 2	ш	39	66
44	t _{PHL}	44	111	2.4 V		OUT	GND								Α	IN		Clr 1 to Q1		50	66
	t _{PHL}	66	112	2			0.10	OUT			2.4 V	A	IN	GND			и	Clr 2 to Q2		50	
44	tpLH	3003	113	2.4 V		OUT	2.4 V			66					IN	5.0 V	u	Clk 1 to Q1	5	39	ns
a	u	(Fig 7)	114	2.4 V	OUT		2.4 V			44					IN	5.0 V	и	Clk 1 to Q 1	66	66	66
44	ш	ш	115					OUT		4	2.4 V	IN	5.0 V	2.4 V				Clk 2 to Q2	66	66	
66	"	es	116						OUT	44	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q 2	"	66	**
a	t _{PHL}	ш	117	2.4 V		OUT	2.4 V			4					IN	5.0 V		Clk 1 to Q1	66	50	66
er .	"		118	2.4 V	OUT		2.4 V								IN	5.0 V	"	Clk 1 to Q 1	66	66	66
66	и	66	119					OUT		66	2.4 V	IN	5.0 V	2.4 V			и	Clk 2 to Q2	ш	ш	66
44			120						OUT	66	2.4 V	IN	5.0 V	2.4 V				Clk 2 to Q 2	86	66	66

```
NOTES:
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- A = Normal clock pulse.
 B = Momentary GND, then 4.5 V.
 C = This note has been deleted.
 D = Momentary 4.5 V, then GND.
 E = Momentary ground, then 2.4 V.
 F = Momentary ground, then 5.5 V.
- * After clock pulse apply –12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15).
- ** Test time limit ≤100 ms.

- 1/ Terminal conditions (pins not designated may be $H \ge 2.0 \text{ V}$, or $L \le 0.8 \text{ V}$, or open).
 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) $H \ge 1.5 \text{ V}$ and L < 1.5 V when using a high speed checker single comparator.
 4/ Tests shall be performed in sequence of the sequence of the sequence of the sequence of the input frequency of the input pulse. The output frequency shall be one-half of the input frequency.
 7/ For CKT A, I_{BG} limits are 0 to 120 μ A.

TABLE III. Group A inspection for device type 04. 1/

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Г Т	est limits	
oubgroup	Cymbo.	STD-883	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{CC}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas.	Min	Max	Unit
1	V _{OH}	method 3006	1	A			2.0 V	4.5 V					~ -			GND	<u> </u>	4 mA	0.8 V	terminal Q1	2.4		V
T _C = 25°C	"	"	2	A			0.8 V	"								"	4 mA		2.0 V	Q 1			"
	"	ш	3		2.0 V	0.8 V		"									4 mA			Q 1			
			4		0.8 V	2.0 V												4 mA		Q1			
"	"	4	5		0.0 V	2.0 V			Α			2.0 V		4 mA	0.8 V			4 IIIA		Q2			"
	"	66	6					**	Α			0.8 V	4 mA		2.0 V					Q 2			"
	"	66	7					"		2.0 V	0.8 V		4 mA			66				Q 2			
u		46	8					"		0.8 V	2.0 V			4 mA		44				Q2			
**	V _{OL}	3007	9	Α			0.8 V	44								"		16 mA	2.0 V	Q1		0.4	
"	"	66	10	Α			2.0 V	"									16 mA		0.8 V	Q 1			
	"	66	11		0.8 V	2.0 V		**								и	16 mA			Q 1		44	"
		66	12		2.0 V	0.8 V												16 mA		Q1		66	
	"	66	13					"	Α			0.8 V		16 mA	2.0 V	и				Q2		66	и
	"	4	14						Α			2.0 V	16 mA		0.8 V	и				Q 2			"
	"	66	15					**		0.8 V	2.0 V		16 mA			и				Q 2		66	"
	"	66	16					"		2.0 V	0.8 V			16 mA						Q2		66	
	V _{IC}		17				-12 mA	"												J1		-1.5	"
	"		18													"			-12 mA	K1			"
			19 20									-12 mA			-12 mA					J2 K2			
			21	-12 mA											-12 IIIA					Clock 1		44	
4	44		22	-12 1104	-12 mA			"								"				Preset 1			"
	"		23			-12 mA		"								"				Clear 1		66	"
	44		24					"	-12 mA											Clock 2			"
			25					"		-12 mA										Preset 2			
44	"		26					44			-12 mA									Clear 2		-	
	I _{IL1}	3009	27	4.5 V		В	0.4 V	5.5 V								"				J1	-0.7	-1.6	mA
	"	4	28	4.5 V	В	4.5 V		"								"			0.4 V	K1		4	"
			29						4.5 V		В	0.4 V			0.414					J2			
			30 31	0.4 V	В		4.5 V		4.5 V	В	4.5 V				0.4 V				4.5 V	K2 Clock 1			
	I _{IL2}	66	32	0.4 V	В	В	4.5 V												4.5 V	Clock 1	-1.25	-3.2	"
	"	и	33	0.4 V		ь	4.5 V		0.4 V	В		4.5 V			4.5 V	44			4.5 V	Clock 2	и	- 44	ш
"			34						0.4 V		В	4.5 V			4.5 V	66				Clock 2		44	
44	I _{IL3}	66	35 A, C	4.5 V		0.4 V	4.5 V	"								ш			4.5 V	Clear 1	-0.7	-1.6	"
	"	es .	35 B	4.5 V		0.4 V	4.5 V	"								"			4.5 V	Clear 1	-1.4	-3.2	ш
	"	4	36 A, C	4.5 V	0.4 V		4.5 V	"								ш			4.5 V	Preset 1	-0.7	-1.6	
	"	44	36 B	4.5 V	0.4 V		4.5 V									"			4.5 V	Preset 1	-1.4	-3.2	"
	"	ш	37 A, C					"	4.5 V		0.4 V	4.5 V			4.5 V					Clear 2	-0.7	-1.6	и
4	"	"	37 B					"	4.5 V		0.4 V	4.5 V			4.5 V	"				Clear 2	-1.4	-3.2	
-			38 A, C						4.5 V	0.4 V		4.5 V			4.5 V					Preset 2	-0.7	-1.6	
	I _{IH1}	3010	38 B 39	GND		GND	2.4 V		4.5 V	0.4 V		4.5 V			4.5 V					Preset 2 J1	-1.4	-3.2 40	
44	IH1 "	3010	40	GND	GND	GIND	2.4 V												2.4 V	K1		40	μA "
			40	GIND	GIND				GND	 	GND	2.4 V		 	-		l		2.4 V	J2	-		
	"	и	42		-	-		"	GND	GND	GIND	2.4 V			2.4 V					K2			"
	I _{IH2}		43	GND		GND	5.5 V		0.10	0.10					2	и				J1		100	
"	"	66	44	GND	GND			"								"			5.5 V	K1		44	"
"	"	66	45						GND		GND	5.5 V				"				J2		**	"
	"		46					"	GND	GND					5.5 V		1			K2		-	

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		1	est limits	
,	-	STD-883 method	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{cc}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas. terminal	Min	Max	Unit
1	I _{IH3}	3010	47	GND		E	GND	5.5 V								GND			4.5 V	Clear 1		160	μА
$T_C = 25^{\circ}C$	"	44	48	GND	E		4.5 V	"								"			GND	Preset 1		"	66
	"	44	49					"	GND		E	GND			4.5 V	"				Clear 2		"	66
	"	66	50					"	GND	E		4.5 V			GND					Preset 2			
"	I _{IH4}	66	51	GND		F	GND	"											4.5 V	Clear 1		200	66
	"	66	52	GND	F		4.5 V	"								"			GND	Preset 1			"
**	"	**	53					"	GND		F	GND			4.5 V	"				Clear 2		"	66
"	"	44	54					44	GND	F		4.5 V			GND	"				Preset 2			
44	"	66	55	5.5 V		GND	GND	"								"			GND	Clock 1		u	
**	"	66	56					"	5.5 V		GND	GND			GND					Clock 2		"	66
4	I _{IH5}	66	57 CKT A, C	2.4 V		GND	GND	"											GND	Clock 1	-50	-700	44
		66	57 CKT B	2.4 V		GND	GND	"								"			GND	Clock 1	-200	-850	- "
			58 CKT A, C						2.4 V		GND	GND			GND					Clock 2	-50	-700	
			58 CKT B	0.417	ONE	4 = 17	0.417		2.4 V		GND	GND			GND			ONE	0.414	Clock 2	-200	-850	
"	I _{OS}	3011	59 ** 60	2.4 V 2.4 V	GND 4.5 V	4.5 V GND	2.4 V 2.4 V	"								и	GND	GND	2.4 V 2.4 V	Q1 Q 1	-20	-57	mA "
			61**					"	2.4 V	GND	4.5 V	2.4 V		GND	2.4 V	44				Q2	"	и	**
4	"	66	62					"	2.4 V	4.5 V	GND	2.4 V	GND	OND	2.4 V	66				Q 2	и	u	
44	Icc	3005	63	GND	4.5 V	GND	GND	"	GND	4.5 V	GND	GND			GND	"			GND	V _{CC}		40	66
	Icc	3005	64	GND	GND	4.5 V	GND	"	GND	GND	4.5 V	GND			GND	"			GND	V _{CC}		40	44
3	Same tests	s, terminal cor	nditions and lin													OUD	11.07						
7 2/ 4/			65	В	A	В	A	4.5 V	В	A	В	A	H <u>3</u> /	L 3/	В	GND "	H 3/	L <u>3</u> /	В	All		H or L	,
T _C = 25°C			66	A	A	В	A		A	A	В	A	Н	L	В	"	Н	L	В	output	as	shown 3	
-			67 68	B B	A	B B	A		B B	A	B B	A	H	L	В	"	H	L	В			-	
			69	A	A	В	A		A	A A	В	A A	H	L	A A		H	L	A				
			70	В	A	В	A		В	A	В	A	H	L	A		Н	-	A				
			71	В	В	A	A		В	В	A	A	-	H	A		-	Н	A			и	
			72	A	В	Ä	Ä	"	A	В	Ä	A	ì	H	A	"	ì	H	A			и	
			73	В	В	A	A	4	В	В	A	A	ī	H	A	ш	ī	H	A			ш	
"			74	В	В	Α	В	"	В	В	Α	В	Ē	Н	A	"	ī	Н	A			"	
			75	A	В	A	В	"	A	В	A	В	Ē	Н	A	"	Ē	Н	A			и	
			76	В	В	Α	В	"	В	В	Α	В	L	Н	Α	"	L	Н	A			и	
"			77	В	Α	Α	В	"	В	Α	Α	В	L	Н	В		L	Н	В				
			78	Α	Α	Α	В	"	Α	Α	Α	В	L	Н	В	"	L	Н	В			u	
			79	В	Α	Α	В	"	В	Α	Α	В	L	Н	В		L	Н	В				
			80	В	Α	В	В	"	В	Α	В	В	Н	L	В	"	Н	L	В				
			81	В	Α	Α	В	"	В	Α	Α	В	Н	L	В		Н	L	В			ii .	
"			82	A	A	A	В	"	Α	A	A	В	Н	L	В	"	Н	L	В	:			
			83	В	A	A	В	"	В	A	A	В	Н	L	В		Н	L	В	- :			
-			84 85	B A	A A	A	A		B A	A A	A	A A	H	L	B B		H	L	B B	- :	ļ	-	
	\vdash		86	B	A	A			B	A	A	A	П	H	В	"	п	H	В				
			90	В	A	A	Α		В	A	A	A	L	П	В		L	п	В				

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16			Test limit	
		STD-883 method	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{CC}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas. terminal	Min	Max	Unit
7 <u>2</u> / <u>4</u> /			87	В	A	A	В	4.5 V	В	Α	A	В	L <u>3</u> /	H <u>3</u> /	A	GND	L <u>3</u> /	H <u>3</u> /	A	All		H or L	
$\Gamma_{\rm C} = 25^{\circ}{\rm C}$			88	Α	A	Α	В	"	Α	A	Α	В	L	Н	Α	66	L	Н	A	Output		as shown	3/
66			89	В	A	Α	В	и	В	A	Α	В	Н	L	A	66	Н	L	A			ii ii	
44			90	В	A	Α	A	"	В	A	Α	A	Н	L	Α	66	Н	L	A	"		ii ii	
44			91	Α	A	Α	A	"	Α	A	Α	A	Н	L	Α	66	Н	L	A	"		и	
44			92	В	A	Α	A	и	В	A	Α	A	L	Н	Α	66	L	Н	A	"		и	
44			93	Α	A	Α	A	"	Α	A	Α	A	L	Н	Α	66	L	Н	A	"		ii ii	
u			94	В	A	Α	A	и	В	A	Α	A	Н	L	Α	66	Н	L	A	"		ii ii	
66			95	A	В	В	В	"	A	В	В	В	Н	H	В	**	Н	Н	В	"		и	
44			96	Α	В	Α	Α	"	Α	В	Α	Α	L	Н	Α	**	L	Н	Α	"			
u			97	Α	A	Α	A	и	Α	A	Α	A	L	Н	Α	66	L	Н	A	"		ii ii	
66			98	Α	Α	Α	Α	"	Α	Α	Α	Α	L	Н	В	66	L	Н	В	"			
66			99	Α	Α	Α	В	"	Α	Α	Α	В	L	Н	В	66	L	Н	В	"		"	
66			100	В	Α	Α	В	"	В	Α	Α	В	Н	L	В	**	Н	L	В	"			
66			101	Α	Α	Α	Α		Α	Α	Α	Α	Η	L	Α	66	Н	L	Α	"			
44			102	Α	A	Α	В	и	Α	Α	Α	В	Н	L	Α	66	Н	L	A	"		ii ii	
66			103	A	A	A	В	"	Α	A	Α	В	Н	L	В	66	Н	L	В	"		"	
u			104	В	Α	Α	В	"	В	Α	Α	В	L	Н	В	66	L	Н	В	"		ii ii	
8 <u>2</u> / <u>4</u> /	Same test	s, terminal co	nditions and li	mits as for	subgroup 7	7, except T	_C = 125°C	and -55°	C.														
9	F _{MAX}	(Fig. 9)	105	IN	5.0 V		2.4 V	5.0 V								GND		OUT	2.4 V	Q1	10		M
Γ _C = 25°C	ii ii	5/	106	IN	5.0 V		2.4 V	"								es .	OUT		2.4 V	Q 1			1
66	и	"	107					"	IN	5.0 V		2.4 V		OUT	2.4 V					Q2	**		
		"	108						IN	5.0 V		2.4 V	OUT		2.4 V	66				Q 2			╆ .
66	t _{PLH1}	3003 (Fig 8)	109	2.4 V	5.0 V	IN	2.4 V	и								66	OUT		2.4 V	Clear 1	5	25	n
66	и	(1.ig 0)	110	2.4 V	IN	5.0 V	2.4 V	и										OUT	2.4 V	to Q 1		66	
			-	2.4 V	IIN	5.0 V	2.4 V											001	2.4 V	to Q1			
			111						2.4 V	5.0 V	IN	2.4 V	OUT		2.4 V					Clear 2	-		
																				to Q 2			
		"	112					"	2.4 V	IN	5.0 V	2.4 V		OUT	2.4 V	-				Preset 2 to Q2	"	"	
66	t _{PHL1}	"	113	2.4 V	5.0 V	IN	2.4 V	"								4		OUT	2.4 V	Clear 1 to Q1	44	40	
	"	"	114	2.4 V	IN	5.0 V	2.4 V									- 44	OUT		2.4 V	Preset 1		- 64	†
																				to Q 1			
66	и	"	115					"	2.4 V	5.0 V	IN	2.4 V		OUT	2.4 V	66				Clear 2 to Q2	4	44	
44	u	4	116	 				и	2.4 V	IN	5.0 V	2.4 V	OUT		2.4 V	66				Preset 2	66		
																				to Q 2			
	t _{PLH2}	3003 (Fig 9)	117	IN	5.0 V	5.0 V	2.4 V	"								**		OUT	2.4 V	Clock 1 to Q1	5	30	r
66			118	IN	5.0 V	5.0 V	2.4 V	"								es	OUT		2.4 V	Clock 1		66	
			110						INI	E 0 \'	E 0 \'	2.4.1/		OUT	2.41/	4				to Q 1	a	4	
			119						IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	_				Clock 2 to Q2	_		
66	"		120						IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	66				Clock 2 to Q 2	66		
	t _{PHL2}		121	IN	5.0 V	5.0 V	2.4 V	"								66		OUT	2.4 V	to Q 2 Clock 1		40	+-
	-PHL2	1						1	1	1	1			1	1	1	1			40.01		1 .0	1

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16			Test limits	
	,	STD-883 method	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{cc}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas. terminal	Min	Max	Unit
9 T _C = 25°C	t _{PHL2}	3003 (Fig 8)	122	IN	5.0 V		2.4 V	5.0 V								GND	OUT	OUT	2.4 V	Clock 1 to Q 1	5	40	ns
	"		123					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2	4		"
44	44		124						IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	и				to Q2 Clock 2	66		и
										0.0 1	0.0 1		00.		2					to Q 2			
10	F _{MAX} <u>5</u> /	(Fig 9)	125	IN	5.0 V		2.4 V	"								"		OUT	2.4 V	Q1	10		MHz
T _C = 125°C	"		126	IN	5.0 V		2.4 V	"									OUT		2.4 V	Q 1	66		"
66	"	н	127					**	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Q2	66		
	"	"	128					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V					Q 2	66		"
es .	t _{PLH1}	3003 (Fig 8)	129	2.4 V	5.0 V	IN	2.4 V	"									OUT		2.4 V	Clear 1 to Q 1	5	39	ns
66	"		130	2.4 V	IN	5.0 V	2.4 V	"										OUT	2.4 V	Preset 1	44		"
44	"	и	131					"	2.4 V	5.0 V	IN	2.4 V	OUT		2.4 V	и				to Q1 Clear 2	66		
	4	и	132						2.4 V	IN	5.0 V	2.4 V		OUT	2.4 V					to Q 2 Preset 2	4		
		,,		0.414	E 0.1/			"	2.4 V	IIN	5.0 V	2.4 V		001	2.4 V			0.17	0.417	to Q2			
	t _{PHL1}		133	2.4 V	5.0 V	IN	2.4 V											OUT	2.4 V	Clear 1 to Q1		50	
	"		134	2.4 V	IN	5.0 V	2.4 V										OUT		2.4 V	Preset 1 to Q 1			
44	44	и	135					"	2.4 V	5.0 V	IN	2.4 V		OUT	2.4 V	и				Clear 2 to Q2	66	4	и
66	"	ш	136					"	2.4 V	IN	5.0 V	2.4 V	OUT		2.4 V	ш				Preset 2	66	"	"
44		3003	137	IN	5.0 V	5.0 V	2.4 V	44										OUT	2.4 V	to Q 2 Clock 1	5	39	ns
	t _{PLH2}	(Fig 9)															OUT	001		to Q1	5	39	IIS
			138	IN	5.0 V	5.0 V	2.4 V										OUT		2.4 V	Clock 1 to Q 1			
66	"	ш	139					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2			"
66	"	ш	140					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2			"
66	t _{PHL2}		141	IN	5.0 V	5.0 V	2.4 V											OUT	2.4 V	to Q 2 Clock 1		50	
	YPHL2																OUT			to Q1			"
			142	IN	5.0 V	5.0 V	2.4 V										OUT		2.4 V	Clock 1 to Q 1			
66	44	ш	143					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V					Clock 2 to Q2	44	"	"
44	44	и	144					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	и				Clock 2	66	4	"
	1															1				to Q 2		1	

```
NOTES:

A = Normal clock pulse.

B = Momentary GND, then 4.5 V.

C = This note has been deleted.

E = Momentary ground, then 5.5 V.

** = Test time limit ≤ 100 ms.

J = This note has been deleted.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open.)

2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.

3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b)

H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

4/ Tests shall be performed in sequence.

5 F<sub>MAX</sub>, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
```

TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1	T	est limits	
		883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
1	V _{OH}	3006	1	Α	2.0 V		4.5 V							GND		4 mA		Q1	2.4		V
T _C = 25°C	4	"	2	Α	0.8 V									"	4 mA			Q 1	"		
4	4	"	3	GND		0.8 V	44							"	4 mA		GND	Q 1			
66	4	"	4			GND	66							**		4 mA	0.8 V	Q1	"		**
er .		"	5				4		2.0 V	Α		4 mA						Q2			"
66	66	"	6				66		0.8 V	Α			4 mA	"				Q 2			
"	**	"	7				66	0.8 V		GND	GND		4 mA	44				Q 2			
66	44	"	8				44	GND			0.8 V	4 mA						Q2	"		"
"	V _{OL}	3007	9	Α	2.0 V		66							44	16 mA			Q 1		0.4	
66	66	"	10	Α	0.8 V		66									16 mA		Q1		66	"
	44	"	11			0.8 V	44									16 mA	2.0 V	Q1			и
		"	12			2.0 V	66							4	16 mA		0.8 V	Q 1			
66	44	"	13						2.0 V	Α			16 mA	"				Q 2			
44	44	"	14				66		0.8 V	Α		16 mA		"				Q2		66	**
66		"	15				4	0.8 V			2.0 V	16 mA						Q2		66	и
	**	"	16				66	2.0 V			0.8 V		16 mA	44				Q 2		66	"
66	V _{IC}		17		-12 mA		44											D1		-1.5	ш
66	66		18	-12 mA			66							**				Clock 1		66	"
es .	4		19			-12 mA	44							"				Clear 1		66	"
"	66		20														-12 mA	Preset 1		66	"
			21						-12 mA									D2			
			22					40 4		-12 mA								Clock 2			
			23 24					-12 mA			-12 mA							Clear 2 Preset 2			
	I _{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V				-12 IIIA						GND	D1	-0.7	-1.6	m/
4	'IL1	3003	26	4.5 V	0.4 V	4.5 V	3.3 V	4.5 V	0.4 V	4.5 V	GND						GIND	D2	-0.7	-1.6	1117
66	44		27	GND	GND	GND	44	1.0 1	0.11	1.0 1	0.10						0.4 V	Preset 1	-1.4	-3.2	"
44	**	"	28				66	GND	GND	GND	0.4 V							Preset 2	-1.4	-3.2	"
44	I _{IL2}	"	29	0.4 V	GND	4.5 V											GND	Clock 1	-1.4	-3.2	"
44	66	"	30 7/	4.5 V	4.5 V	0.4 V	44										GND	Clear 1	-2.1	-4.8	ш
44	44	"	31				66	4.5 V	GND	0.4 V	GND							Clock 2	-1.4	-3.2	"
66	66	"	32 <u>7</u> /				66	0.4 V	4.5 V	4.5 V	GND			"				Clear 2	-2.1	-4.8	ш
66	I _{IH1}	3010	33	4.5 V	2.4 V	GND	44							"			4.5 V	D1		40	μΔ
4	I _{IH1}	"	34	4.51		ONE	66	GND	2.4 V	4.5 V	4.5 V			"				D2		40	
-	I _{IH2}		35	4.5 V	5.5 V	GND		OND	E E V	4511	451						4.5 V	D1		100	
	I _{IH2}		36	2.41/	4.5 V	CNID		GND	5.5 V	4.5 V	4.5 V	ļ	 		-	-	4 E V	D2 Clock 1	-	100	
	I _{IH3}		37 38	2.4 V B	4.5 V 4.5 V	GND 4.5 V	-					-			-	-	4.5 V 2.4 V	Clock 1 Preset 1	-	80	
a a			38	Р	4.5 V	4.5 V	66	GND	4.5 V	2.4 V	4.5 V	-	1		-	-	2.4 V	Clock 2	-	-	
44		"	40	1			44	4.5 V	4.5 V	B B	2.4 V	l			l	1		Preset 2	1		ш
44	I _{IH4}	"	41	5.5 V	4.5 V	GND	66	7.5 V	7.5 V		2.7 V	l			l	1	4.5 V	Clock 1	1	200	ш
44	IIH4		42	B	4.5 V	4.5 V	44										5.5 V	Preset 1			
44	ш	"	43	T -				GND	4.5 V	5.5 V	4.5 V							Clock 2		44	ш
		"	44				**	4.5 V	4.5 V	В	5.5 V							Preset 2			"
ш	I _{IH5}	"	45	В	GND	2.4 V	66										4.5 V	Clear 1		120	"
66	I _{IH5}	"	46				**	2.4 V	GND	В	4.5 V							Clear 2		120	"
a a	I _{IH6}	"	47	В	GND	5.5 V	66										4.5 V	Clear 1		300	"
66	I _{IH6}		48				66	5.5 V	GND	В	4.5 V	1		44	1		1	Clear 2		300	"

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL-STD- 883	Case A, B D Case C	3	2	3	4 14	5 13	6 12	7	8 10	9	10 8	11 7	12 6	13 5	14	Meas.	1	Γest limit	S
		method	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock	Preset	Q2	Q 2	GND	Q 1	Q1	Preset	terminal	Min	Max	Un
1	Ios	3011	49				5.5 V				2			GND		GND	1 GND	Q1	-20	-57	m.
Γ _C = 25°C	"OS		50			GND	5.5 V							"	GND	OND	OND	Q 1	-20	-57	
	"		51				66				GND	GND						Q2	44	**	
			52					GND					GND					Q 2	l "	44	
66	Icc	3005	53	GND	GND		44		GND	GND	GND			"			GND	V _{CC}		30	+
44	Icc	3005	54	GND	GND	GND	66	GND	GND	GND								V _{CC}		30	
3			ditions and limits																		
7 <u>2</u> / <u>4</u> /		Ī	55	В	В	В	4.5 V	В	В	В	В	H 3/	H 3/	GND	H 3/	Н	В	All		H or L	
Γ _C = 25°C			56	В	В	В	7.5 7	В	В	В	A	L L	H	"	H	Ë	A	outputs	as	s shown	3/
23 0			57	В	В	A	44	A	В	В	A	Ē	H		H	È	A	"			
44			58	В	В	A	66	Α	В	В	В	H	Ĺ		L	Н	В			44	
44			59	Α	В	Α	66	Α	В	Α	В	Н	L		L	Н	В			66	
66			60	A	В	В		В	В	Α	В	H	Н		Н	Н	В	u		66	
66			61	Α	Α	В	44	В	Α	Α	В	Н	Н		Н	Н	В	u	L	66	
			62	A	A	В	66	В	Α	Α	Α	L	Н	ш	Н	L	A		Ь——	66	
			63	A	A	A		A	A	A	A	L	H		H	L	A		—		
			64 65	A A	A A	A A		A A	A A	A A	B A	H	L		L	H	B A		 		
4			66	В	A	A		A	A	В	A	H	L		L	Н	A		-	44	
66			67	В	В	A	66	A	В	В	A	H	Ĺ	ш	Ĺ	H	A	ш		66	_
44			68	A	В	A	66	A	В	A	A	Ë	H		H	L.	A				_
44			69	A	В	A	66	A	В	A	В	H	Ĺ		L	Н	В			44	_
66			70	Α	Α	В	66	В	Α	Α	В	Н	Н	"	Н	Н	В			66	
66			71	Α	В	В	66	В	В	Α	В	Η	Н		Н	Н	В	ш		66	
66			72	A	В	В	**	В	В	Α	A	L	Н		Н	L	A			66	
66			73	Α	В	Α		Α	В	Α	Α	L	Н		Н	L	Α	u	L	66	
4			74	В	A	A		A	A	В	A	L	Н		Н	L	A		 	66	
4			75	A	A	A		A	A	A	A	H	ļ.		Ŀ	Н	A		—		
			76 77	A A	A A	A A		A A	A A	A A	B A	H	L		L	H	B A		 		
44			78	A	A	В		В	A	A	A	L	H		Н	L	A		-	44	
66			79	A	A	A	66	A	A	A	A	- È	H	ш	Н.	È	A	ш		66	_
44			80	A	В	A	66	A	В	A	В	H	Ë		ï	H	В				_
es .			81	A	В	A	44	A	В	A	A	H	Ē	"	Ē	Н	A	u u		66	_
44			82	Α	В	В		В	В	Α	Α	L	Н		Н	L	Α			66	_
66			83	Α	В	Α	66	Α	В	Α	Α	L	Н		Н	L	Α	ш		66	
66			84	Α	Α	Α	**	Α	Α	Α	Α	L	Н		Н	L	Α			66	
8 <u>2</u> / <u>4</u> /		s, terminal con-	ditions and limits	as for sub		except T _C =		nd -55°C.													
9	F _{MAX} <u>6</u> /	(Fig. 11)	85	IN	E		5.0 V							GND		OUT	5.0 V	Q1	10		N
_C = 25°C	"		86	IN	E		-								OUT		5.0 V	Q 1			1
44	и	и	87				44		Е	IN	5.0 V	OUT						Q2	44	1	T
			88						Е	IN	5.0 V		OUT					0.2			

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL- STD-883	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	ŝ
		method	Case C Test No.	3 Clock 1	2 D1	1 Clear 1	14 V _{CC}	13 Clear 2	12 D2	11 Clock 2	10 Preset 2	9 Q2	8 0 2	7 GND	6 0 1	5 Q1	4 Preset 1	Meas. terminal	Min	Max	Unit
9 T _C = 25°C	t _{PLH1}	3003 (Fig 10)	89			IN	5.0 V							GND	OUT		J	Clear 1 to Q 1	5	25	ns
и		и	90			J										OUT	IN	Preset 1	"		и
и	44	и	91				66	IN			J		OUT	66				to Q1 Clear 2	и	66	"
	,,	,,										0117						to Q 2			
			92					J			IN	OUT				0.17		Preset 2 to Q2		40	
	t _{PHL1}		93			IN .								a	0117	OUT	J	Clear 1 to Q1			
	_	_	94			J	_							_	OUT		IN	Preset 1 to Q 1	_	_	
и	44	и	95					IN			J	OUT						Clear 2 to Q2	"		
ii ii		ű	96				44	J			IN		OUT	66				Preset 2 to Q 2	и	**	ű
u	t _{PLH2}	3003 <u>5</u> /	97	IN	IN (A)	В								66		OUT	5.0 V	Clock 1	5	30	ns
ш	44	(Fig 11) (Fig 12)	98	IN	IN (A)	5.0 V	66							66	OUT		В	to Q1 Clock 1	и	66	"
		(51- 44)	00						INI (A)	IN	501/	OUT						to Q 1			
		(Fig 11)	99					В	IN (A)		5.0 V	OUT		66				Clock 2 to Q2			
		(Fig 12)	100					5.0 V	IN (A)	IN	В		OUT					Clock 2 to Q 2			
ш	t _{PHL2}	(Fig 12)	101	IN	IN (B)	5.0 V	66							66		OUT	В	Clock 1 to Q1	"	40	"
и	"	(Fig 11)	102	IN	IN (B)	В	4								OUT		5.0 V	Clock 1	"		
и		(Fig 12)	103				44	5.0 V	IN (B)	IN	В	OUT		44				to Q 1			
и		(Fig 11)	104				66	В	IN (B)	IN	5.0 V		OUT	44				to Q2 Clock 2	"	44	
							66							66				to Q 2			
10 T _C = 125°C	F _{MAX} <u>6</u> /	(Fig 11)	105	IN	E											OUT	5.0 V	Q1	10		MH
			106	IN	E									4	OUT		5.0 V	Q 1		-	
		"	107 108				4		E E	IN IN	5.0 V 5.0 V	OUT	OUT					Q2 —			"
									_		0.0 1		00.	66	O			Q 2	-		
	t _{PLH1}	3003 (Fig 10)	109			IN	_							_	OUT		J	Clear 1 to Q 1	5	39	ns
и	44	a	110			J	66							66		OUT	IN	Preset 1 to Q1	"	66	
ш	44	ii ii	111					IN			J		OUT	4				Clear 2 to Q 2	"	4	
			112				4	J			IN	OUT						Preset 2	"		-
	t _{PHL1}		113			IN	44							66		OUT	J	to Q2 Clear 1	и	50	
ш	u	и	114			J	44							66	OUT		IN	to Q1 Preset 1	и	66	
и			115					IN			J	OUT						to Q 1			
и	и	"	116				66	J			IN		OUT	66				to Q2 Preset 2	и	66	
								Ĭ										to Q 2			

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	3
		STD-883 method	Case C															Meas. terminal			
		memou	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminai	Min	Max	Unit
10 T _C = 125°C	t _{PLH2}	3003 <u>5/</u> (Fig 11)	117	IN	IN (A)	В	и									OUT	5.0 V	Clock 1 to Q1	5	39	ns
	"	(Fig 12)	118	IN	IN (A)	5.0 V	66							66	OUT		В	Clock 1 to Q 1	и	66	и
"	"	(Fig 11)	119				66	В	IN (A)	IN	5.0 V	OUT		66				Clock 2 to Q2	и	66	
u	"	(Fig 12)	120					5.0 V	IN (A)	IN	В		OUT	66				Clock 2 to Q 2	a		"
"	t _{PHL2}	(Fig 12)	121	IN	IN (B)	5.0 V	66							es .		OUT	В	Clock 1 to Q1		40	"
и	"	(Fig 11)	122	IN	IN (B)	В	44							66	OUT		5.0 V	Clock 1 to Q 1		44	
"	"	(Fig 12)	123				66	5.0 V	IN (B)	IN	В	OUT		66				Clock 2 to Q2	и	66	
u	"	(Fig 11)	124				44	В	IN (B)	IN	5.0 V		OUT	66				Clock 2 to Q 2	a		"

- NOTES:
 A = Normal clock pulse.
 B = Momentary GND, then 4.5 V.
- $\mathsf{E} = \mathsf{Input}\,\mathsf{D}$ connected to $\ \overline{\mathsf{Q}}\ .$
- J = Input pulse, $t_p \ge 100$ ns, PRR = 1 MHz, $V_{OL} = 0$ V, $V_{OH} = 4.5$ V.
- 1/ Terminal conditions (pins not designated may be $H \ge 2.0 \text{ V}$, or $L \le 0.8 \text{ V}$, or open).

 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.

 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) $H \ge 1.5 \text{ V}$ and L < 1.5 V when using a high speed checker single comparator.

 4/ Tests shall be performed in sequence.

 5/ Tests shall be performed for both D input pulses (A and B).

 6/ FMAX, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

 7/ CKT C limits are -0.7 to -4.8 mA for these tests.

TABLE III. Group A inspection for device type 06. 1/

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	s
5		883	Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11	Meas.			
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J*	ā	GND	Q	K*	K2	terminal	Min	Max	Unit
1	V _{OH}	3006	1	0.8 V	Α		4.5 V			2.0 V	2.0 V	0.8 V		GND	4 mA	2.0 V	0.8 V	Q	2.4		V
T _C = 25°C	*OH	"	2	2.0 V	A		4.5 V			0.8 V	0.8 V	2.0 V	4 mA	"	4 1104	0.8 V	2.0 V	<u></u>	Z.T		
10 = 20 0			_	2.0 1	,,					0.0	0.0 •	2.0 .				0.0 •	2.0 .	Q			
ıı	"	"	3		GND	2.0 V	"	0.8 V				GND	4 mA	66		GND		ā	"		"
			4		GND	0.8 V		2.0 V				GND		66	4 mA	GND		Q			"
	V _{OL}	3007	5	2.0 V	Α					0.8 V	0.8 V	2.0 V		66	16 mA	0.8 V	2.0 V	Q		0.4	"
	" "	"	6	0.8 V	A					2.0 V	2.0 V	0.8 V	16 mA			2.0 V	0.8 V	ā		ш	"
"	"	"	7		GND	0.8 V	"	2.0 V				GND	16 mA					ā		**	"
			8		GND	2.0 V	"	0.8 V				GND			16 mA			Q		66	"
u	V _{IC}		9							-12 mA				66				J1		-1.5	"
u	"		10								-12 mA			66				J2		66	"
и	"		11									-12 mA		66				J*		66	
и	"		12	-12 mA		İ	"	İ										K1		66	
			13														-12 mA	K2		66	
и			14													-12 mA		K*		66	
ш			15		-12 mA		"							66				Clock		66	"
ш			16		121101	-12 mA	"							66				Preset		66	"
и			17					-12 mA										Clear		66	"
и	I _{IL1}	3009	18		GND		5.5 V	В		0.4 V	4.5 V	0.4 V						J1	-0.7	-1.6	mA
ш	""	"	19		GND		"	В		4.5 V	0.4 V	0.4 V		66				J2	"	ш	"
ш			20		0.10		"			1.0 1	0.11	0.4 V		66				J*	"	66	"
и	"	44	21	0.4 V	GND	В						0.11		66		0.4 V	4.5 V	K1		66	"
и	"	44	22	4.5 V	GND	В								66		0.4 V	0.4 V	K2		66	"
	"		23		0.10									66		0.4 V	0.11	K*	44	66	
ш			24		0.4 V		"							66		0.1 4		Clock	"	66	"
и	"	44	25	4.5 V	GND	0.4 V								66		0.4 V	4.5 V	Preset		66	"
	"	44	26		GND	0.1.0		0.4 V		4.5 V	4.5 V	0.4 V		66		0.1 *	1.0 1	Clear		66	"
	I _{IH1}	3010	27		0.10			GND		2.4 V	GND	4.5 V		66				J1		40	μА
	'IH1	"	28					GND		GND	2.4 V	4.5 V		- 44				J2		40	μ/\
	"		29					OND		OND	2.7 V	2.4 V						J*		44	"
	"		30	2.4 V		GND						2.7 V				4.5 V	GND	K1		44	"
и			31	GND		GND								- 44		4.5 V	2.4 V	K2		ш	"
и			32	GIND		GIND								- 44		2.4 V	2.4 V	K*		ш	"
и	"		33		2.4 V											2.7 V		Clock		44	"
и	I _{IH2}		34		2.7 V			GND	-	5.5 V	GND	4.5 V	1		1			J1		100	
и	IIH2		35		-			GND	-	GND	5.5 V	4.5 V	1		1			J2		# H	
и		"	36		 			CIAD	 	CIAD	0.0 v	5.5 V	1	66				J*		66	
и			37	5.5 V	-	GND		-	-	!	-	J.J V	1		1	4.5 V	GND	K1		66	
и	"		38	GND	-	GND		-	-	!	-		1		1	4.5 V	5.5 V	K2		66	
и			39	0.40		0.40							1			5.5 V	0.5 V	K*			"
и	**	44	40		5.5 V		"	†	l	!	l		1		1	0.0 7		Clock	1	66	
и	I _{IH3}		41	GND	3.5 V	2.4 V		-	-	4.5 V	4.5 V	GND	1		1	4.5 V	GND	Preset		80	
u u	"IH3		42	4.5 V	Ä	2.7 V		2.4 V	-	GND	GND	4.5 V	1		1	GND	4.5 V	Clear		80	
и	I _{IH4}		43	GND	A	5.5 V			l	4.5 V	4.5 V	GND	1		1	4.5 V	GND	Preset	1	200	"
и	*IH4 "	44	44	4.5 V	A	0.0 .	"	5.5 V	l	GND	GND	4.5 V	1		1	GND	4.5 V	Clear	1	200	
и	Ios	3011	45	7.5 ¥	GND	GND		0.0 V	-	CITO	CIVE	GND	1		GND	GND	7.0 V	Q	-20	-57	mA
и	.02	"	46		GND	0		GND		!		GND	GND	66	0.10	GND		ā	-20	-57	
	I _{CC}	3005	47					GND										V _{cc}		30	"
		"	48		l	GND	"		l		l				1			V _{cc}		30	"
2	Same tests	, terminal cond	ditions and limits	as for sub	ogroup 1, e	except T _C =	: 125°C a	nd V _{IC} test	s are omitt	ed.											
-	0	Accordant con-	distance and the is-			T	FF00														
3	Same tests	i, terminal cond	ditions and limits	as for sut	ogroup 1, e	except I _C =	: -55°C ar	ia v _{ic} tests	s are omitte	ea.											

TABLE III. Group A inspection for device type 06. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test lin	nits
		883 method	Case C	10	12	13	14	2	1 NC	3	4 J2	5 J*	6	7	8	9 K*	11 K2	Meas. terminal	B 41-		1 10-2
		metriod	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J-	ā	GND	Q	K.	K2	terrinia	Mir	n Max	Uni
7 2/ 4/			49	В	В	Α	4.5 V	В	В	В	В	Α	H 3/	GND	L 3/	Α	В	All		H or	L
_C = 25°C			50	В	В	В		A	В	В	В	Α	L	44	Н	Α	В	output		as show	vn <u>3</u> /
			51	В	В	Α		Α	В	В	В	Α	L		Τ	В	Α	"		66	
			52	В	Α	Α	ı	Α	В	В	В	Α	L	a	Н	В	Α	44		44	
ш			53	В	В	Α		A	В	В	В	A	L	44	Н	В	A	"		66	
и			54	A	В	A		A	В	В	В	Α	L	44	Н	В	В	44		44	
u u			55	Α	Α	Α	и	Α	В	В	В	Α	L	66	Н	В	В	"		4	
			56	A	В	Α	и	A	В	В	В	A	L	66	Н	В	В				
			57	A	В	A	u u	A	В	В	В	A	L		Н	A	A				
			58	A	A	A	и	A	В	В	В	A	L.		H	A	A				
			59	A	В	A		A	В	В	В	A	L		H	A	A				
			60 61	A B	B B	A A		B A	B B	B A	B B	A B	H	-	L	A	A B		-		
			62	В	A	A		A	В	A	В	В	Н		-	A	В		-		
			63	В	В	A	и	A	В	A	В	В	H	-	Ĺ	A	В		-	4	
ш			64	В	В	A	и	A	B	В	A	В	H	4	ī	A	В			66	
			65	В	A	A		A	В	В	Ä	В	H		i i	A	В			44	
и			66	В	В	A	ш	A	В	В	A	В	H	44	Ē	A	В			66	
"			67	В	В	Α	ш	A	В	A	A	A	Н	66	Ī	A	В			66	
"			68	В	A	A	ıı	A	В	A	A	A	Н	66	Ē	A	В			44	
ш			69	В	В	Α	ш	Α	В	Α	Α	Α	Н	4	L	Α	В	**		66	
ii .			70	A	В	Α		Α	В	Α	Α	В	Н	66	L	В	A			44	
"			71	Α	Α	Α	"	Α	В	Α	Α	В	L	66	Н	В	A	"		66	
			72	Α	В	Α		Α	В	Α	Α	В	L		Τ	В	Α	"		66	
u			73	Α	Α	Α	ı	Α	В	Α	Α	В	Н	a	L	В	Α			44	
ш			74	A	В	Α		A	В	Α	A	В	Н	44	L	В	A			66	
и			75	A	В	Α	"	В	В	Α	A	В	Н	44	L	В	A	"		44	
и			76	Α	Α	Α		В	В	Α	Α	В	Н	66	L	В	A	"			
			77	A	В	Α	и	В	В	Α	A	В	Н		L	В	A				
			78	A	В	В		В	В	A	A	В	L		L	В	A				
			79	A	A	В		В	В	A	A	В	L		L	В	A				
			80	A B	В	В		В	В	A	A B	В	L H		L	В	A B		-		
			81 82	В	B B	A A		B A	B B	B B	В	A A	H	-	<u> </u>	A A	В		-		
ш			83	В	A	A		A	В	В	В	A	Н	66	-	A	В		-	66	
			84	В	A	B		A	В	В	В	A	H		L	A	В				
ш			85	В	В	В	и	A	В	В	В	A	Ĺ	66	Н	A	В		-	a	
и			86	В	В	A		A	В	В	В	A	Ĺ	44	H	A	В	44	†	44	
и			87	В	A	A		A	В	В	В	A	Ī.		H	A	В				
ш			88	В	A	A	ш	В	В	В	В	A	Ĺ	44	L.	A	В			66	
и			89	В	A	A	и	A	В	В	В	A	Ĺ	66	H	A	В		†	66	
и			90	A	В	A		A	В	A	A	В	Ĺ		Н	В	A			44	
			91	A	В	В		Α	В	Α	Α	В	L		Н	В	Α	44		44	
er .			92	Α	Α	В	ш	Α	В	Α	Α	В	L	66	Н	В	Α	**		66	

TABLE III. Group A inspection for device type 06. 1/- Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	ts
• .	,	883	Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11	Meas.			
		method	Test No.	K1	Clock	Preset	V _{cc}	Clear	NC	J1	J2	J*	ā	GND	Q	K*	K2	terminal	Min	Max	Unit
9	F _{MAX} <u>5</u> /	(Fig. 14)	93	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	GND		GND	OUT	GND	2.4 V	Q	20		MHz
$T_C = 25^{\circ}C$	F _{MAX} <u>5</u> /	(Fig. 14)	94	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND	OUT			GND	2.4 V	ā	20		MHz
ш	t _{PLH}	3003 (Fig. 13)	95	5.0 V	0.8 V	IN	"	IN		5.0 V	5.0 V	GND	OUT	"		GND	5.0 V	Clear to Q	5	50	ns
и	t _{PLH}		96	"	"	"	"	"		er er	"	"		"	OUT	"		Preset to Q	"	66	"
	t _{PHL}	44	97	"	"	"	"					"		"	OUT			Clear to Q	"	44	"
"	t _{PHL}	44	98				"					"	OUT					Preset to Q	"		
	(Fig. 15)	3003	99	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND		"	OUT	GND	2.4 V	Clock to Q	5	50	ns
и	t _{PLH}	(Fig. 14)	100				"			**		u.	OUT				u	Clock to Q	"		"
	t _{PHL}	66	101				"	ш		66	"	ш			OUT	"	ш	Clock to Q	"	66	"
и	t _{PHL}	44	102	и			"			66	"	u.	OUT	"		"	u	Clock to Q	"	66	"
10	F _{MAX} <u>5</u> /	(Fig. 14)	103	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND		"	OUT	GND	2.4 V	Q	15		MHz
$T_C = 125^{\circ}C$	F _{MAX} <u>5</u> /	(Fig. 14)	104	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND	OUT			GND	2.4 V	ā	15		MHz
u	t _{PLH}	3003 (Fig. 13)	105	5.0 V	0.8 V	IN		IN		5.0 V	5.0 V	GND	OUT			GND	5.0 V	Clear to Q	5	62	ns
	t _{PLH}	\ <u>"</u>	106				44	ш			44				OUT	44	и	Preset to Q	"		
	t _{PHL}		107		ш	u u	4	ш			44	ш			OUT	44		Clear to Q	44	44	
u	t _{PHL}	66	108	"			"			66	"		OUT	"		"	и	Preset to Q	"	66	"
	t _{PLH}	3003	109	2.4 V	IN	5.0 V	"	5.0 V		5.0 V	5.0 V	GND		"	OUT	GND	2.4 V	Clock to Q	5	62	ns
"	t _{PLH}	(Fig. 14)	110	"			"			66	"	и	OUT			"	u	Clock to Q	"	es:	"
	t _{PHL}	44	111				44	ш			44				OUT	44	и	Clock to Q	"		
"	t _{PHL}	66	112				"			66		ш	OUT					Clock to Q		66	

- NOTES:

 A = Normal clock pulse.

 B = Momentary GND, then 4.5 V.

 - 1/ Terminal conditions (pins not designated may be $H \ge 2.0$ V, or $L \le 0.8$ V, or open). $\footnote{2}{\cline{1.5}}$ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum. $\footnote{3}{\cline{1.5}}$ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) $\cline{1.5}$ V and L < 1.5 V when using a high speed checker single comparator. $\footnote{3}{\cline{1.5}}$ Y rests shall be performed in sequence. $\footnote{5}{\cline{1.5}}$ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 07. 1/

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	s
		883 method	Case C Test No.	3 Clock	2 D1	1 Clear	14 V _{CC}	13 Clear	12 D2	11 Clock	10 Preset	9 Q2	8 Q 2	7 GND	6 Q 1	5 Q1	4 Preset	Meas. terminal	Min	Max	Unit
			1001110.	1	٥.	1	•	2	52	2	2		Q 2	0.15	Q 1	~.	1			max	0
1	V _{OH}	3006	1	A	2.0 V		4.5 V							GND		4 mA		Q1	2.4		V
$T_C = 25^{\circ}C$	4	"	2	Α	0.8 V										4 mA			Q 1	"		66
и	4		3			0.8 V								66	4 mA		2.0 V	Q 1	"		44
	**	"	4			2.0 V	ш							66		4 mA	0.8 V	Q1	44		66
и	44	4	5				и		2.0 V	Α		4 mA		66				Q2	41		66
"	"		6				"		0.8 V	Α			4 mA	66				Q 2	"		66
ш	4		7					0.8 V			2.0 V		4 mA	66				Q 2	"		
u u	44	4	8				ш	2.0 V			0.8 V	4 mA		66				Q2			66
u	V _{OL}	3007	9	Α	2.0 V									a	16 mA			Q 1		0.4 V	
	44	"	10	Α	0.8 V									66		16 mA		Q1			66
ш	4		11			0.8 V								66		16 mA	2.0 V	Q 1			
		"	12			2.0 V	и							66	16 mA		0.8 V	Q1			- 44
"			13						2.0 V	Α			16 mA	66				Q 2			66
u		"	14				и		0.8 V	Α		16 mA		66				Q2			66
		"	15				и	0.8 V			2.0 V	16 mA		66				Q2			- 44
	"		16					2.0 V			0.8 V		16 mA	66				Q 2			66
	V _{IC}		17		-12 mA		u							4				D1		-1.5	66
u			18	-12 mA			ű							64				Clock 1			66
и	"		19			-12 mA								66				Clear 1			66
	-		20 21						-12 mA								-12 mA	Preset 1 D2			
ш			22				и		-12 IIIA	-12 mA				44				Clock 2		44	66
ш			23				и	-12 mA		121101				44				Clear 2			66
u u	44		24				ш				-12 mA			66				Preset 2			- 4
ii .	I _{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V							66			0.4 V	D 1	-0.5	-1.6	m/
"	"		26	0.4 V	0.4 V	4.5 V								66			0.4 V	Preset 1			66
"			27					4.5 V	0.4 V	4.5 V	0.4 V							D 2			66
	I _{IL2}		28 29	0.4 V	0.4 V	4.5 V	u	4.5 V	0.4 V	0.4 V	0.4 V			66			GND	Preset 2 Clock 1	-1.0	-3.2	
	IL2	4	30	0.4 V	4.5 V	0.4 V	и							66			4.5 V	Clear 1	"	"3.2	66
"	"	"	31				"	4.5 V	0.4 V	0.4 V	GND			66				Clock 2			**
ш	"	"	32				"	0.4 V	4.5 V	0.8 V	4.5 V			66				Clear 2	"		66
u	I _{IH1}	3010	33	4.5 V	2.4 V	GND	"							66			GND	D1		40	μA
			34					GND	2.4 V	4.5 V	GND						1	D2		40	**
	I _{IH2}	"	35	4.5 V	5.5 V	GND		CND	E E \'	451	CND		1				GND	D1		100	66
			36 37	2.4 V		В	u u	GND	5.5 V	4.5 V	GND		-				GND	D2 Clock 1	-	100 80	-
и	I _{IH3}	4	38	2.4 V	4.5 V	4.5 V	и			 	-		 	44			2.4 V	Preset 1	-	- OU 	66
ш			39				и	В		2.4 V	GND			66				Clock 2			- 66
ш	44	"	40				и	4.5 V	4.5 V	В	2.4 V			66				Preset 2		"	66
u u	I _{IH4}	4	41	5.5 V		В	u							66			GND	Clock 1		200	
	"		42	В	4.5 V	4.5 V				L				66			5.5 V	Preset 1			
	"	"	43				"	B	451	5.5 V	GND		1	66			1	Clock 2			66
	I _{IH5}		44 45	GND	GND	2.4 V		4.5 V	4.5 V	В	5.5 V		-	66			-	Preset 2 Clear 1	-	120	
u	IH5		45	GIND	GIND	2.4 V	ш	2.4 v	GND	GND	-		1	66			1	Clear 1		120	-
u u	I _{IH6}		47	GND	GND	5.5 V	u	2.7 V	0110	0110	-		1	66			 	Clear 1	l	300	44
ш	11116		48	2.10	2,10	2.0 (и	5.5 V	GND	GND				44			1	Clear 2		300	66

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	ts
		883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset	terminal	Min	Max	Ur
1	Ios	3011	49				5.5 V	-						GND		GND	GND	Q1	-20	-57	m
_C = 25°C	"	"	50			GND	"							66	GND			Q 1			
ш	"		51				и				GND	GND						Q2		44	
	"	44	52					GND			O. LD	0.10	GND	66				Q 2	44		T
и	Inc	3005	53	GND	GND		и		GND	GND	GND	GND		66			GND	V _{CC}		30	+
	Icc	3005	54	GND	GND	GND	"	GND	GND	GND	GND			44				V _{CC}		30	
3		-	ditions and limits				5ºC and \														
7 <u>2</u> / <u>4</u> /			55	В	В	В	4.5 V	В	В	В	В	H <u>3</u> /	H <u>3</u> /	GND	H <u>3</u> /	H <u>3</u> /	В	All		H or L	
$\Gamma_{\rm C} = 25^{\circ}{\rm C}$			56	В	В	В	"	В	В	В	Α	L	Н	64	Н	L	Α	outputs	8	as shown	<u>3</u> /
			57	В	В	A	"	A	В	В	Α	L	Н		Н	L	A				
			58	В	В	A	"	Α	В	В	В	Н	L	44	L	Н	В	ш			
			59	Α	В	A		Α	В	Α	В	Н	L		L	Н	В				
			60	A	В	В		В	В	A	В	Н	Н		Н	Н	В				
			61 62	A	A	B B	"	B B	A	A	В	<u>H</u>	H	-	H	H	B A				
			63	A A	A A	A		A	A	A	A	<u> </u>	H		H	L	A			"	
			64	A	A	A		A	A	A	В	H	П	44	L	H	В				
и			65	A	A	A		A	A	A	A	H	-	66		H	A				_
			66	В	A	A	"	A	A	В	A	H	Ĺ	66	<u> </u>	H	A	и			_
ш			67	В	В	A	и	A	В	В	A	H	ī	- 4	Ī	H	A			44	
и			68	A	В	A	"	A	В	A	A	Ĺ	Н		H	L	A	"		"	
"			69	Α	В	Α	"	Α	В	Α	В	Н	L	66	L	Н	В	"		"	
ii .			70	Α	Α	В	"	В	Α	Α	В	Н	Н	66	Н	Н	В			"	
и			71	Α	В	В	"	В	В	Α	В	Н	Н	66	Н	Н	В			"	
			72	Α	В	В		В	В	Α	Α	L	Н		Н	L	Α	"		44	
			73	Α	В	Α	"	Α	В	Α	Α	L	Н	**	Н	L	Α	"		"	
			74	В	Α	Α	"	Α	Α	В	Α	L	Н	66	Н	L	Α			"	
и			75	A	A	A	"	Α	A	Α	Α	Н	L	44	L	Н	A			"	
ii .			76	Α	Α	Α		A	Α	Α	В	Н	L	66	L	Н	В				
и			77	Α	Α	A	"	Α	Α	Α	Α	Н	L	ш	L	Н	A			"	
			78	Α	Α	В		В	Α	Α	Α	L	Н	44	Н	L	A			44	
			79	Α	Α	A	"	Α	A	Α	Α	L	Н	66	H	L	A	ш			
		1	80	A	В	A	"	A	В	Α	В	Н	L	**	L	Н	В	"		44	
u u			81	Α	В	Α	ii ii	Α	В	A	A	н		66		Н	A			44	

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	s
• .	_	883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear 1	V _{cc}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
9	F _{MAX}	(Fig. 11)	82	IN	E	5.0 V	5.0 V							GND		OUT	5.0 V	Q1	10		MHz
$T_C = 25^{\circ}C$	ű		83	IN	E	5.0 V	"							"	OUT		5.0 V	Q 1	ű		"
"	u	и	84				"	5.0 V	E	IN	5.0 V	OUT		u				Q2	"		"
"	"	"	85				"	5.0 V	Е	IN	5.0 V		OUT	ű				Q 2			
44	t _{PLH}	3003 ((Fig. 10)	86			IN	"							"	OUT		IN	Clear 1 to Q 1	5	25	ns
44	и		87			IN	"							"		OUT	IN	Preset 1 to Q1	"	**	"
			88				"	IN			IN		OUT	"				Clear 2 to Q 2			
44		ts.	89				"	IN			IN	OUT		и				Preset 2 to Q2	a	и	и
44	t _{PHL}	ш	90			IN	"							"		OUT	IN	Clear 1 to Q1		33	"
44	и		91			IN	"							"	OUT		IN	Preset 1 to Q 1	"	36	"
	и	и	92				"	IN			IN		OUT					Clear 2	ш	36	
																		to Q 2			
"			93				"	IN			IN	OUT		"				Preset 2 to Q2		33	
"	t _{PLH}	3003 <u>5</u> / (Fig. 11)	94	IN	IN (A)	В	"							a		OUT	5.0 V	Clock 1 to Q1	5	25	ns
44	"	(Fig. 12)	95	IN	IN (A)	5.0 V	"							"	OUT		В	Clock 1 to Q 1		"	"
44	и	(Fig. 11)	96				86	В	IN (A)	IN	5.0 V	OUT		и				Clock 2 to Q2	и	и	и
44	"	(Fig. 12)	97				66	5.0 V	IN (A)	IN	В		OUT	"				Clock 2 to Q 2	и	и	"
44	t _{PHL}	(Fig. 12)	98	IN	IN (B)	5.0 V	66							"		OUT	В	Clock 1	и	33	и
		(Fig. 11)	99	IN	IN (B)	В	"							"	OUT		5.0 V	to Q1 Clock 1		и	"
		(Fig. 12)	100					5.0 V	IN (B)	IN	В	OUT		"				to Q 1	и		
		(Fig. 12)	100					5.0 V	IN (B)	IN	5.0 V	001	OUT	и				to Q2	u	и	
		(Fig. 11)	101					Р	IIN (D)	IIN	5.0 V		001					to Q 2			

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	S
		883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear	V _{cc}	Clear 2	D2	Clock 2	Preset 2	Q2	Q2	GND	1	Q1	Preset 1	terminal	Min	Max	Unit
10	F _{MAX} 6/	(Fig. 11)	102	IN.	Е	5.0 V	5.0 V							GND		OUT	5.0 V	Q1	10		MH
T _C = 125°C	"	"	103	IN	Е	5.0 V	66							u	OUT		5.0 V	<u>0</u> 1			
	ш	"	104					5.0 V	Е	IN	5.0 V	OUT		и				Q2	ш		
	ű	и	105				"	5.0 V	Ē	IN	5.0 V		OUT	u				Q 2			и
"	t _{PLH}	3003	106			IN								и	OUT		IN	Clear 1	5	31	ns
	UPLH .	((Fig. 10)	100			IIV.									001		liv.	to Q 1	3	31	113
	ar.	ш	107			IN	66									OUT	IN	Preset 1 to Q1			"
"	u	"	108				"	IN			IN		OUT					Clear 2			ш
																		to Q 2			
"			109				"	IN			IN	OUT		u				Preset 2 to Q2		u	"
"	t _{PHL}	u	110			IN								u		OUT	IN	Clear 1		39	ш
			111			IN									OUT		IN	to Q1 Preset 1		42	и
			111			IIN									001		IIN	to Q 1		42	
			112					18.1			INI		OUT	u						40	
			112				-	IN			IN		001					Preset 2		42	
																		to Q 2			
			113				-	IN			IN	OUT						Clear 2 to Q2		39	
"	t _{PLH}	3003 <u>5</u> / (Fig. 11)	114	IN	IN (A)	В	66							u u		OUT	5.0 V	Clock 1 to Q1	5	31	ns
	и	(Fig. 12)	115	IN	IN (A)	5.0 V	86							u	OUT		В	Clock 1	ш	ш	"
																		to Q 1			
	u	(Fig. 11)	116				66	В	IN (A)	IN	5.0 V	OUT		u				Clock 2	u	ű	
	,,	(5) (0)						E 0.17	D. 1 (A)				0117					to Q2			
-	-	(Fig. 12)	117				_	5.0 V	IN (A)	IN	В		OUT	_				Clock 2 to Q 2	_	_	
и	t _{PHL}	(Fig. 12)	118	IN	IN (B)	5.0 V	66							u		OUT	В	Clock 1 to Q1	и	39	"
	u	(Fig. 11)	119	IN	IN (B)	В	66							u	OUT		5.0 V	Clock 1	u	ű	- "
																		to Q 1			
	ш	(Fig. 12)	120					5.0 V	IN (B)	IN	В	OUT		u				Clock 2	u		"
4		/Fin 441	404				64	-	INL (D)	INI	501/		OUT					to Q2			ļ.,
-		(Fig. 11)	121				_	В	IN (B)	IN	5.0 V		OUT					Clock 2			
																		to Q 2			

- $$\begin{split} & \text{NOTES:} \\ & \text{A = Normal clock pulse.} \\ & \text{B = Momentary GND, then 4.5 V.} \\ & \text{E = Input D connected to } \overline{Q} \ \ . \end{split}$$
- 1/ Terminal conditions (pins not designated may be $H \ge 2.0 \text{ V}$, or $L \le 0.8 \text{ V}$, or open). 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum. 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) $H \ge 1.5 \text{ V}$ and L < 1.5 V when using a high speed checker single comparator. 4/ Tests shall be performed in sequence. 5/ Tests shall be performed for both D input pulses (A and B). 6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

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5. PACKAGING

5.1 <u>Packaging requirements</u>. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

- 6.1 <u>Intended use.</u> Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
 - 6.2 <u>Acquisition requirements.</u> Acquisition documents should specify the following:
 - a. Title, number, and date of the specification.
 - b. PIN and compliance identifier, if applicable_ (see 1.2).
 - c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
 - d. Requirements for certificate of compliance, if applicable.
 - e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
 - Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
 - g. Requirements for product assurance options.
 - h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
 - I Requirements for "JAN" marking.
 - j. Packaging Requirements (see 5.1)
- 6.3 <u>Qualification</u>. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.
- 6.4 <u>Superseding information</u>. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

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6.5 <u>Abbreviations, symbols, and definitions.</u> The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND	Electrical ground (common terminal)
V _{IN}	Voltage level at an input terminal

- 6.6 <u>Logistic support.</u> Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
- 6.7 <u>Substitutability.</u> The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	SN5472 (Circuit A)
01	DM5472 (Circuit B)
01	MC5472 (Circuit C)
02	SN5473 (Circuit A)
02	DM5473 (Circuit B)
02	S5473 (Circuit C)
03	SN54107 (Circuit A)
03	DM54107 (Circuit B)
03	S54107 (Circuit C)
04	SN5476 (Circuit A)
04	DM5476 (Circuit B)
04	S5476 (Circuit C)
05	5474 (Circuit A)
05	DM5474 (Circuit B)
06	5470
07	SN5479 (Circuit A)
07	MC5479 (Circuit B)

6.8 <u>Change from previous issue.</u> Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

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Custodians:

Army - CR Navy - EC Air Force - 11 DLA - CC Preparing activity: DLA - CC

Review activities:

Army – SM, MI Navy - AS, CG, MC, SH TD Air Force – 03, 19, 99 (Project 5962-2096)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.