AMD Geode™ NX Processors Data Book

April 2006

Publication ID: 31177H

Trademarks

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1 Overview

1.1 General Description

The AMD Geode™ NX 1750@14W processor*, AMD Geode NX 1500@6W processor*, and AMD Geode NX 1250@6W processor* (here after referred to as Geode NX processor unless otherwise specified) were designed to power the next generation of embedded computing platforms, delivering extreme performance for Windows® XP, Windows XPe, Windows CE, and Linux.

The Geode NX processor is manufactured using a 0.13 µm process and provide industry-leading processing power for cutting-edge embedded applications. Figure 1-1 shows a typical NX processor-based system block diagram.

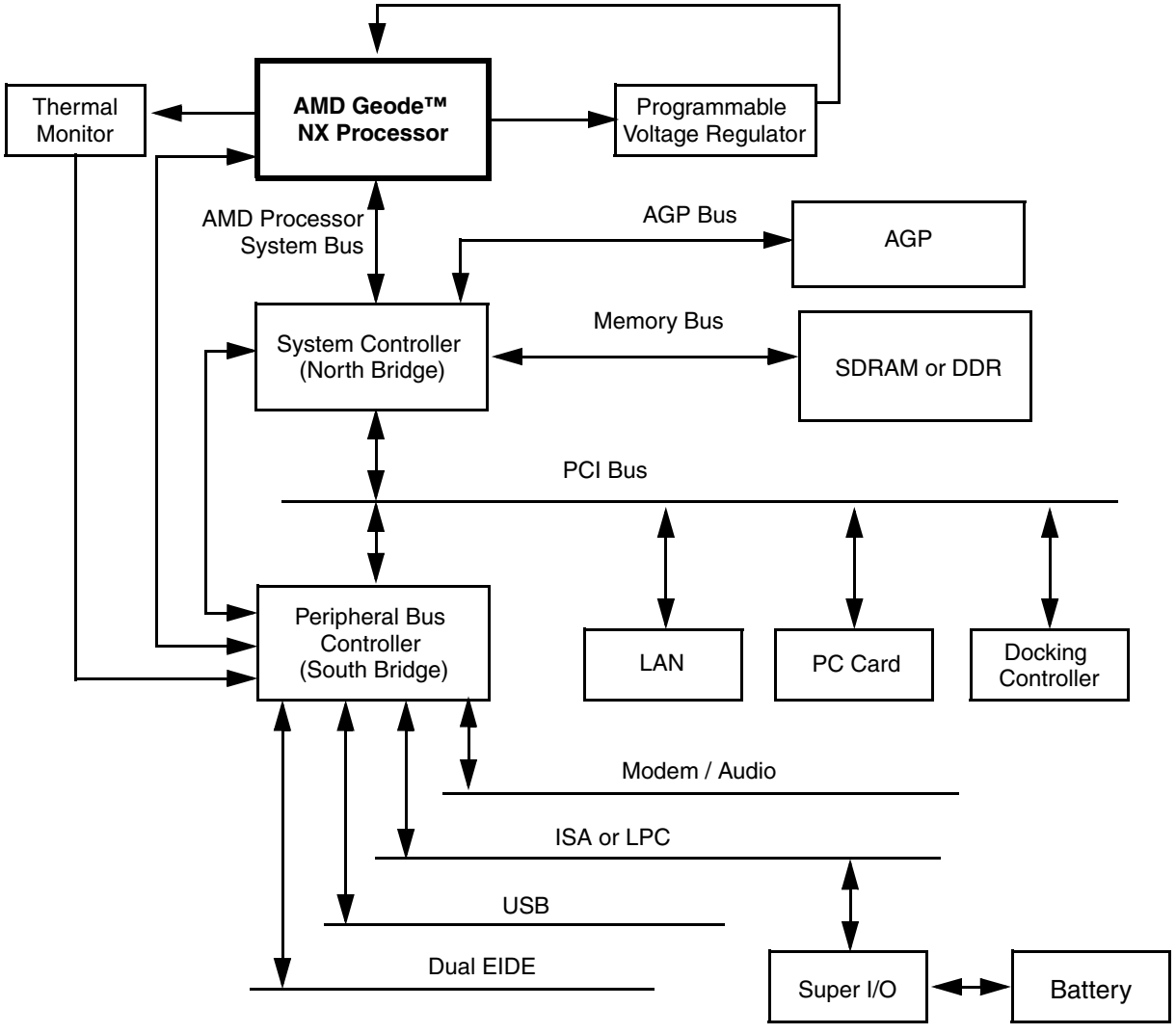


Figure 1-1. Typical System Block Diagram

*The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

The Geode NX processor implements AMD PowerNow!™ technology, which achieves lower power states by adjusting the processor's voltage and/or frequency. The NX 1500@6W* and NX 1250@6W* use fixed operating voltages, and are therefore only able to achieve lower power by adjusting the processor's frequency, while the NX 1750@14W* can be adjusted in frequency and voltage for lower power operation. See Section 5.4.1 "Valid Voltage and Frequency Combinations" on page 49 for more information. The Geode NX processor is available in a low-profile, lidless organic pin grid array (OPGA) package.

The Geode NX processor features seventh-generation microarchitecture with integrated L2 cache that supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The high-speed execution core in the processor includes multiple x86 instruction decoders, a dual-ported 128 KB split level-one (L1) cache (made up of a 64 KB L1 instruction cache and a 64 KB L1 data cache), a 256 KB L2 integrated cache, three independent integer pipelines, three address calculation pipelines, and a fully pipelined, out-of-order, floating-point engine.

The processor's microarchitecture supports AMD 3DNow!™ Professional technology, a high-performance cache architecture, and the 266 MHz, 2.1 GB per second AMD processor system bus. The AMD processor system bus is designed to combine the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling, to provide an extremely powerful, scalable bus available for any x86 processor. The AMD processor system bus operates at twice the front side bus (FSB) frequency.

The Geode NX processor is binary-compatible with existing x86 software and backwards compatible with applications optimized for enhanced 3DNow!, MMX®, and SSE instructions. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the Geode NX processor can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The implemented 3DNow! Professional technology includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as streaming video for the Internet, as well as new instructions for digital signal processing (DSP) and communications applications.

1.2 Microarchitecture Summary

The following features summarize the Geode NX processor's microarchitecture:

- Advanced 0.13 μm technology for higher frequency scaling and lower power consumption
- 128 KB L1 cache (made up of a 64 KB L1 instruction cache and a 64 KB L1 data cache)
- 256 KB L2 cache with hardware data prefetch
- Pipelined floating-point execution unit that executes a peak of three x87 instructions per clock cycle
- Support for MMX, SSE, and 3DNow! Professional instruction sets for high-performance multimedia instruction processing
- Dynamic transitions between higher performance and lower power processor performance states are supported by AMD PowerNow! software and the Windows® XP operating system
- ACPI 1.0b and ACPI 2.0 compliant power management
- Three out-of-order, superscalar, pipelined integer units
- Three out-of-order, superscalar, pipelined address calculation units
- A 266 MHz AMD processor system bus enabling leading-edge system bandwidth for data movement-intensive applications

*The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

1.3 Special Features and Requirements

This data book provides the electrical, thermal and mechanical specifications for the AMD Geode NX processor in the OPGA package. System builders have three choices when determining the optimal solution for their design needs:

- AMD Geode™ NX 1250@6W processor* for value embedded applications requiring fanless performance.
- AMD Geode™ NX 1500@6W processor* for fanless, high performance (up to 1GHz) with very low power consumption designs.
- AMD Geode™ NX 1750@14W processor*, highest performance for demanding graphics, multimedia and high horsepower applications.

The Geode NX processor has some very important operational conditions that the board designer must take into account. They include:

- A tighter processor core voltage tolerance is required for all negative excursions. A total tolerance of –50 mV is required for the voltage delivered to the core of all versions of this processor. This DC tolerance is inclusive of any AC transients that may occur due to changing processor current requirements. See Figure 5-1 "V_{CC_CORE} Voltage Waveform" on page 48 for a graphical representation of this tolerance. Proper output filter component layout is critical to achieving this tolerance at the higher $\frac{dI}{dt}$ loading of these processors.
- The Geode NX processor has a 133 MHz FSB. By using both edges of the FSB clock, the processor is able to achieve a maximum of 266 million transfers per second (MTPS) per data line for the AMD processor system bus. The increased speed of the FSB at low voltage places additional design constraints on the implementation of the AMD processor system bus. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) and the *AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860) for additional information on circuitry and layout guidelines required to fully support this processor.
- The Geode NX processor supports the following ranges:
  - — The operational voltage for the NX 1250@6W processor* is fixed at 1.1V.
  - — The operational voltage for the NX 1500@6W processor* is fixed at 1.0V.
  - — The operational voltage range for the NX 1750@14W processor* is from 1.05V to 1.25V. Specific implementations may choose not to utilize the entire range due to other operational constraints.
- The Geode NX processor has a 6x start-up multiplier.
- The Geode NX processor is compatible with processor system boards that implement an FSB detect circuit. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) and *AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860) for implementation details.

*The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

2 Signal Definitions

Figure 2-1 is a logic symbol diagram for the AMD Geode™ NX processor, showing the logical grouping of the input and output signals.

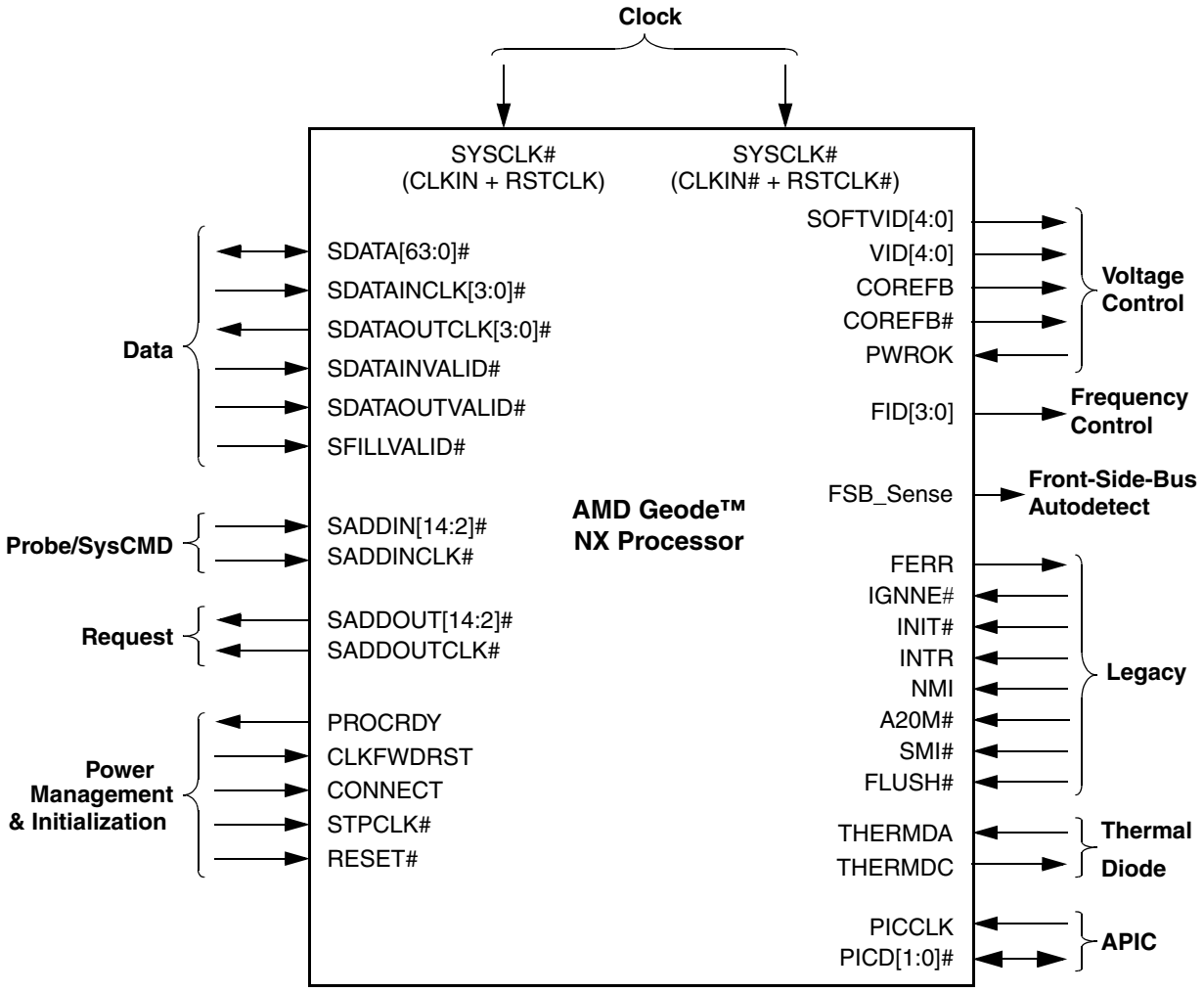


Figure 2-1. Logic Symbol Diagram

2.1 Interface Signals Architecture

The architecture is designed to deliver excellent data movement bandwidth for next-generation x86 platforms as well as the high-performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 64-bit bidirectional data channel), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull, low-voltage, swing-signaling technology contained within the Socket A socket.

For more information, see Section 2.1.3 "AMD Processor System Bus Signals", Section 2.3.4 "AMD Processor System Bus Interface Signals" on page 26, and the *AMD Athlon™ Processor System Bus Specification* (publication ID 21902).

2.1.1 Signaling Technology

The AMD processor system bus uses a low-voltage, swing-signaling technology, that has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers that require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or de-asserted by the source. Termination resistors are not needed because the driver is impedance-matched to the circuit board and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about signals, see Section 2.3 "Signal Descriptions" on page 25.

2.1.2 Push-Pull (PP) Drivers

The AMD Geode NX processors support push-pull (PP) drivers. The system logic configures the processor with the configuration parameter called SysPushPull (1 = PP). The impedance of the PP drivers is set to match the impedance of the circuit board by two external resistors connected to the ZN and ZP pins.

See Section 2.3.12 "Power, Ground and Compensation Circuit Connections" on page 31 for more information.

2.1.3 AMD Processor System Bus Signals

The AMD processor system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Section 5.0 "Electrical Specifications" on page 47 and the *AMD Athlon™ Processor System Bus Specification* (publication ID 21902).

2.2 Pin Assignments

This subsection defines the pin assignments:

- Figure 2-2 on page 15 and Figure 2-3 on page 16 shows the Organic Pin Grid Array (OPGA) for the Geode NX processor, top and bottom views respectively. Because some of the pin names are too long to fit in the grid, they are abbreviated.
- Table 2-1 on page 17 lists all the pins sorted by pin number along with the abbreviation (where necessary) and some additional pin information.
- Table 2-2 on page 23 is a quick reference and sorts the pins alphabetically by signal name (full name; no abbreviation or other parameters are called out) with the corresponding pin number.

PGA Orientation Pins

No pin is present at pin locations A1 and AN1. Circuit board designers should not allow for a PGA socket pin at these locations.

For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) *and AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860).

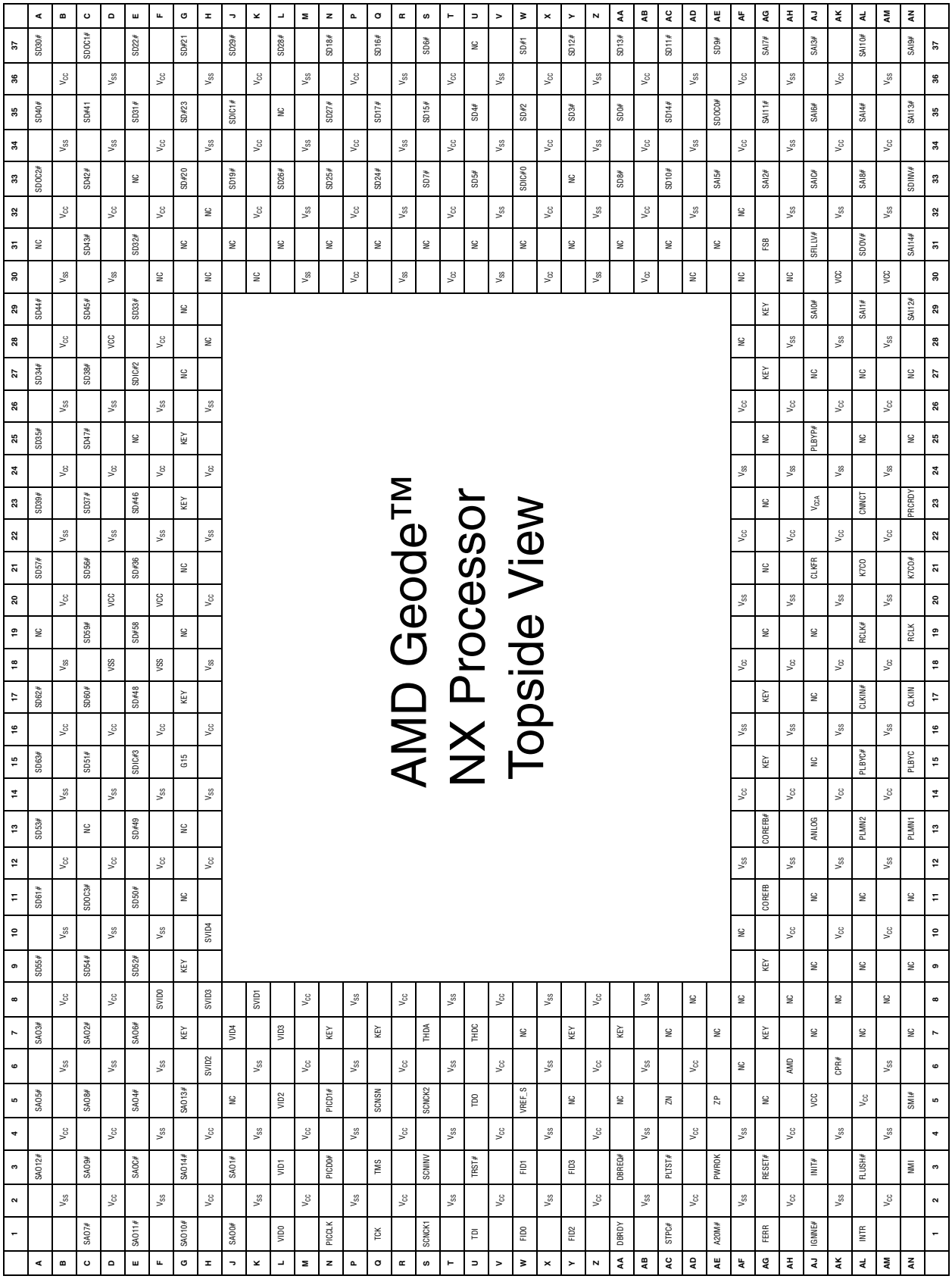


Figure 2-2. Processor Pin Diagram—Topside View

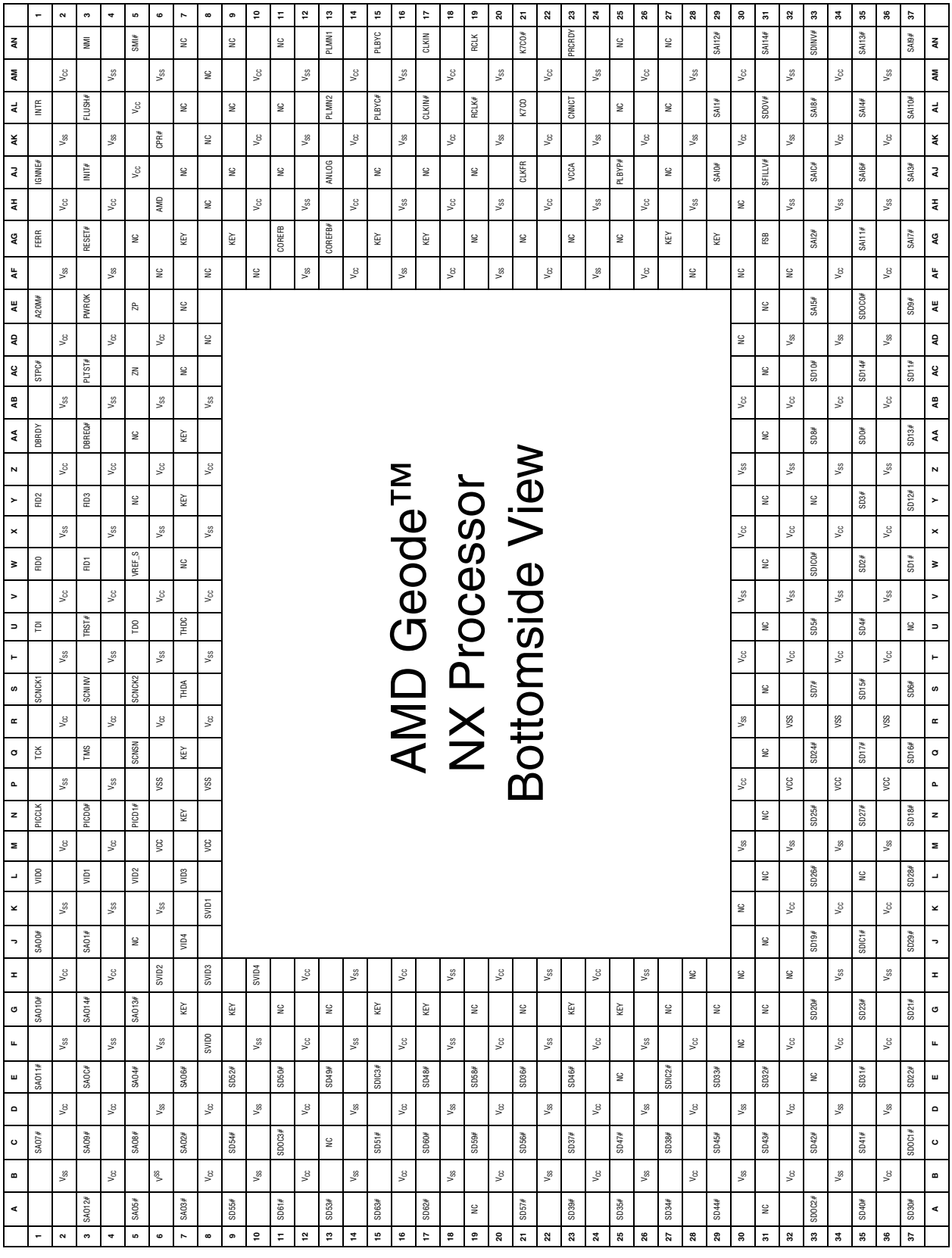


Figure 2-3. Processor Pin Diagram—Bottomside View

Table 2-1 cross-references Socket A pin locations to signal names and is sorted by pin number. Other table parameters are:

- **Signal Name (Abbreviation) column** - The full signal name and the abbreviation name used in the pin diagrams (Figure 2-2 on page 15 and Figure 2-3 on page 16).
- **Level column** - Shows the electrical specification for this pin.
  — "P" indicates a push-pull mode driven by a single source.
  — "O" indicates open-drain mode that allows devices to share the pin.

Note: The Geode NX processor supports push-pull drivers. For more information, see Section 2.1.2 "Push-Pull (PP) Drivers" on page 14.

- **Port column** - Shows the signal type:
  — "I" indicates input,
  — "O" indicates output,
  — "B" indicates bidirectional,
- **Ref. (Reference) column** - Indicates if this signal should be referenced to V_{SS} (G) or VCC_CORE (P) planes for the purpose of signal routing with respect to the current return paths.
- A "–" is used to indicate that the description is not applicable for the pin.

Table 2-1. Pin Assignment - Sorted by Pin Number

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
A1	No Pin	-	-	-
A3	SADDOUT12# (SAO12#)	P	O	G
A5	SADDOUT5# (SAO5#)	P	O	G
A7	SADDOUT3# (SAO3#)	P	O	G
A9	SDATA55# (SD55#)	P	B	P
A11	SDATA61# (SD61#)	P	B	P
A13	SDATA53# (SD53#)	P	B	G
A15	SDATA63# (SD63#)	P	B	G
A17	SDATA62# (SD62#)	P	B	G
A19	NC Pin	-	-	-
A21	SDATA57# (SD57#)	P	B	G
A23	SDATA39# (SD39#)	P	B	G
A25	SDATA35# (SD35#)	P	B	P
A27	SDATA34# (SD34#)	P	B	P
A29	SDATA44# (SD44#)	P	B	G
A31	NC Pin	-	-	-
A33	SDATAOUTCLK2# (SDOC2#)	P	O	P
A35	SDATA40# (SD40#)	P	B	G
A37	SDATA30# (SD30#)	P	B	P
B2	V_{SS}	-	-	-
B4	V_{CC_CORE} (V_{CC})	-	-	-
B6	V_{SS}	-	-	-
B8	V_{CC_CORE} (V_{CC})	-	-	-
B10	V_{SS}	-	-	-
B12	V_{CC_CORE} (V_{CC})	-	-	-
B14	V_{SS}	-	-	-
B16	V_{CC_CORE} (V_{CC})	-	-	-
B18	V_{SS}	-	-	-
B20	V_{CC_CORE} (V_{CC})	-	-	-
B22	V_{SS}	-	-	-
B24	V_{CC_CORE} (V_{CC})	-	-	-

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
B26	V_{SS}	-	-	-
B28	V_{CC_CORE} (V_{CC})	-	-	-
B30	V_{SS}	-	-	-
B32	V_{CC_CORE} (V_{CC})	-	-	-
B34	V_{SS}	-	-	-
B36	V_{CC_CORE} (V_{CC})	-	-	-
C1	SADDOUT7# (SAO7#)	P	O	G
C3	SADDOUT9# (SAO9#)	P	O	G
C5	SADDOUT8# (SAO8#)	P	O	G
C7	SADDOUT2# (SAO2#)	P	O	G
C9	SDATA54# (SD54#)	P	B	P
C11	SDATAOUTCLK3# (SDOC3#)	P	O	G
C13	NC Pin	-	-	-
C15	SDATA51# (SD51#)	P	B	P
C17	SDATA60# (SD60#)	P	B	G
C19	SDATA59# (SD59#)	P	B	G
C21	SDATA56# (SD56#)	P	B	G
C23	SDATA37# (SD37#)	P	B	P
C25	SDATA47# (SD47#)	P	B	G
C27	SDATA38# (SD38#)	P	B	G
C29	SDATA45# (SD45#)	P	B	G
C31	SDATA43# (SD43#)	P	B	G
C33	SDATA42# (SD42)	P	B	G
C35	SDATA41# (SD41#)	P	B	G
C37	SDATAOUTCLK1# (SDOC1#)	P	O	G
D2	V_{CC_CORE} (V_{CC})	-	-	-
D4	V_{CC_CORE} (V_{CC})	-	-	-
D6	V_{SS}	-	-	-
D8	V_{CC_CORE} (V_{CC})	-	-	-
D10	V_{SS}	-	-	-
D12	V_{CC_CORE} (V_{CC})	-	-	-

Table 2-1. Pin Assignment - Sorted by Pin Number (Continued)

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
D14	V_{SS}	-	-	-
D16	V_{CC_CORE} (V_{CC})	-	-	-
D18	V_{SS}	-	-	-
D20	V_{CC_CORE} (V_{CC})	-	-	-
D22	V_{SS}	-	-	-
D24	V_{CC_CORE} (V_{CC})	-	-	-
D26	V_{SS}	-	-	-
D28	V_{CC_CORE} (V_{CC})	-	-	-
D30	V_{SS}	-	-	-
D32	V_{CC_CORE} (V_{CC})	-	-	-
D34	V_{SS}	-	-	-
D36	V_{SS}	-	-	-
E1	SADDOUT11# (SAO11#)	P	O	P
E3	SADDOUTCLK# (SAOC#)	P	O	G
E5	SADDOUT4# (SAO4#)	P	O	P
E7	SADDOUT6# (SAO6#)	P	O	G
E9	SDATA52# (SD52#)	P	B	P
E11	SDATA50# (SD50#)	P	B	P
E13	SDATA49# (SD49#)	P	B	G
E15	SDATAINCLK3# (SDIC3#)	P	I	G
E17	SDATA48# (SD48#)	P	B	P
E19	SDATA58# (SD58#)	P	B	G
E21	SDATA36# (SD36#)	P	B	P
E23	SDATA46# (SD46#)	P	B	P
E25	NC Pin	-	-	-
E27	SDATAINCLK2# (SDIC2#)	P	I	G
E29	SDATA33# (SD33#)	P	B	P
E31	SDATA32# (SD32#)	P	B	P
E33	NC Pin	-	-	-
E35	SDATA31# (SD31#)	P	B	P
E37	SDATA22# (SD22#)	P	B	G
F2	V_{SS}	-	-	-
F4	V_{SS}	-	-	-
F6	V_{SS}	-	-	-
F8	SOFTVID0 (SVID0)	O	O	-
F10	V_{SS}	-	-	-
F12	V_{CC_CORE} (V_{CC})	-	-	-
F14	V_{SS}	-	-	-
F16	V_{CC_CORE} (V_{CC})	-	-	-
F18	V_{SS}	-	-	-
F20	V_{CC_CORE} (V_{CC})	-	-	-
F22	V_{SS}	-	-	-
F24	V_{CC_CORE} (V_{CC})	-	-	-
F26	V_{SS}	-	-	-
F28	V_{CC_CORE} (V_{CC})	-	-	-
F30	NC Pin	-	-	-
F32	V_{CC_CORE} (V_{CC})	-	-	-
F34	V_{CC_CORE} (V_{CC})	-	-	-
F36	V_{CC_CORE} (V_{CC})	-	-	-
G1	SADDOUT10# (SAO10#)	P	O	P
G3	SADDOUT14# (SAO14#)	P	O	G
G5	SADDOUT13# (SAO13#)	P	O	G
G7	Key Pin	-	-	-
G9	Key Pin	-	-	-
G11	NC Pin	-	-	-
G13	NC Pin	-	-	-
G15	Key Pin	-	-	-
G17	Key Pin	-	-	-
G19	NC Pin	-	-	-
G21	NC Pin	-	-	-
G23	Key Pin	-	-	-
G25	Key Pin	-	-	-
G27	NC Pin	-	-	-
G29	NC Pin	-	-	-
G31	NC Pin	-	-	-
G33	SDATA20# (SD20#)	P	B	G
G35	SDATA23# (SD23#)	P	B	G
G37	SDATA21# (SD21#)	P	B	G
H2	V_{CC_CORE} (V_{CC})	-	-	-
H4	V_{CC_CORE} (V_{CC})	-	-	-
H6	SOFTVID2 (SVID2)	O	O	-
H8	SOFTVID3 (SVID3)	O	O	-
H10	SOFTVID4 (SVID4)	O	O	-
H12	V_{CC_CORE} (V_{CC})	-	-	-
H14	V_{SS}	-	-	-
H16	V_{CC_CORE} (V_{CC})	-	-	-
H18	V_{SS}	-	-	-
H20	V_{CC_CORE} (V_{CC})	-	-	-
H22	V_{SS}	-	-	-
H24	V_{CC_CORE} (V_{CC})	-	-	-
H26	V_{SS}	-	-	-
H28	NC Pin	-	-	-
H30	NC Pin	-	-	-
H32	NC Pin	-	-	-
H34	V_{SS}	-	-	-
H36	V_{SS}	-	-	-
J1	SADDOUT0# (SAO0#)	P	O	-
J3	SADDOUT1# (SAO1#)	P	O	-
J5	NC Pin	-	-	-

Table 2-1. Pin Assignment - Sorted by Pin Number (Continued)

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
J7	VID4	O	O	-
J31	NC Pin	-	-	-
J33	SDATA19# (SD19#)	P	B	G
J35	SDATAINCLK1# (SDIC1#)	P	I	P
J37	SDATA29# (SD29#)	P	B	P
K2	V_{SS}	-	-	-
K4	V_{SS}	-	-	-
K6	V_{SS}	-	-	-
K8	SOFTVID1 (SVID1)	O	O	-
K30	NC Pin	-	-	-
K32	V_{CC_CORE} (V_{CC})	-	-	-
K34	V_{CC_CORE} (V_{CC})	-	-	-
K36	V_{CC_CORE} (V_{CC})	-	-	-
L1	VID0	O	O	-
L3	VID1	O	O	-
L5	VID2	O	O	-
L7	VID3	O	O	-
L31	NC Pin	-	-	-
L33	SDATA26# (SD26#)	P	B	P
L35	NC Pin	-	-	-
L37	SDATA28# (SD28#)	P	B	P
M2	V_{CC_CORE} (V_{CC})	-	-	-
M4	V_{CC_CORE} (V_{CC})	-	-	-
M6	V_{CC_CORE} (V_{CC})	-	-	-
M8	V_{CC_CORE} (V_{CC})	-	-	-
M30	V_{SS}	-	-	-
M32	V_{SS}	-	-	-
M34	V_{SS}	-	-	-
M36	V_{SS}	-	-	-
N1	PICCLK	0	I	-
N3	PICD0#	0	B	-
N5	PICD1#	0	B	-
N7	Key Pin	-	-	-
N31	NC Pin	-	-	-
N33	SDATA25# (SD25#)	P	B	P
N35	SDATA27# (SD27#)	P	B	P
N37	SDATA18# (SD18#)	P	B	G
P2	V_{SS}	-	-	-
P4	V_{SS}	-	-	-
P6	V_{SS}	-	-	-
P8	V_{SS}	-	-	-
P30	V_{CC_CORE} (V_{CC})	-	-	-
P32	V_{CC_CORE} (V_{CC})	-	-	-
P34	V_{CC_CORE} (V_{CC})	-	-	-
P36	V_{CC_CORE} (V_{CC})	-	-	-

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
Q1	TCK	P	I	-
Q3	TMS	P	I	-
Q5	SCANSHIFTEN (SCNSN)	P	I	-
Q7	Key Pin	-	-	-
Q31	NC Pin	-	-	-
Q33	SDATA24# (SD24#)	P	B	P
Q35	SDATA17# (SD17#)	P	B	G
Q37	SDATA16# (SD16#)	P	B	G
R2	V_{CC_CORE} (V_{CC})	-	-	-
R4	V_{CC_CORE} (V_{CC})	-	-	-
R6	V_{CC_CORE} (V_{CC})	-	-	-
R8	V_{CC_CORE} (V_{CC})	-	-	-
R30	V_{SS}	-	-	-
R32	V_{SS}	-	-	-
R34	V_{SS}	-	-	-
R36	V_{SS}	-	-	-
S1	SCANCLK1 (SCNCK1)	P	I	-
S3	SCANINTEVAL (SCNINV)	P	I	-
S5	SCANCLK2 (SCNCK2)	P	I	-
S7	THERMDA (THDA)	-	-	-
S31	NC Pin	-	-	-
S33	SDATA7# (SD7#)	P	B	G
S35	SDATA15# (SD15#)	P	B	P
S37	SDATA6# (SD6#)	P	B	G
T2	V_{SS}	-	-	-
T4	V_{SS}	-	-	-
T6	V_{SS}	-	-	-
T8	V_{SS}	-	-	-
T30	V_{CC_CORE} (V_{CC})	-	-	-
T32	V_{CC_CORE} (V_{CC})	-	-	-
T34	V_{CC_CORE} (V_{CC})	-	-	-
T36	V_{CC_CORE} (V_{CC})	-	-	-
U1	TDI	P	I	-
U3	TRST#	P	I	-
U5	TDO	P	O	-
U7	THERMDC (THDC)	-	-	-
U31	NC Pin	-	-	-
U33	SDATA5# (SD5#)	P	B	G
U35	SDATA4# (SD4#)	P	B	G
U37	NC Pin	-	-	-
V2	V_{CC_CORE} (V_{CC})	-	-	-
V4	V_{CC_CORE} (V_{CC})	-	-	-
V6	V_{CC_CORE} (V_{CC})	-	-	-
V8	V_{CC_CORE} (V_{CC})	-	-	-
V30	V_{SS}	-	-	-

Table 2-1. Pin Assignment - Sorted by Pin Number (Continued)

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
V32	V_{SS}	-	-	-
V34	V_{SS}	-	-	-
V36	V_{SS}	-	-	-
W1	FID0	O	O	-
W3	FID1	O	O	-
W5	VREF_SYS (VREF_S)	-	I	-
W7	NC Pin	-	-	-
W31	NC Pin	-	-	-
W33	SDATAINCLK0# (SDIC0#)	P	I	G
W35	SDATA2# (SD2#)	P	B	G
W37	SDATA1# (SD1#)	P	B	P
X2	V_{SS}	-	-	-
X4	V_{SS}	-	-	-
X6	V_{SS}	-	-	-
X8	V_{SS}	-	-	-
X30	V_{CC_CORE} (V_{CC})	-	-	-
X32	V_{CC_CORE} (V_{CC})	-	-	-
X34	V_{CC_CORE} (V_{CC})	-	-	-
X36	V_{CC_CORE} (V_{CC})	-	-	-
Y1	FID2	O	O	-
Y3	FID3	O	O	-
Y5	NC Pin	-	-	-
Y7	Key Pin	-	-	-
Y31	NC Pin	-	-	-
Y33	NC Pin	-	-	-
Y35	SDATA3# (SD3#)	P	B	G
Y37	SDATA12# (SD12#)	P	B	P
Z2	V_{CC_CORE} (V_{CC})	-	-	-
Z4	V_{CC_CORE} (V_{CC})	-	-	-
Z6	V_{CC_CORE} (V_{CC})	-	-	-
Z8	V_{CC_CORE} (V_{CC})	-	-	-
Z30	V_{SS}	-	-	-
Z32	V_{SS}	-	-	-
Z34	V_{SS}	-	-	-
Z36	V_{SS}	-	-	-
AA1	DBRDY	P	O	-
AA3	DBREQ#	P	I	-
AA5	NC Pin	-	-	-
AA7	Key Pin	-	-	-
AA31	NC Pin	-	-	-
AA33	SDATA8# (SD8#)	P	B	P
AA35	SDATA0# (SD0#)	P	B	G
AA37	SDATA13# (SD13#)	P	B	G
AB2	V_{SS}	-	-	-
AB4	V_{SS}	-	-	-

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
AB6	V_{SS}	-	-	-
AB8	V_{SS}	-	-	-
AB30	V_{CC_CORE} (V_{CC})	-	-	-
AB32	V_{CC_CORE} (V_{CC})	-	-	-
AB34	V_{CC_CORE} (V_{CC})	-	-	-
AB36	V_{CC_CORE} (V_{CC})	-	-	-
AC1	STPCLK# (STPC#)	P	I	-
AC3	PLLTEST# (PLTST#)	P	I	-
AC5	ZN	P	-	-
AC7	NC Pin	-	-	-
AC31	NC Pin	-	-	-
AC33	SDATA10# (SD10#)	P	B	P
AC35	SDATA14# (SD14#)	P	B	G
AC37	SDATA11# (SD11#)	P	B	G
AD2	V_{CC_CORE} (V_{CC})	-	-	-
AD4	V_{CC_CORE} (V_{CC})	-	-	-
AD6	V_{CC_CORE} (V_{CC})	-	-	-
AD8	NC Pin	-	-	-
AD30	NC Pin	-	-	-
AD32	V_{SS}	-	-	-
AD34	V_{SS}	-	-	-
AD36	V_{SS}	-	-	-
AE1	A20M#	P	I	-
AE3	PWROK	P	I	-
AE5	ZP	P	-	-
AE7	NC Pin	-	-	-
AE31	NC Pin	-	-	-
AE33	SADDIN5# (SAI5#)	P	I	G
AE35	SDATAOUTCLK0# (SDOC0#)	P	O	P
AE37	SDATA9# (SD9#)	P	B	G
AF2	V_{SS}	-	-	-
AF4	V_{SS}	-	-	-
AF6	NC Pin	-	-	-
AF8	NC Pin	-	-	-
AF10	NC Pin	-	-	-
AF12	V_{SS}	-	-	-
AF14	V_{CC_CORE} (V_{CC})	-	-	-
AF16	V_{SS}	-	-	-
AF18	V_{CC_CORE} (V_{CC})	-	-	-
AF20	V_{SS}	-	-	-
AF22	V_{CC_CORE} (V_{CC})	-	-	-
AF24	V_{SS}	-	-	-
AF26	V_{CC_CORE} (V_{CC})	-	-	-
AF28	NC Pin	-	-	-
AF30	NC Pin	-	-	-

Table 2-1. Pin Assignment - Sorted by Pin Number (Continued)

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
AF32	NC Pin	-	-	-
AF34	V_{CC_CORE} (V_{CC})	-	-	-
AF36	V_{CC_CORE} (V_{CC})	-	-	-
AG1	FERR	P	O	-
AG3	RESET#	-	I	-
AG5	NC Pin	-	-	-
AG7	Key Pin	-	-	-
AG9	Key Pin	-	-	-
AG11	COREFB	-	-	-
AG13	COREFB#	-	-	-
AG15	Key Pin	-	-	-
AG17	Key Pin	-	-	-
AG19	NC Pin	-	-	-
AG21	NC Pin	-	-	-
AG23	NC Pin	-	-	-
AG25	NC Pin	-	-	-
AG27	Key Pin	-	-	-
AG29	Key Pin	-	-	-
AG31	FSB_Sense (FSB)	-	O	G
AG33	SADDIN2# (SAI2#)	P	I	G
AG35	SADDIN11# (SAI11#)	P	I	G
AG37	SADDIN7# (SAI7#)	P	I	P
AH2	V_{CC_CORE} (V_{CC})	-	-	-
AH4	V_{CC_CORE} (V_{CC})	-	-	-
AH6	AMD Pin	-	-	-
AH8	NC Pin	-	-	-
AH10	V_{CC_CORE} (V_{CC})	-	-	-
AH12	V_{SS}	-	-	-
AH14	V_{CC_CORE} (V_{CC})	-	-	-
AH16	V_{SS}	-	-	-
AH18	V_{CC_CORE} (V_{CC})	-	-	-
AH20	V_{SS}	-	-	-
AH22	V_{CC_CORE} (V_{CC})	-	-	-
AH24	V_{SS}	-	-	-
AH26	V_{CC_CORE} (V_{CC})	-	-	-
AH28	V_{SS}	-	-	-
AH30	NC Pin	-	-	-
AH32	V_{SS}	-	-	-
AH34	V_{SS}	-	-	-
AH36	V_{SS}	-	-	-
AJ1	IGNNE#	P	I	-
AJ3	INIT#	P	I	-
AJ5	V_{CC_CORE} (V_{CC})	-	-	-
AJ7	NC Pin	-	-	-
AJ9	NC Pin	-	-	-
AJ11	NC Pin	-	-	-
AJ13	Analog (ANLOG)	-	-	-
AJ15	NC Pin	-	-	-
AJ17	NC Pin	-	-	-
AJ19	NC Pin	-	-	-
AJ21	CLKFWDRST (CLKFR)	P	I	P
AJ23	V_{CCA}	-	-	-
AJ25	PLLBYPASS# (PLBYP#)	P	I	-
AJ27	NC Pin	-	-	-
AJ29	SADDIN0# (SAI0#)	P	I	-
AJ31	SFILLVALID# (SFILLV#)	P	I	G
AJ33	SADDINCLK# (SAIC#)	P	I	G
AJ35	SADDIN6# (SAI6#)	P	I	P
AJ37	SADDIN3# (SAI3#)	P	I	G
AK2	V_{SS}	-	-	-
AK4	V_{SS}	-	-	-
AK6	CPU_PRESENCE# (CPR#)	-	-	-
AK8	NC Pin	-	-	-
AK10	V_{CC_CORE} (V_{CC})	-	-	-
AK12	V_{SS}	-	-	-
AK14	V_{CC_CORE} (V_{CC})	-	-	-
AK16	V_{SS}	-	-	-
AK18	V_{CC_CORE} (V_{CC})	-	-	-
AK20	V_{SS}	-	-	-
AK22	V_{CC_CORE} (V_{CC})	-	-	-
AK24	V_{SS}	-	-	-
AK26	V_{CC_CORE} (V_{CC})	-	-	-
AK28	V_{SS}	-	-	-
AK30	V_{CC_CORE} (V_{CC})	-	-	-
AK32	V_{SS}	-	-	-
AK34	V_{CC_CORE} (V_{CC})	-	-	-
AK36	V_{CC_CORE} (V_{CC})	-	-	-
AL1	INTR	P	I	-
AL3	FLUSH#	P	I	-
AL5	V_{CC_CORE} (V_{CC})	-	-	-
AL7	NC Pin	-	-	-
AL9	NC Pin	-	-	-
AL11	NC Pin	-	-	-
AL13	PLLMON2 (PLMN2)	O	O	-
AL15	PLLBYPASSCLK# (PLBYC#)	P	I	-
AL17	CLKIN#	P	I	P
AL19	RSTCLK# (RCLK#)	P	I	P
AL21	K7CLKOUT (K7CO)	P	O	-
AL23	CONNECT (CNNCT)	P	I	P
AL25	NC Pin	-	-	-

Table 2-1. Pin Assignment - Sorted by Pin Number (Continued)

Pin No.	Signal Name (Abbreviation)	Level	Port	Ref.
AL27	NC Pin	-	-	-
AL29	SADDIN1# (SAI1#)	P	I	-
AL31	SDATAOUTVALID# (SDOV#)	P	I	P
AL33	SADDIN8# (SAI8#)	P	I	P
AL35	SADDIN4# (SAI4#)	P	I	G
AL37	SADDIN10# (SAI10#)	P	I	G
AM2	V_{CC_CORE} (V_{CC})	-	-	-
AM4	V_{SS}	-	-	-
AM6	V_{SS}	-	-	-
AM8	NC Pin	-	-	-
AM10	V_{CC_CORE} (V_{CC})	-	-	-
AM12	V_{SS}	-	-	-
AM14	V_{CC_CORE} (V_{CC})	-	-	-
AM16	V_{SS}	-	-	-
AM18	V_{CC_CORE} (V_{CC})	-	-	-
AM20	V_{SS}	-	-	-
AM22	V_{CC_CORE} (V_{CC})	-	-	-
AM24	V_{SS}	-	-	-
AM26	V_{CC_CORE} (V_{CC})	-	-	-
AM28	V_{SS}	-	-	-
AM30	V_{CC_CORE} (V_{CC})	-	-	-
AM32	V_{SS}	-	-	-
AM34	V_{CC_CORE} (V_{CC})	-	-	-
AM36	V_{SS}	-	-	-
AN1	No Pin	-	-	-
AN3	NMI	P	I	-
AN5	SMI#	P	I	-
AN7	NC Pin	-	-	-
AN9	NC Pin	-	-	-
AN11	NC Pin	-	-	-
AN13	PLLMON1 (PLMN1)	O	B	-
AN15	PLLBYPASSCLK (PLBYC)	P	I	-
AN17	CLKIN	P	I	P
AN19	RSTCLK (RCLK)	P	I	P
AN21	K7CLKOUT# (K7CO#)	P	O	-
AN23	PROCRDY (PRCRDY)	P	O	P
AN25	NC Pin	-	-	-
AN27	NC Pin	-	-	-
AN29	SADDIN12# (SAI12#)	P	I	G
AN31	SADDIN14# (SAI14#)	P	I	G
AN33	SDATAINVALID# (SDINV#)	P	I	P
AN35	SADDIN13# (SAI13#)	P	I	G
AN37	SADDIN9# (SAI9#)	P	I	G

Table 2-2. Pin Assignment - Sorted Alphabetically by Signal Name

Signal Name	Pin No.
A20M#	AE1
AMD Pin	AH6
Analog	AJ13
CLKFWDRST	AJ21
CLKIN	AN17
CLKIN#	AL17
CONNECT	AL23
COREFB	AG11
COREFB#	AG13
CPU_PRESENCE#	AK6
DBRDY	AA1
DBREQ#	AA3
FERR	AG1
FID0	W1
FID1	W3
FID2	Y1
FID3	Y3
FLUSH#	AL3
FSB_Sense	AG31
IGNNE#	AJ1
INIT#	AJ3
INTR	AL1
K7CLKOUT	AL21
K7CLKOUT#	AN21
Key Pin (Total of 16)	G7, G9, G23, AA7, AG9, AG17, AG27, AG29, G15, G17, G25, N7, Q7, Y7, AG7, AG15
NC Pin (Total of 71)	G11, J31, K30, N31, S31, U31, W7, W31, Y5, Y31, AA5, AA31, AC7, AC31, AD8, AD30, AE7, AE31, AF6, AF8, AF10, AF28, AF30, AF32, AG5, AG19, AG21, AG23, AG25, AH8, AH30, AJ7, AJ9, AJ11, AJ15, AJ17, AJ19, AJ27, AK8, AL7, AL9, AL11, AL25, AL27, AM8, AN7, AN9, AN11, AN25, AN27, A19, A31, C13, E25, E33, F30, G13, G19, G21, G27, G29, G31, H28, H30, H32, J5, L31, L35, Q31, U37, Y33

Signal Name	Pin No.
NMI	AN3
No Pin	A1, AN1
PICCLK	N1
PICD0#	N3
PICD1#	N5
PLLBYPASS#	AJ25
PLLBYPASSCLK	AN15
PLLBYPASSCLK#	AL15
PLLMON1	AN13
PLLMON2	AL13
PLLTEST#	AC3
PROCRDY	AN23
PWROK	AE3
RESET#	AG3
RSTCLK	AN19
RSTCLK#	AL19
SADDIN0#	AJ29
SADDIN1#	AL29
SADDIN2#	AG33
SADDIN3#	AJ37
SADDIN4#	AL35
SADDIN5#	AE33
SADDIN6#	AJ35
SADDIN7#	AG37
SADDIN8#	AL33
SADDIN9#	AN37
SADDIN10#	AL37
SADDIN11#	AG35
SADDIN12#	AN29
SADDIN13#	AN35
SADDIN14#	AN31
SADDINCLK#	AJ33
SADDOUT0#	J1
SADDOUT1#	J3
SADDOUT2#	C7
SADDOUT3#	A7
SADDOUT4#	E5
SADDOUT5#	A5
SADDOUT6#	E7
SADDOUT7#	C1
SADDOUT8#	C5
SADDOUT9#	C3
SADDOUT10#	G1
SADDOUT11#	E1
SADDOUT12#	A3
SADDOUT13#	G5
SADDOUT14#	G3
SADDOUTCLK#	E3
SCANCLK1	S1

Signal Name	Pin No.
SCANCLK2	S5
SCANINTEVAL	S3
SCANSHIFTEN	Q5
SDATA0#	AA35
SDATA1#	W37
SDATA2#	W35
SDATA3#	Y35
SDATA4#	U35
SDATA5#	U33
SDATA6#	S37
SDATA7#	S33
SDATA8#	AA33
SDATA9#	AE37
SDATA10#	AC33
SDATA11#	AC37
SDATA12#	Y37
SDATA13#	AA37
SDATA14#	AC35
SDATA15#	S35
SDATA16#	Q37
SDATA17#	Q35
SDATA18#	N37
SDATA19#	J33
SDATA20#	G33
SDATA21#	G37
SDATA22#	E37
SDATA23#	G35
SDATA24#	Q33
SDATA25#	N33
SDATA26#	L33
SDATA27#	N35
SDATA28#	L37
SDATA29#	J37
SDATA30#	A37
SDATA31#	E35
SDATA32#	E31
SDATA33#	E29
SDATA34#	A27
SDATA35#	A25
SDATA36#	E21
SDATA37#	C23
SDATA38#	C27
SDATA39#	A23
SDATA40#	A35
SDATA41#	C35
SDATA42#	C33
SDATA43#	C31
SDATA44#	A29
SDATA45#	C29

Table 2-2. Pin Assignment - Sorted Alphabetically by Signal Name (Continued)

Signal Name	Pin No.
SDATA46#	E23
SDATA47#	C25
SDATA48#	E17
SDATA49#	E13
SDATA50#	E11
SDATA51#	C15
SDATA52#	E9
SDATA53#	A13
SDATA54#	C9
SDATA55#	A9
SDATA56#	C21
SDATA57#	A21
SDATA58#	E19
SDATA59#	C19
SDATA60#	C17
SDATA61#	A11
SDATA62#	A17
SDATA63#	A15
SDATAINCLK0#	W33
SDATAINCLK1#	J35
SDATAINCLK2#	E27
SDATAINCLK3#	E15
SDATAINVALID#	AN33
SDATAOUTCLK0#	AE35
SDATAOUTCLK1#	C37
SDATAOUTCLK2#	A33
SDATAOUTCLK3#	C11
SDATAOUTVALID#	AL31
SFILLVALID#	AJ31
SMI#	AN5
SOFTVID0	F8
SOFTVID1	K8
SOFTVID2	H6
SOFTVID3	H8
SOFTVID4	H10
STPCLK#	AC1
TCK	Q1
TDI	U1
TDO	U5
THERMDA	S7
THERMDC	U7
TMS	Q3
TRST#	U3

Signal Name	Pin No.
V_{CC_CORE} (Total of 101)	B12, B16, B20, B28, B32, D2, D4, D8, D12, D16, D20, D24, D28, D32, F12, F16, F20, F24, F28, F32, F34, F36, H2, H4, H12, H16, H20, H24, K32, K34, K36, M2, M4, M6, M8, P30, P32, P34, P36, R2, R4, R6, R8, T30, T32, T34, T36, V2, V4, V6, V8, X30, X32, X34, X36, Z2, Z4, Z6, Z8, AB30, AB32, AB34, AB36, AD2, AD4, AD6, AF14, AF18, AF22, AF26, AF34, AF36, AH2, AH4, AH10, AH14, AH18, AH22, AH26, AJ5, AK10, AK14, AK18, AK22, AK26, AK30, AK34, AK36, AL5, AM2, AM10, AM14, AM18, AM22, AM26, AM30, AM34, B4, B8, B24, B36,
V_{CCA}	AJ23
VID0	L1
VID1	L3
VID2	L5
VID3	L7
VID4	J7
VREF_SYS	W5

Signal Name	Pin No.
V_{SS} (Total of 101)	B2, B6, B10, B14, B18, B22, B26, B30, B34, D6, D10, D14, D18, D22, D26, D30, D34, D36, F2, F4, F6, F10, F14, F18, F22, F26, H14, H18, H22, H26, H34, H36, K2, K4, K6, M30, M32, M34, M36, P2, P4, P6, P8, R30, R32, R34, R36, T2, T4, T6, T8, V30, V32, V34, V36, X2, X4, X6, X8, Z30, Z32, Z34, Z36, AB2, AB4, AB6, AB8, AD32, AD34, AD36, AF2, AF4, AF12, AF16, AF20, AF24, AH12, AH16, AH20, AH24, AH28, AH32, AH34, AH36, AK2, AK4, AK12, AK16, AK20, AK24, AK28, AK32, AM4, AM6, AM12, AM16, AM20, AM24, AM28, AM32, AM36
ZN	AC5
ZP	AE5

2.3 Signal Descriptions

2.3.1 Clock Interface Signals

Signal Name	Pin No.	Port	Description
SYSCLK	--	--	**System Clock.** SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system clock generator. See CLKIN and RSTCLK (SYSCLK) signal description.
SYSCLK#	--	--	
CLKIN	AN17	I	**Clock In and Reset Clock.** Connect CLKIN with RSTCLK and name it SYSCLK. Connect CLKIN# with RSTCLK# and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.
CLKIN#	AL17	I	
RSTCLK	AL19	I	
RSTCLK#	AL19	I	
K7CLKOUT	AL21	O	**K7 Clock Output.** These signals are each terminated with a resistor pair, 100 ohms to V_{CC_CORE} and 100 ohms to V_{SS}. The effective termination resistance and voltage are 50 ohms and $V_{CC\_CORE}/2$. Route as short as possible from the processor pins.
K7CLKOUT#	AN21	O	

2.3.2 Power Management and Initialization Interface Signals

Signal Name	Pin No.	Port	Description
PROCRDY	AN23	O	**Processor Ready.** An output from the system used for power management and clock-forward initialization at reset.
CONNECT	AL23	I	**Connect.** An input from the system used for power management and clock-forward initialization at reset.
CLKFWDRST	AJ21	I	**Clock Forward Reset.** Resets the clock-forward circuitry for both the system and processor.
STPCLK#	AC1	I	**Stop Clock.** An input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
RESET#	AG3	I	**Reset.** When asserted, RESET# causes the initialization of all processor states and invalidates cache blocks without write back of previous data.
CPU_PRESENCE	AK6	--	**CPU Presence.** CPU_PRESENCE# is connected to V_{SS} on the processor package. If pulled up on the circuit board, it may be used to detect the presence or absence of a processor.

2.3.3 Southbridge Interface Signals

Signal Name	Pin No.	Port	Description
FERR	AG1	O	**Floating Point Error.** An output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a totem-pole-driven active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the “Required Circuits” chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363).
IGNNE#	AJ1	I	**Ignore Numeric Errors.** When asserted, this signal tells the processor to ignore numeric errors.

2.3.3 Southbridge Interface Signals (continued)

Signal Name	Pin No.	Port	Description
INIT#	AJ3	I	**Interrupt Integer Registers.** When asserted, INIT# resets the integer registers without affecting the floating point registers or the internal caches. Execution starts at 0FFFF_FFF0h
INTR	AL1	I	**Interrupt.** An input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
NMI	AN3	I	**Non-Maskable Interrupt.** An input from the system that causes a non-maskable interrupt.
A20M#	AE1	I	**Address Bit 20.** An input from the system used to simulate address wrap-around in the 20-bit 8086.
SMI#	AN5	I	**System Management Interrupt.** An input that causes the processor to enter the system management mode.
FLUSH#	AL3	I	**Flush.** FLUSH# must be tied to V_{CC_CORE} with a pull-up resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.

2.3.4 AMD Processor System Bus Interface Signals

Signal Name	Pin No.	Port	Description
VREF_SYS	W5	I	**System Bus Voltage Reference.** This input drives the threshold voltage for the AMD processor system bus input receivers. The value of VREF_SYS is system specific. In addition, to minimize V_{CC_CORE} noise rejection from VREF_SYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) and *AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860).
SDATA[63:0]#	See Table 2-2 on page 23	B	**System Data Bus.** Bidirectional interface to and from the processor and system for data movement. Data is skewed-aligned with either the SDATAINCLK[3:0]# or SDATAOUTCLK[3:0]# signal. Both rising and falling edges are used to transfer data.
SDATAINCLK[3:0]#	E15, E27, J35, W33	I	**System Data Input Clock.** The single-ended forwarded clock driven by the system to transfer data on SDATA[63:0]#. Each 16-bit data word is skewed-aligned with this clock. Both rising and falling edges are used to transfer data.
SDATAOUTCLK[3:0]	C11, A33, C37, AE35	O	**System Data Output Clock.** The single-ended forwarded clock driven by the system to transfer data on SDATA[63:0]#. Each 16-bit data word is skewed-aligned with this clock. Both rising and falling edges are used to transfer data.
SDATAINVALID#	AN33	I	**System Data Input Valid.** This input is driven by the system and controls the flow of data into the processor. SDATAINVALID# can be used to introduce an arbitrary number of cycles between octawords into the processor.
SDATAOUTVALID#	AL31	I	**System Data Output Valid.** This input is driven by the system and controls the flow of data from the processor. SDATAOUTVALID# can be used to introduce an arbitrary number of cycles between quadwords into the processor.

2.3.4 AMD Processor System Bus Interface Signals (continued)

Signal Name	Pin No.	Port	Description
SFILLVALID#	AJ31	I	**System Bus Fill Valid.** When asserted, validates the current memory or I/O data transfer into the processor. The system can tie this pin to the asserted state (validating all fills), or use it to enable or cancel fills as they progress. The processor can sample SFILLVALID# at D0 or D1 (that is, the first or second data beat).
SADDIN[14:2]#	See Table 2-2 on page 23	I	**System Address Inputs.** The unidirectional system address and command interface into the processor from the system. It is used to transfer probes or data movement commands into the processor. All probes and commands on SADDIN[14:2]# are skewed-aligned with the forward clock, SADDINCLK#.
SADDINCLK#	AJ33	I	**System Address Input Clock.** The single-ended forwarded clock for SADDIN[14:2]# driven by the system. Both rising and falling edges are used to transfer probes or commands.
SADDOUT[14:2]#	See Table 2-2 on page 23	I	**System Address Outputs.** The unidirectional system address interface from the processor to the system. It is used to transfer processor commands or probe responses to the system. All commands on SADDOUT[14:0#] are skewed-aligned with the forward clock SADDOUTCLK#.
SADDOUTCLK#	E3	I	**System Address Output Clock.** The single-ended forwarded clock for SADDOUT[14:2]# driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
SADDIN[1:0]#	AL29, AJ29		**System Address Inputs and Outputs bits 1 and 0.** The NX processor does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to V_{CC} with pull-up resistors, if this bit is not supported by the Northbridge. SADDOUT[1:0]# are tied to V_{CC} with pull-up resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ Processor System Bus Specification* (publication ID 21902).
SADDOUT[1:0]#	J3, J1		

2.3.5 APIC Interface Signals

Signal Name	Pin No.	Port	Description
PICCLK	N1	I	**APIC Clock and Interrupts.** The Advanced Programmable Interrupt Controller (APIC) feature provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. PICD[1:0]# are the bidirectional message passing signals used for the APIC and are driven to the Southbridge or a dedicated I/O APIC. PICCLK must be driven with a valid clock input. Refer to VCC_2.5V Generation Circuit, found in the section, “Motherboard Required Circuits” of the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) for the required supporting circuity. For more information, see Table 5-8 "PICD[1:0]# and PICCLK (APIC Pins) DC Characteristics" on page 52.
PICD[1:0]#	N5, N3	B	

2.3.6 FSB Interface Signals

Signal Name	Pin No.	Port	Description
FSB_Sense	AG31	O	**Front Side Bus Sense.** This signal may be used by an external circuit to automatically detect the Front Side Bus (FSB) setting of the processor. This pin is always pulled low by the package, indicating that the FSB of the processor is 133 MHz. The FSB_Sense pin is 3.3V tolerant.

2.3.7 Frequency ID Interface Signals

Signal Name	Pin No.	Port	Description
FID[3:0]	Y3, Y1, W3, W1	O	**Frequency Identification Outputs.** After PWROK is asserted to the processor the FID[3:0] pins drive a value of: FID[3:0] = 0110 that corresponds to a 6x SYSCLK multiplier for the 133 MHz FSB. This information is used by the Northbridge to create the SIP (Serial Initialization Packet) stream that the Northbridge sends to the processor after RESET# is de-asserted. For more information, see Section 3.4 "SYSCLK Multipliers" on page 42 and Table 5-7 "FID[3:0] DC Characteristics" on page 51.

2.3.8 Thermal Diode Interface Signals

Signal Name	Pin No.	Port	Description
THERMDA	S7	--	**Thermal Diode Anode and Cathode.** These signals are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system. See Table 5-16 "Thermal Diode Electrical Characteristics" on page 59 for more details.
THERMDC	U7	--	

2.3.9 Voltage Control Interface Signals

Signal Name	Pin No.	Port	Description
COREFB	AG11	--	**Core Feedback.** These are outputs to the system that provide processor core voltage feedback to the system.
COREFB#	AG13	--	
PWROK	AE3	I	**Power Okay.** The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification. For more information, Section 5.10 "Signal and Power-Up Requirements" on page 61.

2.3.9 Voltage Control Interface Signals (continued)

Signal Name	Pin No.	Port	Description
SOFTVID[4:0]	H10, H8, H6, K8, F8	O	**Soft Voltage ID/Voltage ID Mux.** AMD PowerNow!™ technology can use the FID_Change protocol described in Section 4.1 on page 9 to transition the SOFTVID[4:0] outputs and therefore V_{CC_CORE} as part of processor performance state transitions. **Note:** The NX 1750@14W processor* supports multiple core voltages whereas the NX 1500@6W and NX 1250@6W processors* support only one core voltage (NX 1500@6W = 1.0V) (NX 1250@6W = 1.1V). The VID[4:0] (Voltage ID) and SOFTVID[4:0] (Software driven Voltage ID) outputs are used by the DC/DC power converter to select the processor core voltage. The VID[4:0] pins are shorted to ground or left unconnected on the package and must be pulled up on the circuit board. The SOFTVID[4:0] pins are open-drain and 2.5V tolerant. Refer to the *VCC_2.5V Generation Circuit* found in the *Motherboard Required Circuits* section of the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) for the required supporting circuitry. The circuit board is required to implement a VID multiplexer to select a deterministic voltage for the processor at power-up before the PWROK input is asserted. Before PWROK is asserted, the VID multiplexer drives the VID value from VID[4:0] pins to the DC/DC converter for V_{CC_CORE}. After PWROK is asserted, the VID multiplexer drives the VID value from the SOFTVID[4:0] pins to the DC/DC converter for V_{CC_CORE} of the processor. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) and the *AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860) for the recommended VID multiplexer circuit. The SOFTVID[4:0] pins are driven by the processor to select the maximum V_{CC_CORE} of the processor as reported by the Maximum VID field of the FidVidStatus MSR (MSR C001_0042h) within 20 ns of PWROK assertion. Before PWROK is asserted, the SOFTVID[4:0] outputs are not driven to a deterministic value. The SOFTVID[4:0] outputs must be used to select V_{CC_CORE} after PWROK is asserted. Any time the RESET# input is asserted, the SOFTVID[4:0] pins will be driven to select the maximum voltage. **Note:** The Start-up VID and Maximum VID fields of the FidVidStatus MSR report the same value that corresponds to the nominal voltage that the processor requires to operate at maximum frequency. AMD PowerNow! technology can use the FID_Change protocol described in Section 3.1 "Power Management States" on page 33 to transition the SOFTVID[4:0] outputs and therefore V_{CC_CORE} as part of processor performance state transitions. The VID codes used by the processor are defined in Table 2-3 "SOFTVID[4:0] and VID[4:0] Code to Voltage Definition" on page 30. *The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.
VID[4:0]	J7, L7, L5, L3, L1	O	

Table 2-3. SOFTVID[4:0] and VID[4:0] Code to Voltage Definition

VID[4:0]	V_{CC_CORE} (V)	VID[4:0]	V_{CC_CORE} (V)
00000	2.000	10000	1.275
00001	1.950	10001	1.250
00010	1.900	10010	1.225
00011	1.850	10011	1.200
00100	1.800	10100	1.175
00101	1.750	10101	1.150
00110	1.700	10110	1.125
00111	1.650	10111	1.100
01000	1.600	11000	1.075
01001	1.550	11001	1.050
01010	1.500	11010	1.025
01011	1.450	11011	1.000
01100	1.400	11100	0.975
01101	1.350	11101	0.950
01110	1.300	11110	0.925
01111	Shutdown	11111	Shutdown

2.3.10 Test Measurement Interface Signals

Signal Name	Pin No.	Port	Description
TCK	Q1	I	**JTAG Interface Pins.** TCK, TMS, TDI, TRST#, and TDO pins should be connected directly to the circuit board debug connector. Pull up TDI, TCK, TMS, and TRST# to V_{CC_CORE} with pull-up resistors.
TMS	Q3	I	
TDI	U1	i	
TRST#	U3	I	
TDO	U5	O	
PLLTEST#	AC3	I	**PLL Bypass and Test.** These signals makeup the PLL bypass and test interface. This interface is tied disabled on the circuit board. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to V_{CC_CORE} with pull-up resistors.
PLLBYPASS#	AJ25	I	
PLLMON1	AN13	B	
PLLMON2	AL13	O	
PLLBYPASSCLK	AN15	I	
PLLBYPASSCLK#	AL15	I	
DBRDY	AA1	O	**Debug Ready and Debug Request.** DBRDY and DBREQ# are routed to the debug connector. DBREQ# is tied to V_{CC_CORE} with a pull-up resistor.
DBREQ#	AA3	I	
SCANSHIFTEN	Q5	I	**Scan Interface.** This interface is AMD internal and is tied disabled with pull-down resistors to ground on the circuit board.
SCANINTEVAL	S3	I	
SCANCLK1	S1	I	
SCANCLK2	S5	I	

2.3.11 Key Pin, AMD Pin, Analog Pin and No Connect Pins

Signal Name	Pin No.	Port	Description
Key Pins	See Table 2-2 on page 23	--	**Key Pins (Total of 16).** These 16 locations are for processor type keying for forwards and backwards compatibility. Circuit board designers should treat Key Pins like NC (no connect) Pins. See the NC Pins signal description for more information. A socket designer has the option of creating a top mold piece that allows PGA Key Pins only where designated. However, sockets that populate all 16 Key Pins must be allowed, so the circuit board must always provide for pins at all Key Pin locations.
AMD Pin	AH6	--	**AMD Pin.** AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, circuit board socket design should account for the possibility that a contact could be loaded in this position. The circuit board should treat the AMD Pin (AH6) as an NC Pin. A socket designer has the option of creating a top mold piece that blocks this pin location. However, sockets that populate the AMD pin must be allowed, so the circuit board must always provide for a NC type pin at this pin location. AMD Socket A processors do not implement a pin at location AH6. When a socket that does not provide a pin hole at location AH6 is used, a non-AMD PGA370 part does not fit into Socket A.
Analog Pin	AJ13	--	**Analog Pin.** Treat this pin as a NC.
NC Pins	See Table 2-2 on page 23	--	**No Connection Pins (Total of 71).** The circuit board should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.

2.3.12 Power, Ground and Compensation Circuit Connections

Signal Name	Pin No.	Port	Description
V_{CCA}	AJ23	--	**Power Connection A.** V_{CCA} is the processor PLL supply. For information about the V_{CCA} pin, see Table 5-2 "V_{CCA} Electrical Characteristics" on page 47 and the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363).
V_{CC_CORE}	See Table 2-2 on page 23	--	**Power Connection (Total of 101).**
V_{SS}	See Table 2-2 on page 23	--	**Ground Connection (Total of 101).**
ZN	AC5	--	**Z Negative and Positive.** These are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP (Serial Initialization Packet) parameter SysPushPull asserted), ZN is tied to V_{CC_CORE} with a resistor that has a resistance matching the impedance Z_0 of the transmission line. ZP is tied to V_{SS} with a resistor that has a resistance matching the impedance Z_0 of the transmission line.
ZP	AE5	--	

3 Power Management

This chapter describes the power management features of the AMD Geode™ NX processor. The power management features of the processor are compliant with the ACPI 1.0b and ACPI 2.0 specifications and support AMD PowerNow!™ technology.

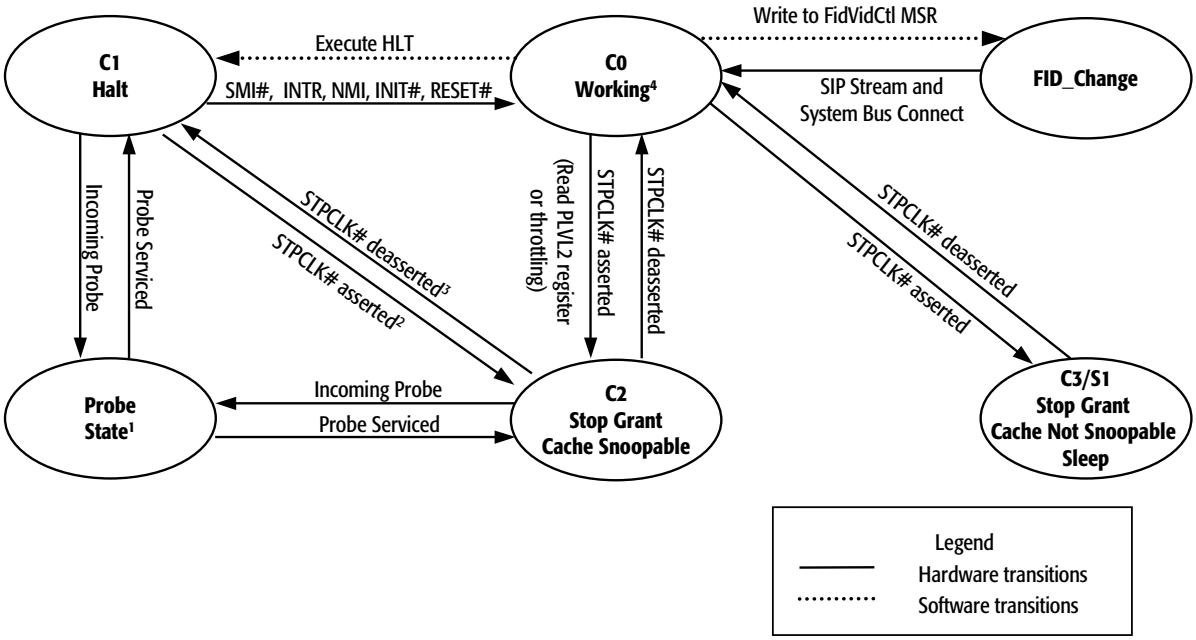
3.1 Power Management States

The Geode NX processor has a variety of operating states that support different power management goals. In addition to the standard operating state, the processor supports low-power Halt and Stop Grant states and the FID_Change state. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems, for processor power management. AMD PowerNow! technology software is used to control processor performance states with operating systems that do not support ACPI 2.0-defined processor performance state control.

Figure 3-1 shows the power management states of the processor. The figure includes the ACPI "Cx" naming convention for these states.

The sections that follow provide an overview of the power management states. For more details, refer to the *AMD Athlon™ Processor System Bus Specification* (publication ID 21902).

Note: In all power management states that the processor is powered, the system must not stop the system clock (SYSCLK/SYSCLK#) to the processor.



Note: The System Bus is connected during the following states:
1) The Probe state
2) During transitions between the Halt state and the C2 Stop Grant state
3) During transitions between the C2 Stop Grant state and the Halt state
4) C0 Working state

Figure 3-1. Processor Power Management States

3.1.1 Working State

The Working state is the state in which the processor is executing instructions.

3.1.2 Halt State

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD processor system bus. The processor only enters the low power state dictated by the CLK_Ctl MSR (MSR C001_001Bh) if the system controller (Northbridge) disconnects the AMD processor system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor exits the Halt state and enters the Stop Grant state. The processor initiates a system bus connect, if it is disconnected, then issues a Stop Grant special cycle. When STPCLK# is de-asserted, the processor exits the Stop Grant state and re-enters the Halt state. The processor issues a Halt special cycle when reentering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, INTR, NMI, RESET#, or SMI#, or via a local APIC interrupt message. When the Halt state is exited the processor initiates an AMD processor system bus connect if it is disconnected.

3.1.3 Stop Grant States

The processor enters the Stop Grant state upon recognition of assertion of the STPCLK# input. After entering the Stop Grant state, the processor issues a Stop Grant special bus cycle on the AMD processor system bus. The processor is not in a low-power state at this time, because the AMD processor system bus is still connected. After the Northbridge disconnects the AMD processor system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK_Ctl MSR (MSR C001_001Bh). If the Northbridge needs to probe the processor during the Stop Grant state while the system bus is disconnected, it must first connect the system bus. Connecting the system bus places the processor into the higher power probe state. After the Northbridge has completed all probes of the processor, the Northbridge must disconnect the AMD processor system bus again so that the processor can return to the low-power state. During the Stop Grant states, the processor latches INIT#, INTR, NMI, SMI#, or a local APIC interrupt message if they are asserted.

The Stop Grant state is exited upon the de-assertion of STPCLK# or the assertion of RESET#. When STPCLK# is de-asserted, the processor initiates a connect of the AMD processor system bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized. If RESET# is sampled asserted during the Stop Grant state, the processor exits the Stop Grant state and the reset process begins.

There are two mechanisms for asserting STPCLK#: hardware and software.

The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. Typically this is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and de-asserted until THERM# is de-asserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge.

The operating system places the processor into the C2 Stop Grant state by reading the P_LVL2 register in the Southbridge.

If an ACPI Thermal Zone is defined for the processor, the operating system can initiate throttling with STPCLK# using the ACPI defined P_CNT register in the Southbridge. The Northbridge connects the AMD processor system bus, and the processor enters the Probe state to service cache snoops during Stop Grant for C2 or throttling.

In C2, probes are allowed, as shown in Figure 3-1 on page 33.

- If an ACPI Thermal Zone is defined for the processor, the operating system can initiate throttling with STPCLK# using the ACPI defined P_CNT register in the Southbridge. The Northbridge connects the AMD processor system bus, and the processor enters the Probe state to service cache snoops during Stop Grant for C2 or throttling.
- The operating system places the processor into the C3 Stop Grant state by reading the P_LVL3 register in the Southbridge. In C3, the operating system and Northbridge hardware enforce a policy that prevents the processor from being probed. The Southbridge de-asserts STPCLK# and brings the processor out of the C3 Stop Grant state if a bus master request, interrupt, or any other enabled resume event occurs.
- The Stop Grant state is also entered for the S1, Powered On Suspend, system sleep state based on a write to the SLP_TYP and SLP_EN fields in the ACPI-defined Power Management 1 control register in the Southbridge. During the S1 sleep state, system software ensures no bus master or probe activity occurs. The Southbridge de-asserts STPCLK# and brings the processor out of the S1 Stop Grant state when any enabled resume event occurs.

3.1.4 Probe State

The Probe state is entered when the Northbridge connects the AMD processor system bus to probe the processor (for example, to snoop the processor caches) when the processor is in the Halt or Stop Grant state. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state. When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). When probe activity is completed the processor only returns to a low-power state after the Northbridge disconnects the AMD processor system bus again.

3.1.5 FID_Change State

The FID_Change State is part of the AMD processor system bus FID_Change Protocol. During the FID_Change state the Frequency Identification (FID[4:0]) code that determines the core frequency of the processor and Voltage Identification (VID[4:0]) driven on the SOFTVID[4:0] pins are transitioned to change the core frequency and core voltage of the processor. The NX 1750@14W processor* supports multiple core voltages whereas the NX 1500@6W and NX 1250@6W processors* support only one core voltage (NX 1500@6W = 1.0V) (NX 1250@6W = 1.1V).

Note: The FID[3:0] pins of the processor do not transition as part of the FID_Change protocol.

3.1.6 Processor Performance States and the FID_Change Protocol

The FID_Change protocol is used by AMD PowerNow! software to transition the processor from one performance state to another. The FID_Change protocol is also used for ACPI 2.0-compliant processor performance state control.

Processor performance states are combinations of processor core voltage and core frequency. Processor performance states are used in embedded systems to optimize the power consumption of the processor (and therefore battery powered run-time) based upon processor utilization.

Table 5-4 "Voltage and Frequency Combinations" on page 49. specifies the valid voltage and frequency combinations supported by the processor based upon the maximum core frequency and the maximum nominal core voltage.

The core frequency multiplier is determined by a 5-bit Frequency ID (FID) code (MSR C001_0041h[4:0]). The core voltage is determined by a 5-bit Voltage ID (VID) code (MSR C001_0041h[12:8]).

Before PWROK is asserted to the processor, the VID[4:0] outputs of the processor dictate the core voltage level of the processor.

After PWROK is asserted, the core voltage of the processor is dictated by the SOFTVID[4:0] outputs. The SOFTVID[4:0] outputs of the processor are not driven to a deterministic value until after PWROK is asserted to the processor. The circuit board therefore must provide a 'VID Multiplexer' to drive the VID[4:0] outputs to the DC/DC converter for the core voltage of the processor before PWROK is asserted and drive the SOFTVID[4:0] outputs to the DC/DC converter after PWROK is asserted.

The FID[3:0] signals are valid within 100 ns after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. For warm reset, the FID[3:0] signals become valid within 100 ns after RESET# is asserted. For signal timing requirements refer to Section 5.10 "Signal and Power-Up Requirements" on page 61.

After RESET# is de-asserted, the FID[3:0] outputs are not used to transmit FID information for subsequent software controlled changes in the operating frequency of the processor.

Processor performance state transitions are required to occur as two separate transitions. The order of these transitions depends on whether the transition is to a higher or lower performance state.

When transitioning from a lower performance state to a higher performance state the order of the transitions is:

1) The FID_Change protocol is used to transition to the higher voltage, while keeping the frequency fixed at the current setting.
2) The FID_Change protocol is then used to transition to the higher frequency, while keeping the voltage fixed at the higher setting.

When transitioning from a high performance state to a lower performance state the order of the transitions is:

1) The FID_Change protocol is used to transition to the lower frequency, while keeping the voltage fixed at its current setting.
2) The FID_Change protocol is then used to transition to the lower voltage, while keeping the frequency fixed at the lower setting.

The processor provides two MSRs to support the FID_Change protocol: the FidVidCtl MSR (MSR C001_0041h) and the FidVidStatus MSR (MSR C001_0042h). For a definition of these MSRs and their use, refer to the *BIOS Requirements for AMD PowerNow™ Technology Application Note* (publication ID 25264)

*The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

3.1.6.1 FID_Change Protocol Example

In any FID_Change transition, only the core voltage or core frequency of the processor is transitioned. Two FID_Change transitions are required to transition the voltage and frequency to a valid performance state. When the voltage is being transitioned, the frequency is held constant by transitioning to the same FID[3:0] as the current FID reported in the FidVidStatus MSR (MSR C001_0042h).

Example

1) System software determines that a change in processor performance state is required.
2) System software executes a WRMSR instruction to write to the FidVidCtl MSR (MSR C001_0041h) to dictate:
   - The new VID[4:0] code that will be driven to the DC/DC converter from the SOFTVID[4:0] outputs of the processor that selects the new core voltage level.
   - The new FID[4:0] code that will be used by the processor to dictate its new operating frequency.
   - A Stop Grant Timeout Count (SGTC[19:0], MSR C001_0041h[51:32]) value that determines how many SYSCLK/SYSCLK# 133 MHz clock periods the processor will remain in the FID_Change state. This time accounts for the time that it takes for the PLL of the processor to lock to the new core frequency and the time that it takes for the core voltage of the processor to ramp to the new value.
3) The FIDCHGRATIO bit (MSR C001_0041h[20]) must be set to 1.
4) The VIDC bit (MSR C001_0041h[17]) must be set to 1 if the voltage is going to be changed.
5) The FIDC bit (MSR C001_0041h[16]) must be set to 1 if the frequency is going to be changed.
6) Writing the SGTC field (MSR C001_0041h[51:32]) to a non-zero value initiates the FID_Change protocol.

On the instruction boundary that the SGTC field of the FidVidCtl MSR is written to a non-zero value, the processor stops code execution and issues a FID_Change special cycle on the AMD processor system bus.

The FID_Change special cycle has a data encoding of 0007_0002h that is passed on SDATA[31:0].

SDATA[36:32] contain the new FID[4:0] code during the FID_Change special cycle. The Northbridge is required to capture this FID[4:0] code when the FID_Change special cycle is run.

In response to receiving the FID_Change special cycle, the Northbridge is required to disconnect. The Northbridge completes any in-progress bus cycles and then disable its arbiter before disconnecting the AMD processor system bus so that it will not initiate a AMD processor system bus connect based on bus master or other activity. The Northbridge must disconnect the AMD processor system bus or the system will hang because the processor is not executing any operating system or application code and is waiting for the AMD processor system bus to disconnect so that it can continue with the FID_Change protocol. The Northbridge initiates an AMD processor system bus disconnect in the usual manner; it de-asserts CONNECT.

The processor allows the disconnect to complete by de-asserting PROCRDY. The Northbridge completes the disconnect by asserting CLKFWDRST.

Once the AMD processor system bus has been disconnected in response to a FID_Change special cycle, the Northbridge is not allowed to initiate a re-connect, the processor is responsible for the eventual re-connect.

After the AMD processor system bus is disconnected, the processor enters a low-power state where the clock grid is ramped down by a value specified in the CLK_CTL MSR (MSR C001_001Bh).

After entering the low-power state, the processor will:

- Begin counting down the value that was programmed into the SGTC field.
- Drive the new VID[4:0] value on SOFTVID[4:0], causing its core voltage to transition.
- Drive the new FID[4:0] value to its PLL, causing the PLL to lock to the new core frequency.

When the SGTC count reaches zero, the processor ramps its entire clock grid to full frequency (the PLL is already locked to) and signal that it is ready for the Northbridge to transmit the new SIP (Serial Initialization Packet) stream associated with the new processor core operating frequency. The processor signals this by pulsing PROCRDY high and then low.

The Northbridge responds to this high pulse on PROCRDY by pulsing CLKFWDRST low and then transferring a SIP stream as it does after PROCRDY is de-asserted after the de-assertion of RESET#. The difference is that the SIP stream that the Northbridge transmits to the processor now corresponds to the FID[4:0] that was transmitted on SDATA[36:32] during the FID_Change special cycle.

After the SIP stream is transmitted, the processor initiates the AMD processor system bus connect sequence by asserting PROCRDY. The Northbridge responds by de-asserting CLKFWDRST. The forward clocks are started and the processor issues a Connect special cycle.

The AMD processor system bus connection causes the processor to resume execution of operating system and application code at the instruction that follows the WRMSR to the FidVidCtl MSR (MSR C001_0041h) that started the FID_Change protocol and processor performance state transition.

Figure 3-2 illustrates the processor SOFTVID transition during the AMD processor system bus disconnect in response to a FID_Change special cycle.

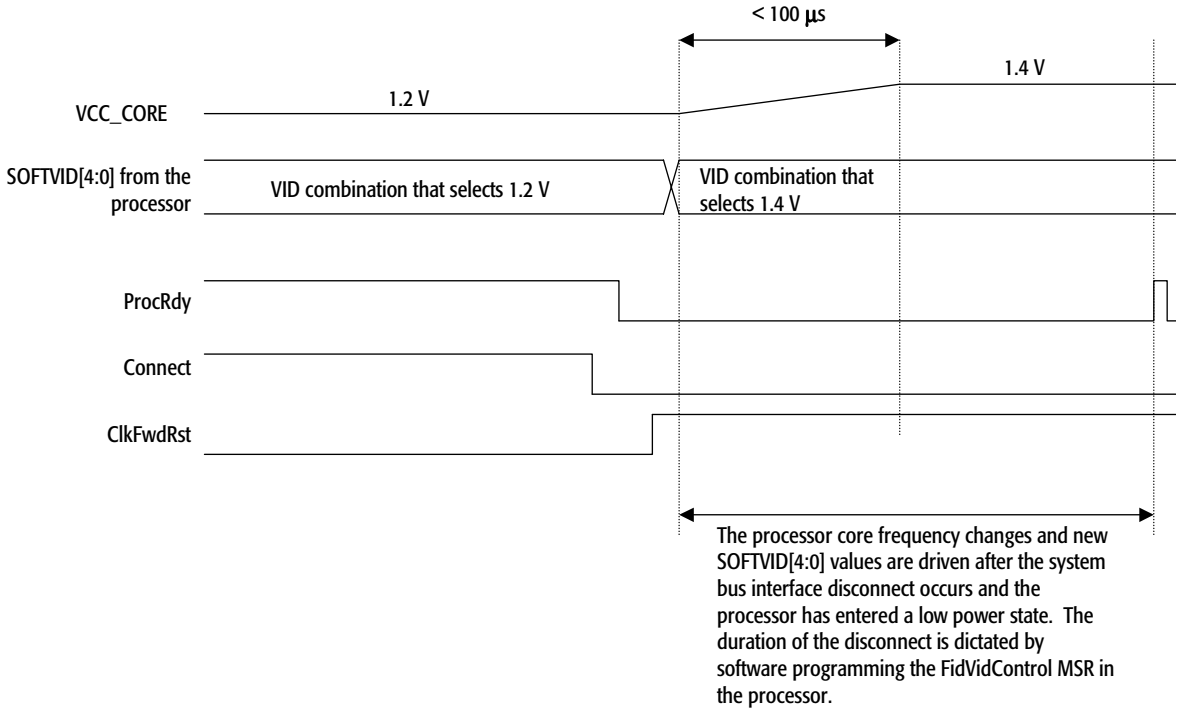


Figure 3-2. SOFTVID Transition During the AMD Processor System Bus Disconnect for FID_Change

3.2 Connect and Disconnect Protocol

Significant power savings of the processor only occur if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

3.2.1 Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD processor system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a Connect special cycle.

AMD processor system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt, Stop Grant, or FID_Change special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# de-assertion, or completion of a FID_Change transition. Reconnect is initiated by the Northbridge to probe the processor.The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge de-asserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the de-assertion of CONNECT on a rising edge of SYSCLK and de-asserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: The Northbridge must disconnect the processor from the AMD processor system bus before issuing the Stop Grant special cycle to the PCI bus or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.

In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# de-assertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been de-asserted).

For more information, see the *AMD Athlon™ Processor System Bus Specification* (publication ID 21902)for the definition of the C-bit and the Connect special cycle.

Figure 3-3 shows STPCLK# assertion resulting in the processor in the Stop Grant state and the AMD processor system bus disconnected.

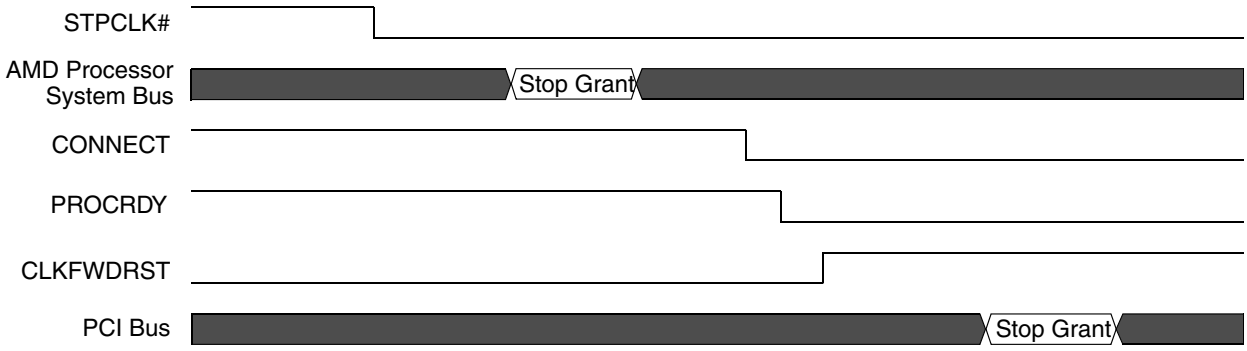


Figure 3-3. AMD Processor System Bus Disconnect Sequence in the Stop Grant State

An example of the AMD processor system bus disconnect sequence is as follows:

1. The peripheral controller (Southbridge) asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted, it enters the Stop Grant state and then issues a Stop Grant special cycle.
3. When the special cycle is received by the Northbridge, it de-asserts CONNECT, assuming no probes are pending, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by de-asserting PROCRDY.
5. The Northbridge asserts CLKFWDRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the processor enters a low-power state. The Northbridge passes the Stop Grant special cycle along to the Southbridge.

Figure 3-4 shows the signal sequence of events that takes the processor out of the Stop Grant state, connects the processor to the AMD processor system bus, and puts the processor into the Working state.

The following sequence of events removes the processor from the Stop Grant state and connects it to the system bus:

1) The Southbridge de-asserts STPCLK#, informing the processor of a wake event.
2) When the processor recognizes STPCLK# de-assertion, it exits the low-power state and asserts PROCRDY, notifying the Northbridge to connect to the bus.
3) The Northbridge asserts CONNECT.
4) The Northbridge de-asserts CLKFWDRST, synchronizing the forwarded clocks between the processor and the Northbridge.

The processor issues a Connect special cycle on the system bus and resumes operating system and application code execution.

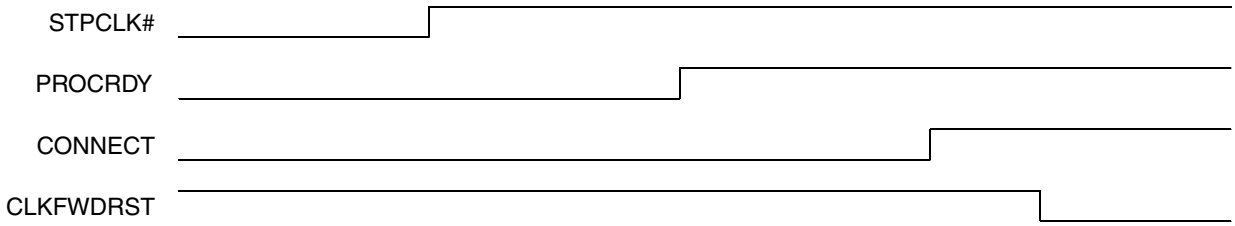
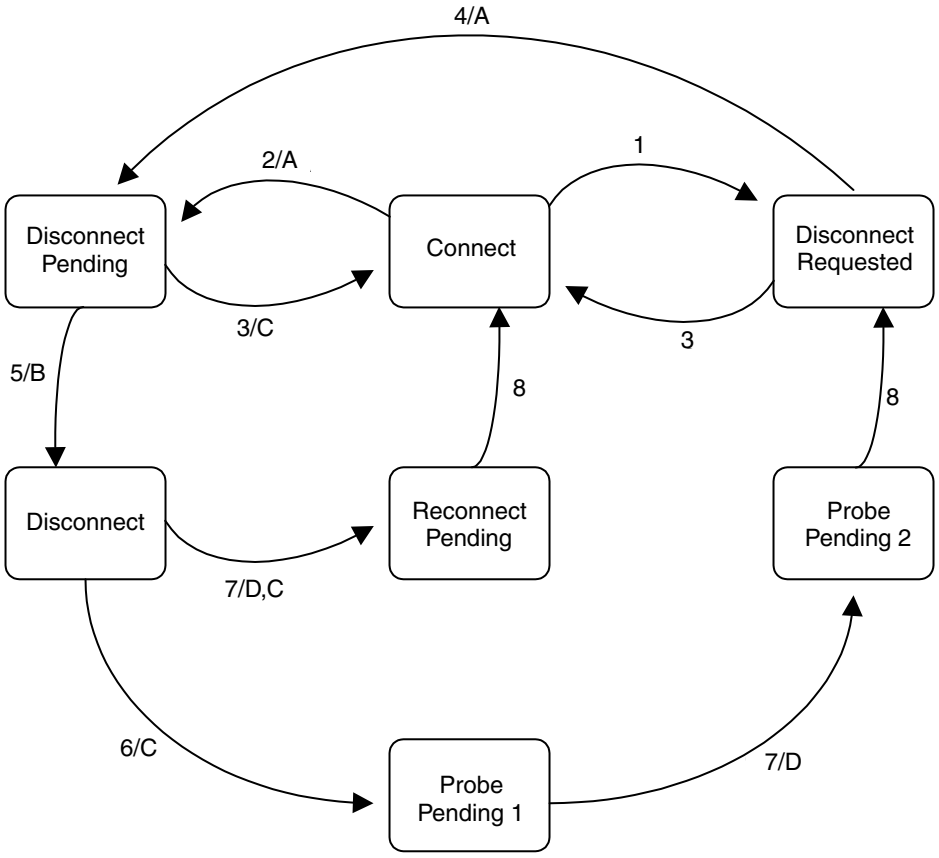


Figure 3-4. Exiting the Stop Grant State and Bus Connect Sequence

3.2.2 Connect State Diagram

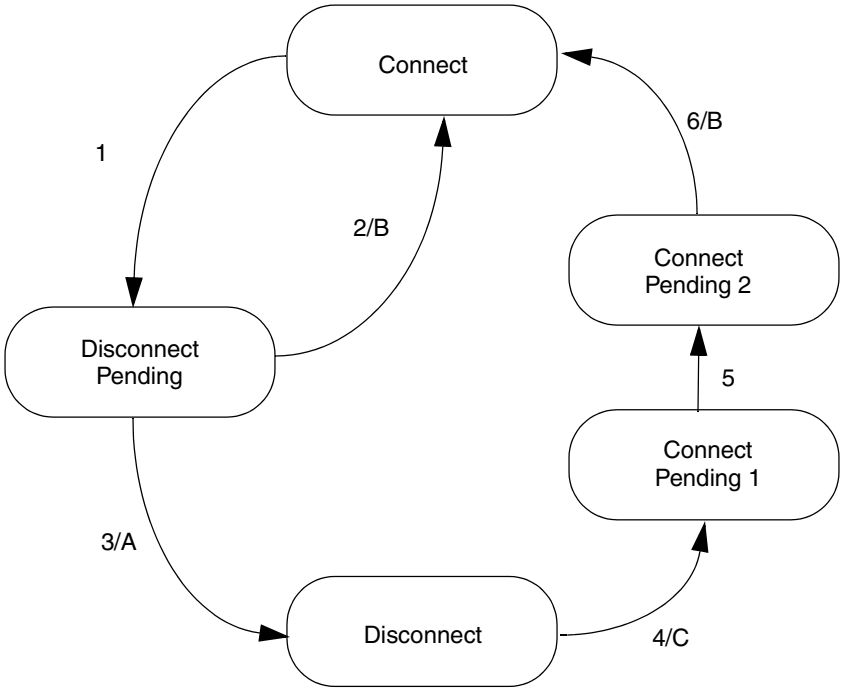
Figure 3-5 and Figure 3-6 on page 41 describe the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending.
2	A disconnect is requested and no probes are pending.
3	A Connect special cycle from the processor.
4	No probes are pending.
5	PROCRDY is de-asserted.
6	A probe needs service.
7	PROCRDY is asserted.
8	Three SYSCLK periods after CLKFWDRST is de-asserted. Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after de-asserting CLKFWDRST.

	Action
A	De-assert CONNECT eight SYSCLK periods after last SysDC sent.
B	Assert CLKFWDRST.
C	Assert CONNECT.
D	De-assert CLKFWDRST.

Figure 3-5. Northbridge Connect State Diagram



	Condition
1	CONNECT is de-asserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	De-assert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWDRST is de-asserted by the Northbridge.
6	Forward clocks start three SYSCLK periods after CLKFWDRST is de-asserted.

	Action
A	CLKFWDRST is asserted by the Northbridge.
B	Issue a Connect special cycle. (Note 1)
C	Return internal clocks to full speed and assert PROCRDY.

Note 1. The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# de-assertion) occurs. If the AMD processor system bus is connected so the Northbridge can probe the processor, a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).

Figure 3-6. Processor Connect State Diagram

3.3 Clock Control

The processor implements a Clock Control (CLK_CTL) MSR (MSR C001_001Bh) that determines the internal clock divisor when the AMD processor system bus is disconnected.

Refer to the *AMD Geode™ NX Processors BIOS Considerations Application Note* (publication ID 32483) and the BIOS Requirements for *BIOS Requirements for AMD PowerNow™ Technology Application Note* (publication ID 25264) for more details on the CLK_CTL register.

3.4 SYSCLK Multipliers

The processor provides two mechanisms for communicating processor core operating frequency information to the Northbridge. These are the processor FID[3:0] outputs and the FID_Change special cycle. The FID[3:0] outputs specify the core frequency of the processor as a multiple of the input clock (SYSCLK/SYSCLK#) of the processor. This processor supports an input clock, or Front Side Bus (FSB), that runs up to 133 MHz.

The FID[3:0] signals are valid after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. The FID[3:0] outputs of the processor provide processor operating frequency information the Northbridge uses when creating the SIP stream the Northbridge sends to the processor after RESET# is de-asserted. The FID[3:0] outputs always select a 6x SYSCLK multiplier for the Geode NX processor: FID[3:0] = 0110.

Software uses the FID_Change protocol to transition the processor to the desired performance state.

The FID[3:0] outputs are not used as part of the FID_Change protocol and do not change from their RESET# value during software-controlled processor core frequency transitions.

The FID_Change special cycle is used to communicate processor operating frequency information to the Northbridge during software-controlled processor core voltage and frequency (performance state) transitions. The FidVidCtl MSR (MSR C001_0041h) allows software to specify a 5-bit FID value during software-controlled processor performance state transitions. The additional bit allows transitions to lower SYSCLK multipliers of 3x and 4x as well as all other SYSCLK multipliers supported by the processor.

For a description of the FID_Change protocol refer Section 3.1.5 on page 35.

Table 3-1 lists the FID[4:0] SYSCLK multiplier codes for the processor used by software to dictate the core frequency of the processor and the 5-bit value driven on SDATA[36:32]# by the processor during the FID_Change special bus cycle.

Note: Only clock multipliers associated with operating frequencies specified in Section 5.0 "Electrical Specifications" on page 47 are valid for this processor. Software distinguishes the speed grade of the processor by reading the MFID field of the FidVidStatus MSR (MSR C001_0042h).

Table 3-1. FID[4:0] SYSCLK Multiplier Combinations (Note 1)

FID[4:0] (Note 2, Note 3, Note 4)	Clock Mode	SDATA[36:32]# (Note 5)	FID[4:0] (Note 2, Note 3, Note 4)	Clock Mode	SDATA[36:32]# (Note 5)
00000	11x	11111	10000	3x	01111
00001	11.5x	11110	10001	Reserved	Reserved
00010	12x	11101	10010	4x	01101
00011	12.5x	11100	10011	Reserved	Reserved
00100	5x	11011	10100	13x	11100
00101	5.5x	11010	10101	13.5x	11100
00110	6x	11001	10110	14x	11100
00111	6.5x	11000	10111	Reserved	Reserved
01000	7x	10111	11000	15x	11100
01001	7.5x	10110	11001	Reserved	Reserved
01010	8x	10101	11010	16x	11100
01011	8.5x	10100	11011	16.5x	11100
01100	9x	10011	11100	17x	11100
01101	9.5x	10010	11101	18x	11100
01110	10x	10001	11110	Reserved	Reserved
01111	10.5x	10000	11111	Reserved	Reserved

Note 1. On power up, the FID[3:0] pins are set to a clock multiplier value of 6x for the NX 1750@14W and NX 1500@6W processors* and 5x for the NX 1250@6W processor*. After reset, software is responsible for transitioning the processor to the desired frequency.

Note 2. Value programmed into the FidVidCtl MSR (MSR C001_0041h).

Note 3. The maximum FID that may be selected by software is reported in the FidVidStatus MSR (MSR C001_0042h).

Note 4. BIOS initializes the CLK_Ctl MSR (MSR C001_001Bh) during the POST routine to the desired value. The CPU ID and implemented features such as PowerNow! and S2K Bus Disconnect have implications to the appropriate value for this register. Refer to the *AMD Geode™ NX Processors BIOS Considerations Application Note* (publication ID 32483) and the BIOS Requirements for *BIOS Requirements for AMD PowerNow™ Technology Application Note* (publication ID 25264) for more details on the CLK_Ctl register.

Note 5. Value driven on SDATA[36:32]# pins during the FID_Change special bus cycle. The SDATA bus is active Low, so the SDATA[36:32]# values listed are what would be observed on the circuit board with a digital storage scope.

*The AMD Geode NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

3.5 Special Cycles

In addition to the special cycles documented in the *AMD Athlon™ Processor System Bus Specification* (publication ID 21902) the processor supports the SMM Enter, SMM Exit, and FID_Change special cycles.

Table 3-2 defines the contents of SDATA[31:0] during the special cycles.

Table 3-2. Processor Special Cycle Definition

Special Cycle	Contents of SDATA[31:0]
SMM Enter	0005_0002h
SMM Exit	0006_0002h
FID_Change (Note 1)	0007_0002h

Note 1. The new FID[4:0] taken from the FID[4:0] field of the FidVidCtl MSR (MSR C001_0041h) is driven on SDATA[36:32] during the FID_Change special cycle.

4 CPUID Support

The CPUID for the AMD Geode™ NX processors is 681. The processor version and feature set recognition can be performed through the use of the CPUID instruction that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction see:

- *AMD Athlon™ and AMD Duron™ Processor Recognition Application Note Addendum* (publication ID 21922)
- *AMD Processor Recognition Application Note* (publication ID 20734)

5 Electrical Specifications

This section provides information on electrical connections, absolute maximum ratings, and DC/AC characteristics for the AMD Geode™ NX processor. All current specified as being sourced by the processor is *negative*. All current specified as being sunk by the processor is *positive*.

5.1 Electrical Connections

5.1.1 NC, AMD, Analog, and Key Pins

The circuit board should provide a plated hole for a NC (No Connect) pin (total of 71, see Table 2-2 "Pin Assignment - Sorted Alphabetically by Signal Name" on page 23 for pin assignments). The pin hole should not be electrically connected to anything.

The AMD Pin (pin AH6), Analog Pin (pin AJ13) and Key Pins (total of 16, see Table 2-2 "Pin Assignment - Sorted Alphabetically by Signal Name" on page 23 for pin assignments) should be treated like a NC pin.

See Section 2.3.11 "Key Pin, AMD Pin, Analog Pin and No Connect Pins" on page 31 for more details regarding these pins.

5.1.2 Decoupling

See the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) and *AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860), or contact your local AMD FAE (Field Applications Engineer) for information about the decoupling required on the circuit board for use with the Geode NX processors.

5.2 Absolute Maximum Ratings

Do not subject the processor to conditions that exceed the absolute ratings listed in Table 5-1, as such conditions may adversely affect long-term reliability or result in functional damage.

5.3 V_{CCA} Electrical Characteristics

V_{CCA} (pin AJ23) is the processor PLL supply. Table 5-2 provides the voltage and current values for the V_{CCA} pin.

Table 5-1. Absolute Ratings

Symbol	Parameter	Min	Max
V_{CC_CORE}	Processor Core Supply	–0.5V	$V_{CC\_CORE\_NOM}$ + 0.5V
V_{CCA}	Processor PLL Supply	–0.5V	V_{CCA_Max} + 0.5V
$T_{STORAGE}$	Storage Temperature of Processor	–40ºC	100ºC

Table 5-2. V_{CCA} Electrical Characteristics

Symbol	Parameter	Min	Nom	Max	Units
V_{VCCA}	V_{CCA} Voltage (Note 1)	2.25	2.5	2.75	V
				$\lvert V_{VCCA} - V_{CC\_CORE} \rvert < 1.60V$ (Note 2)	--
I_{VCCA}	V_{CCA} Current (Note 3)	0		50	mA/GHz

Note 1. Minimum and maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted.

Note 2. For more information, refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) and the *AMD Geode™ NX Processors Addendum to AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 31860)

Note 3. Measured at 2.5V.

5.4 V_{CC_CORE} Electrical Characteristics

Table 5-3 provides the electrical characteristics for V_{CC_CORE}. Figure 5-1 shows the processor core voltage (V_{CC_CORE}) waveform response to perturbation. The time t_{MAX_AC} (positive AC transient excursion time) represents the maximum allowable time above the DC tolerance threshold.

Table 5-3. V_{CC_CORE} Electrical Characteristics

Symbol	Parameter	Limit (Note 1)	Units
$V_{CC\_CORE\_AC\_MAX}$	Maximum excursion above $V_{CC\_CORE\_NOM}$ (Note 2)	150	mV
$V_{CC\_CORE\_DC\_MAX}$	Maximum static voltage above $V_{CC\_CORE\_NOM}$ (Note 2)	100	mV
$V_{CC\_CORE\_MIN}$	Minimum voltage below $V_{CC\_CORE\_NOM}$ (Note 2)	–50	mV
t_{MAX_AC}	Maximum excursion time for AC transients	10	µs

Note 1. All voltage measurements are taken differentially at the COREFB/COREFB# pins while the processor is in the working state.

Note 2. V_{CC_CORE} nominal values and absolute minimum allowable V_{CC_CORE} voltage for the Geode NX processors is provided in Table 5-4 "Voltage and Frequency Combinations" on page 49.

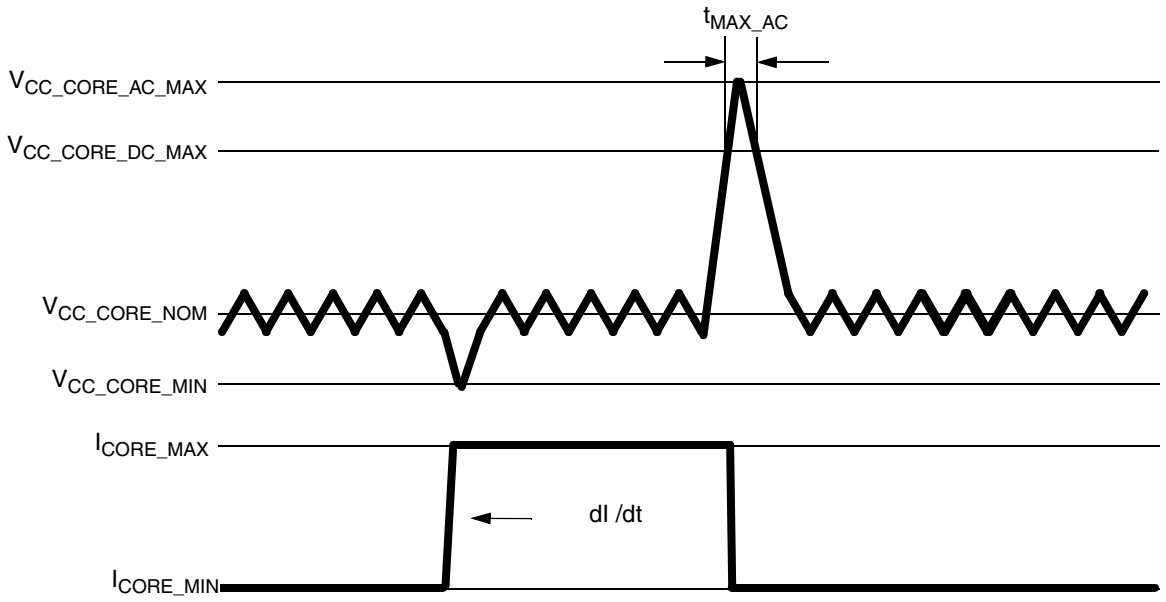


Figure 5-1. V_{CC_CORE} Voltage Waveform

5.4.1 Valid Voltage and Frequency Combinations

Table 5-4 characterizes the valid voltage and frequency combinations for the AMD Geode NX processor. The Frequency column corresponds to the rated frequency of the processor. The Maximum FID (MFID) field in the FidVid-Status MSR (MSR C001_0042h[20:16]) is used by software to determine the maximum frequency of the processor. Section 3.1 "Power Management States" on page 33 describes how AMD PowerNow!™ software uses this information to implement processor performance states

Table 5-4. Voltage and Frequency Combinations

AMD Geode™ NX Processor (Note 1)	$V_{CC\_CORE\_NOM}$ Voltage (Note 2, Note 3)	Frequency (Note 4)
NX 1250@6W Processor	1.10V (Note 5)	≤667 MHz
NX 1500@6W Processor	1.00V (Note 6)	≤1000 MHz
NX 1750@14W Processor	1.05V (Note 7)	≤1000 MHz
	1.10V	1067 MHz
	1.15V	1133 MHz
	1.20V	1200 MHz
	1.25V	1400 MHz

Note 1. The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.
Note 2. All voltages listed are nominal. See Figure 5-1 on page 48 for AC and DC transient voltage tolerances.
Note 3. The maximum processor die temperature is 95°C for all voltage and frequency combinations.
Note 4. The "≤" symbol indicates that the BIOS vendor can use any performance state equal to or less than the specified frequency at a given voltage.
Note 5. The absolute minimum voltage, inclusive of all tolerances and excursions, is 1.05V.
Note 6. The absolute minimum voltage, inclusive of all tolerances and excursions, is 0.95V.
Note 7. The absolute minimum voltage, inclusive of all tolerances and excursions, is 1.00V.

5.5 DC Characteristics

Table 5-5. SYSCLK and SYSCLK# DC Characteristics (Note 1)

Symbol	Parameter	Min	Max	Units
$V_{Threshold-DC}$	Crossing before transition is detected (DC)	400		mV
$V_{Threshold-AC}$	Crossing before transition is detected (AC)	450		mV
I_{LEAK_P}	Leakage current through P-channel pull up to V_{CC_CORE}	–250		µA
I_{LEAK_N}	Leakage current through N-channel pull down to V_{SS} (Ground)		250	µA
V_{CROSS}	Differential signal crossover		V_{CC_CORE}/2 +/– 100	mV
C_{PIN}	Capacitance (Note 2)		25	pF

Note 1. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together.)

Note 2. The SYSCLK and SYSCLK# signals have twice the listed capacitance because they connect to two input pads (i.e., CLKIN/RSTCLK and CLKIN#/RSTCLK#).

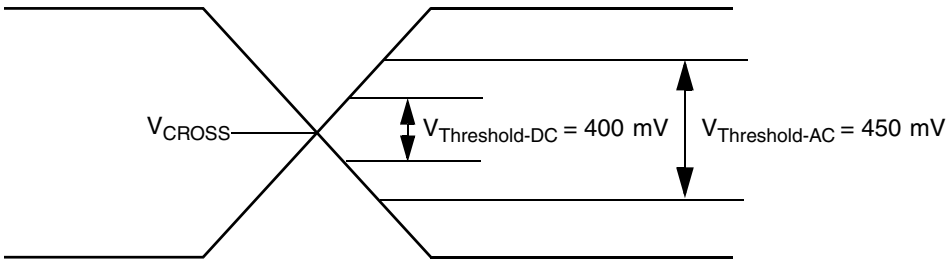


Figure 5-2. SYSCLK and SYSCLK# Differential Clock Signals

Table 5-6. SOFTVID[4:0] and VID[4:0] DC Characteristics

Symbol	Parameter	Min	Max	Units
I_{OL}	Output Current Low	6		mA
SOFTVID_V_{OH}	SOFTVID[4:0] Output High Voltage	--	2.625 (Note 1)	V
			$\lvert$ SOFTVID_V_{OH} – V_{CC_CORE} $\rvert$ < 1.60 (Note 2)	
VID_V_{OH}	VID[4:0] Output High Voltage	--	5.25 (Note 3)	V

Note 1. The SOFTVID pins must not be pulled above 2.625V, which is 2.5V +5%.
Note 2. Refer to the "VCC_2.5V Generation Circuit" found in the "Motherboard Required Circuits," section of the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363).
Note 3. The VID pins are either open circuit or pulled to ground. It is recommended that these pins are not pulled above 5.25V, which is 5.0V +5%.

.

Table 5-7. FID[3:0] DC Characteristics

Symbol	Parameter	Min	Max	Units
I_{OL}	Output Current Low	6		mA
V_{OH}	Output High Voltage	--	2.625 (Note 1)	V
			$\lvert V_{OH} - V_{CC\_CORE} \rvert$ < 1.60V (Note 2)	

Note 1. The FID[3:0] pins must not be pulled above 2.625V, which is 2.5V +5%.
Note 2. Refer to the "VCC_2.5V Generation Circuit" found in the "Motherboard Required Circuits" section of the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363).

Table 5-8. PICD[1:0]# and PICCLK (APIC Pins) DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	Input High Voltage (Note 1)		1.7	2.625 (Note 2)	V
		$V_{CC\_CORE} < V_{CC\_CORE\_MAX}$		$\lvert V_{IH} - V_{CC\_CORE} \rvert \leq 1.60V$ (Note 3)	
V_{IL}	Input Low Voltage (Note 1)		-300	700	mV
V_{OH}	Output High Voltage			2.625 (Note 2)	V
		$V_{CC\_CORE} < V_{CC\_CORE\_MAX}$		$\lvert V_{OH} - V_{CC\_CORE} \rvert \leq 1.60V$ (Note 3)	
V_{OL}	Output Low Voltage		-300	400	mV
$\lvert_{LEAK\_P}$	TRI-STATE Leakage Pull-up	$V_{IN} = V_{SS}$ (Ground)	-1		mA
$\lvert_{LEAK\_N}$	TRI-STATE Leakage Pull-down	$V_{IN} = 2.5V$		1	mA
I_{OL}	Output Low Current	V_{OL} Max	9		mA
C_{PIN}	Pin Capacitance		4	12	pF

Note 1. Characterized across DC supply voltage range.
Note 2. The 2.625V value is equal to 2.5V +5%.
Note 3. Refer to VCC_2.5V Generation Circuit found in the Motherboard Required Circuits, of the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363).

Table 5-9. AMD Processor System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{REF}	DC Input Reference Voltage (Note 1)		$(0.5 \times V_{CC\_CORE}) - 50$	$(0.5 \times V_{CC\_CORE}) + 50$	mV
$I_{VREF\_LEAK\_P}$	V_{REF} TRI-STATE Leakage Pull-up	$V_{IN} = V_{REF}$ Nominal	–100		µA
$I_{VREF\_LEAK\_N}$	V_{REF} TRI-STATE Leakage Pull-down	$V_{IN} = V_{REF}$ Nominal		100	µA
V_{IH}	Input High Voltage	$1.20V \leq V_{CC\_CORE}$ (Note 2)	$V_{REF} + 200$	$V_{CC\_CORE} + 500$	mV
		$V_{CC\_CORE} < 1.20V$ (Note 2)	$V_{REF} + 100$	$V_{CC\_CORE} + 500$	mV
V_{IL}	Input Low Voltage	$1.20V \leq V_{CC\_CORE}$ (Note 2)	–300	$V_{REF} - 200$	mV
		$V_{CC\_CORE} < 1.20V$ (Note 2)	–300	$V_{REF} - 100$	mV
I_{LEAK_P}	TRI-STATE Leakage Pull-up	$V_{IN} = V_{SS}$ (Ground)	–250		µA
I_{LEAK_N}	TRI-STATE Leakage Pull-down	$V_{IN} = V_{CC\_CORE}$ Nominal		250	µA
C_{IN}	Input Pin Capacitance			7	pF
R_{ON}	Output Resistance (Note 3)		$0.90 \times R_{setN,P}$	$1.1 \times R_{setN,P}$	Ω
R_{setP}	Impedance Set Point, P Channel (Note 3)		40	70	Ω
R_{setN}	Impedance Set Point, N Channel (Note 3)		40	70	Ω

Note 1. V_{REF} is nominally set to 50% of V_{CC_CORE} with actual values that are specific to circuit board design implementation. V_{REF} must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the ±50 mV specification listed above.

Note 2. The selection of a 1.2V break in the V_{IH} and V_{IL} parameters is somewhat arbitrary, reflecting the need for tighter tolerances at lower voltage to maintain noise margin.

Note 3. Measured at $V_{CC\_CORE}/2$.

Table 5-10. General DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	Input High Voltage (Note 1) (Note 2) (Note 3)	$1.2V \le V_{CC\_CORE}$	$0.5 \times V_{CC\_CORE} + 200$	$V_{CC\_CORE} + 300$	mV
		$V_{CC\_CORE} < 1.20V$	$0.5 \times V_{CC\_CORE} + 100$	$V_{CC\_CORE} + 300$	mV
V_{IL}	Input Low Voltage (Note 1) (Note 2) (Note 3)	$1.2V \le V_{CC\_CORE}$	–300	$0.5 \times V_{CC\_CORE} - 200$	mV
		$V_{CC\_CORE} < 1.20V$	–300	$0.5 \times V_{CC\_CORE} - 100$	mV
V_{OH}	Output High Voltage (Note 3)		$V_{CC\_CORE} - 200$	$V_{CC\_CORE} + 300$	mV
V_{OL}	Output Low Voltage (Note 3)		–300	200	mV
I_{LEAK_P}	TRI-STATE Leakage Pull-up	$V_{IN} = V_{SS}$ (Ground)	–250		µA
I_{LEAK_N}	TRI-STATE Leakage Pull-down	$V_{IN} = V_{CC\_CORE}$ Nominal		250	µA
I_{OH}	Output High Current (Note 4)			–6	mA
I_{OL}	Output Low Current (Note 5)		6		mA
C_{PIN}	Pin Capacitance			12	pF

Note 1. Characterized across DC supply voltage range.
Note 2. The selection of a 1.2V break in the V_{IH} and V_{IL} parameters is somewhat arbitrary, reflecting the need for tighter tolerances at lower voltages to maintain noise margin.
Note 3. Values specified at nominal V_{CC_CORE}. Scale parameters between $V_{CC\_CORE\_MIN}$ and $V_{CC\_CORE\_MAX}$.
Note 4. I_{OL} and I_{OH} are measured at V_{OL} maximum and V_{OH} minimum, respectively.
Note 5. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.

5.6 AC Characteristics

Table 5-11. SYSCLK and SYSCLK# AC Characteristics

Symbol	Parameter	Min @		Max @		Units
	Clock Frequency	50	133	50	133	MHz
	Duty Cycle	30%	30%	70%	70%	
t_1	Period (Note 1) (Note 2)	10	7.5			ns
t_2	High Time	1.8	1.05			ns
t_3	Low Time	1.8	1.05			ns
t_4	Fall Time			2	2	ns
t_5	Rise Time			2	2	ns
	Period Stability			± 300	± 300	ps

Note 1. Circuitry driving the AMD processor system bus clock inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20 dB attenuation point, as measured into a 10 or 20 pF load must be less than 500 kHz.

Note 2. Circuitry driving the AMD processor system bus clock inputs may purposely alter the AMD processor system bus clock frequency (spread spectrum clock generators). In no cases can the AMD processor system bus period violate the minimum specification above. AMD processor system bus clock inputs can vary from 100% of the specified frequency to 99% of the specified frequency at a maximum rate of 100 kHz.

Figure 5-3 shows a sample waveform.

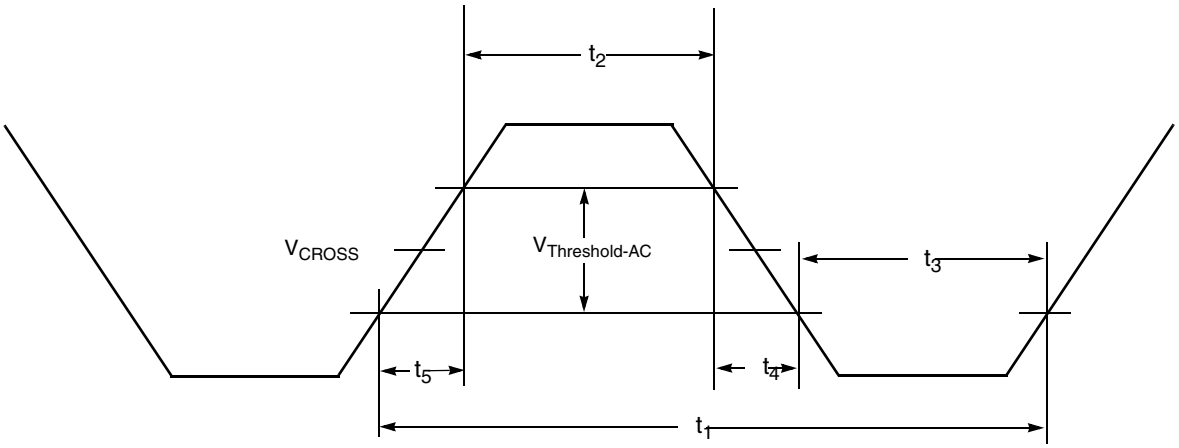


Figure 5-3. SYSCLK Waveform

Table 5-12. PICD[1:0]# and PICCLK (APIC Pins) AC Characteristics

Symbol	Parameter	Min	Max	Units
T_{RISE}	Signal Rise Time (Note 1)	1.0	3.0	V/ns
T_{FALL}	Signal Fall Time (Note 1)	1.0	3.0	V/ns
T_{SU}	Setup Time	1		ns
T_{HD}	Hold Time	1		ns

Note 1. Edge rates indicate the range for characterizing the inputs.

Table 5-13. AMD Processor System Bus AC Characteristics

Group Note 1	Symbol	Parameter	Min	Max	Units
All Signals (Note 2)	T_{RISE}	Output Rise Slew Rate	1	3	V/ns
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns
Forward Clocks	$T_{SKEW-DIFFEDGE}$ (Note 3)	Output skew with respect to a different clock edge	–	770	ps
	T_{SU} (Note 4)	Input Data Setup Time	300		ps
	T_{HD} (Note 4)	Input Data Hold Time	300		ps
	C_{IN}	Capacitance on input clocks	3	7	pF
	C_{OUT}	Capacitance on output clocks	4	7	pF
Sync	T_{VAL} (Note 5) (Note 6)	RSTCLK to Output Valid	250	2000	ps
	T_{SU} (Note 5) (Note 7)	Setup to RSTCLK	500		ps
	T_{HD} (Note 5) (Note 7)	Hold from RSTCLK	1000		ps

Note 1. The parameters are grouped based on the source or destination of the signals involved.
Note 2. Rise and fall time ranges are guidelines over which the I/O has been characterized.
Note 3. $T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
Note 4. Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.
Note 5. The synchronous signals include PROCRDY, CONNECT, and CLKFWDRST.
Note 6. T_{VAL} is RSTCLK rising edge to output valid for PROCRDY. Measure the signal at the receiver end of a 50 ohm trace. Subtract the delay effect of the transmission line.
Note 7. T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.

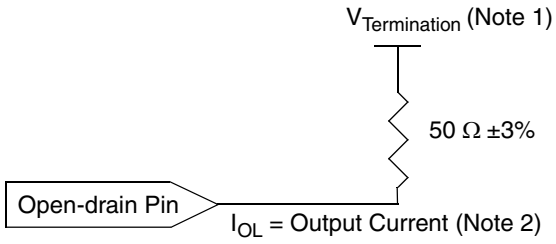
Table 5-14. General AC Characteristics

Symbol	Parameter	Min	Max	Units
T_{SU}	Sync Input Setup Time (Note 1) (Note 2)	2.0		ns
T_{HD}	Sync Input Hold Time (Note 1) (Note 2)	0.0		ps
T_{DELAY}	Output Delay with respect to RSTCLK (Note 2)	0.0	6.1	ns
T_{BIT}	Input Time to Acquire (Note 3) (Note 4)	20.0		ns
T_{RPT}	Input Time to Reacquire (Note 5) (Note 6) (Note 7) (Note 8)	40.0		ns
T_{RISE}	Signal Rise Time (Note 9)	1.0	3.0	V/ns
T_{FALL}	Signal Fall Time (Note 9)	1.0	3.0	V/ns
T_{VALID}	Time to Data Valid (Note 10)		100	ns

Note 1. These are aggregate numbers.
Note 2. Edge rates indicate the range over which inputs were characterized.
Note 3. This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2 x f_{RST}.
Note 4. The approximate value for standard case in normal mode operation.
Note 5. This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.
Note 6. Re-assertions of the signal within this time are not guaranteed to be seen by the core.
Note 7. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
Note 8. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.
Note 9. In asynchronous operation, the signal must persist for this time to enable capture.
Note 10. Time to valid is for any open-drain pins. See requirements 7 and 8 of Section 5.10.1.1 "Signal Sequence and Timing Description" on page 61 for more information.

5.7 Open-Drain Test Circuit

Figure 5-4 is a test circuit that may be used on automated test equipment (ATE) to test for validity on open-drain pins.



Note 1. $V_{Termination}$ = 1.2 V for VID and FID pins
$V_{Termination}$ = 1.0 V for APIC pins

Note 2. I_{OL} = –6 mA for VID and FID pins
I_{OL} = –9 mA for APIC pins

Figure 5-4. General ATE Open-Drain Test Circuit

5.8 FID_Change Induced PLL Lock Time

Table 5-15 shows the time required for the PLL of the processor to lock at the new frequency specified in a FID_Change transition.

Software must program the SGTC field of the FidVidCtl MSR (MSR C001_0041h) to produce a FID_Change duration equal to or greater than the FID_Change induced PLL lock time.

For more information about the FID_Change protocol, see Section 3.1 "Power Management States" on page 33.

Table 5-15. FID_Change Induced PLL Lock Time

Parameter	Max	Units
FID_Change Induced PLL Lock Time	50	µs

5.9 Thermal Diode Characteristics

The AMD Geode™ NX processor provides a diode that can be used in conjunction with an external temperature sensor to determine the die temperature of the processor. The diode anode (THERMDA) and cathode (THERMDC) are available as pins on the processor. Refer to Section 2.3.8 "Thermal Diode Interface Signals" on page 28 for more details.

5.9.1 Thermal Diode Electrical Characteristics

Table 5-16 shows the processor electrical characteristics of the on-die thermal diode.

5.9.2 Thermal Protection Characterization

The following section describes parameters relating to thermal protection. The implementation of thermal control circuitry to control processor temperature is left to the manufacturer to determine how to implement.

Thermal limits in circuit board design are necessary to protect the processor from thermal damage. $T_{SHUTDOWN}$ is the temperature for thermal protection circuitry to initiate shutdown of the processor. T_{SD_DELAY} is the maximum time allowed from the detection of the over-temperature condition to processor shutdown to prevent thermal damage to the processor.

Systems that do not implement thermal protection circuitry or that do not react within the time specified by T_{SD_DELAY} can cause thermal damage to the processor during a fan failure or if the processor is powered up without a heatsink. The processor relies on thermal circuitry on the circuit board to turn off the regulated core voltage to the processor in response to a thermal shutdown event.

Thermal protection circuitry reference designs and thermal solution guidelines are found in the following documents:

- *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363)
- *AMD Thermal, Mechanical, and Chassis Cooling Design Guide* (publication ID 23794)

Table 5-17 shows the $T_{SHUTDOWN}$ and T_{SD_DELAY} specifications necessary for circuitry in circuit board design for thermal protection of the processor.

Table 5-16. Thermal Diode Electrical Characteristics

Symbol	Parameter	Min	Nom	Max	Units
I	Sourcing current (Note 1)	5		300	µA
$n_{f, lumped}$	Lumped ideality factor (Note 2) (Note 3) (Note 4)	1.00000	1.00374	1.00900	
$n_{f, actual}$	Actual ideality factor (Note 3) (Note 4)		1.00261		
R_T	Series Resistance (Note 3) (Note 4)		0.93		ohms

Note 1. The sourcing current should always be used in forward bias only.
Note 2. Characterized at 95°C with a forward bias current pair of 10 µA and 100 µA. AMD recommends using a minimum of two sourcing currents to accurately measure the temperature of the thermal diode.
Note 3. Not 100% tested. Specified by design and limited characterization.
Note 4. The lumped ideality factor adds the effect of the series resistance term to the actual ideality factor. The series resistance term indicates the resistance from the pins of the processor to the on-die thermal diode. The value of the lumped ideality factor depends on the sourcing current pair used.

Table 5-17. Guidelines for Platform Thermal Protection of the Processor

Symbol	Parameter (Note 1) (Note 2) (Note 3)	Max	Units
$T_{SHUTDOWN}$	Thermal diode shutdown temperature for processor protection	125	°C
T_{SD_DELAY}	Maximum allowed time from $T_{SHUTDOWN}$ detection to processor shutdown	500	ms

Note 1. The thermal diode is not 100% tested, it is specified by design and limited characterization.
Note 2. The thermal diode is capable of responding to thermal events of 40°C/s or faster.
Note 3. The Geode NX processor provides a thermal diode for measuring die temperature of the processor. The processor relies on thermal circuitry on the circuit board to turn off the regulated core voltage to the processor in response to a thermal shutdown event. Refer to *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) for thermal protection circuitry designs.

5.9.3 Part-Specific Thermal Power Performance Specifications

The tables in this section specify the part-specific thermal power performance specifications for the Geode NX processor. This includes the nominal DC operating voltage of the processor core in the C0 Working state and the Stop Grant state.

Table 5-18. Thermal Power Performance Specifications

Frequency in MHz	V_{CC_CORE} (Core Voltage)	Thermal Power Max		Maximum Die Temperature
		Working State C0 (Note 1)	Stop Grant C3/S1 (Note 1) (Note 2)	
AMD Geode™ NX 1250@6W Processor (Note 3)				
667	1.10V	9.0W (Note 4) (6.0W typical)	3.0W	95°C
AMD Geode™ NX 1500@6W Processor (Note 3)				
1000	1.00V	9.0W (Note 4) (6.0W typical)	3.0W	95°C
AMD Geode™ NX 1750@14W Processor (Note 3)				
1400	1.25V	25.0W (Note 4) (14.0W typical)	3.0W	95°C

Note 1. See Figure Figure 3-1 "Processor Power Management States" on page 33.

Note 2. Power measurements are at 500 MHz and 1.05V.The AMD processor system bus is disconnected and has a low power ratio of 1/64 for Stop Grant disconnect and a low power ratio of 1/64 Halt disconnect applied to the core clock grid of the processor.

Note 3. The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

Note 4. Thermal design power represents the maximum sustained power dissipated while executing publicly-available software or instruction sequences under normal system operation at nominal V_{CC_CORE}. Thermal solutions must monitor the temperature of the processor to prevent the processor from exceeding its maximum die temperature.

5.10 Signal and Power-Up Requirements

This chapter describes the AMD Geode™ NX processor's power-up requirements during system power-up and warm resets.

5.10.1 Power-Up Requirements

5.10.1.1 Signal Sequence and Timing Description

Figure 5-5 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

Note: Figure 5-5 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.

The signal timing requirements for Figure 5-5 are as follows:

1) RESET# must be asserted before PWROK is asserted.

   The Geode NX processor does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 ns** prior to the assertion of PWROK.

   In practice, a Southbridge asserts RESET# milliseconds before PWROK is asserted.

2) All circuit board voltage planes must be within specification before PWROK is asserted.

   PWROK is an output of the voltage regulation circuit on the circuit board. PWROK indicates that V_{CC_CORE} and all other voltage planes in the system are within specification.

   The circuit board is required to delay PWROK assertion for a minimum of three milliseconds from the 3.3V supply being within specification. This delay ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

   The processor core voltage, V_{CC_CORE}, must be within specification before PWROK is asserted as dictated by the VID[4:0] pins strapped on the processor package. Before PWROK assertion, the processor is clocked by a ring oscillator. Before PWROK is asserted, the SOFTVID[4:0] outputs of the processor are not driven to a deterministic value. The processor drives the SOFTVID[4:0] outputs to the same value as dictated by the VID[4:0] pins within 20 ns of PWROK assertion.

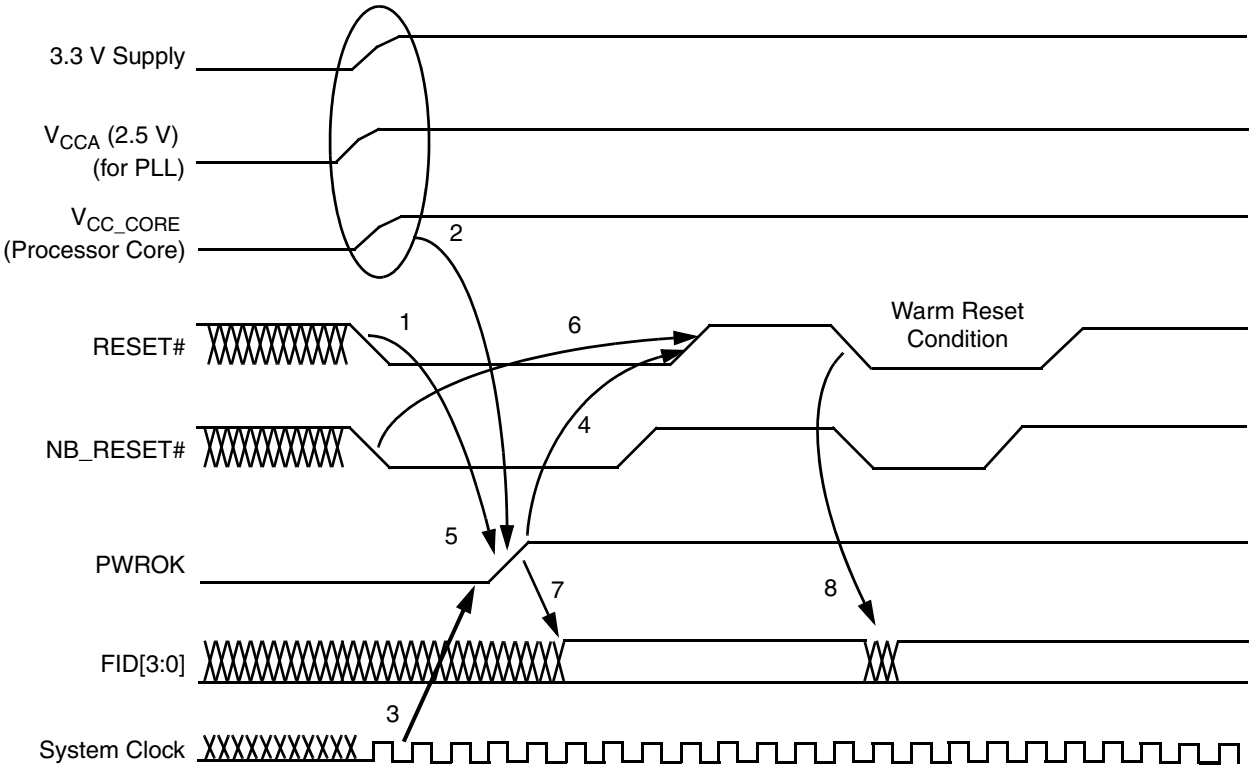


Figure 5-5. Signal Relationship Requirements During Power-Up Sequence

The processor PLL is powered by V_{CCA}. The processor PLL does not lock if V_{CCA} is not high enough for the processor logic to switch for some period before PWROK is asserted. V_{CCA} must be within specification at least 5 µs before PWROK is asserted.

In practice V_{CCA}, V_{CC_CORE}, and all other voltage planes must be within specification for several milliseconds before PWROK is asserted.

After PWROK is asserted, the processor PLL locks to its operational frequency.

3) The system clock (SYSCLK/SYSCLK#) must be running before PWROK is asserted.

   When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock must be valid at this time. The system clocks are designed to be running after 3.3V has been within specification for 3 ms.

4) PWROK assertion to de-assertion of RESET#.

   The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1 ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the de-assertion of RESET# be at least **1.0 ms**. Southbridge enforces a delay of 1.5 to 2.0 ms between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# de-assertion.

5) PWROK must be monotonic and meet the timing requirements as defined in Table 5-14 "General AC Characteristics" on page 57. The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6) NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is de-asserted. In practice all Southbridge enforces this requirement.

   If NB_RESET# does not assert until after RESET# has de-asserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP (Serial Initialization Packet) transfer. There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is de-asserted.

7) The FID[3:0] signals are valid within 100 ns after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) for the specific implementation and additional circuitry required.

8) The FID[3:0] signals become valid within 100 ns after RESET# is asserted. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363) for the specific implementation and additional circuitry required.

5.10.1.2 Clock Multiplier Selection (FID[3:0])

The chipset samples the FID[3:0] signals in a chipset-specific manner from the processor and uses this information to determine the correct SIP. The chipset then sends the SIP information to the processor for configuration of the AMD processor system bus for the clock multiplier that determines the processor frequency indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, that are synchronous to SYSCLK.

For more information, see Section 2.3.7 "Frequency ID Interface Signals" on page 28.

5.10.1.3 Serial Initialization Packet (SIP) Protocol

Refer to *AMD Athlon™ Processor System Bus Specification* (publication ID 21902) for details of the SIP protocol.

5.10.2 Processor Warm Reset Requirements

Processor and Northbridge Reset Pins

RESET# cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same as PCI RESET#. The minimum assertion for PCI RESET# is 1 ms. Southbridge enforces a minimum assertion of RESET# for the processor, Northbridge, and PCI of 1.5 to 2.0 ms.

6 Mechanical Data

The AMD Geode™ NX processor connects to the motherboard through a Pin Grid Array (PGA) socket named Socket A. This processor utilizes the organic pin grid array (OPGA) package type described in this chapter. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide* (publication ID 24363).

6.1 Die Loading

The processor die on the OPGA package is exposed at the top of the package. This feature facilitates heat transfer from the die to an approved heat sink. Any heat sink design should avoid loads on corners and edges of die. The OPGA package has compliant pads that serve to bring surfaces in planar contact. Tool-assisted zero insertion force sockets should be designed so that no load is placed on the substrate of the package.

Table 6-1 shows the mechanical loading specifications for the processor die. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 6-1.

Table 6-1. Mechanical Loading

Location	Dynamic (Max)	Static (Max)	Units
Die Surface (Note 1)	100	30	lbf
Die Edge (Note 2)	10	10	lbf

Note 1. Load specified for coplanar contact to die surface.
Note 2. Load defined for a surface at no more than a two-degree angle of inclination to die surface.

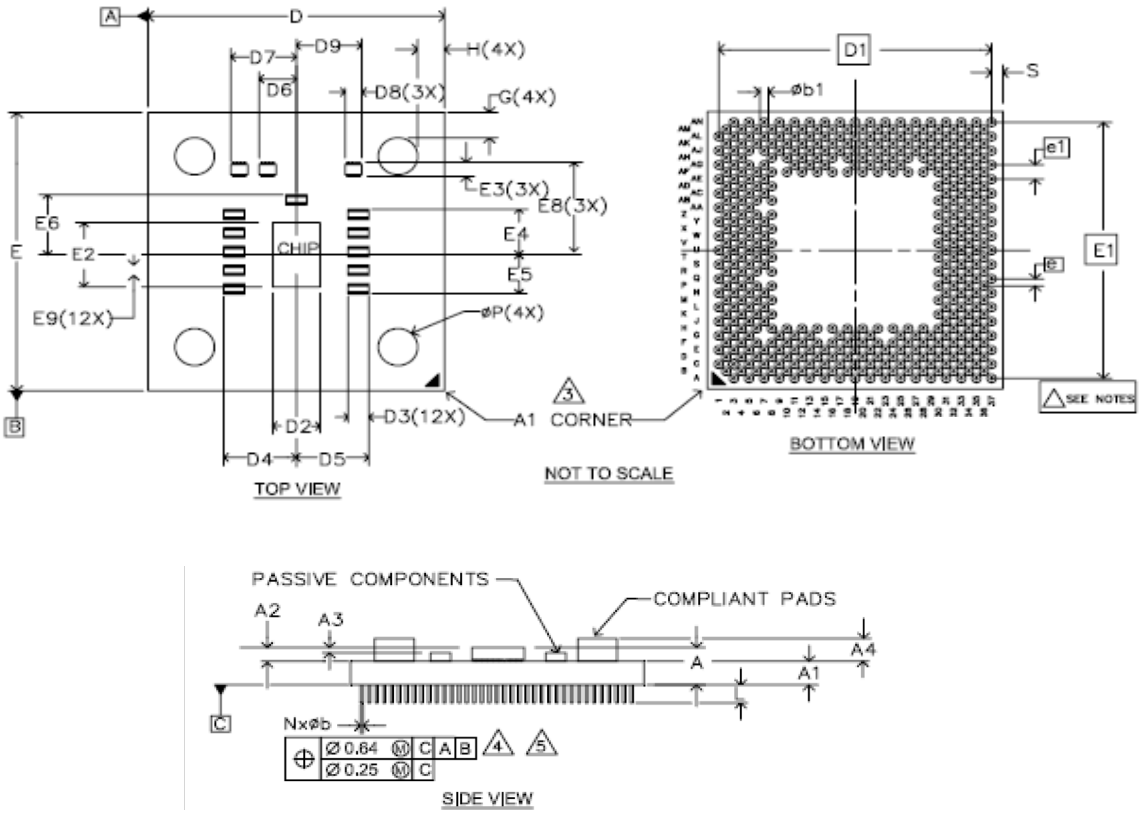
6.2 OPGA Package Descriptions

Table 6-2 shows the part number 28104 OPGA package dimensions in millimeters assigned to the letters and symbols used in the package diagram, Figure 6-1 on page 64.

Table 6-2. 28104 OPGA Package Dimensions

Letter or Symbol	Min Dimension (Note 1)	Max Dimension (Note 1)	Letter or Symbol	Min Dimension (Note 1)	Max Dimension (Note 1)
D/E	49.27	49.78	G/H	–	4.50
D1/E1	45.72 BSC		A	1.917 REF	
D2	7.47 REF		A1	0.977	1.177
D3	3.30	3.60	A2	0.80	0.88
D4	10.78	11.33	A3	0.116	–
D5	10.78	11.33	A4	–	1.90
D6	8.13	8.68	ϕP	–	6.60
D7	12.33	12.88	ϕb	0.43	0.50
D8	3.05	3.35	ϕb1	1.40 REF	
D9	12.71	13.26	S	1.435	2.375
E2	11.33 REF		L	3.05	3.31
E3	2.35	2.65	M	37	
E4	7.87	8.42	N	453	
E5	7.87	8.42	e	1.27 BSC	
E6	10.73	11.28	e1	2.54 BSC	
E8	13.28	13.83	Mass (Note 2)	11.0 g REF	
E9	1.66	1.96			

Note 1. Dimensions are given in millimeters.
Note 2. The mass consists of the completed package, including processor, surface mounted parts, and pins.



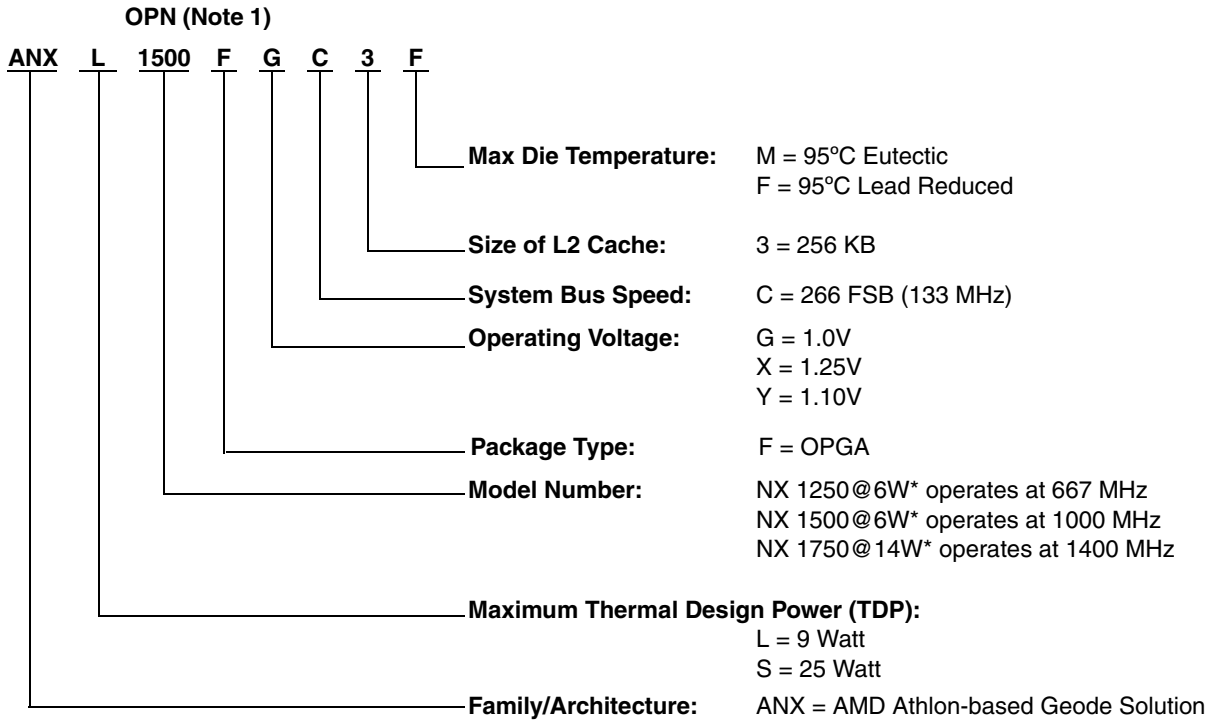
GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner is marked with a triangle on both sides of the package identifies pin A1 corner and can be used for handling and orientation purposes.
4. Pin tips should have radius.
5. Symbol "M" determines pin matrix size and "N" is number of pins.
6. "x" in front of package variation denotes non-qualified package per AMD 01-002.3.
7. The following features are not shown on drawings:
   a) Marking on die, label on package
   b) Laser elements
   c) Die and passive fiducials
8. The die is centered on the package.

Figure 6-1. 28104 OPGA Package Outline

7 Ordering Information

Ordering information for the AMD Geode™ NX processor is contained in this section. The ordering part number (OPN) is formed by a combination of the elements shown in Figure 7-1 below. ***This OPN is given as an example only.***



Note 1. Spaces are added to the ordering number shown above for viewing clarity only.

Figure 7-1. OPN for the AMD Geode™ NX Processors

Table 7-1. Valid OPN Combinations

Family/Architecture	Base Model No.	FSB/Cache	Max Die Temperature
ANX	L1250FY	C3	M
	L1500FG		
	S1750FX		
ANX	L1250FY	C3	F
	L1500FG		
	S1750FX		
Note: Consult your local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations possibly not listed.			

*The AMD Geode™ NX 1750@14W processor operates at 1.4 GHz, the NX 1500@6W processor operates at 1.0 GHz, and the NX 1250@6W processor operates at 667 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodenxbenchmark.

A Supporting Documentation

A.1 Thermal Diode Calculations

This section contains information about the calculations for the on-die thermal diode of the AMD Geode™ NX processor. For electrical information about this thermal diode, see Table 5-16 "Thermal Diode Electrical Characteristics" on page 59.

A.1.1 Ideal Diode Equation

The ideal diode equation uses the variables and constants defined in Table A-1.

Table A-1. Constants and Variables for the Ideal Diode Equation

Equation Symbol	Variable, Constant Description
$n_{f, lumped}$	Lumped ideality factor
k	Boltzmann constant
q	Electron charge constant
T	Diode temperature (Kelvin)
V_{BE}	Voltage from base to emitter
I_C	Collector current
I_S	Saturation current

Equation 1 shows the ideal diode calculation.

$$V_{BE} = n_{f,\,lumped} \cdot \frac{k}{q} \cdot T \cdot \ln\left(\frac{I_C}{I_S}\right)$$

Equation 1.

Sourcing two currents and using Equation 1 derives the difference in the base-to-emitter voltage that leads to finding the diode temperature as shown in Equation 2. The use of dual sourcing currents allows the measurement of the thermal diode temperature to be more accurate and less susceptible to die and process revisions. Temperature sensors that utilize series resistance cancellation can use more than two sourcing currents and are suitable to be used with the AMD thermal diode. Equation 2 is the formula for calculating the temperature of a thermal diode.

$$T = \frac{V_{BE,\,high} - V_{BE,\,low}}{n_{f,\,lumped} \cdot \frac{k}{q} \cdot \ln\left(\frac{I_{high}}{I_{low}}\right)}$$

Equation 2.

A.1.2 Temperature Offset Correction

A temperature offset may be required to correct the value measured by a temperature sensor. An offset is necessary if a difference exists between the lumped ideality factor of the processor and the ideality factor assumed by the temperature sensor. The lumped ideality factor can be calculated using the equations in this section to find the temperature offset that should be used with the temperature sensor.

Table A-2 shows the constants and variables used to calculate the temperature offset correction.

Table A-2. Temperature Offset Equation Constants and Variables

Equation Symbol	Variable, Constant Description
$n_{f, actual}$	Actual ideality factor
$n_{f, lumped}$	Lumped ideality factor
$n_{f, TS}$	Ideality factor assumed by temperature sensor
I_{high}	High sourcing current
I_{low}	Low sourcing current
$T_{die, spec}$	Die temperature specification
T_{offset}	Temperature offset

The formulas in Equation 3 and Equation 4 can be used to calculate the temperature offset for temperature sensors that do not employ series resistance cancellation. The result is added to the value measured by the temperature sensor. Contact the vendor of the temperature sensor being used for the value of $n_{f,TS}$. Refer to the document, *On-Die Thermal Diode Characterization* (publication ID 25443) for further details.

Equation 3 shows the equation for calculating the lumped ideality factor ($n_{f,\ lumped}$) in sensors that do not employ series resistance cancellation.

$$n_{f,\ lumped} = n_{f,\ actual} + \frac{R_T \cdot (I_{high} - I_{low})}{\frac{k}{q}(T_{die,\ spec} + 273.15) \cdot \ln\left(\frac{I_{high}}{I_{low}}\right)}$$

Equation 3.

Equation 4 shows the equation for calculating temperature offset (T_{offset}) in sensors that do not employ series resistance cancellation.

$$T_{offset} = (T_{die,\ spec} + 273.15) \cdot \left(1 - \frac{n_{f,\ lumped}}{n_{f,\ TS}}\right)$$

Equation 4.

Equation 5 is the temperature offset for temperature sensors that utilize series resistance cancellation. Add the result to the value measured by the temperature sensor. Note that the value of $n_{f,TS}$ in Equation 5 may not equal the value used in Equation 4.

$$T_{offset} = (T_{die,\ spec} + 273.15) \cdot \left(1 - \frac{n_{f,\ actual}}{n_{f,\ TS}}\right)$$

Equation 5.

A.2 Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document.

A.2.1 Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILLVALID#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.
- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

A.2.2 Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
  - An octaword is 16 bytes (128 bits)
  - A cache line is eight quadwords (64 bytes)
- Addressing—Memory is addressed as a series of bytes on 8-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table A-3 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with brackets and a colon (for example, bits [9:1]). The same applies for signal or bus names. The highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

A.2.3 Abbreviations and Acronyms

Table A-3 contains the definitions of abbreviations used in this document.

Table A-3. Definitions of Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga–
Gb	Gigabit
GB	Gigabyte
H	Henry
h	Hexadecimal
K	Kilo–
KB	Kilobyte
M	Mega–
Mb	Megabit
MB	Megabyte
MHz	Megahertz
m	Milli–
ms	Millisecond
mW	Milliwatt
µ	Micro–
µA	Microampere
µF	Microfarad
µs	Microsecond
µV	Microvolt
n	nano–
nA	nanoampere
ns	nanosecond
ohm	Ohm
p	pico–
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table A-4 contains the definitions of acronyms that may have been used in this document.

A.2.4 Web Sites and Support

- www.amd.com

Other web sites of interest include the following:
- JEDEC home page—www.jedec.org
- IEEE home page—www.computer.org
- AGP Forum—www.agpforum.org

Table A-4. Definitions of Acronyms

Acronyms	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
CPGA	Ceramic Pin Grid Array
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
FIFO	First In, First Out
FSB	Front Side Bus
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor to Transistor Logic
MSB	Most Significant Bit
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-drain
OPGA	Organic Pin Grid Array

Acronyms	Meaning
PGA	Pin Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor to Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer

A.3 Revision History

This document is a report of the revision/creation process of the data book for the AMD Geode™ NX processor. Any revisions (i.e., additions, deletions, parameter corrections, etc.) are recorded in the table(s) below.

Table A-5. Revision History

Date	Revision	Description
May 2004	A	Initial release
September 2004	B	See revision B for details.
October 2004	C	Removed “Preliminary” label and changed “LeadFree” to “Lead Reduced”
March 2005	D	Corrected information in notes for Tables 6-2 and 8-2 concerning minimum voltage.
June 2005	E	Major addition was adding APIC interface. See revision E for details.
September 2005	F	Big re-write / organizational layout changes. See revision F for details.
March 2006	G	Updated mechanical data section with 28104 OPGA package dimensions and incorporated other minor edits.
April 2006	H	Updated Section 7.0 "Ordering Information" on page 65 with three new OPNs: ANXL1250FYC3F, ANXL1500FGC3F, and ANXS1750FXC3F. An F in the last character of the order number means 95ºC Lead Reduced.

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