NXP Advanced UARTs SC28L201 and SC28L202

Advanced UARTs with 256-byte FIFOs and real-time data error detection

Offering very high data integrity over a broad range of operating conditions, these Advanced UARTs interface directly with standard microprocessors for high efficiency in polled and interrupt-driven systems.

Key features

- Single (SC28L201) and Dual (SC28L202) channel UARTs
- Pin programming to Intel and Motorola bus interface
- Bit-by-bit, real-time transmission error checking for very high data integrity
- 256-character FIFOs for each receiver and transmitter
- Full-duplex, independent asynchronous receivers and transmitters
- Fully compatible with IMPACT family
  - Supports 3- and 5-V operation (inputs tolerant to 5 V)
  - Industrial temperature range (-40 to 85 °C)
  - Pin programming for Intel and Motorola bus interfaces
- Baud rates up to 3.125 Mbps in twenty-seven standard rates for each receiver and transmitter
- Up to sixteen programmable I/O ports
- Programmable data format, counter/timer, baud rate, channel mode, etc.
- Versatile arbitrating interrupt system
- Watchdog™ timer for receiver
- Power-saving options
- Programmable channel mode (normal, auto echo, local and remote loopback, multi-drop)

Applications

- Telecommunications and networking routers
- Servers and concentrators
- VoIP systems
- Machine and engine control
- Precision robotics
- Security
- Gaming systems
- Home automation

The NXP Advanced UARTs SC28L201 and SC28L202 perform bit-by-bit, real-time error checking during transmission. They check data for accuracy as it's being sent, so the processor doesn't have to review data when it returns.

Data sent by the transmitter is returned by the remote receiver. During its return, the data is compared, about one bit-time later, with the data just sent. The arbitration block examines all interrupting sources and delivers, based on highest value or priority, the condition and identity of each source. Any errors immediately generate an interrupt.

As a result, the processor doesn't have to evaluate transmission status, it simply reads the dynamic arbitration register.

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Each receiver and transmitter is buffered by a 256-character FIFO. This essentially eliminates receiver over-run and transmitter under-run, and reduces interrupt overhead in interrupt-driven systems.

For added security, the flow-control capability of each UART channel can disable a remote transmitter when the receiver is full.

Programmable options

Each UART channel supports baud rates up to 3.125 Mbps and is compatible with 3- and 5-V operation. The channel modes and data formats for each channel are fully programmable. Each channel has a character-recognition system that can be used for general-purpose or Xon/Xoff character recognition, or for address recognition during wake-up mode.

Each receiver and transmitter can select its operating speed as one of twenty-seven fixed baud rates, as a 16x clock derived from one of two programmable counter/timers, or as an external 1x or 16x clock. The baud-rate generator and the counter/timer can operate directly from a crystal or from external clock inputs.

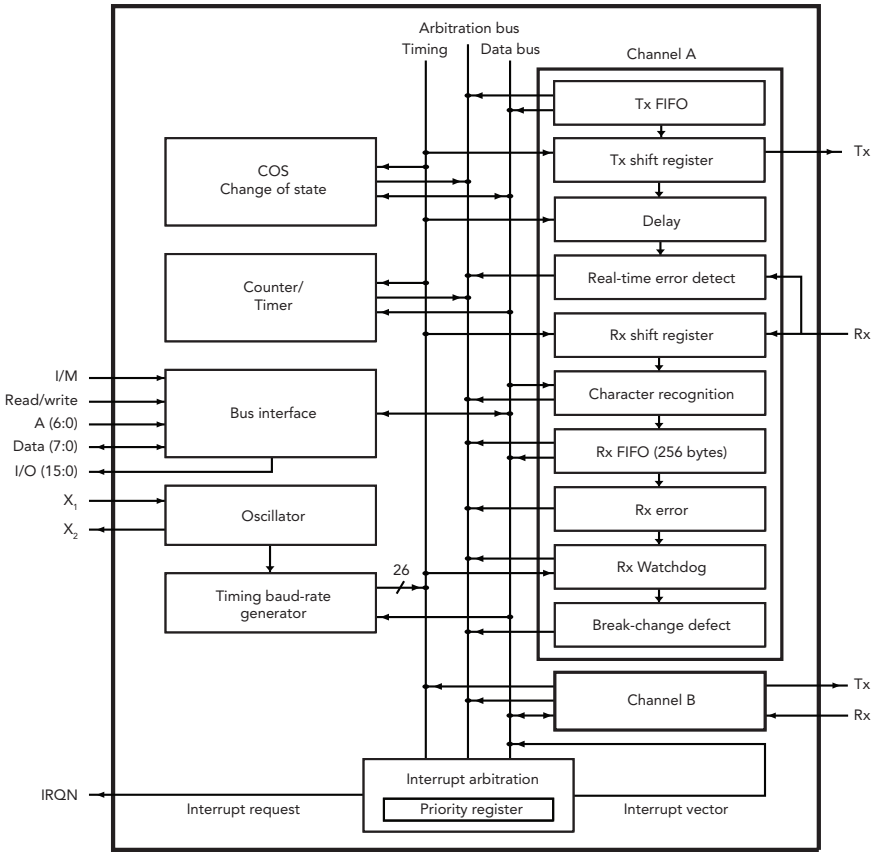
Each channel is supported by an 8-bit I/O, for a total of sixteen programmable I/O. The I/O are typically used for modem control and DMA interfaces, or as general-purpose I/O ports. All the ports have change-of-state detectors. The input sections are always active, so output signals are available to the internal circuits as well as to the processor.

Versatile arbitrating interrupt system

The interrupt system in each UART channel fully supports "single-query" polling. Each output port can be configured to provide a total of six separate interrupt-type outputs that can be switched to open drain (wire-ORed). Each FIFO can be programmed independently for up to 256 interrupt levels, and there is a Watchdog timer and receiver time-out for each receiver.

Other features include line-break detection and generation, automatic RS-485 (wake-up) mode for multi-drop applications, start-end break interrupt/status, power-saving items such as on-chip crystal oscillator with power-down mode.

For more information about the DUARTs, please visit www.nxp.com/interface. Email your technical questions to Interface.Support@nxp.com.



SC28L202 block diagram

Ordering information

Type number	UART channel	Package	Dimensions
SC28L201A1DGG	1 (Single)	TSSOP48	12.5 x 6.1 x 1.2 mm
SC28L202A1DGG	2 (Dual)	TSSOP56	14.0 x 6.1 x 1.2 mm

Recommended application notes

Document number	Title
AN10313	Reduce CPU overhead with Intelligence Interrupt Arbitration (I^2A) feature
AN10380	Ensure data integrity with real-time error detection

Date of release: November 2006
Document order number: 9397 750 15765
Printed in the USA