CUBIT-*Pro* Device
CellBus™ Bus Switch
TXC-05802

DATA SHEET

FEATURES

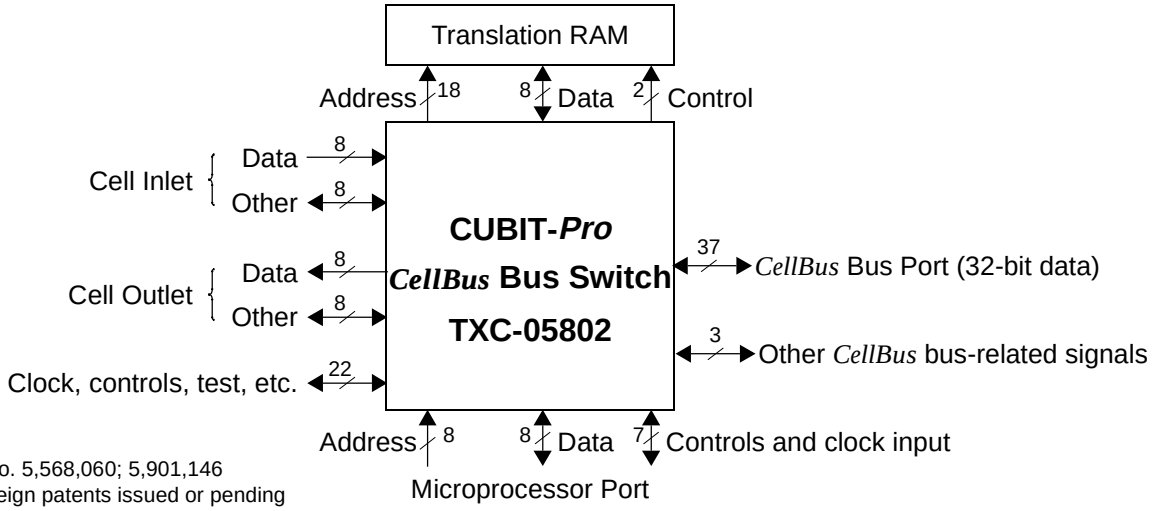
- UTOPIA and 16-Bit (ATM or PHY) Layer cell interfaces
- Inlet-side address translation and routing header insertion, using external SRAM of up to 256 kB
- Programmable OAM-cell and RM-cell routing
- *CellBus* bus access request, grant reception and bus transmission
- *CellBus* bus cell reception and address recognition
- Outlet cell queuing: various modes
- Ability to insert GFC field in real time
- Ability to insert FECN indication, under programmable conditions
- Ability to send and receive cells for control purposes over same *CellBus* bus
- Cell insertion and extraction via microprocessor port
- Master bus arbiter and frame pulse generator included in each CUBIT-*Pro*, with enabling pin
- Internal GTL transceivers for *CellBus* bus connection
- Interface port to translation table in SRAM
- Microprocessor control port, selectable for Intel or Motorola interface
- +5 V and +3.3 V power supplies
- 208-pin plastic quad flat package

DESCRIPTION

CUBIT-*Pro*™ is a single-chip solution for implementing cost effective ATM access systems. It is based on the *CellBus*™ Bus Architecture *(CellBus)*. Such systems are constructed from a number of CUBIT-*Pro* devices, all interconnected by a 37-line common bus, the *CellBus* bus. When operating at a 38 MHz clock rate, a *CellBus* bus system can handle 1 Gbit/s of net ATM cell bandwidth. CUBIT-*Pro* supports unicast and multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing, and outlet cell queuing.

APPLICATIONS

- xDSL Access Multiplexer
- Remote Access Equipment
- Cable Modem Access Multiplexer
- ATM LAN hub
- ATM multiplexer/concentrator
- Small-stand-alone ATM switch
- Add-Drop Ring Switch
- Edge switching equipment



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LIST OF FIGURES

BLOCK DIAGRAM

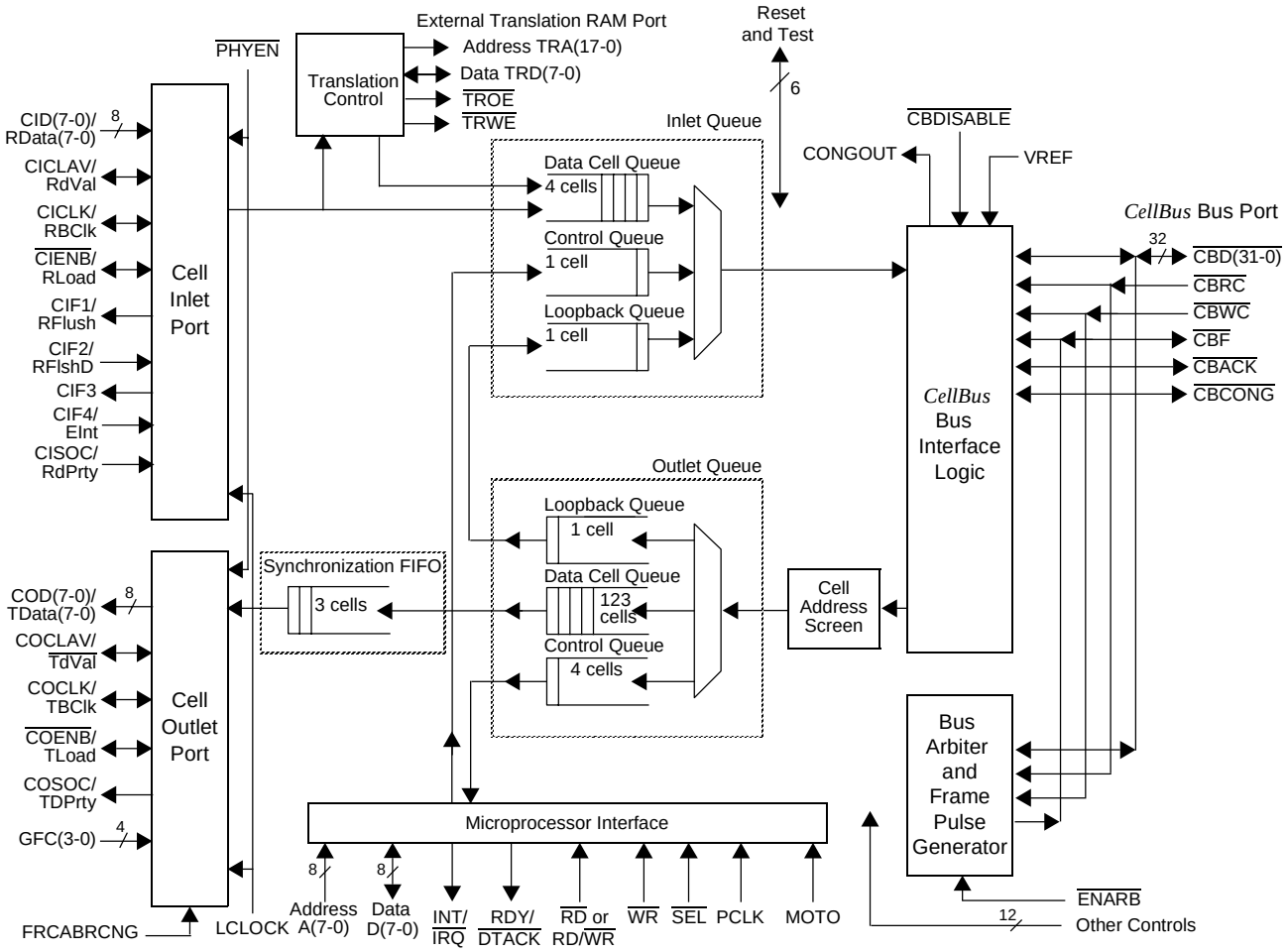


Figure 1. CUBIT-*Pro* TXC-05802 Block Diagram

A block diagram of the CUBIT-*Pro* device is shown in Figure 1. Further information on device operation and the interfaces to external circuits is provided below in the following Operation section.

On the cell inlet side of the CUBIT-*Pro* is circuitry associated with accepting cells from the line and passing them to the *CellBus* bus with an appropriate header. The Cell Inlet Port block is pin-selectable to be compliant with either the ATM Forum UTOPIA (Universal Test and Operations Physical Interface for ATM) interface, a TranSwitch 16-Bit interface, or the TranSwitch ALI-25 device interface. Incoming cells may carry a *CellBus* Routing Header and translated outgoing VPI/VCI address, the translation function having been performed externally, or this address translation and routing header insertion may be done by the CUBIT-*Pro* Translation Control block. Translation and routing header tables to support this function are contained in an external static RAM (up to 256k x 8 bits). They support VPI and/or VPI/VCI address translation. The incoming cells then pass through a FIFO queue in the Inlet Queue block to the *CellBus* Bus Port via the *CellBus* Bus Interface Logic block. When there is a cell in this 4-cell data cell queue, the CUBIT-*Pro* makes a bus access request, and waits for a grant from the Bus Arbiter and Frame Pulse Generator block of the one CUBIT-*Pro* device attached to the bus that has been enabled to perform these two functions. When a bus access grant is received, the CUBIT-*Pro* sends the cell to the bus, in standard *CellBus* bus format. The cell can then be received by any connected CUBIT-*Pro* or CUBIT-Pros. In addition to these incoming data cells, the CUBIT-*Pro* can also send Control cells from the local microprocessor to the bus via the Microprocessor Interface block. Special cells of Loopback type received from the bus may also be returned to the bus, re-directed back to the CUBIT-*Pro* which launched the original Loopback cell. Both the Control cells and the Loopback cells have 1-cell inlet queues.

On the cell outlet side, cells of proper unicast address, broadcast address or selected multicast address, received from the bus via the *CellBus* Bus Interface Logic block, are recognized by the Cell Address Screen block and routed into a FIFO structure in the Outlet Queue block. The unicast address is unique per device, set by device straps. Each CUBIT-*Pro* may be programmed to accept cells associated with multicast sessions. From zero up to the full 256 multicast sessions may be accepted independently by each CUBIT-*Pro* on the bus. Data cells from the bus go into a 123-cell outlet data cell queue structure. Control cells and Loopback cells arriving from the bus are routed to the 4-cell outlet control queue, and the 1-cell outlet loopback queue, respectively. The outlet data cell FIFO structure can be treated as a single 123-cell queue, or it can be subdivided into four individual queues for traffic of different service types. The four-queue split is typically into high-speed control data cells, CBR cells, VBR cells, and ABR cells, in decreasing order of outlet service priority. This allows for delay minimization of critical service types, and for more efficient traffic management. At the cell outlet, provisions are made for insertion of an outgoing Generic Flow Control (GFC) field and an Explicit Forward Congestion Indication (EFCI) bit.

OPERATION

INTRODUCTION TO *CellBus* BUS ARCHITECTURE

CellBus Bus Operation

The CUBIT-*Pro* is a versatile CMOS VLSI device for implementing ATM switching functions. Various ATM cell switching or multiplexing structures can be formed by interconnection of a number of CUBIT-*Pro* devices over a 37-line parallel bus with 32 data bits, the *CellBus* bus. Since the interconnect structure is a bus, communications between any of the devices on the bus is possible. Each cell placed onto the *CellBus* bus by a CUBIT-*Pro* device can be routed either to one single CUBIT-*Pro* (unicast addressing), or to multiple CUBIT-*Pro* devices (multicast or broadcast addressing). Depending upon the needs of an application, up to 32 CUBIT-*Pro* devices may be interconnected on one *CellBus* bus. With a maximum bus frequency of more than 38 MHz, the raw bandwidth of the *CellBus* bus exceeds 1 Gbit/s.

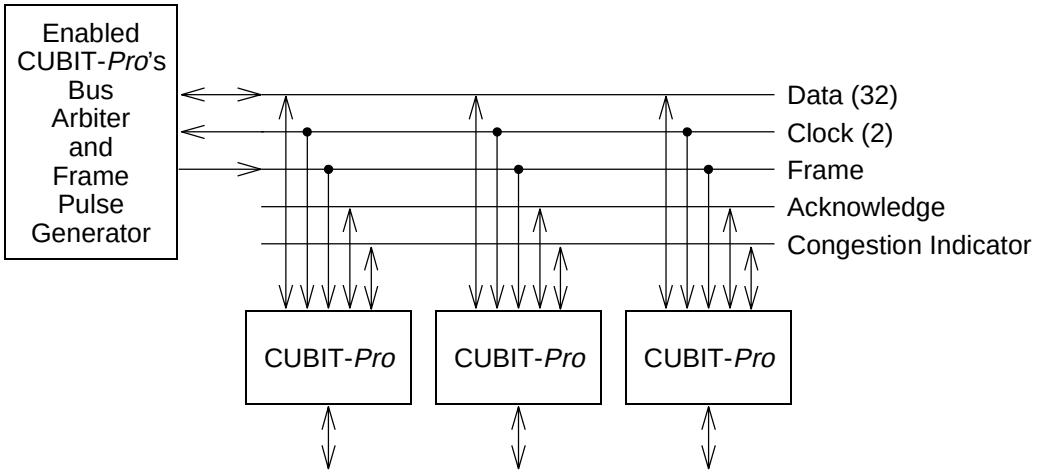


Figure 2. *CellBus* Bus Structure

The *CellBus* bus, shown in Figure 2, is a shared bus, and can be implemented either on a single circuit card, or in a backplane configuration among multiple circuit cards. Since multiple CUBIT-Pros share the same bus, bus access contention must be resolved. This access contention is resolved by use of a central arbitration function. CUBIT-Pros will request bus access, and the central Bus Arbiter will grant access back, in response. The circuitry for this Bus Arbiter is included inside the CUBIT-*Pro* device. Any one CUBIT-*Pro* in a system may be selected to perform the bus arbitration function by setting its $\overline{\text{ENARB}}$ pin low.

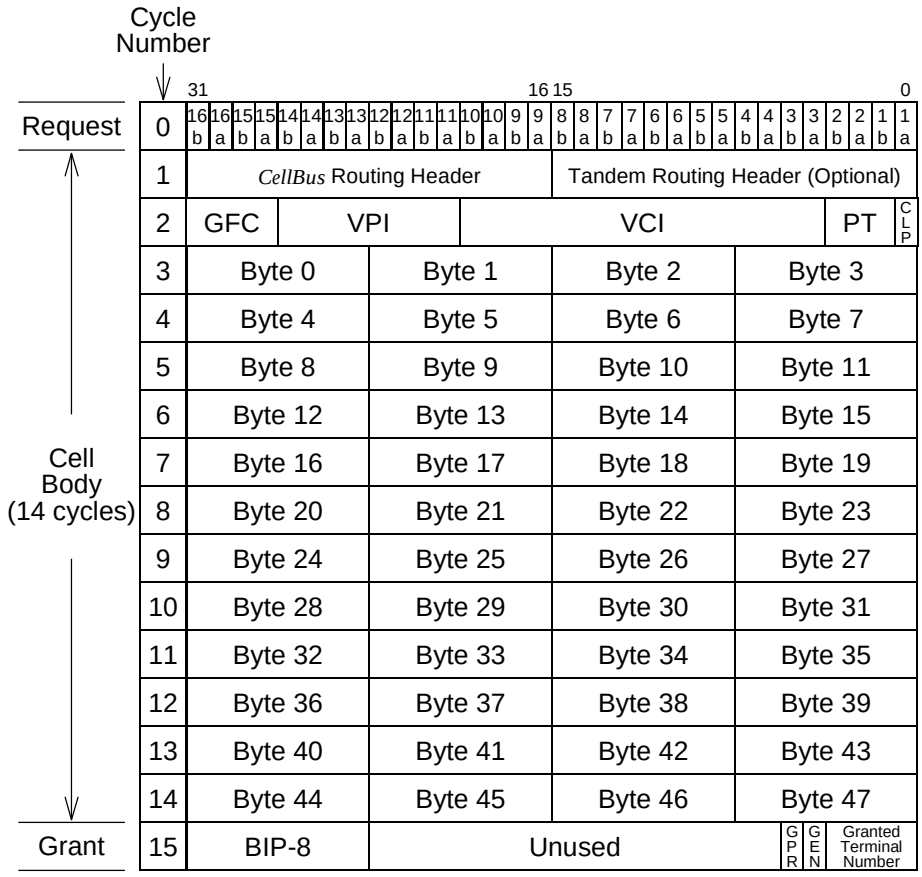


Figure 3. *CellBus* Bus Frame Format

The *CellBus* bus has a framed format 16 clock cycles long and 32 bits wide, which is illustrated in Figure 3. The first cycle of each frame is the Request cycle (Cycle 0), during which those CUBIT-Pros which have a cell to send to the bus each make an access request by asserting one or two assigned bits on the bus. The $\overline{\text{CBF}}$, $\overline{\text{CBACK}}$ and $\overline{\text{CBCONG}}$ signals are asserted during a Request cycle. The device address assigned to each CUBIT-*Pro* by device straps ($\overline{\text{UA(4-0)}}$ at pins 2-6) uniquely specifies which two bits it may assert during the bus Request cycle time. For example, $\overline{\text{UA(4-0)}}$ = HHHHH selects bits 1a and 1b. By asserting one of its assigned bits, or the other, or both, access requests of three different priorities may be made (controlled via bits P1, P0 in memory address 0AH). A central Bus Arbiter accepts these access requests, executes an arbitration algorithm (highest priority served first, round-robin within each priority), and issues a bus access grant during the final cycle of the frame, the Grant cycle (Cycle 15). Each grant issued by the arbiter is for one CUBIT-*Pro* to send one cell to the bus. Whichever CUBIT-*Pro* is issued a grant during a Grant cycle will transmit its cell during the 14 Cell Body clock cycles of the next bus frame, and will also drive an 8-bit cell parity check during the Grant cycle of that bus frame. Each cell sent can be of unicast, multicast, or broadcast type. CUBIT-Pros will accept single-address cells routed to an address defined by their address straps, all broadcast cells, and selected multicast cells. Thus, cells may be sent from any one CUBIT-*Pro* to any one CUBIT-*Pro* or to multiple CUBIT-Pros.

The CUBIT-*Pro* can be operated in either 16-user or 32-user mode, selectable via the $\overline{\text{U32}}$ pin, as shown in Figure 4. For the 16-user mode the *CellBus* bus frame is identical to Figure 3. However, in 32-user mode the frame is duplicated, so that an odd and even frame are provided. The distinction between the two frames is given by the location of the frame pulse. The cycles for both frames are the same, except for the meaning of the Request cycle. The Request cycle in the even frame coincides with the frame pulse, whereas in the odd frame the pulse is not present. Furthermore, in the even frame CUBIT-Pros 0-15 (lower 16 users) request access to the bus and in the odd frame CUBIT-Pros 16-31 (upper 16 users) request access to the bus. The full bus bandwidth is available to be shared among all the users on the bus in either 16 or 32-user mode.

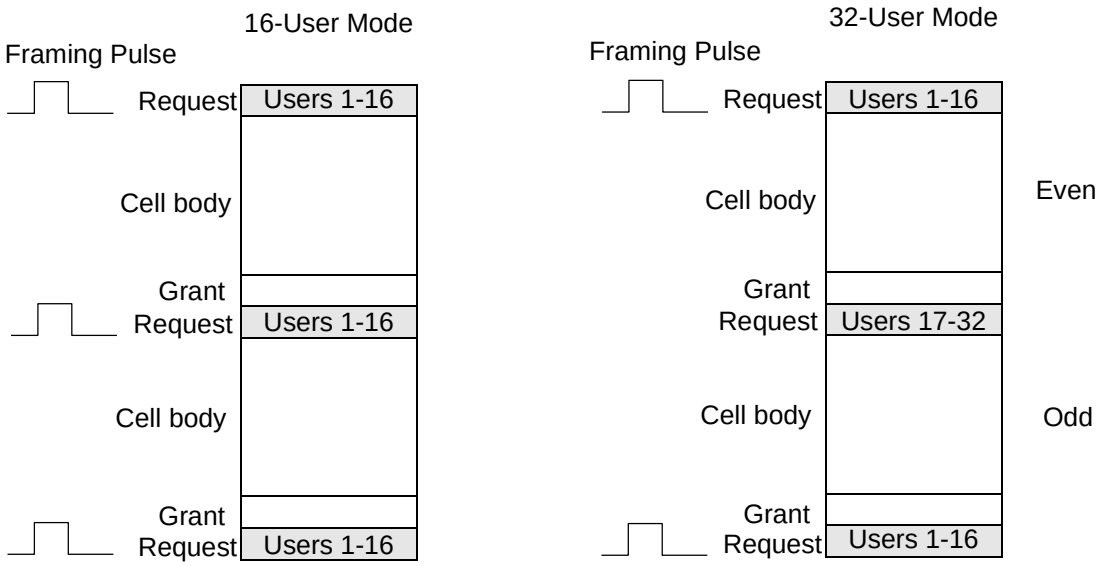


Figure 4. *CellBus* Bus 16/32-User Modes - Frame Formats

To detect *CellBus* bus errors, a BIP-8 (Bit Interleave Parity byte) is calculated over the 54-byte data field that extends from the first Tandem Routing Header byte through the final payload data byte, Byte 47. The BIP-8 is generated by the transmitting CUBIT-*Pro* using the following algorithm. The first byte of the Tandem Routing Header is exclusive-or gated with an all-ones byte, creating a starting seed value. This seed value is then exclusive-or gated with the second byte of the Tandem Routing Header. The result is then exclusive-or gated with the next byte in the cell. This process is repeated with every successive byte in the cell, through Byte 47 of the payload, and the final result is transmitted as the BIP-8 byte in cycle 15. The receiving CUBIT-*Pro* performs the same process and compares the generated BIP-8 with the received BIP-8. If no errors are detected the receiving CUBIT-*Pro* pulls $\overline{\text{CBACK}}$ low, acknowledging receipt of a cell. The *CellBus* Routing Header has its own CRC-4 field and is not included in the BIP-8 calculation. A cell with a BIP-8 or CRC-4 error is discarded.

The only signals required to operate the bus which are not sourced by a CUBIT-*Pro* device are two transfer clocks: write clock ($\overline{\text{CBWC}}$) and read clock ($\overline{\text{CBRC}}$). These clock signals are of the same frequency, but may be slightly phase-offset to allow for reliable bus operation. The framing pulse used to define the bus frame cycle is sent out by one of the CUBIT-Pros, and the arbitration function is also performed by the same CUBIT-*Pro*. Each CUBIT-*Pro* contains the circuitry for both the Bus Arbiter and the Frame Pulse Generator. Only one CUBIT-*Pro* will have this circuitry enabled, by setting control pin $\overline{\text{ENARB}}$.

CellBus Bus Cell Routing

The *CellBus* bus architecture allows several types of cell routing from any one inlet port to the outlet ports of the CUBIT-Pros on the *CellBus* bus:

- Point-to-Point Routing: In Unicast or Single Address cell routing a cell coming into an inlet port is transferred to a single outlet port. The CUBIT-*Pro* can address a cell to itself, effectively implementing both the inlet and outlet ports.
- Point-to-Multipoint (Broadcast): A cell coming into the inlet port can be routed to the outlet ports of all the CUBIT-Pros on the *CellBus* bus.
- Point-to-Multipoint (Multicast): In multicast routing the cell arriving at the inlet port is sent to the subset of outlet ports that belong to the specific multicast session by means of selection in the receiving CUBIT-Pros.

For each of the routing methods the cells can be sent to different output queues according to whether the cell is used as a data cell or as control/loopback cell. Furthermore, data cells can be selected to go to four different data outlet queues: Control Data queue, Constant Bit Rate (CBR) queue, Variable Bit Rate (VBR) queue, and Available Bit Rate (ABR) queue. The CUBIT-*Pro* can be programmed to receive cells into separate queues (split-queue mode) or not (single-queue mode).

The encoding rules for the two-byte *CellBus* Bus Routing Header in Bits 31-16 of Cycle 1 are summarized in Figure 5.

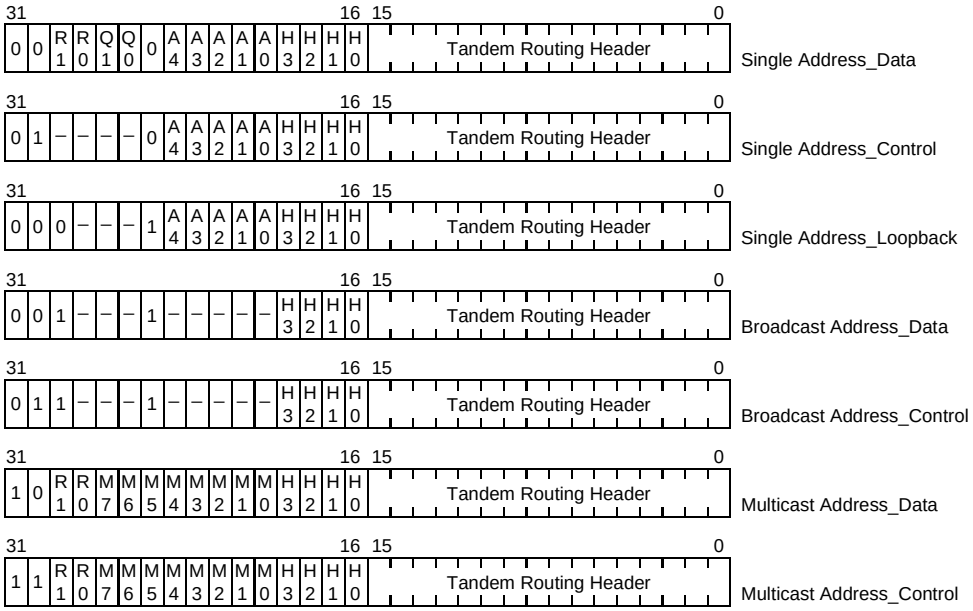


Figure 5. *CellBus* Bus Routing Header Formats

CellBus Bus Routing Header Format

The *CellBus* Bus Routing Header contains the following fields, as shown in Figure 5:

R: Multi-PHY selector field (2 bits). Not interpreted by CUBIT-*Pro* currently (passed through intact). This field is ignored.

Q: Queue selection field for split-queue mode (2 bits). 00 is outlet Control Data queue, 01 is Constant Bit Rate (CBR) queue, 10 is Variable Bit Rate (VBR) queue, 11 is Available Bit Rate (ABR) queue. This coding is only valid for data cells which contain Q1,Q0 fields in the header. For multicast and broadcast cell routing, cells are routed to the VBR and CBR queues, respectively, when using split-queue mode.

A: CUBIT-*Pro* single address field (5 bits, for 32 addresses). A0 is the LSB. For example, A(4-0)=00000 is the address value for the CUBIT whose five device identity straps $\overline{\text{UA(4--0)}}$ are all tied high (HHHHH).

M: Multicast number field (8 bits, for 256 multicast sessions). M0 is the LSB.

H: CRC-4 field. This 4-bit field (H3-H0) provides Routing Header error protection across the *CellBus* bus in both directions. It is calculated over the 12-bit word (X11-X0) in bits 31-20 of the Routing Header using the following logic:

$$H3 = \overline{(X7 \oplus X9 \oplus X3 \oplus X10 \oplus X8 \oplus X5 \oplus X2)}$$

$$H2 = (X6 \oplus X8 \oplus X2 \oplus X9 \oplus X7 \oplus X4 \oplus X1)$$

$$H1 = \overline{(X5 \oplus X7 \oplus X1 \oplus X8 \oplus X6 \oplus X3 \oplus X0)}$$

$$H0 = (X8 \oplus X10 \oplus X11 \oplus X4 \oplus X9 \oplus X6 \oplus X3 \oplus X0)$$

where $\oplus$ represents logical exclusive-or. For cells arriving from the *CellBus* bus, the CUBIT-*Pro* automatically calculates the corresponding CRC-4 and sets to 1 the status bit CRCF (bit 7 in register 08H) if it is not the same as that in bits H3-H0 of the received Routing Header. This status bit may be enabled to cause an interrupt signal to the microprocessor by setting to 1 the enable bit INTEN7 (bit 7 in register 09H). For cells supplied to the cell inlet interface from an external source for transmission via the *CellBus* bus, the CRC-4 may either be supplied in the input signal by use of external logic (as is required for the CUBIT device) or it may be generated internally and inserted into the Routing Header by the CUBIT-*Pro*. Setting control bit CRC4EN to 1 (bit 3 in register 0EH) activates the internal CRC-4 insertion for all incoming cells (i.e., not only data cells, but also control cells and loopback cells). When control bit CRC4I (bit 4 in register 0EH) is set to 1 the internally generated CRC-4 is inverted for testing purposes. This bit has no effect on an externally-supplied CRC-4. For operation in the CUBIT TXC-05801 mode with an externally-supplied CRC-4, bit CRC4EN should be set to 0, which is the default at power-up/reset.

Tandem Routing Header Format

The two-byte Tandem Routing Header format in Bits 15-0 of Cycle 1 is the same as the *CellBus* Bus Routing Header format, if it is to be used by a cascaded *CellBus* bus, or may conform to a different specification if it is used by another system. The Tandem Routing Header is passed unchanged through the *CellBus* bus.

CellBus Bus Status Signals and Monitoring

The CUBIT-*Pro* provides the capability to monitor the activity on the *CellBus* bus. The essential signals that determine whether the bus is active (in the absence of any cell traffic) are the clock signals and the frame pulse.

The *CellBus* bus clocks (read and write) are generated externally to the CUBIT-*Pro*. If either of these clocks fails, the entire bus will cease operation. The CUBIT-*Pro* provides the capability to detect the absence of clock signal for more than the equivalent of 32 processor clock (PCLK) cycles. The failure detection is performed independently for the *CellBus* Bus Read Clock ($\overline{\text{CBRC}}$) and the *CellBus* Bus Write Clock ($\overline{\text{CBWC}}$).

Two bits (register 05H bits CBLORC and CBLOWC) in the CUBIT-*Pro* memory map are used to indicate the clock loss event. Once the event is detected, these bits in register 05H will remain set to one until the microprocessor reads the register, at which point the register will be cleared. These events can be used to generate a microprocessor interrupt provided that the appropriate bits in the interrupt enable register (address 06H, bits INTENA1 and INTENA0) are 1.

The second monitoring function concerns the detection of loss of frame. The detection mechanism looks for two consecutive missing *CellBus* bus frame pulses in 32-user mode ($\overline{\text{U32}}$ = Low), and four consecutive missing *CellBus* bus frame pulses in 16-user mode. The *CellBus* Bus Read Clock must be present to detect Loss of Frame Pulse. If *CellBus* Bus Read Clock is present and *CellBus* Bus Write Clock is not, then both CBLOWC and CBLOF will be set. CBLOF can generate an interrupt to the microprocessor assuming that the appropriate interrupt enable bit is 1 (register 06H, bit 2: INTENA2).

CUBIT-*Pro* CELL INLET AND OUTLET PORTS

The Cell Inlet and Outlet ports constitute the main interfaces for the cell traffic between the CUBIT-*Pro* and other devices in either the upper ATM or Physical (PHY) Layers. Several interfaces are supported by the device: UTOPIA 8-bit mode, TranSwitch 16-Bit mode, TranSwitch ALI-25 device interface mode, and Back-to-Back (CUBIT-*Pro*-to-CUBIT-*Pro* interface).

The CUBIT-*Pro* can provide address translation if selected via the input pin $\overline{\text{TRAN}}$ (pin 154). If no translation is selected, the external hardware must provide the *CellBus* Bus Routing Header, the Tandem Routing Header (optional), and the ATM cell. If translation mode is selected, the hardware is required only to provide the ATM cell and the CUBIT-*Pro* will perform the translation based on the information programmed into the attached translation SRAM.

For all the modes the cell size is selectable via external pins $\overline{\text{LMODE2}}$, $\overline{\text{LMODE1}}$ and $\overline{\text{LMODE0}}$ (pins 156, 157, and 158, respectively), as described below. This feature permits the CUBIT-*Pro* to accommodate the requirements for different designs.

Additionally, the UTOPIA and 16-Bit modes can be selected to behave as either the master (ATM layer device) or the slave (PHY layer device). The selection between ATM and PHY layer device for the UTOPIA and 16-Bit modes is made via the $\overline{\text{PHYEN}}$ pin (pin 48), where a low enables PHY layer device operation.

The CUBIT-*Pro* allows the selection of the clock for the cell Inlet/Outlet operation from three different sources: *CellBus* bus clocks ($\overline{\text{CBRC}}$, pin 78 and $\overline{\text{CBWC}}$, pin 77), processor clock (PCLK, pin 32), or an externally supplied clock (LCLOCK, pin 45). The clock selected will be used for the UTOPIA and 16-Bit ATM layer device modes, the ALI-25 (cell inlet clock) mode, and the Back-to-Back (cell inlet clock) mode, for which the CUBIT-*Pro* sources the interface clock. For all other modes the clock is an input to the CUBIT-*Pro*. The selection of the clock source for the cell interfaces is performed via two control bits in register 0BH: CLKS1, CLKS0. The coding for the clock selection is as follows:

CLKS1, CLKS0 = 0,0: Cell interface clock = *CellBus* bus clock divided by 2^{LINEDIV}
CLKS1, CLKS0 = 0,1: Cell interface clock = LCLOCK clock divided by 2^{LINEDIV}
CLKS1, CLKS0 = 1,0: Cell interface clock = PCLK clock divided by 2^{LINEDIV}
CLKS1, CLKS0 = 1,1: Reserved, do not use

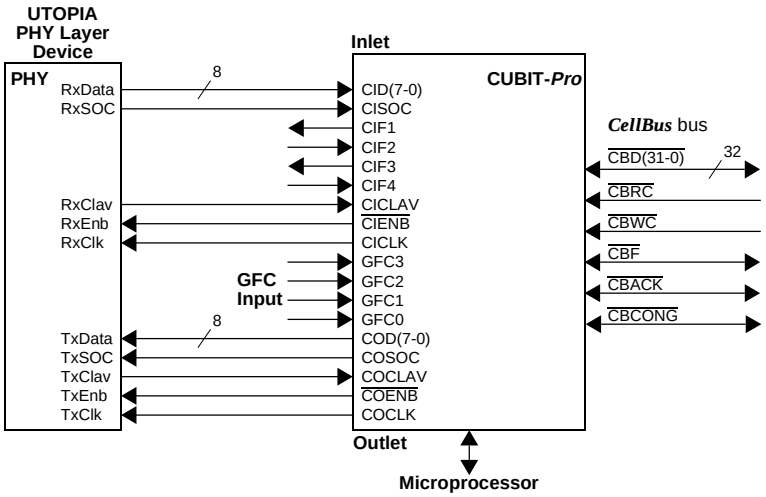
8-Bit UTOPIA Mode - ATM and PHY Layer Emulation

Typical signal connections for the CUBIT-*Pro* when operating in UTOPIA mode are illustrated in Figures 6 and 7, for ATM Layer and PHY Layer cell level handshake modes, respectively. The operating mode options for UTOPIA mode are controlled by the input pins $\overline{\text{TRAN}}$, $\overline{\text{PHYEN}}$, $\overline{\text{LMODE2}}$, $\overline{\text{LMODE1}}$ and $\overline{\text{LMODE0}}$, as indicated in the tables of Figures 6 and 7. $\overline{\text{TRAN}}$ selects the internal translation mode, if asserted. In UTOPIA mode, $\overline{\text{PHYEN}}$ determines whether the CUBIT-*Pro* emulates an ATM or PHY device. $\overline{\text{LMODE2}}$, $\overline{\text{LMODE1}}$ and $\overline{\text{LMODE0}}$ determine the cell inlet/outlet cell size.

When internal translation is used, the cell I/O is exactly that defined by UTOPIA, with 53-byte inlet cells. For applications in which the internal translation function is not used, the timing and logical flow of the cell I/O is still identical to that of UTOPIA, except that 57-byte or 55-byte inlet cells are used, instead of 53. The additional bytes are the Routing Header bytes which would be inserted by the CUBIT-*Pro* if the translation function were used, but are instead added by an external translation function. The pin connections and the different inlet and outlet byte counts per cell in the various modes are shown in the table of Figure 6 for ATM Layer emulation. Similarly, Figure 7 shows the pin connections and byte counts for PHY Layer emulation.

The $\overline{\text{ABRENA}}$ pin must be held high or left floating (it has internal pull-up) for proper UTOPIA mode operation.

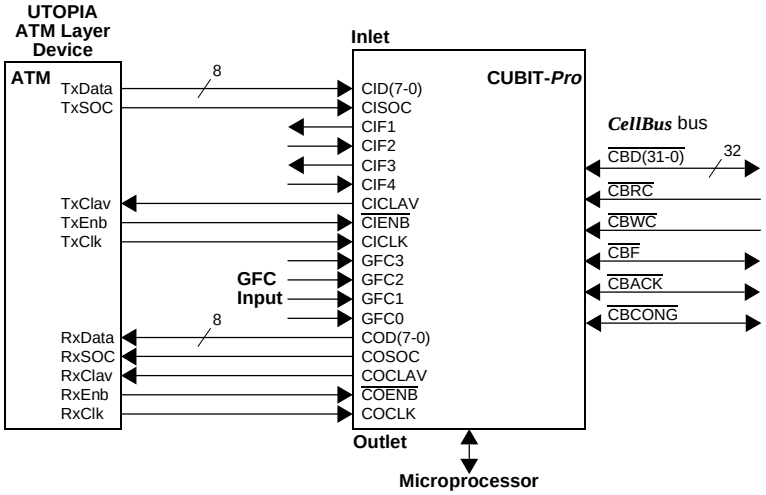
Figure 6. ATM Layer Emulation 8-Bit UTOPIA Mode Signal Connections and Operating Mode Selection



PHYEN	TRAN	LMODE2	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
High	High	High	X	High	UTOPIA, 57 bytes: cell plus *CellBus* Bus Routing Header plus two bytes of Tandem Routing Header	UTOPIA, 53-byte cell
High	High	High	High	Low	UTOPIA, 57 bytes: cell plus *CellBus* Bus Routing Header plus two bytes of Tandem Routing Header	UTOPIA, 55 bytes: cell plus Tandem Routing Header
High	High	Low	Low	High	UTOPIA, 55 bytes: cell plus *CellBus* Bus Routing Header	UTOPIA, 53-byte cell
High	High	Low	Low	Low	UTOPIA, 55 bytes: cell plus *CellBus* Bus Routing Header	UTOPIA, 55 bytes: cell plus Tandem Routing Header
High	Low	High	High	High	UTOPIA, 53-byte cell	UTOPIA, 53-byte cell
High	Low	High	High	Low	UTOPIA, 53-byte cell	UTOPIA, 55 bytes: cell plus Tandem Routing Header
High	High	Low	High	High	Reserved	Reserved
High	Low	Low	High	High	Reserved	Reserved
High	Low	Low	High	Low	Reserved	Reserved
High	Low	Low	Low	High	Reserved	Reserved

Note: High = V_{DD5} = +5V; Low = V_{SS} = Ground; X = Don't Care

Figure 7. PHY Layer Emulation 8-Bit UTOPIA Mode Signal Connections and Operating Mode Selection

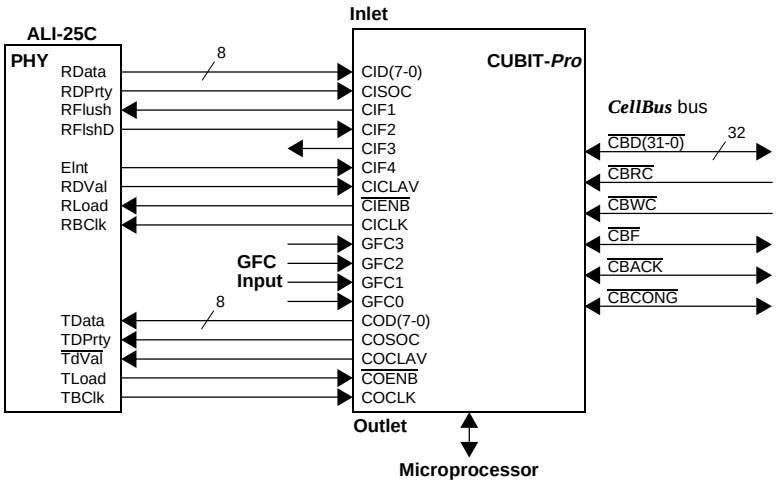


PHYEN	TRAN	LMODE2	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
Low	High	High	X	High	UTOPIA, 57 bytes: cell plus *CellBus* Bus Routing Header plus two bytes of Tandem Routing Header	UTOPIA, 53-byte cell
Low	High	High	High	Low	UTOPIA, 57 bytes: cell plus *CellBus* Bus Routing Header plus two bytes of Tandem Routing Header	UTOPIA, 55 bytes: cell plus Tandem Routing Header
Low	High	Low	Low	High	UTOPIA, 55 bytes: cell plus *CellBus* Bus Routing Header	UTOPIA, 53-byte cell
Low	High	Low	Low	Low	UTOPIA, 55 bytes: cell plus *CellBus* Bus Routing Header	UTOPIA, 55 bytes: cell plus Tandem Routing Header
Low	Low	High	High	High	UTOPIA, 53-byte cell	UTOPIA, 53-byte cell
Low	Low	High	High	Low	UTOPIA, 53-byte cell	UTOPIA, 55 bytes: cell plus Tandem Routing Header
Low	High	Low	High	High	Reserved	Reserved
Low	Low	Low	High	High	Reserved	Reserved
Low	Low	Low	High	Low	Reserved	Reserved
Low	Low	Low	Low	High	Reserved	Reserved

ALI-25 Mode

The CUBIT-*Pro* supports the ALI-25 interface devices, and connects directly to the ALI-25C with no glue logic, as shown in Figure 8. In ALI-25 mode there is always translation, because the ALI-25C device cannot produce a *CellBus* Bus Routing Header or Tandem Routing Header. Two exception conditions in the ALI-25C are supported through CUBIT-*Pro* pins CIF1, CIF2 and CIF4. The output pin CIF1 connects directly to the RFlush input pin of the ALI-25C. If, due to an error condition in the ALI-25C, RDVal is unexpectedly de-asserted at its CICLAV input, the CUBIT-*Pro* will assert CIF1 to flush the ALI-25C and declare a start-of-cell (SOC) error. The ALI-25C uses its RFlshD output pin to acknowledge via the CUBIT-*Pro*'s CIF2 input pin that the flush was completed. The second exception condition accommodated is the flagging of a HEC error by the ALI-25C. If a HEC error is found, the ALI-25C asserts its EInt output pin, which drives the CIF4 input pin of the CUBIT-*Pro* and causes it to increment its HEC Error Counter.

The $\overline{\text{ABRENA}}$ pin must be held high or left floating (it has internal pull-up).



PHYEN	TRAN	LMODE2	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
X	Low	High	Low	High	ALI-25: 53-byte cell	ALI-25: 53-byte cell

Figure 8. ALI-25 Mode Signal Connections and Operating Mode Selection

Back-to-Back Mode

The Back-to-Back mode is used to support interconnection of two *CellBus* buses, as shown in Figure 9. If pin $\overline{\text{TRAN}}$ is low, each of the CUBIT-Pros has a translation memory connected, the cell address translation function is active, and the inlet cells are 53 bytes long. The cells from the outlet can either be 55 or 53 bytes long. If 55 bytes are selected, the cell will carry the Tandem Routing Header from the *CellBus* bus.

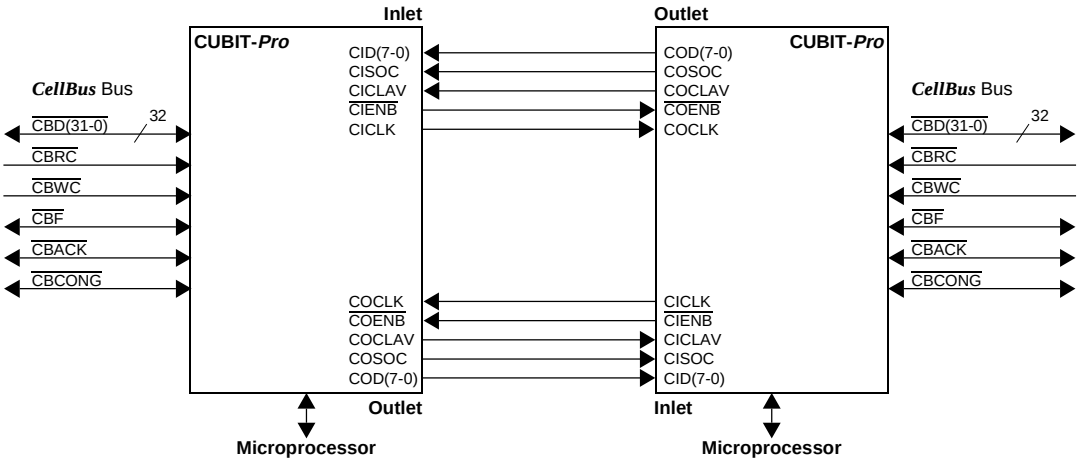
If $\overline{\text{TRAN}}$ is high, the translation function is not used. The transfers into the cell inlet will 55 bytes long. The two initial bytes are presented to the CUBIT-*Pro* as the *CellBus* Bus Routing Header. The cell outlet can present cells of either 55 or 53 bytes, whether or not internal translation is performed on the cell inlet side. If 55 bytes are selected, the cell will carry the Tandem Routing Header from the *CellBus* bus.

The cell outlet will carry two extra bytes which are the Tandem Routing Header from the *CellBus* bus. These two bytes are presented to the inlet port of the connected CUBIT-*Pro*, which uses them as a *CellBus* Bus Routing Header when it puts the cell on the bus.

In order to avoid re-transmission of multicast or broadcast cells from one *CellBus* bus to another, and back again, a CUBIT-*Pro* which is operating in the Back-to-Back mode will reject all incoming broadcast and multicast cells which originated from its own inlet side.

The timing of this mode is similar to that for UTOPIA ATM Layer emulation mode, except that the directionality of the COCLAV, $\overline{\text{COENB}}$ and COCLK signals is reversed, as shown in the connections diagrams of Figures 6 and 9.

The $\overline{\text{ABRENA}}$ pin must be held high or left floating (it has internal pull-up).

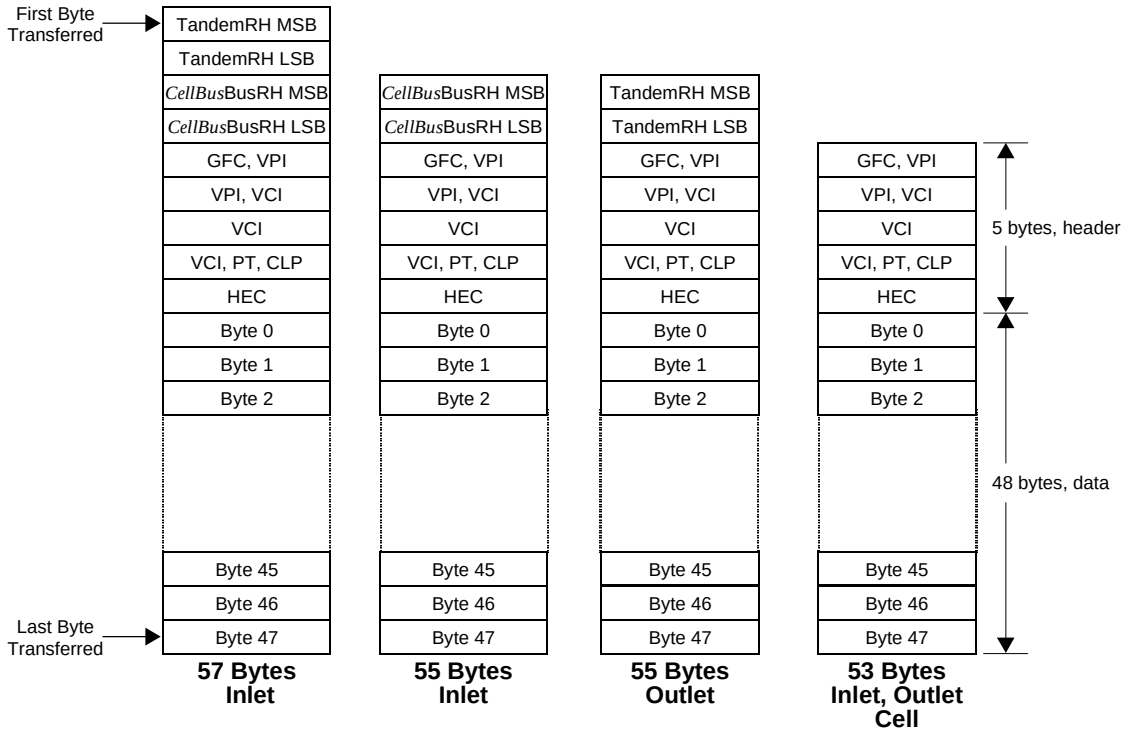


PHYEN	TRAN	LMODE2	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
X	High	High	Low	Low	Back-to-Back: 55 bytes, cell plus two bytes of *CellBus* Bus Routing Header	Back-to-Back: 55 bytes, cell plus two bytes of Tandem Routing Header
X	Low	High	Low	Low	Back-to-Back: 53-byte cell	Back-to-Back: 53-byte cell
X	Low	Low	Low	Low	Back-to-Back: 53-byte cell	Back-to-Back: 55 bytes, cell plus two bytes of Tandem Routing Header
X	High	Low	High	Low	Back-to-Back: 55 bytes, cell plus two bytes of *CellBus* Bus Routing Header	Back-to-Back: 53-byte cell

Figure 9. Back-to-Back Mode Signal Connections and Operating Mode Selection

Byte Ordering for UTOPIA, ALI-25 and Back-to-Back Modes

Byte ordering for the three cell inlet and outlet alternatives described above is illustrated in Figure 10.



Note: RH = Routing Header

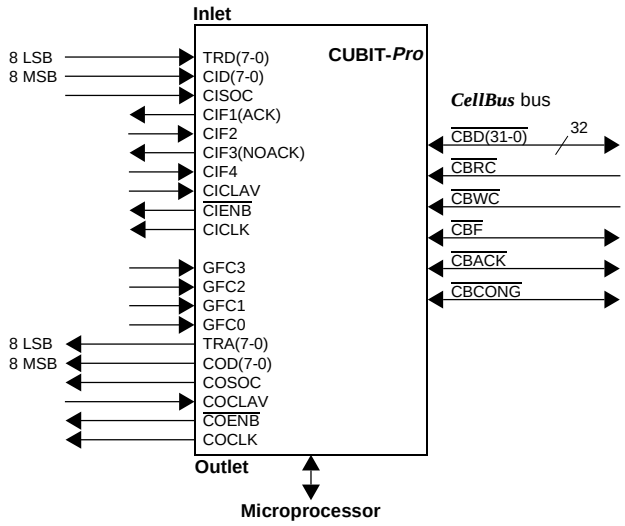
Figure 10. Byte Ordering on Cell Inlet and Outlet in UTOPIA, ALI-25 and Back-to-Back Modes

16-Bit Cell Interface Mode - ATM and PHY Layer Emulation

16-Bit cell interface mode can be selected to emulate an ATM Layer UTOPIA device, or alternatively to emulate a PHY Layer UTOPIA device, as shown in Figures 11 and 12, respectively.

16-Bit mode is enabled by setting device strap pin $\overline{\text{ABRENA}}$ low, with the settings of $\overline{\text{TRAN}}$, $\overline{\text{LMODE2}}$, $\overline{\text{LMODE1}}$ and $\overline{\text{LMODE0}}$ selected according to the table in Figure 11 for ATM Layer emulation, or according to the table in Figure 12 for PHY Layer emulation. The PHY Layer emulation is enabled with $\overline{\text{PHYEN}}$.

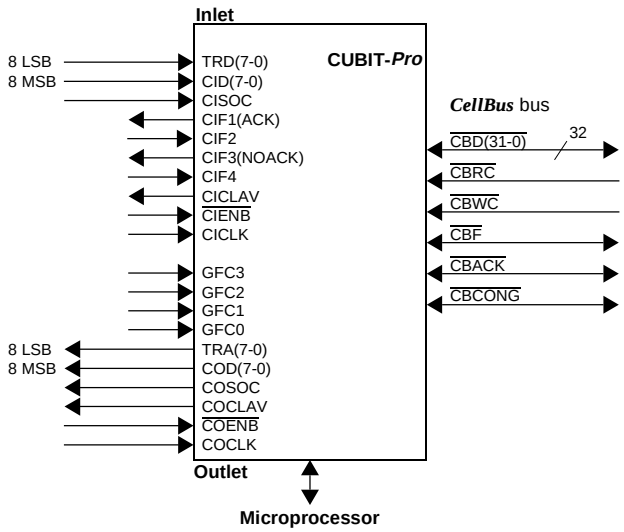
The timing of the 16-Bit mode is identical to that of the UTOPIA mode, but the data width is expanded to a word of 16 bits in and out. The translation RAM is not used in this case. The extra 8 inlet bits are connected to the pins used for the data of the translation RAM, TRD (7-0), and the extra 8 outlet pins are the pins for the 8 LSB of the translation RAM address output, TRA (7-0).



PHYEN	TRAN	LMODE2	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
High	X	Low	High	Low	16-Bit: 29 words, cell plus one word of Tandem Routing Header, plus one word of *CellBus* Bus Routing Header	16-Bit: 28 words, cell plus one word of Tandem Routing Header
High	X	Low	High	High	16-Bit: 29 words, cell plus one word of Tandem Routing Header, plus one word of *CellBus* Bus Routing Header	16-Bit: 27-word cell
High	X	High	X	X	16-Bit: 28 words, cell, plus one word of *CellBus* Bus Routing Header	16-Bit: 28 words, cell plus one word of Tandem Routing Header
High	X	Low	Low	High	16-Bit: 28 words, cell, plus one word of *CellBus* Bus Routing Header	16-Bit: 27-word cell
High	X	Low	Low	Low	Reserved	Reserved

Figure 11. ATM Layer Emulation 16-Bit Mode Signal Connections and Operating Mode Selection

Figure 12. PHY Layer Emulation 16-Bit Mode Signal Connections and Operating Mode Selection



PHYEN	TRAN	LMODE2	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
Low	X	Low	High	Low	16-Bit: 29 words, cell plus one word of Tandem Routing Header, plus one word of *CellBus* Bus Routing Header	16-Bit: 28 words, cell plus one word of Tandem Routing Header
Low	X	Low	High	High	16-Bit: 29 words, cell plus one word of Tandem Routing Header, plus one word of *CellBus* Bus Routing Header	16-Bit: 27-word cell
Low	X	High	X	X	16-Bit: 28 words, cell, plus one word of *CellBus* Bus Routing Header	16-Bit: 28 words, cell plus one word of Tandem Routing Header
Low	X	Low	Low	High	16-Bit: 28 words, cell, plus one word of *CellBus* Bus Routing Header	16-Bit: 27-word cell
Low	X	Low	Low	Low	Reserved	Reserved

Word Ordering for 16-Bit Cell Interface Mode

The word ordering for 16-Bit mode is shown in Figure 13.

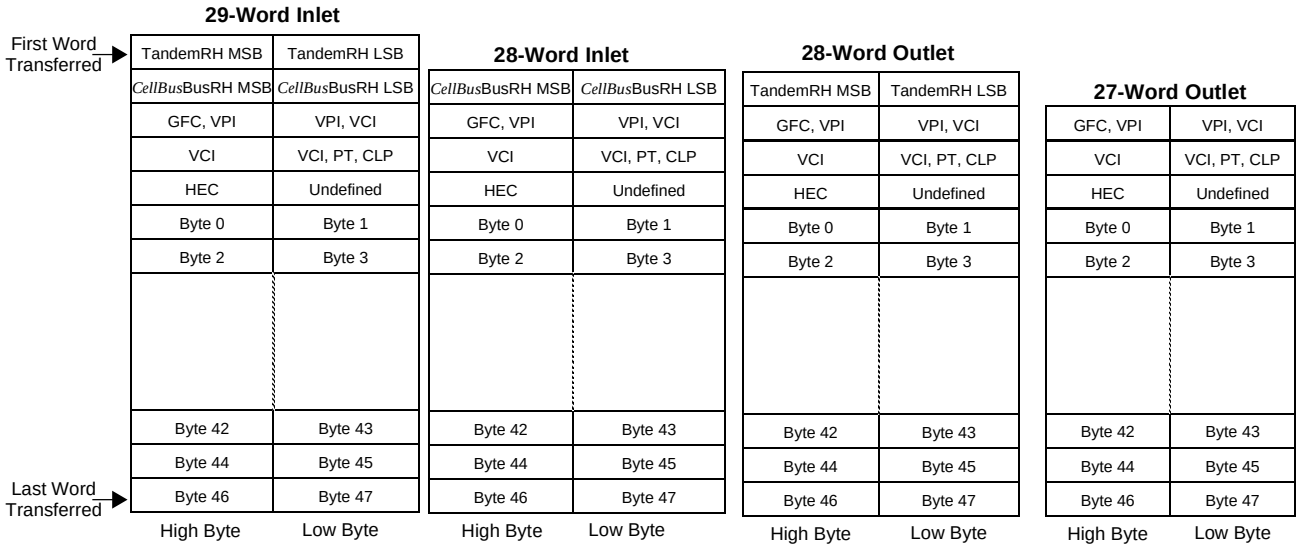


Figure 13. Word Ordering on Cell Inlet and Outlet in 16-Bit Mode

TRAFFIC MANAGEMENT FUNCTIONS

Dynamic Generic Flow Control (GFC) Field Insertion

The CUBIT-*Pro* can insert the value of the first nibble of the ATM cell header in real time. The value of the GFC nibble is supplied to the CUBIT-*Pro* via the input pins GFC(3-0). The insertion of the GFC value is enabled via the control bit GFCENA.

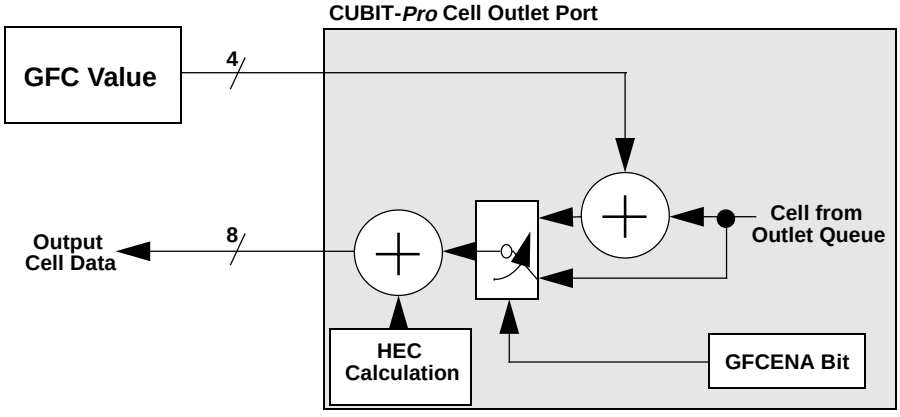


Figure 14. GFC Insertion on the Outlet Queue (GFCENA = 1)

If control bit GFCENA (Control Register Address 0CH, Bit 1) is set to one, then the state of the four Generic Flow Control input pins GFC(3-0) will be accepted during the leading rising edge of the clock for the first byte of the ATM cell header and inserted as an outgoing GFC on the following cell (see timing diagram in Figure 47 for details). Therefore the GFC value is inserted into the next outgoing cell.

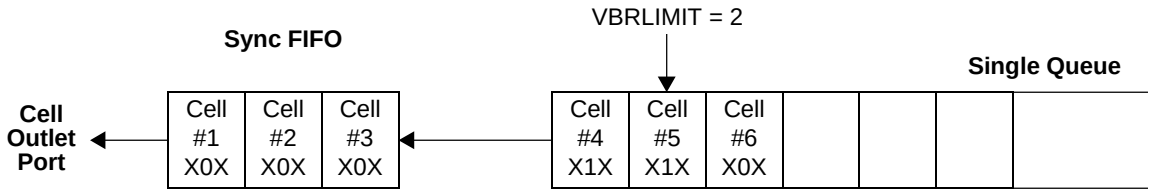
Forward Explicit Congestion Notification (FECN)

The CUBIT-*Pro* can notify an impending congested state by setting to one the middle bit of the Payload Type (PT) field in the ATM cell header. This Explicit Forward Congestion Indication bit (EFCI) will be asserted on a cell if both of two conditions occur at the same time:

a) Bit 0 in register 0CH is set to one (IFECN = 1), and

b) QM (bit 2 in register 0CH) = 0 and VBR Limit reached, or QM=1 and VBR Limit or CBR Limit reached.

The activation of the EFCI bit in the single-queue (QM = 0) and split-queue (QM = 1) modes is illustrated in Figures 15 and 16, respectively.

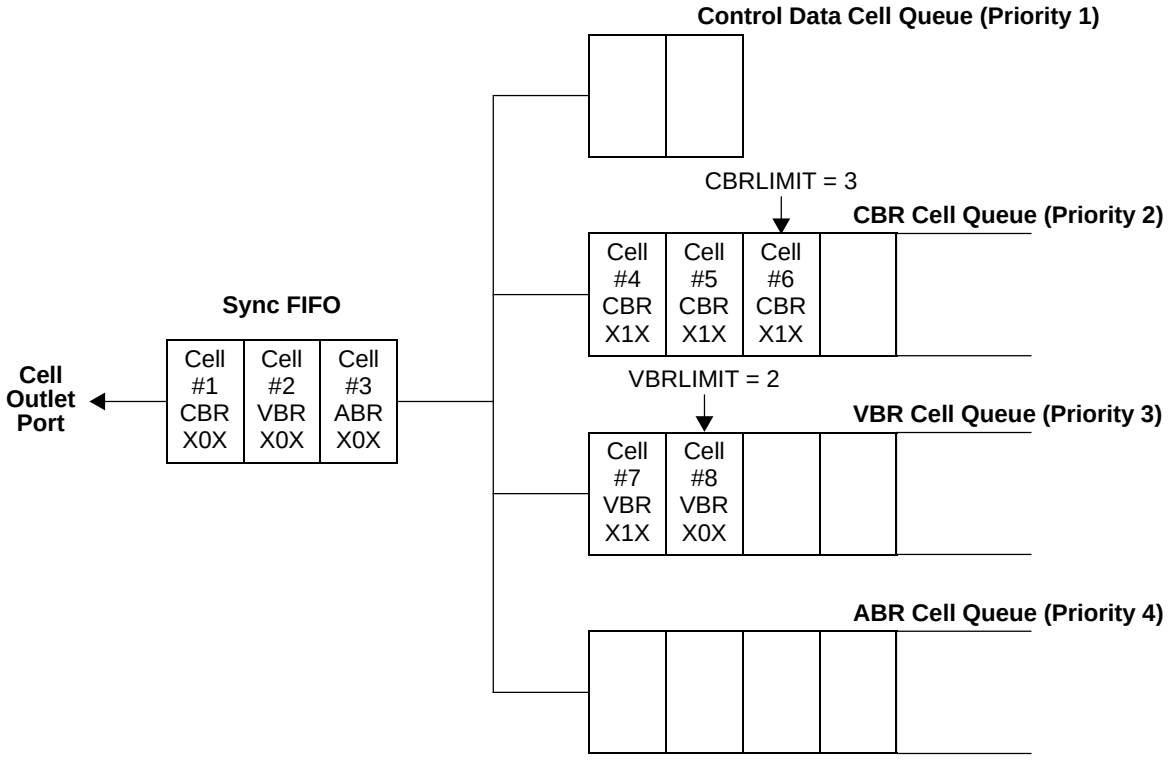


Note: The IFECN control bit is set to 1. The EFCI congestion indication is the middle bit of the PT sequence (X0X or X1X). Its value is determined when the cell leaves the queue.

Figure 15. Example of Congestion Indication in Single-Queue Mode (QM = 0)

Figure 15 shows a starting condition for the single-queue mode soon after the congestion conditions a) and b) have both become present, with three cells in the queue when VBRLIMIT is set to 2. Cells #1, #2 and #3 reached the Sync FIFO before the congestion occurred, so they are not marked with a congestion indication and have a PT value of X0X. The first cell in the queue (cell #4) is marked with a congestion indication (PT = X1X) and it moves into the Sync FIFO when the outlet link is free and Cell #1 is sent to the cell outlet port. Cells #5 and #6 then shift to the left, putting Cell #6 at the VBRLIMIT = 2 boundary, so congestion persists and Cell # 5 is also marked with PT = X1X. When this cell moves into the Sync FIFO, Cell #6 shifts left and it is the only cell left in the queue, assuming no more cells have joined the queue. Since the queue length of 1 is now less than VBRLIMIT = 2, condition b) no longer exists and cell #6 carries no congestion marking (PT = X0X).

Figure 16 shows a starting condition for the split-queue mode some time after congestion conditions a) and b) have both become present, with three cells in the CBR cell queue when CBRLIMIT = 3 and two cells in the VBR cell queue when VBRLIMIT = 2 (i.e., both queues are at the congestion level).



Note: The IFECN control bit is set to 1. The EFCI congestion indication is the middle bit of the PT sequence (X0X or X1X). Its value is determined when the cell leaves the queue.

Figure 16. Example of Congestion Indication in Split-Queue Mode (QM=1)

As before, cells #1, #2 and #3 left the queues before the congestion occurred and are not marked for congestion indication (PT = X0X). When the outlet link becomes free and the cells in the Sync FIFO shift to the left, cells flow in to the Sync FIFO from the four data cell queues in priority order. Since the VBR queue contains two cells when VBRLIMIT = 2, congestion continues to exist while all cells in the CBR cell queue are moved into the Sync FIFO, so cells #4, #5 and #6 are marked with congestion indications (PT = X1X). Now, assuming no more cells are joining the queues, the CBR cell queue is empty but the VBR cell queue is still at the VBRLIMIT value with two cells, so cell #7 is also marked with a congestion indication. But when it moves to the Sync FIFO only one cell is left in the VBR cell queue, so conditions a) and b) no longer both exist, and this cell #8 is not marked with a congestion indication (PT = X0X).

Congestion Indication from *CellBus* Bus to Cell Inlet

In the event of congestion being experienced at the output port of the receiving CUBIT-*Pro*, three bits are relayed back to the sending CUBIT-*Pro* to allow for congestion control. The output signals provided by the sending CUBIT-*Pro* are:

- CONGOUT: This output pin signal has a dual function which can be selected with bit EBP (bit 2 in register 0EH). If EBP=0 (default at power-up/reset) CONGOUT is a straight GTL-to-CMOS translation of the *CellBus* bus signal $\overline{\text{CBCONG}}$. If EBP=1, then CONGOUT is an indication that the receiving CUBIT-*Pro* is experiencing congestion or impending congestion. These two situations correspond to the case where the outlet queue of the receiving CUBIT-*Pro* is full or the congestion limit (almost full) for that queue has been reached, respectively. In the case of almost full the cell will not be lost if CLP=0 in cycle 2, but a full queue will not accept any cells. In this case, a NACK will also be received. A pulse is available on the CONGOUT output (pin 155) of the CUBIT-*Pro* sending the cell after a receiving CUBIT-*Pro* experiences congestion (for UTOPIA, 16-Bit, and Back-to-Back modes).
- ACK: Positive acknowledge which indicates that the cell was accepted at the destination CUBIT-*Pro*. A pulse is provided on the CIF1 output (pin 118) of the CUBIT-*Pro* sending the cell if the cell is successfully accepted (for UTOPIA, 16-Bit, and Back-to-Back modes).
- NACK: Negative acknowledge which indicates the cell was not forwarded to the outlet queue of the receiving CUBIT-*Pro*. A pulse is provided on the CIF3 output (pin 115) of the CUBIT-*Pro* sending the cell if the cell is not forwarded, but dropped (for UTOPIA, 16-Bit, and Back-to-Back modes).

  Note: The EBP bit (address 0EH, bit 2) must be set to enable the ACK and NACK functions of CIF1 and CIF3 in the UTOPIA and back-to-back modes. The ACK and NACK functions of CIF1 and CIF3 are always enabled in the 16-Bit mode.

Paralleling Cell Inlet/Outlet Ports for Redundancy

If the control bit ONLINE (control register address 0CH, bit 7) is set to zero, then all of the CUBIT-*Pro* cell outlet interface output pins will be taken to the high impedance (Hi-Z) state and the cell inlet data input pins will be disabled. Thus two CUBIT-Pros may be paralleled for redundancy, each connected to a separate *CellBus* bus. Cells will only be accepted from, or sent to, the line by the CUBIT-*Pro* in which ONLINE = 1.

INLET-SIDE TRANSLATION

Introduction

The translation function on the inlet side operates using information stored in an external static RAM, and can provide the following functions:

Virtual Path Identifier (VPI) translation or
VPI/VCI translation (where VCI is Virtual Circuit Identifier), and
CellBus Bus Routing Header insertion, and
Tandem Routing Header insertion, and
F4 flow cell routing, and
F5 flow cell routing.

All translation operations start by performing a translation table lookup based on the VPI number of the incoming cell. Within the routing table record for that VPI is control information for that VPI, indicating whether cells are to be routed based on VPI number alone or on VPI and VCI.

If VPI-only routing is selected, a translated VPI number, accompanied by *CellBus* Bus and Tandem Routing Headers, is retrieved from the translation record for that VPI. In this case, the VCI number of the incoming cell is not changed. If VPI translation is selected, separate routing for F4 OAM flow cells and RM-VPC cells on that VPI can be programmed, allowing selective handling of these OAM-cells and RM-cells by a *CellBus* bus system.

If the VPI is instead programmed for VCI translation, then a two-step procedure is used to accomplish the translation. The VPI record, accessed first, indicates the size and position in memory of the VCI translation table. Using this information, and the VCI address of the cell, a VCI translation record is accessed. This translation record contains the VPI and VCI numbers to be assigned to the cell, along with the *CellBus* Bus and Tandem Routing Headers. When VPI/VCI translation is selected, separate routing for F5 OAM flow cells and RM-VCC cells on that VCI can be programmed, allowing selective handling of these OAM-cells and RM-cells in a manner similar to that of F4 OAM flow cells and RM-VPC cells.

In both cases, the cells with the translated headers and *CellBus* Bus and Tandem Routing Headers are forwarded to the bus in sequential order. Translation does not add delay to cells passing through the inlet side to the *CellBus* bus.

Translation RAM Connections

The CUBIT-*Pro* can address up to 256k bytes of translation SRAM (TRAM). The connections to the TRAM are shown in Figure 17. The TRAM access time requirement is dependent upon the cell inlet clock speed (i.e., in ATM Layer mode: *CellBus* bus clock, or PCLK, or LCLOCK; in PHY Layer mode: CICLK), see Figures 33 and 34. An access time of 35 nanoseconds or less will support the maximum *CellBus* bus speed.

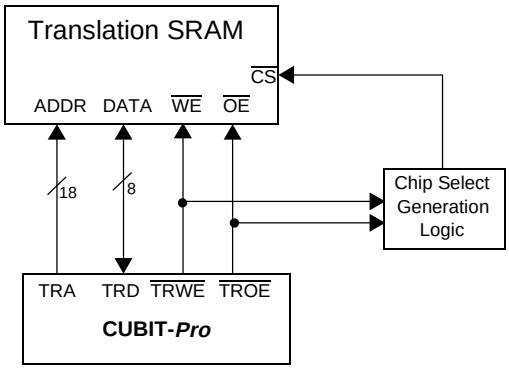


Figure 17. Translation RAM Connections

The chip select should be implemented according to the number of SRAM devices used in the design. If a single 256k x 8 SRAM is used, the memory can be permanently selected, or if a low-power application is required then the memory can be selected only when the CUBIT-*Pro* needs to access the SRAM (use $\overline{\text{TROE}}$ and $\overline{\text{TRWE}}$, as shown in Figure 17).

Translation RAM Control

When the CUBIT-*Pro* device is configured to perform translation (input pin $\overline{\text{TRAN}}$ low), it replaces received values of VPI or VPI and VCI numbers with new values, and adds Routing Headers to the cells forwarded to the *CellBus* bus. The VPI/VCI number and Routing Header information that is inserted comes from translation record entries in the TRAM. The TRAM is organized into a block of VPI records and a block of VCI records, the contents of which are established by system control.

Translation RAM Organization

The translation RAM partitioning is shown in Figure 18. The lower portion of the TRAM contains the translation records for VPIs. When the UNI mode is enabled (control bit UNI=1), the number of VPI entries is 256. When NNI mode is enabled (UNI=0), 4096 VPI entries are present.

Depending on whether the Tandem Routing Header is enabled the VP Record has: four bytes if the Tandem Routing Header (TRH) is not used (control bit TRHENA=0), and six bytes if the TRH is used (TRHENA=1). The size of the VPI memory space in this mode ranges from 1024 bytes (UNI mode, no TRH, 4 x 256) to 24576 bytes (NNI and TRH, 6 x 4096).

The memory space above the VPI section is the VCI translation record storage space, divided into a number of VCI pages. Each VCI page contains the translation records for 128, 256, 512, or 1024 VCIs.

Depending on whether Tandem Routing Header is enabled the VC Record has: six bytes if the Tandem Routing Header (TRH) is not used (control bit TRHENA=0), and eight bytes if the TRH is used (TRHENA=1).

The number of VCI records per page (VRP) depends on the settings of the VRPS[1,0] control bits in register 0EH as follows:

VRPS[1,0]=0,0: VRP is 256

VRPS[1,0]=0,1: VRP is 512

VRPS[1,0]=1,0: VRP is 1024

VRPS[1,0]=1,1: VRP is 128

The total size of the TRAM which the CUBIT-*Pro* can support is up to 262,144 bytes (256k). Hence, the number of VCI translation table pages which can be supported is a function of memory size, and the states of control bits UNI and TRHENA. For example, the maximum number (M) of VCI memory pages, for maximum memory size, is as follows:

VRPS[1,0]=0,0: VRP is 256
if UNI=1, TRHENA = 1; M = (262144-(256*6))/(256*8) = 127 VCI Pages,

if UNI=1, TRHENA = 0; M = (262144-(256*4))/(256*6) = 170 VCI Pages.

VRPS[1,0]=0,1: VRP is 512
if UNI=1, TRHENA = 1; M = (262144-(256*6))/(512*8) = 63 VCI Pages,

if UNI=1, TRHENA = 0; M = (262144-(256*4))/(512*6) = 85 VCI Pages.

VRPS[1,0]=1,0: VRP is 1024
if UNI=1, TRHENA = 1; M = (262144-(256*6))/(1024*8) = 31 VCI Pages,

if UNI=1, TRHENA = 0; M = (262144-(256*4))/(1024*6) = 42 VCI Pages.

VRPS[1,0]=1,1: VRP is 128
if UNI=1, TRHENA = 1; M = (262144-(256*6))/(128*8) = 254 VCI Pages,

if UNI=1, TRHENA = 0; M = Min[(262144-(256*4))/(128*6), 256] = Min [340,256] = 256 VCI Pages.

if VRPS[1,0]=1,1, VRP is 128. The maximum number of addressable pages is 256, even though, theoretically, 340 pages could fit in a SRAM of 256k bytes.

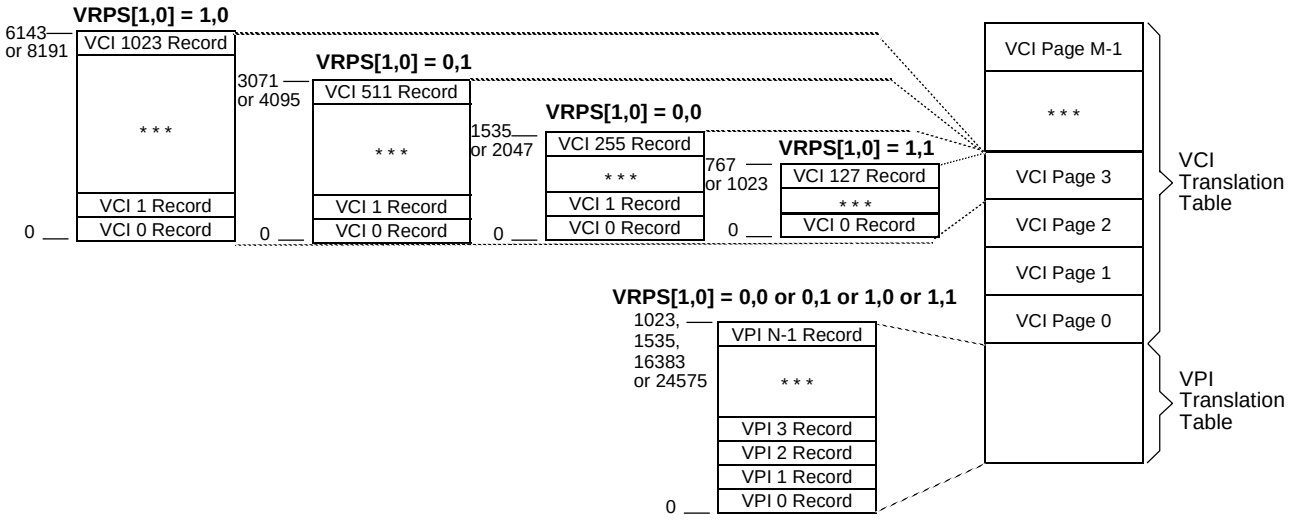


Figure 18. Translation RAM Organization

VCI Page 0 Organization

This page may optionally be used for OAM-cells routing, RM-cells routing, or data cells routing. For OAM/RM and reserved VCs, bit OAMRMEN (bit 1 in register 0EH) must be set to 1. If OAM/RM routing is enabled (OAMRMEN=1) then the organization of VCI Page 0 is as shown in Figure 19.

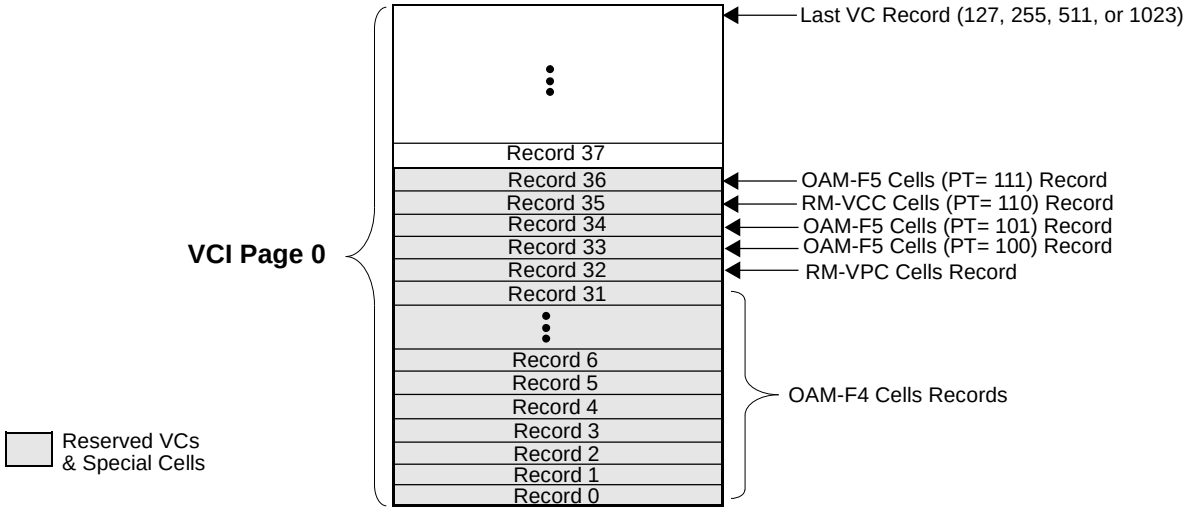


Figure 19. VCI Page 0 Organization (Bit OAMRMEN=1)

If the device is required to operate in CUBIT TXC-05801 applications, then bit OAMRMEN must be set to 0, which is the power-up/reset default.

Translation Procedure

Translation is performed in a two-step procedure, starting with examining the incoming VPI number. A full 8-bit (UNI=1) or 12-bit (UNI=0) VPI number may be used. The incoming VPI number is used to address a VPI translation record. If the translation is to be done on VPI only, leaving the VCI number intact, then the VPI number and routing header are contained in the VPI translation record. If VPI and VCI translation is to be done, then the VPI record contains a pointer to the location of one or more "pages" of VCI translation records. Each "page" is a set of translation records for either 128, 256, 512, or 1024 consecutive VCI numbers (depending on the settings of bits VRPS[1,0] in register 0EH). Up to sixteen such VCI pages may be assigned to any VPI. The only restriction is that the VCI pages for each VPI must be assigned in consecutive VCI address space from zero upwards. Within this assigned space, the VCI number of the incoming cell is used to address a particular VCI translation record containing the new VPI and VCI numbers and the routing header.

OAM/RM cells are routed either from the VP record or VC record that is marked for this special cells routing, as detailed in the section below entitled “OAM-Cells and RM-Cells Record Format”.

For the translation operation the CUBIT-*Pro* uses several data structures. These data structures can be of three different types:

VP Record
VC Record
OAM/RM Record

Each of these records contains one or more control bits in the first byte of the record (byte 0), which determines whether the routing is per VP, per VC, or per OAM/RM cell. The control bits are described next.

Translation Records Control Bits

Four control bits, labelled as A, P, E and I, are used in byte 0 of translation records, as described below:

Active (A) Bit:
If the A bit is set to one in a translation record, then that VPI or VCI is active. Cells received with this VPI or VCI will be translated and forwarded to the bus, unless bit I is set to one. If A=0, then cells received on this VPI or VCI will be considered misrouted, unless I=1.

VPI Translation Enable Bit (P):
If this bit is one in a VPI translation record, then a VPI-only translation is made. If it is set to zero, a combined VPI and VCI translation is made.

OAM/RM Cell Routing Enable Bit (E):
If bit E is set to one in a VPI record, then VCIs numbered 0 through 31 of that VPI will be routed according to OAM/RM records contained in record numbers 0 through 31 of VCI page zero. Additionally, if bit E is set to one in a VPI record, then cells of that VPI with VCI =6 and having the PT = 110 will be routed according to the OAM translation record contained in record number 32 of VCI page zero. Regular data cells (not conforming to the above rules) are routed according to the VP and/or VC record. If bit E is set to one in a VCI record, then cells of that VPI having the PT = 100, 101, 110, and 111(Payload Type Indicator, in ATM cell header) will be routed according to the OAM translation record contained in record numbers 33, 34, 35, and 36 of VCI page zero, respectively.

Ignore Bit (I):
If the ignore bit is one (I=1) in an active VP or VC (i.e., A=1 in the translation record) then incoming cells bearing this VP or VC number are discarded, but not counted as misrouted cells. If control bit NOTIGN (bit 5 in register 0EH) is set to 1, then connections with I=1 will be treated as if I=0.

OAM/RM Routing Mode Bits (C1,C0):
These bits are used to determine on which VPI/VCI OAM/RM cells are routed. The possible combinations are:

C1,C0 = 0,0: the cell header is translated according to the values in the OAM/RM record (this value and OAMRMEN=0 should be selected for applications supporting CUBIT TXC-05801 functionality)

C1,C0 = 0,1: for F4 flow this virtual path connection (VPC) OAM cells/RM-VPC cells are not routed according to the OAM/RM record. Instead, these cells are routed according to the VP record corresponding to the incoming VP.
For F5 flow this virtual circuit connection (VCC) OAM cells/RM-VCC cells are not routed according to the OAM/RM record. Instead, these cells are routed according to the VC record corresponding to the incoming VP/VC combination.

C1,C0 = 1,0: attach *CellBus* Bus Routing Header (CBRH) and Tandem Routing Header (TRH) only, and preserve the incoming VP/VC combination

C1,C0 = 1,1: reserved

Note: In order to use Tandem Routing Header, TRHENA =1 must be selected regardless of the table values.

CellBus Bus Routing Header

The *CellBus* Bus Routing Header is a 16-bit structure, which is formatted as described earlier in the *CellBus* Bus Cell Routing subsection. Additional detail is provided in Appendix A of "*CellBus* Bus Technical Manual and CUBIT-*Pro* Applications", TranSwitch document number TXC-05802-TM1.

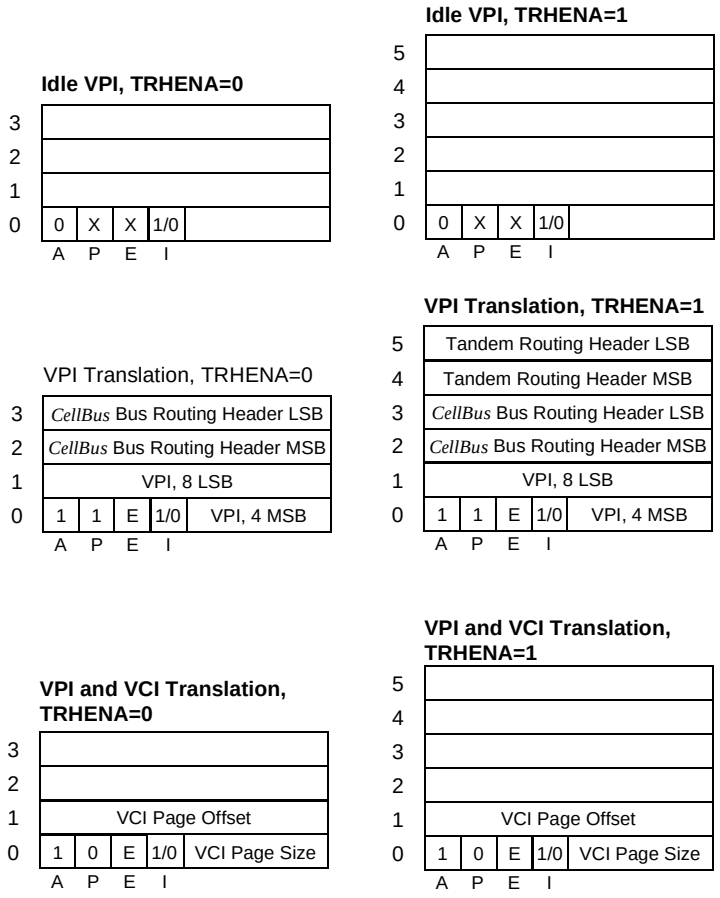
Tandem Routing Header

If the Tandem Routing Header is to be used as a *CellBus* Bus Routing Header, as when passed through a CUBIT-*Pro* in back-to-back mode, it must follow the same construction rules as a *CellBus* Bus Routing Header. If the Tandem Routing Header is used for some proprietary purposes, its format will follow a different specification.

Translation Record Formats

VPI Translation Record Formats

VPI translation records are four bytes long if TRHENA=0, or six bytes long if TRHENA=1, as shown in Figure 20. Each VPI may be either idle or busy. If it is busy, then each VPI may be set for VPI-only translation, or for combined VPI/VCI translation. The control bits (A, P, E and I) and Routing Headers are described in the preceding sections.



If the VPI is unused, then the MSB (Active bit, A) of relative address zero is set to zero, indicating idle. If a cell arrives with this VPI number, it is discarded and is counted as a misrouted cell.

If the VPI is busy and is to have VPI number translation only, then the A bit is set=1, and the P bit is set=1. In this case, the VPI to be inserted on the cell is contained in the 4 LSB of relative address zero (4 MSB of new VPI), and in relative address one (8 LSB of new VPI). *CellBus* Bus and Tandem Routing Headers are also contained in the next two or four bytes.

If the VPI is busy and is set for combined VPI/VCI number translation, a reference is generated to a VCI translation record. The VPI is set active (A=1), and is set for VCI translation (P=0). The 4 LSB of relative address zero contain the VCI Page Size, which is the number of assigned VCI pages, each of 128, 256, 512, or 1024 VCI records, allocated to this VPI (range from 1 to 16, where 0H=16). Relative address one contains the VCI Page Offset, which indicates where among the VCI pages the first utilized page starts.

Figure 20. VPI Translation Record Formats

The calculation of the start address for the VP record when there is no Tandem Routing Header (control bit TRHENA=0) is performed as follows:

$$VP\_Start\_Addr = VP\# \times 4$$

If TRHENA=1 then:

$$VP\_Start\_Addr = VP\# \times 6$$

VCI Translation Record Formats

VCI translation records are six bytes long if TRHENA=0, and eight bytes long if TRHENA=1, as shown in Figure 21. Each VCI may be either idle or busy.

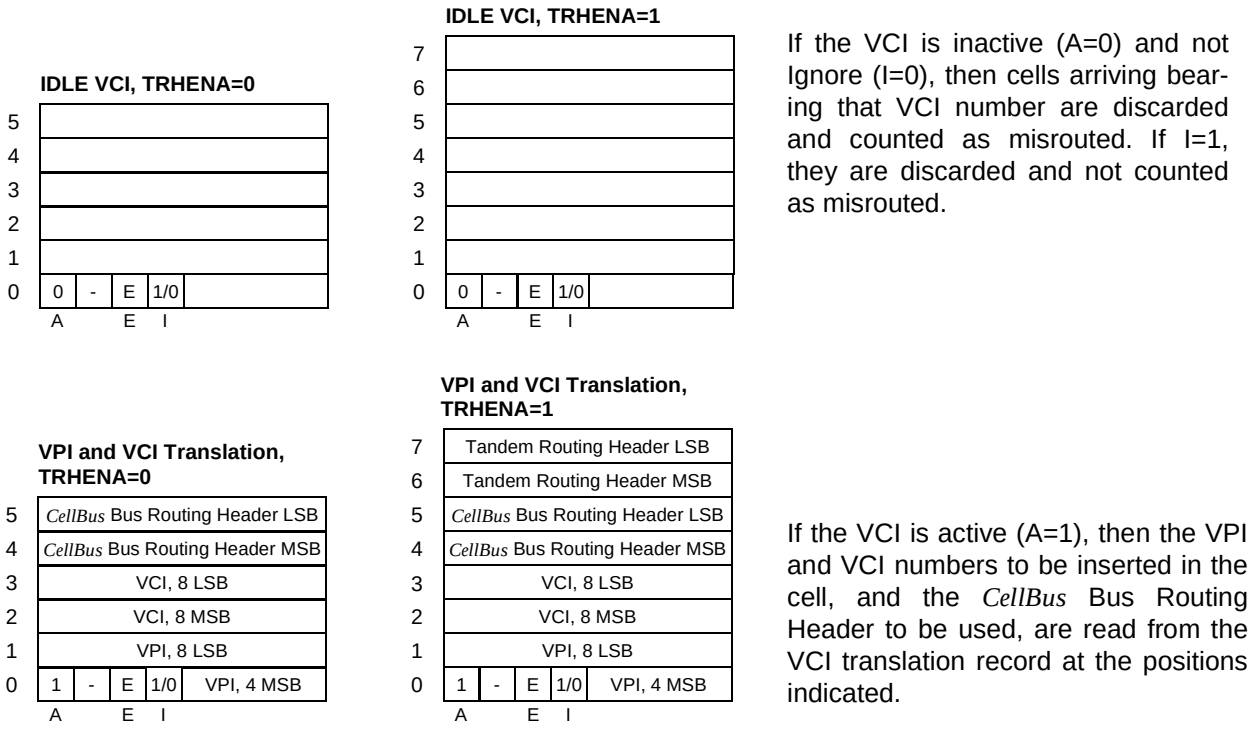


Figure 21. VCI Translation Record Formats

The calculation of the start address for the VC record uses information from the VP table addressed by the VP of the incoming cell, as well as information of the VCI of the incoming cell. The information required from the VP record is the VCI Page Offset (VPO). In the case with no Tandem Header Translation (control bit TRHENA=0 in register 0AH) and in UNI mode (control bit UNI=1 in register 0AH) the start address of the VC record corresponding to an incoming VP/VC, assuming a given number of VCI records per page (VRP, determined by the control bits VRPS1 and VRPS0 in register 0EH) is calculated (in decimal format) as follows:

VC_Start_Address = 1024 + VPO x VRP x 6 + VCI x 6

or with TRHENA=1 and UNI=1:

VC_Start_Address = 1536 + VPO x VRP x 8 + VCI x 8

or with TRHENA=0 and UNI=0:

VC_Start_Address =16384 + VPO x VRP x 6 + VCI x 6

or with TRHENA=1 and UNI=0:

VC_Start_Address = 24576 + VPO x VRP x 8 + VCI x 8.

OAM-Cells and RM-Cells Record Format

OAM/RM and reserved VC cells routing can be performed on any VP/VC combination with the appropriate programming of the E-bit in the VP or VC translation record, and setting OAMRMEN bit (bit 1 in register 0EH) to 1. For compatibility with CUBIT TXC-05801 applications, the bit OAMRMEN should be set to 0 (default).

Both F4 and F5 flows are supported in the CUBIT-*Pro*. Depending on which flow is routed, two algorithms are used by the CUBIT-*Pro* (assuming OAMRMEN=1). The algorithm for F5-flow is depicted in Figure 22. The PT field of the ATM cell header coming in a VP/VC that is set for VP/VC translation (with E-bit set to 1 in the VC translation record) will be checked for all possible values and routed to VCI Page 0 according to the flow shown in Figure 22.

For F4 flow a cell coming in any VP will be sent to VCI Page 0 if the VCI is within numbers 0-31 (OAMRMEN=1) according to the algorithm shown in Figure 23.

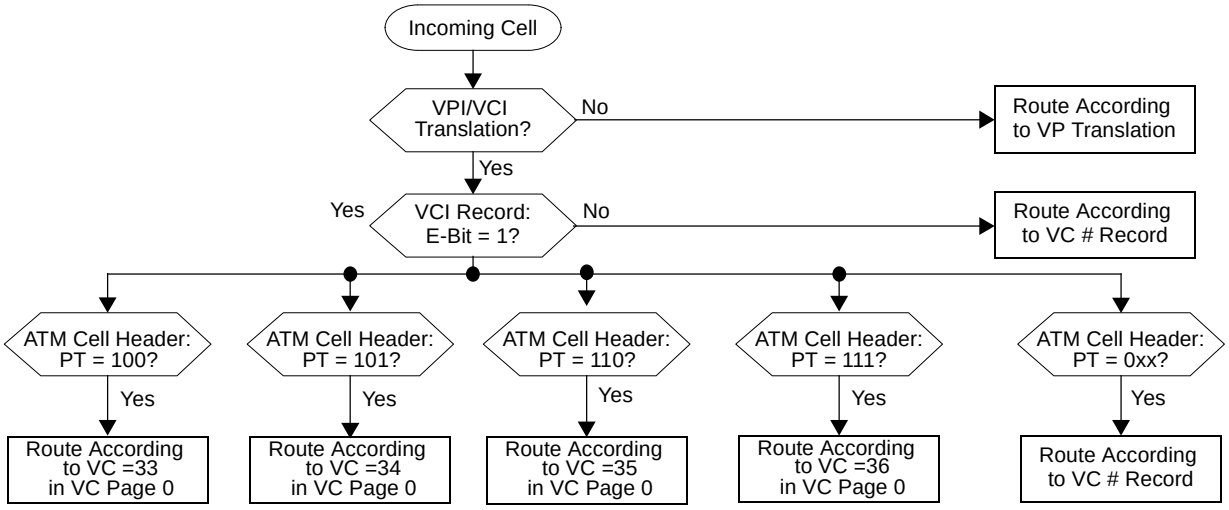


Figure 22. OAM F5 and RM-VCC Cell Routing (Bit OAMRMEN=1)

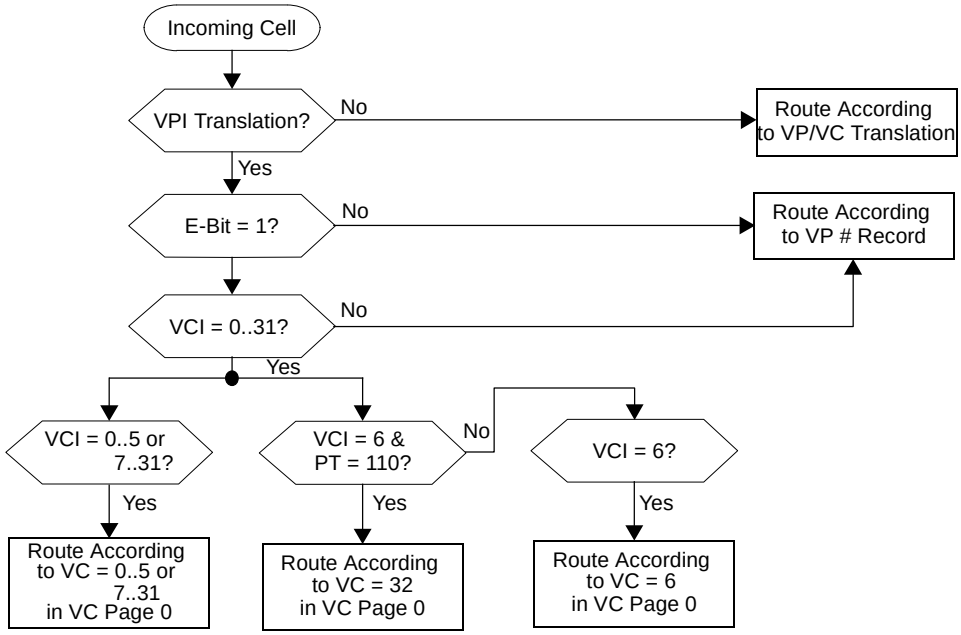
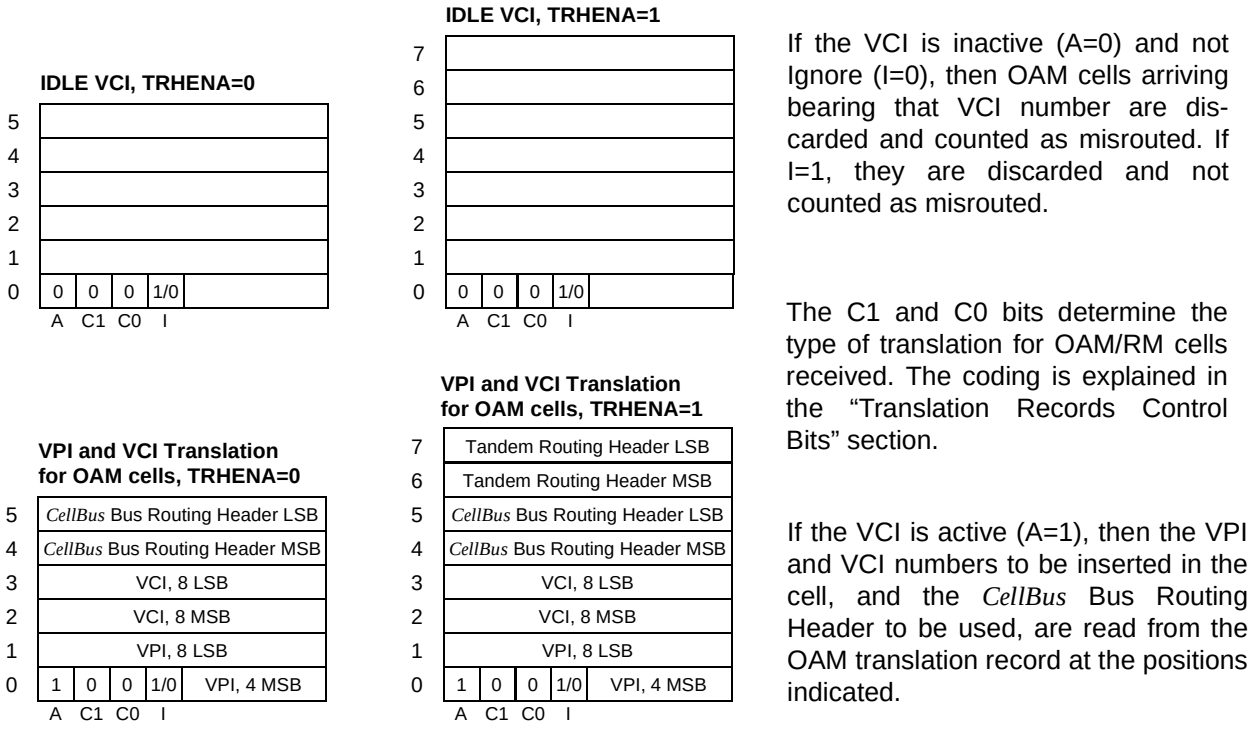


Figure 23. OAM F4 and RM-VPC Cell Routing (Bit OAMRMEN=1)

The corresponding formats for OAM translation records are shown in Figure 24.



If the VCI is inactive (A=0) and not Ignore (I=0), then OAM cells arriving bearing that VCI number are discarded and counted as misrouted. If I=1, they are discarded and not counted as misrouted.

The C1 and C0 bits determine the type of translation for OAM/RM cells received. The coding is explained in the "Translation Records Control Bits" section.

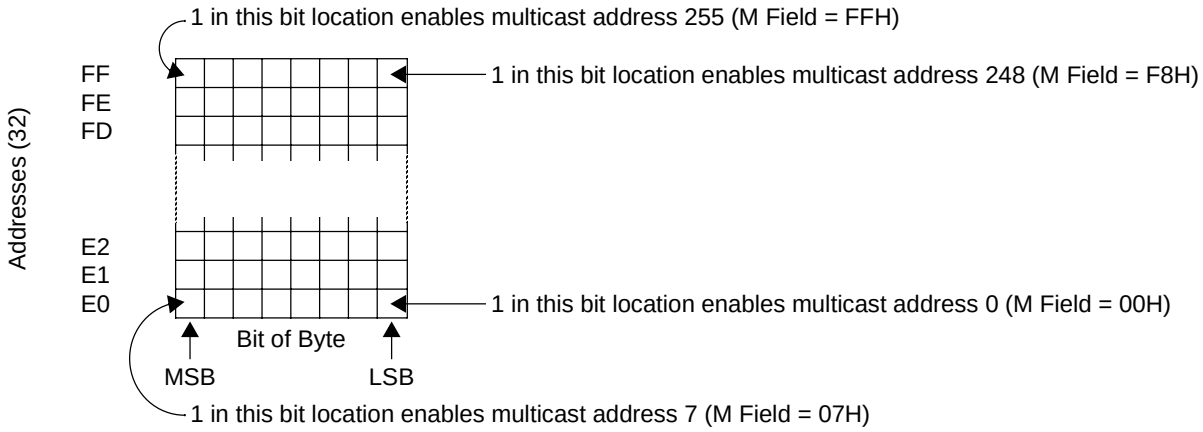
If the VCI is active (A=1), then the VPI and VCI numbers to be inserted in the cell, and the *CellBus* Bus Routing Header to be used, are read from the OAM translation record at the positions indicated.

Note: OAM/RM Translation Records are optional. They are located in VCI page zero.

Figure 24. OAM/RM-Cells Translation Record Formats

MULTICAST NUMBER MEMORY

A multicast address control cell or multicast address data cell can be sent to a number of CUBIT-*Pro*s, and a single CUBIT-*Pro* can receive cells with a number of different addresses. This is controlled by the setup of the Multicast Number Memory (addresses E0H-FFH in the CUBIT-*Pro* memory map), which is a block of 32 bytes. Each of the 256 bits in the block maps to one multicast address, as shown in Figure 25. When a bit is set to 1, the CUBIT-*Pro* is enabled to receive the corresponding multicast address cell. Each CUBIT-*Pro* can be set to receive any or all of the 256 possible multicast addresses.



Note: The M Field refers to the *CellBus* Bus Routing Header for Multicast Address cells (see Figure 5).

Figure 25. Multicast Number Memory

THE *CellBus* BUS INTERFACE

Thirty-seven lines comprise the *CellBus* bus interface, as shown in Figure 2. There are thirty-two Data lines, with Frame, Acknowledge, and Congestion Indicator lines, all sourced by a CUBIT-*Pro* device, and two Clock lines sourced by external drivers.

Operation with Internal GTL Transceivers

Gunning Transceiver Logic (GTL) transceivers for *CellBus* bus Data, Frame, Acknowledge, and Congestion Indicator lines are contained internally in the CUBIT-*Pro*, along with two clock line GTL receivers. Each of the drivers has a maximum current sink capability of 48 mA and is capable of driving a bus on a card or on a back-plane directly. Each of the GTL lines is to be pulled-up at each of its ends by a 50 ohm (+/- 5%) resistor (metal film or carbon composition) to a +1.2 V low-impedance supply. Each end of each line should have a filtering capacitor connected from the +1.2 V supply to ground, as shown in Figure 26.

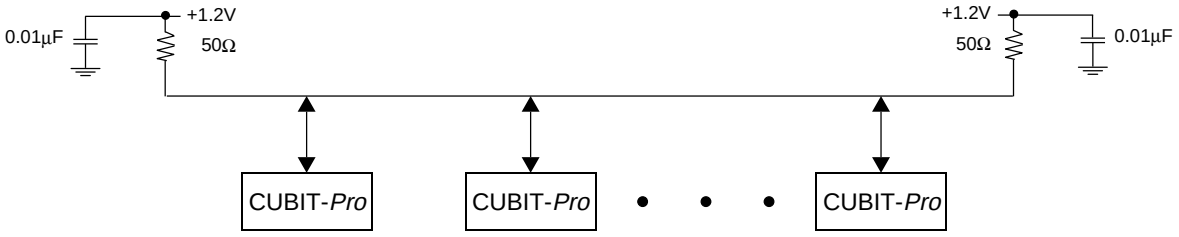


Figure 26. External Circuit Requirements for GTL Transceivers

In the CUBIT-*Pro* pinout, all of the pins involved with the bus interface are aligned along one side of the package between pins 50 and 112. This side of the package must be aligned toward the board connector, or toward the bus, with as little board trace length as possible between the pins and the connector or bus, to maximize operating speed.

Clock Source

Two GTL-level clock signals must be driven to the *CellBus* bus from an external source. These are the write clock, $\overline{\text{CBWC}}$, and the read clock, $\overline{\text{CBRC}}$. A phase relationship keeping the write clock between 0.5 and 4 nanoseconds behind the read clock is needed to ensure proper synchronous bus operation. When the clock driver is driven from the center of the backplane (i.e., no greater than half a backplane length from any card) a minimum phase distance of 0.5 ns or more must be maintained. When the driver is at one of the ends, a more conservative 2-4 ns minimum is required. In any *CellBus* bus implementation, on the backplane and on each card, care must be taken to ensure that these two lines are routed together. The capacitive and inductive loadings of the two lines should be as nearly equal as possible, to maintain performance. At the drive point, a delay line should be used to maintain a stable delay, and the read and write clock drivers must be units of the same integrated circuit package. All of these precautions will ensure the most stable clocks and permit the highest possible operating speed.

Bus Arbiter Selection

One copy of the *CellBus* Bus Arbiter circuitry is included inside each CUBIT-*Pro* device. Enabling of the arbiter on a particular CUBIT-*Pro* is done by connecting the $\overline{\text{ENARB}}$ pin of that device to ground (V_{SS}). Normally, one arbiter is turned on and the remaining arbiters on that bus are turned off. It is the responsibility of the overall system control to decide which CUBIT-*Pro* will have its arbiter enabled, and to enable it. Failure of an arbiter can be detected by using the NOGRT indications. If multiple CUBIT-Pros are indicating NOGRT failures, an arbiter failure is indicated. It is again the responsibility of system control to enable another arbiter.

Upon switching from one arbiter to another, the receiving devices on the bus will automatically re-align to the new frame position within one *CellBus* bus frame.

OUTLET-SIDE QUEUE MANAGEMENT

The CUBIT-*Pro* contains a 123-cell queuing FIFO for data on its outlet side. This FIFO may be operated as a single 123-cell FIFO, or it may be split into four independent FIFOs.

Single Queue Operation

If control bit QM at Address 0CH, Bit 2 is zero, then the outlet has a single 123-cell FIFO. This mode is appropriate when a single type of traffic is to be switched by the system. In this case cell congestion, for purposes of causing a FECN (if enabled by control bit IFECN at Address 0CH, Bit 0), is established by the register VBRLIMIT at Address 12H.

Split-Queue Operation

If QM = 1, the outlet FIFO is split into 4 separate queues. These are, in order of service priority, Control Data (highest priority), CBR, VBR, and ABR. The Control Data cell queue is fixed in length at 2 cells, and the ABR queue at 32 cells. The congestion threshold on the ABR queue is set at 28. The size of the CBR queue is set by the contents of register CBRLEN at Address 10H, and its congestion point by CBRLIMIT at Address 11H. The remaining FIFO cells are assigned to the VBR queue. The length of the VBR queue is (123-2-32-CBRLEN = 89-CBRLEN), and its congestion limit is set by VBRLIMIT at Address 12H.

Note the differences between the control data queue section of the split outlet queue, the control cell receive buffer and the control cell transmit buffer (all referred to as control queue):

1. The control data queue section of the split outlet queue accepts cells from the *CellBus* bus that have a single address data routing header with the Q field set to 00 (see Figure 5).
2. The control cell receive buffer (address 60H-93H) accepts cells from the *CellBus* bus that have a single address control routing header (see Figure 5).
3. The control cell transmit buffer is loaded by the microprocessor with a cell to be sent to the *CellBus* bus. It can have any of the *CellBus* Bus Routing Header formats shown in Figure 5.

Multicast and Broadcast cells in split-queue mode are sent to the VBR and CBR queues, respectively.

MICROPROCESSOR INTERFACE

General Description

The CUBIT-*Pro* Microprocessor Port will support an I/O interface characteristic of either Intel or Motorola microprocessors, as shown in Figure 27.

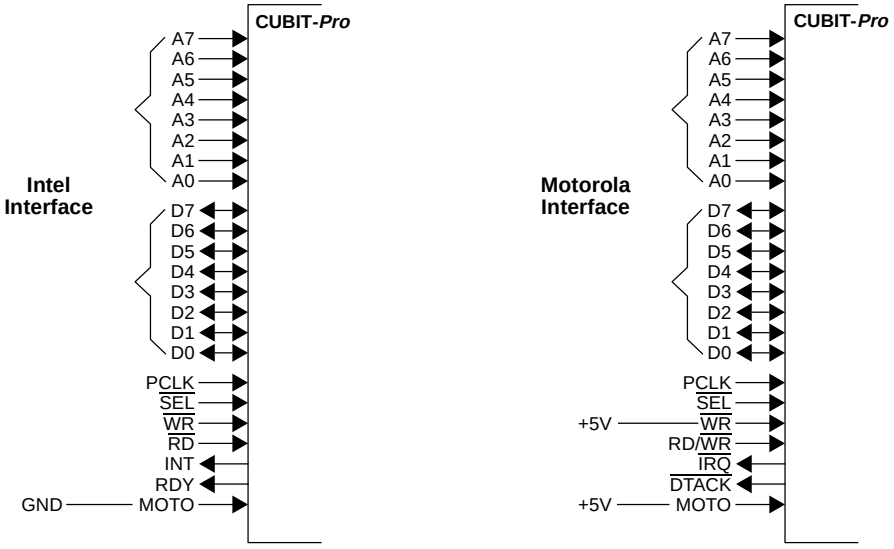


Figure 27. Microprocessor Port Interface Connections

The connections for address A(7-0), data D(7-0), select ($\overline{SEL}$) and processor clock (PCLK) are the same for both cases. Differences are listed below.

Intel Mode

Enabled when device strap MOTO is connected to V_{SS} (ground). Connections are as shown in Figure 27. The differences to support Intel mode are:

$\overline{WR}$ pin is low to execute a write command,

$\overline{RD}$ pin is low to execute a read command,

Interrupt INT is active high,

Ready RDY is active high. When set low, it requests microprocessor wait time.

Motorola Mode

Enabled when device strap MOTO is connected to V_{DD5} (+5V). Connections are as shown in Figure 27. The differences to support Motorola mode are:

$\overline{WR}$ pin is not used and must be pulled up to +5 volts,

RD/$\overline{WR}$ pin is high to execute a read command or low to execute a write command,

Interrupt $\overline{IRQ}$ is active low,

Data Transfer Acknowledge $\overline{DTACK}$ is active low. When inactive, and pulled high by an external pull-up resistor, it requests microprocessor wait time.

Interrupts

The CUBIT-*Pro* allows the generation of interrupts based on thirteen different events. The events are latched in two status registers located at addresses 05H and 08H, as shown in Figures 28 and 29. Any of the events will generate an interrupt provided the corresponding interrupt enable bit, located in registers at addresses 06H and 09H, is set to one.

If any of the events occurs, the corresponding status bit will be set to one. All the status bits in a register are cleared when it is read, except for any bits for which the events still persist. Some enabled interrupts may not be cleared in the absence of the *CellBus* bus clocks. Such interrupts will persist until the clocks are re-applied. It is possible, however, to mask any interrupt regardless of the absence or presence of the *CellBus* bus clocks. The events reported are explained below:

1. Status register at address 05H:

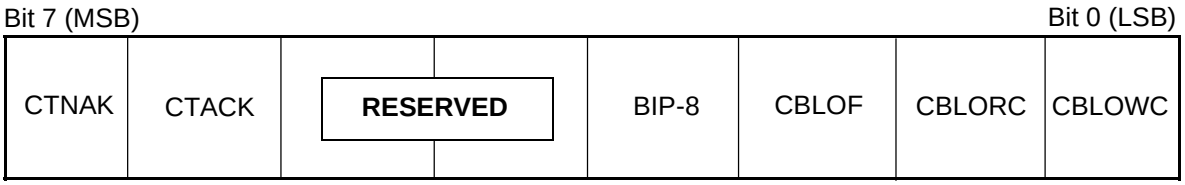


Figure 28. CUBIT-*Pro* Status Register at Address 05H

CTNAK Microprocessor Control Cell Negative Acknowledge:

If a cell is transmitted from the Microprocessor Control queue to the *CellBus* bus and is not received by the destination CUBIT-*Pro*, this bit is set to 1.

CTACK Microprocessor Control Cell Positive Acknowledge:

If a cell is transmitted from the Microprocessor Control queue to the *CellBus* bus and is successfully received by the destination CUBIT-*Pro*, this bit is set to 1.

BIP-8 Error:

If the BIP-8 field (Grant cycle) of the *CellBus* bus cell body in a cell received from the *CellBus* bus does not match the calculated BIP-8, this bit is set to 1 (see Figure 3).

CBLOF *CellBus* Bus Loss of Frame Pulse Error:

In the event that the *CellBus* bus frame pulse is not present for more than 4 consecutive 16-cycle frames, or if the *CellBus* Bus Write Clock is not present, this bit is set to 1.

CBLORC *CellBus* Bus Loss of Read Clock Error:

If the *CellBus* Bus Read Clock is not present, this bit will be set to 1.

CBLOWC *CellBus* Bus Loss of Write Clock Error:

If the *CellBus* Bus Write Clock is not present, this bit will be set to 1.

Note: It is recommended to provide the control processor an independent means of forcing an external hardware reset. In order to insure proper device initialization, after the loss of either the *CellBus* Bus Write Clock or the *CellBus* Bus Read Clock, an external hardware reset must be applied via the $\overline{\text{RESET}}$ pin. The hardware reset must be applied in the presence of all input clock signals.

2. Status register at address 08H:

Bit 7 (MSB) Bit 0 (LSB)

CRCF	CRQOVF	CRQCAV	INSOC	CTSENT	NOGRT	**RESERVED**	OCOVF

Figure 29. CUBIT-*Pro* Status Register at Address 08H

CRCF CRC-4 Error:

If the CRC-4 field H(3-0) of the *CellBus* Bus Routing Header in a cell received from the *CellBus* bus does not match the calculated CRC-4, this bit is set to 1 (see Figure 5).

CRQOVF Control Receive Queue Overflow:

An overflow will occur, and this bit will be set to 1, when more than four cells try to accumulate in the control receive queue.

CRQCAV Control Receive Queue Cell Available:

When a control cell has been received from the *CellBus* bus and placed in the receive buffer (addresses 60H-93H) this bit will be set to 1. This bit is cleared to 0 after the microprocessor writes a 1 to CRQSENT.

INSOC Inlet Start of Cell:

In the ATM Layer Emulation UTOPIA 8-bit ($\overline{\text{PHYEN}}$ = High) and ATM Layer Emulation 16-Bit ($\overline{\text{PHYEN}}$ = High) modes and the Back-to-Back mode, if CISOC is not present in the same clock cycle that CICLAV is asserted, or if CISOC is asserted before the end of the current cell, the INSOC bit is set to 1.

In the PHY Layer Emulation UTOPIA 8-bit ($\overline{\text{PHYEN}}$ = Low) and PHY Layer Emulation 16-Bit ($\overline{\text{PHYEN}}$ = Low) modes, if CISOC is not present in the same clock cycle that $\overline{\text{CIENB}}$ is asserted (after CICLAV has been asserted signaling the transfer of the first byte of the cell), or if CISOC is asserted before the end of the current cell, the INSOC bit is set to 1. If the ONLINE bit is set to 0 to disable cell acceptance at the cell inlet, arrival of a cell will cause INSOC to be set to 1. In order to prevent generation of false interrupts, the interrupt-enable bit for INSOC (INTEN4) should also be set to 0 when ONLINE is set to 0 in PHY layer emulation mode.

In ALI-25 mode, if RDVal is deasserted prematurely an INSOC error will occur.

CTSENT Control Cell Sent:

When the microprocessor requests that a control cell be sent to the *CellBus* bus, this bit will be set to 1 after the cell has been sent.

NOGRT No Grant:

If the CUBIT-*Pro* device has requested a *CellBus* bus grant and has not received it after the number of frames indicated by the TIME register (address 0FH), this bit will be set to 1.

OCOVF Outlet Cell Overflow:

In the single-queue mode an overflow will occur, and this bit will be set to 1, when more than 123 cells try to accumulate in the outlet queue.

In the split-queue mode this overflow will occur if any of the following events occurs:

a. More than 32 cells try to accumulate in the ABR queue
b. More than CBRLEN (address 10H) cells try to accumulate in the CBR queue
c. More than (89 minus CBRLEN) cells try to accumulate in the VBR queue
d. More than 2 cells try to accumulate in the control queue.

Control Queue Send and Receive

The formats of send (transmit) and receive control cells are shown in Figure 30. Reference to Figure 1 will be helpful for understanding how cells are handled by the inlet and outlet control queues.

A cell can be sent from the microprocessor to the *CellBus* bus by using the control cell transmit buffer (Inlet Control Queue in Figure 1). This ability allows the microprocessor to send any type of data, control or loopback cell to any CUBIT-*Pro* on the *CellBus* bus. The microprocessor first writes a 56-byte transmit cell with the format shown in Figure 30 to the control cell transmit buffer (Addresses A0H-D7H in the CUBIT-*Pro* memory map). Then a 1 is written to control bit CTRDY (Address 0AH, Bit 1). The cell will be sent to the *CellBus* bus after any pending data cells, and the CTSENT bit (Address 08H, Bit 3) will then be set to 1 and the CTRDY bit will be reset to 0. Another such cell send sequence may be started after CTSENT has been received.

A four-cell FIFO buffer (Outlet Control Queue in Figure 1) is provided for reception of control cells from the *CellBus* bus, since control cells can arrive from several sources and may have to wait for the microprocessor to accept them from the CUBIT-*Pro*. The FIFO output is the 52-byte memory segment CRQ(51-0) at Addresses 93H-60H. When this segment acquires a received control cell the CUBIT-*Pro* sets its interrupt bit CRQCAV to 1 (Address 08H, Bit 5). This bit may be enabled to cause an interrupt to the microprocessor (by setting interrupt enable bit INTEN5 to 1 in Address 09H, Bit 5). When an interrupt or polling process causes the microprocessor to read the interrupt event status register at Address 08H it will detect the CRQCAV indication that a control cell is available for reading. It must then read CRQ(51-0) and set control bit CRQSENT to 1 upon completion (Address 0AH, Bit 0). This notifies the CUBIT-*Pro* to reset CRQCAV to 0 and place the next control cell in CRQ(51-0), either immediately from the adjacent FIFO cell, if occupied, or whenever the next cell arrives in the FIFO from the *CellBus* bus. The CUBIT-*Pro* resets CRQSENT to 0.

The CUBIT-*Pro* has a handshake mechanism whereby an interrupt can be generated indicating whether the cell was received or not. Two bits are available, CTACK and CTNAK (bits 6 and 7 in register 05H) which are set if the cell sent from the microprocessor interface was or was not accepted at the destination, respectively. These interrupts are enabled by setting to 1 bits 6 and 7 in register 06H (INTENA6 and INTENA7).

Control cell transmission and reception may still be performed regardless of the state of control bit ONLINE (Address 0CH, Bit 7).

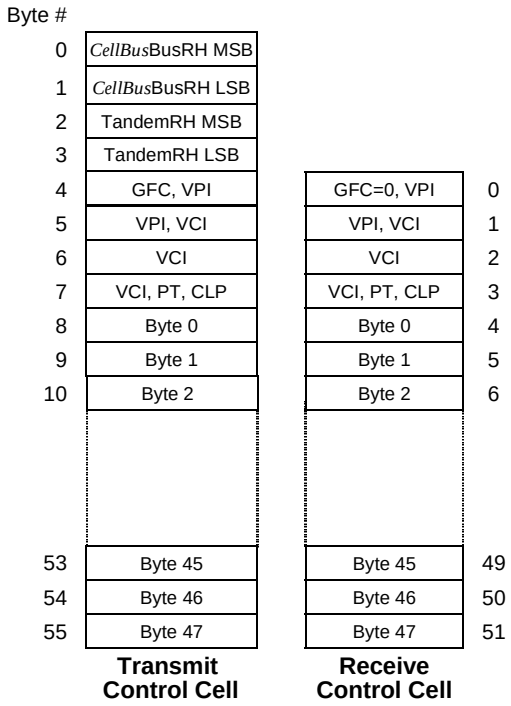
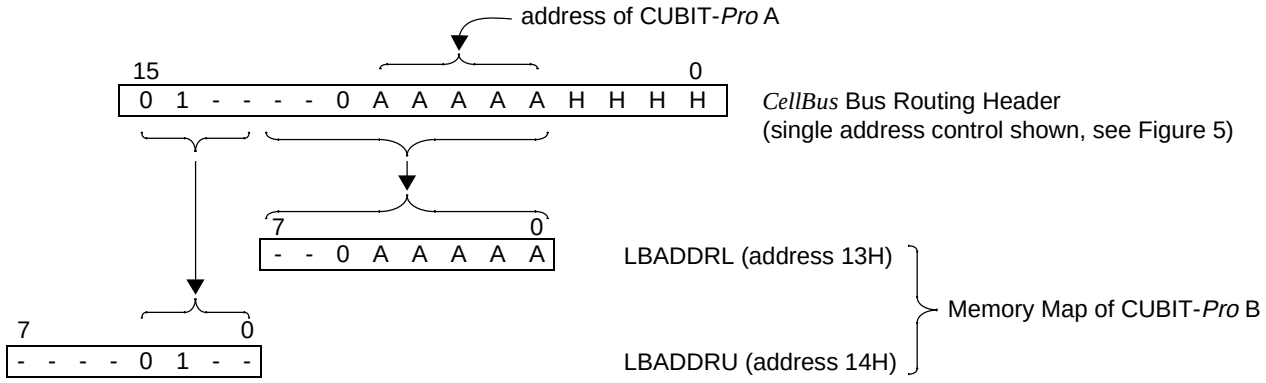


Figure 30. Transmit and Receive Control Cell Formats

LOOPBACK CELL SEND, RECEIVE AND RELAY

The loopback function is provided for diagnostic purposes. It may be used on-line (ONLINE = 1), or off-line (ONLINE = 0). A loopback path for a cell from CUBIT-*Pro* A to CUBIT-*Pro* B and back to CUBIT-*Pro* A can be set up by loading the LBADDR registers in Addresses 13H and 14H of CUBIT-*Pro* B with the single address control *CellBus* Bus Routing Header of CUBIT-*Pro* A, as shown in Figure 31. The microprocessor then writes a cell with a single address loopback Routing Header for CUBIT-*Pro* B into the control transmit buffer (Addresses A0H-D7H) of CUBIT-*Pro* A and causes the cell to be sent. When CUBIT-*Pro* B receives the cell it will use the contents of LBADDR to form a new Routing Header for the cell and send it back to CUBIT-*Pro* A. CUBIT-*Pro* A will receive the cell and place it in the control receive buffer where it can be examined by the microprocessor.

The above description assumes that the loopback cell originates in the control transmit buffer of CUBIT-*Pro* A, but it could also be received from the inlet port. Any of the seven Routing Header formats shown in Figure 5 could actually be loaded in the LBADDR register of CUBIT-*Pro* B instead of the single address control *CellBus* Bus Routing Header of CUBIT-*Pro* A, with a corresponding change in the final destination of the loopback cell.



Note: - indicates don't care state

Figure 31. Loading the Loopback Registers

All aspects of system operation are the responsibility of the control system implemented for use of the CUBIT-*Pro* devices. Care must be taken to ensure that no more than one CUBIT-*Pro* is trying to set up a loop-back into the same CUBIT-*Pro*, or mis-routing will ensue.

MEMORY MAP RESET STATES

The general conditions for resetting the memory map states are:

1. all input clock signals are present, and
2. the $\overline{\text{DEVHIZ}}$ and $\overline{\text{TSTMODE}}$ input pins are high.

There are two alternative reset conditions that reset the memory map registers 04H through FFH to the values shown in the following table:

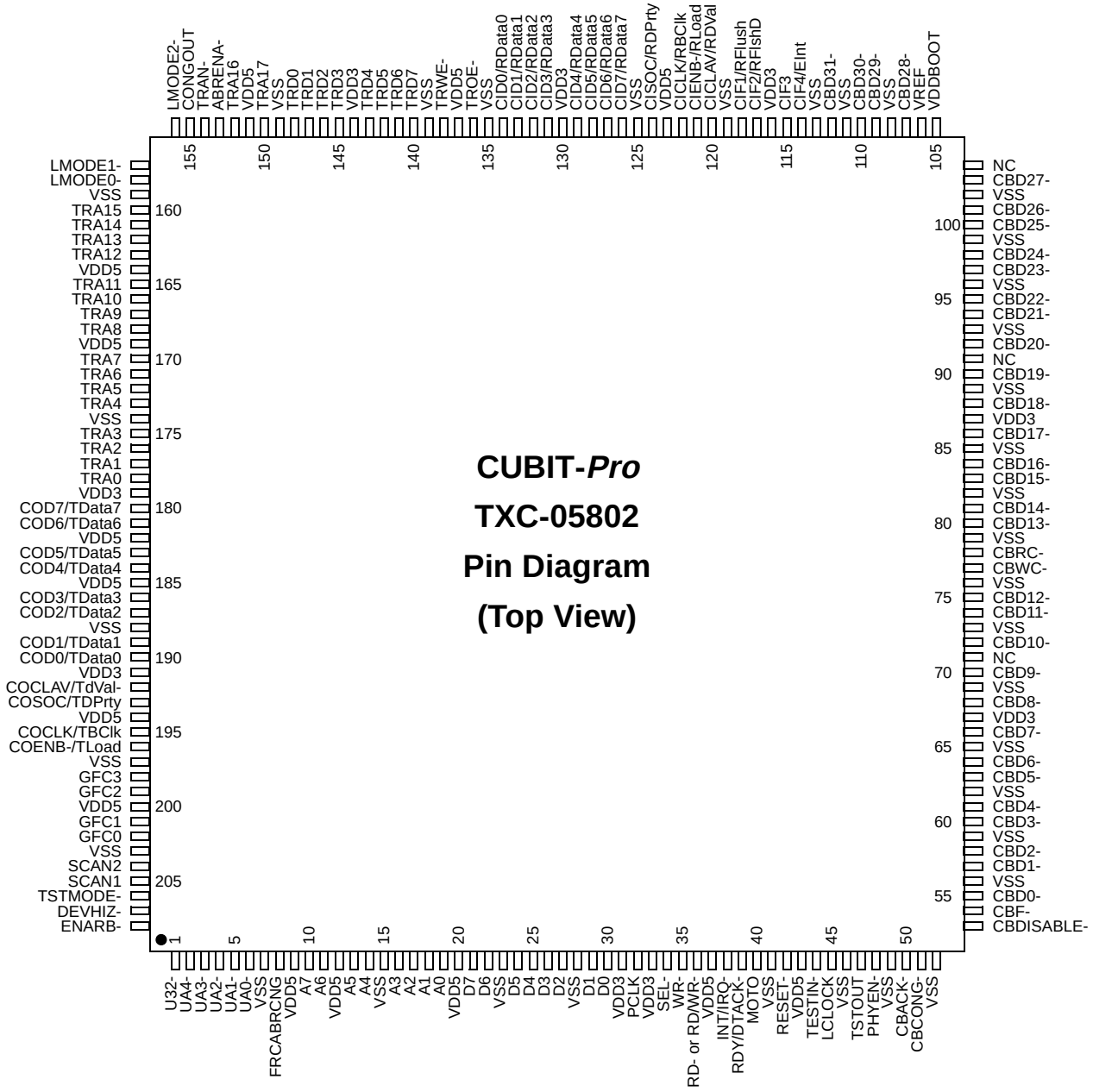
1. power-up, or
2. hardware reset applied via the $\overline{\text{RESET}}$ input pin.

Address (Hex)	0A	17	1E	60 - 93, A0-D7	E0 - FF	Others
Reset Value (Hex)	40	XX(1)	XX(2)	XX(3)	XX(3)	00(4)

Notes:

1. Reset value depends on content of location 00H in TRAM.
2. Reset value depends on state of pins $\overline{\text{ABRENA}}$, $\overline{\text{U32}}$, $\overline{\text{ENARB}}$ and $\overline{\text{UA(4-0)}}$.
3. Undefined value after power-up. Pre-existing value is not affected by hardware reset.
4. Except reserved addresses, which contain undefined values after power-up and hardware reset.
5. It is recommended to provide the control processor an independent means of forcing an external hardware reset. In order to insure proper device initialization, after the loss of either the *CellBus* Bus Write Clock or the *CellBus* Bus Read Clock, an external hardware reset must be applied via the $\overline{\text{RESET}}$ pin. The hardware reset must be applied in the presence of all input clock signals.

PIN DIAGRAM



Note: Due to space limitations, active low (inverted) or active-on-falling-edge signals are indicated by '-' at the end of their symbol (e.g., LMODE1- is equivalent to $\overline{\text{LMODE1}}$).

Figure 32. CUBIT-*Pro* TXC-05802 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT PINS

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD5	9, 12, 20, 37, 43, 123, 137, 151, 164, 169, 182, 185, 194, 200	P		$\mathbf{V_{DD5}}$: +5 volt supply voltage, ±5%
VDD3	31, 33, 67, 87, 116, 130, 144, 179, 191	P		$\mathbf{V_{DD3}}$: +3.3 volt supply voltage, ±5%
VSS	7, 15, 23, 28, 41, 46, 49, 52, 56, 59, 62, 65, 69, 73, 76, 79, 82, 85, 89, 93, 96, 99, 102, 108, 111, 113, 119, 125, 135, 139, 149, 159, 174, 188, 197, 203	P		$\mathbf{V_{SS}}$: Ground, 0 volt reference.
VDDBOOT	105	P		**VDDBOOT:** +5V supply voltage, ± 10%, which must be present for the *CellBus* bus disable function to work.
NC	71, 91, 104	--		**No Connect**: NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of NC pins may impair performance or cause damage to the device. Some NC pins may be assigned functions in future upgrades of the device. Compatibility of the CUBIT-*Pro* TXC-05802 device in existing CUBIT TXC-05801 applications may rely upon these pins having been left floating.

* Note: I=Input; O=Output; OD=Open Drain Output; P=Power

CELL INLET

Symbol**	Pin No.	I/O/P	Type*	Name/Function
CICLAV/ RDVal	120	I/O	TTL/ TTL 4 mA	**Cell Inlet Cell Available:** The direction of the CICLAV signal depends on the mode selected: ATM Layer emulation: An active high input signal from the PHY Layer device to indicate that it has a complete cell to transfer. This applies to UTOPIA and 16-Bit modes. PHY Layer emulation: An active high output signal to indicate that the CUBIT-*Pro* has space to receive a cell from the ATM Layer device. This applies to UTOPIA and 16-Bit modes. Back-to-Back mode: CICLAV is an active high input signal. ALI-25 mode: RDVal signal (input).
CICLK/ RBClk	122	I/O	TTL/ TTL 6 mA	**Cell Inlet Clock:** Transfer clock. Rising edge of CICLK is used for data transfer. ATM Layer emulation: The clock is an output. This applies to UTOPIA and 16-Bit modes. PHY Layer emulation: The clock is an input. This applies to UTOPIA and 16-Bit modes. Back-to-Back mode: The clock is an output. ALI-25 mode: RBClk signal (output). Maximum clock speed of 42 MHz with a 40/60 duty cycle.
CID(7-4) CID(3-0)/ RData(7-0)	126-129, 131-134	I	TTL	**Cell Inlet Data:** Byte-parallel input data. RData(7-0) input in ALI-25 mode.
$\overline{\text{CIENB}}$/ RLoad	121	I/O	TTL/ TTL 4 mA	**Cell Inlet Enable:** The direction of the $\overline{\text{CIENB}}$ signal depends on the mode selected: ATM Layer emulation: An active low output signal indicating that input data and CISOC will be sampled at the end of the next cycle. This applies to UTOPIA, 16-Bit, and Back-to-Back modes. PHY Layer emulation: An active low input signal indicating that input data and CISOC will be sampled at the end of the next clock cycle. This applies to UTOPIA and 16-Bit modes ALI-25 mode: RLoad signal (output).
CIF1/ RFlush	118	O	TTL 4 mA	**Cell Inlet Flag 1:** Active high positive cell receipt acknowledge (ACK) in UTOPIA, 16-Bit, and Back-to-Back modes. RFlush in ALI-25 mode.
CIF2/RFlshD	117	I	TTL	**Cell Inlet Flag 2:** Pin not used for PHY in UTOPIA, 16-Bit and Back-to-Back modes. RFlshd in ALI-25 mode.
CIF3	115	O	TTL 4 mA	**Cell Inlet Flag 3:** Active high cell rejection indication (NACK) in UTOPIA, 16-Bit and Back-to-Back modes. Disregard in ALI-25 mode.
CIF4/EInt	114	I	TTL	**Cell Inlet Flag 4:** EInt in ALI-25 mode.
CISOC/ RDPrty	124	I	TTL	**Cell Inlet Start of Cell:** Start-of-Cell indication for UTOPIA and 16-Bit modes. RDPrty parity in ALI-25 mode. (Note: Parity output of ALI-25 device is ignored by the CUBIT-*Pro*).

* See Input, Output and I/O Parameters section for Type definitions.
** Signals which are active when low or upon their falling edges are shown as negated (overlined).

CELL OUTLET

Symbol	Pin No.	I/O/P	Type	Name/Function
COCLAV/ $\overline{\text{TdVal}}$	192	I/O	TTL/ TTL 4 mA	**Cell Outlet Cell Available:** The direction of the COCLAV signal depends on the mode selected: ATM Layer emulation: An active high input from the PHY layer device to indicate that it can accept the transfer of a complete cell. This applies to UTOPIA and 16-Bit modes PHY Layer emulation: An active high output that the CUBIT-*Pro* asserts to indicate that it can transfer a complete cell to the ATM layer device. This applies to UTOPIA and 16-Bit modes. Back-to-Back mode: COCLAV is an active high output signal. ALI-25 mode: $\overline{\text{TdVal}}$ signal (output).
COCLK/ TBClk	195	I/O	TTL/ TTL 6 mA	**Cell Outlet Clock:** Transfer clock. Rising edge of COCLK is used for data transfer. ATM Layer emulation: This is an output clock. This applies to UTOPIA and 16-Bit modes. PHY Layer emulation: This is an input clock. This applies to UTOPIA, Back-to-Back, and 16-Bit modes. ALI-25 mode: TBClk signal (input). Maximum clock speed of 42 MHz with a 40/60 duty cycle.
COD(7-6) COD(5-4) COD(3-2) COD(1-0)/ TData(7-0)	180, 181, 183, 184, 186, 187, 189, 190	O	TTL 4 mA	**Cell Outlet Data:** Byte-parallel output data. TData(7-0) output in ALI-25 mode.
$\overline{\text{COENB}}$/ TLoad	196	I/O	TTL/ TTL 4 mA	**Cell Outlet Enable:** An active low enable signal which occurs during clock cycles when COD(7-0) data and/or COSOC are active. ATM Layer emulation: An active low output signal. This applies to UTOPIA and 16-Bit modes. PHY Layer emulation: An active low input signal. This applies to UTOPIA and 16-Bit modes. Back-to-Back mode: $\overline{\text{COENB}}$ is an active low input signal. ALI-25 mode: TLoad signal (input).
COSOC/ TDPrty	193	O	TTL 4 mA	**Cell Outlet Start of Cell:** Start-of-Cell for UTOPIA and 16-Bit modes. TDPrty parity output in ALI-25 mode.
GFC(3-2) GFC(1-0)	198, 199, 201, 202	I	TTLp	**Generic Flow Control:** Inlet for GFC nibble to be inserted at cell outlet.
FRCABRCNG	8	I	TTLp	**Force ABR Congestion:** Active high signal to force a congestion indication for any ABR cells received.
LCLOCK	45	I	TTLp	**Line Clock:** Rising edge used for data transfer. This clock input is used for the cell Inlet/Outlet timing assuming that CLKS1,CLKS0=0,1 in register 0BH.

CellBus BUS PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{CBACK}}$	50	I/O	GTL	***CellBus* Bus Acknowledge:** Active low acknowledge.
$\overline{\text{CBCONG}}$	51	I/O	GTL	***CellBus* Bus Congestion Indicator:** Active low congestion indicator.
$\overline{\text{CBD(31-24)}}$	112, 110, 109, 107, 103, 101, 100, 98	I/O	GTL	***CellBus* Bus Data:** Active low 32-bit parallel data input/output bus.
$\overline{\text{CBD(23-16)}}$	97, 95, 94, 92, 90, 88, 86, 84	I/O	GTL	
$\overline{\text{CBD(15-8)}}$	83, 81, 80, 75, 74, 72, 70, 68	I/O	GTL	
$\overline{\text{CBD(7-0)}}$	66, 64, 63, 61, 60, 58, 57, 55	I/O	GTL	
$\overline{\text{CBF}}$	54	I/O	GTL	***CellBus* Bus Frame:** 16-clock cycle structure.
$\overline{\text{CBRC}}$	78	I	GTL	***CellBus* Bus Read Clock:** Accepts data from bus. Falling edge used for data transfer.
$\overline{\text{CBWC}}$	77	I	GTL	***CellBus* Bus Write Clock:** Puts data on the bus. Falling edge used for data transfer.
CONGOUT	155	O	TTL 4 mA	***CellBus* Bus Congestion:** If EBP=1, indicates congestion or impending congestion detected after the CUBIT-*Pro* sends a cell to the *CellBus* bus. This indication is provided in UTOPIA, 16-Bit and Back-to-Back Modes. If EBP=0 this signal is a GTL-to-CMOS translation of *CellBus* bus signal $\overline{\text{CBCONG}}$.
$\overline{\text{CBDISABLE}}$	53	I	CMOS	***CellBus* Bus Disable:** Active low signal to tri-state the entire *CellBus* bus regardless of the state of the V_{DD3} and V_{DD5} power supplies. (This signal is not part of the *CellBus* bus.)
VREF	106	I	Reference Voltage	**VREF:** Reference voltage for GTL receivers. VREF is approximately 2/3 V_{tt}, where V_{tt} is the backplane termination voltage (nominally Vtt = +1.2V). The input connection to this pin is not part of the *CellBus* bus.

MICROPROCESSOR PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
A(7-6) A(5-4) A(3-0)	10, 11, 13, 14, 16-19	I	TTL	**Address Bus:** 8-bit address lines from microprocessor, used to address CUBIT-*Pro* register memory. A0 is LSB. High is logic 1.
D(7-6) D(5-2) D(1-0)	21, 22, 24-27, 29, 30	I/O	TTL/ TTL 8 mA	**Data Bus:** Bidirectional 8-bit data lines used for transferring data to and from microprocessor. D0 is LSB. High is logic 1.
INT/$\overline{\text{IRQ}}$	38	O	TTL 4 mA	**Interrupt:** Active high for Intel, active low for Motorola.
MOTO	40	I	TTL	**Motorola Mode:** Select Motorola operation if high, Intel if low.
PCLK	32	I	TTL	**Processor Clock:** Rising edge used for data transfer.
$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	36	I	TTL	**Read/Write:** Data transfer command for CUBIT-*Pro* memory. Read (low) for Intel. Read (high) / Write (low) for Motorola.
RDY/$\overline{\text{DTACK}}$	39	OD	TTL 6 mA	**Ready or Data Transfer Acknowledge:** Active high Ready for Intel, active low Data Transfer Acknowledge for Motorola. This output is an open-drain buffer which requires an external pull-up resistor.
$\overline{\text{SEL}}$	34	I	TTL	**Select:** Active low signal to enable data transfer.
$\overline{\text{WR}}$	35	I	TTL	**Write:** Active low write command for transferring data to CUBIT-*Pro* memory in Intel mode. This input must be held high in Motorola mode.

TRANSLATION RAM ACCESS PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
TRA(17-16) TRA(15-12) TRA(11-8) TRA(7-4) TRA(3-0)	150, 152, 160-163, 165-168, 170-173, 175-178	O	TTL 4 mA	**Translation RAM Address Bus:** 18-bit address output for up to 256k byte Translation RAM. TRA(7-0) are cell data outlet 8 LSB if $\overline{\text{ABRENA}}$ is enabled. TRA0 is LSB. High is logic 1.
TRD (7-4) TRD (3-0)	140-143, 145-148	I/O	TTL/ TTL 4 mA	**Translation RAM Data Bus:** Bidirectional 8-bit data bus. TRD(7-0) are cell data inlet 8 LSB if $\overline{\text{ABRENA}}$ is enabled. TRD0 is LSB. High is logic 1.
$\overline{\text{TROE}}$	136	O	TTL 4 mA	**Translation RAM Output Enable:** Active low output enable.
$\overline{\text{TRWE}}$	138	O	TTL 4 mA	**Translation RAM Write Enable:** Active low write enable.

CONTROL STRAPS

Symbol*	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{ABRENA}}$	153	I	TTLp	**16-Bit Mode Enable:** Active low signal to select the 16-Bit operating mode. The additional 8 data bits are carried by TRD(7-0) acting as the 8 LSB for cell data inlet and by TRA(7-0) acting as the 8 LSB for cell data outlet.
$\overline{\text{DEVHIZ}}$	207	I	TTLp	**Device High Impedance:** Active low signal to set all outputs to high-impedance (Hi-Z) state.
$\overline{\text{ENARB}}$	208	I	TTLp	**Enable Arbiter:** Active low signal to enable internal copy of Bus Arbiter and Frame Pulse Generator.
$\overline{\text{LMODE2}}$ $\overline{\text{LMODE1}}$ $\overline{\text{LMODE0}}$	156, 157, 158	I	TTLp	**Operating Mode:** Three active low signals for selection of CUBIT-*Pro* cell Inlet/Outlet operating mode. Please see Figures 6-9, 11, 12 for details.
$\overline{\text{TRAN}}$	154	I	TTLp	**Translation Enable:** An active low signal to enable header translation by the CUBIT-*Pro*.
$\overline{\text{UA(4-0)}}$	2-6	I	TTLp	**Unit Address:** Five active low device identity straps, used to identify each CUBIT-*Pro* device in a system containing up to 32 devices.
$\overline{\text{U32}}$	1	I	TTLp	**Unit 32:** Control strap for setting maximum number of CUBIT-Pros that can be connected to the *CellBus* bus. Set low for 32 CUBIT-Pros, high (or floating) for 16.
$\overline{\text{PHYEN}}$	48	I	TTLp	**PHY Layer Enable:** a low enables PHY Layer emulation in UTOPIA and 16-Bit modes

* Note: All control straps are active low inputs. They are pulled up internally and will be inactive if left unconnected. They must be set low to enable the associated function.

RESET AND TEST PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RESET}}$	42	I	TTL	**Reset:** Active low device reset (minimum duration 300 nanoseconds).
$\overline{\text{TSTMODE}}$	206	I	--	**Test Mode:** Active low signal to enable device test by manufacturer. Tie to V_{DD5}.
SCAN1	205	I	--	**Scan 1:** Internal test function. Tie to V_{SS}.
SCAN2	204	I	--	**Scan 2:** Internal test function. Tie to V_{SS}.
TSTOUT	47	O	--	**Internal Test Pin:** Leave floating.
$\overline{\text{TESTIN}}$	44	I	--	**Internal Test Mode Input:** Tie to V_{DD5}.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage, +5V	V_{DD5}	-0.3	+7.0	V	Note 1
Supply voltage, +3.3V	V_{DD3}	-0.3	+6.0	V	Note 1
DC input voltage	V_{IN}	-0.3	V_{DD5} +0.3	V	Note 1
Storage temperature range	T_S	-55	+150	^oC	Note 1
Component Temperature x Time	TI		+270 x 5	^oC x s	Note 1
Ambient operating temperature	T_A	-40	+85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		29.5		$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD5}	4.75	5.00	5.25	V	
I_{DD5}		25	48	mA	See Notes 1 and 2
P_{DD5}		125	250	mW	See Notes 1 and 2
V_{DD3}	3.14	3.30	3.46	V	
I_{DD3}		106	289	mA	See Notes 1 and 2
P_{DD3}		350	1000	mW	See Notes 1 and 2
V_{DDBOOT}	4.75	5.00	5.25	V	
I_{DDBOOT}		0.01	0.10	mA	See Note 2
P_{DDBOOT}		0.05	0.525	mW	See Note 2
P_{TOTAL}		475	1250	mW	See Notes 1 and 2

Notes:
1. Typical values are based on measurements made with nominal voltages, 25 ^oC ambient, and 40 MHz UTOPIA and *CellBus* bus clocks.
2.) All I_{DD} and P_{DD} values are dependent upon V_{DD} and the bus operation.

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	$0.7 * V_{DD5}$			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			$0.2 * V_{DD5}$	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current	-10	1	10	µA	
Input capacitance		5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	
Input capacitance		5		pF	

INPUT PARAMETERS FOR TTLp (TTL WITH INTERNAL PULL-UP)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input current	-35	-115	-214	µA	$V_{IN}=V_{SS}$
Input leakage current			10	µA	$V_{IN}=V_{DD5}$
Input capacitance		5		pF	

OUTPUT PARAMETERS FOR TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -4.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 4.0 mA
Tri-state leakage current	-10		10	µA	
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

OUTPUT PARAMETERS FOR 6 mA (OPEN-DRAIN)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.4	V	V_{DD}=4.75; I_{OL}= 6.0 mA
I_{OL}			6.0	mA	

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to V_{DD5}. If this resistor is not provided the output behaves as tri-state.

OUTPUT PARAMETERS FOR TTL 6 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -6.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 6.0 mA
Tri-state leakage current	-10		10	µA	
I_{OL}			6.0	mA	
I_{OH}			-6.0	mA	

OUTPUT PARAMETERS FOR TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -8.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 8.0 mA
Tri-state leakage current	-10		10	µA	
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

INPUT/OUTPUT PARAMETERS FOR GTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.86				$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.66	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5	6.0	pF	
V_{OL}	0.2		0.4	V	
Tri-state leakage current	-10		10	µA	
I_{OL}		33	48	mA	

INPUT/OUTPUT PARAMETERS FOR TTL/TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

INPUT/OUTPUT PARAMETERS FOR TTL/TTL 6 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -6.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 6.0$
I_{OL}			6.0	mA	
I_{OH}			-6.0	mA	

INPUT/OUTPUT PARAMETERS FOR TTL/TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

TIMING CHARACTERISTICS

Detailed timing diagrams for the CUBIT-*Pro* device are provided in Figures 33 through 54, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum load capacitance of 25 pF unless otherwise indicated. Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ for input signals or $(V_{OH}+V_{OL})/2$ for output signals.

DUTY CYCLE OF INPUT CLOCK SIGNALS

The duty cycle of the input clock signals is defined as the ratio of the duration of the high pulse to the clock signal period, express as a percentage. The required duty cycle values are defined in the following table:

Input Clock Symbol	Input Clock Duty Cycle			
	Min	Typ	Max	Unit
CICLK	40		60	%
PCLK	40		60	%
COCLK	40		60	%
LCLOCK	40		60	%
CBRC	40		60	%
CBWC	40		60	%

FREQUENCY OF INPUT CLOCK SIGNALS

The required frequency values are defined in the following table:

Input Clock Symbol	Input Clock Frequency			
	Min	Typ	Max	Unit
CICLK			42	MHz
PCLK			42	MHz
COCLK			42	MHz
LCLOCK			42	MHz
CBRC			42	MHz
CBWC			42	MHz

CONTROL / TRANSLATION RAM INTERFACE

The timing for the translation RAM interface has to be referenced to the appropriate clock selection for the cell inlet clock. Therefore, the timing shown in Figures 33 and 34 shows timings with respect to four different clocks:

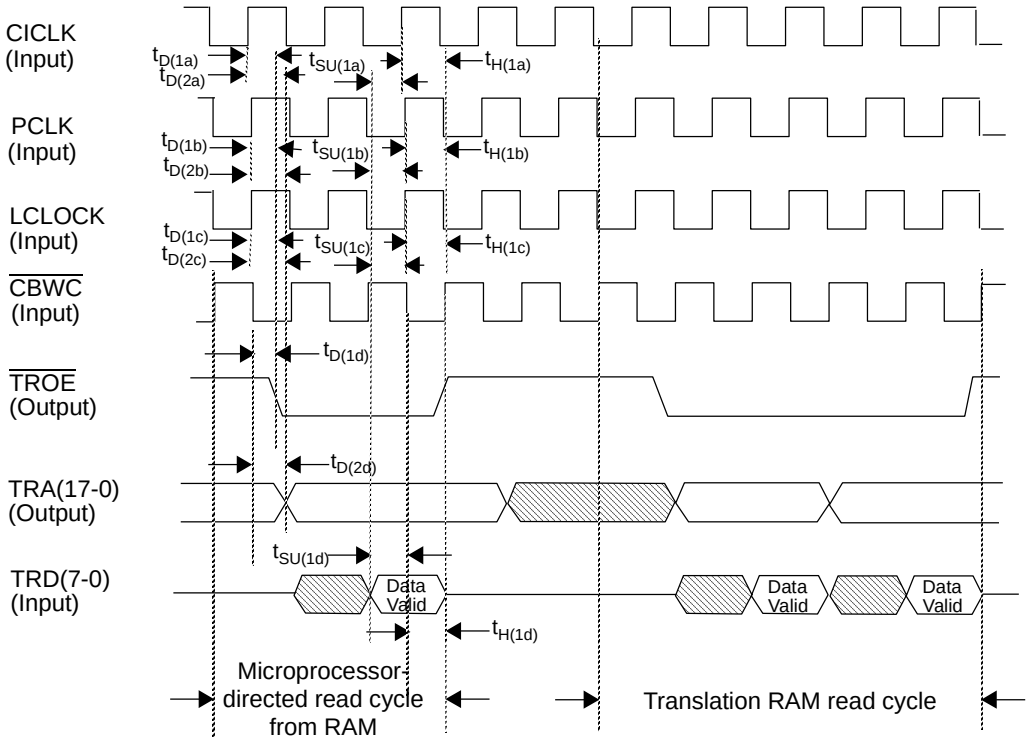
$\overline{\text{CBWC}}$: CLKS[1:0] = 0,0 in UTOPIA/16-Bit (ATM Layer), Back-to-Back, and ALI-25 modes

LCLOCK: CLKS[1:0] = 0,1 in UTOPIA/16-Bit (ATM Layer), Back-to-Back, and ALI-25 modes

PCLK: CLKS[1:0] = 1,0 in UTOPIA/16-Bit (ATM Layer), Back-to-Back, and ALI-25 modes

CICLK: $\overline{\text{PHYEN}}$ = Low only for UTOPIA/16-Bit (PHY Layer)

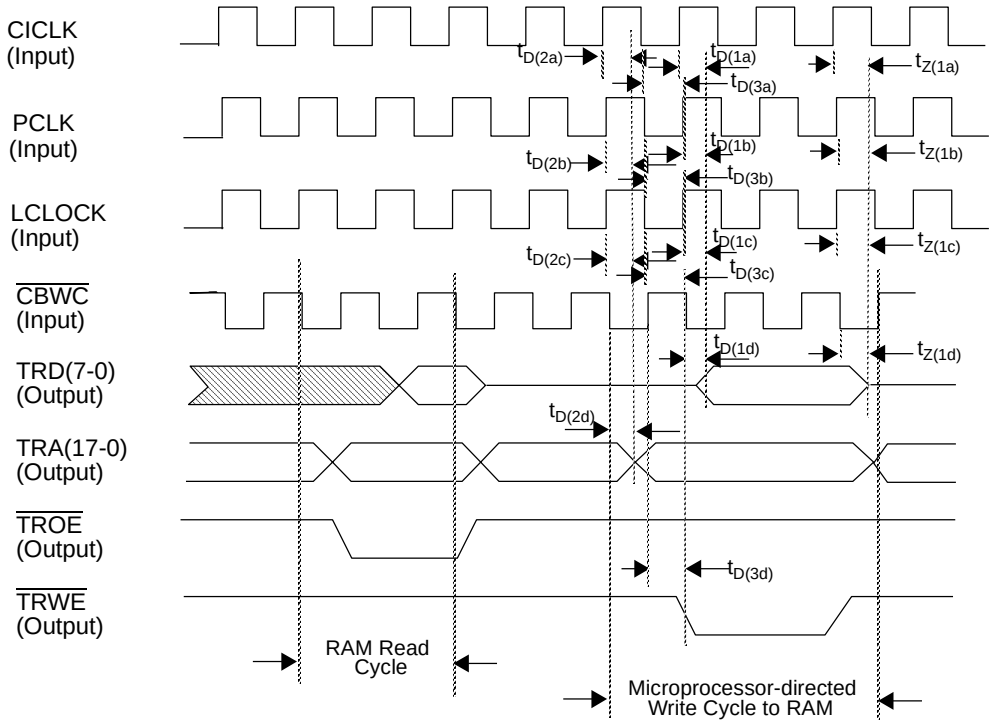
Figure 33. Translation RAM Timing - Read from RAM



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{TROE}}$ output delay after CICLK↑ (PHY Mode)	$t_{D(1a)}$	4.0		14	ns
$\overline{\text{TROE}}$ output delay after PCLK↑	$t_{D(1b)}$	4.0		16	ns
$\overline{\text{TROE}}$ output delay after LCLOCK↑	$t_{D(1c)}$	4.0		14	ns
$\overline{\text{TROE}}$ output delay after $\overline{\text{CBWC}}$↓	$t_{D(1d)}$	4.0		20	ns
TRA(17-0) output delay after CICLK↑	$t_{D(2a)}$	4.0		16	ns
TRA(17-0) output delay after PCLK↑	$t_{D(2b)}$	4.0		16	ns
TRA(17-0) output delay after LCLOCK↑	$t_{D(2c)}$	4.0		16	ns
TRA(17-0) output delay after $\overline{\text{CBWC}}$↓	$t_{D(2d)}$	4.0		21	ns
TRD(7-0) setup time before CICLK↑	$t_{SU(1a)}$	1.0			ns
TRD(7-0) setup time before PCLK↑	$t_{SU(1b)}$	1.0			ns
TRD(7-0) setup time before LCLOCK↑	$t_{SU(1c)}$	1.0			ns
TRD(7-0) setup time before $\overline{\text{CBWC}}$↓	$t_{SU(1d)}$	1.0			ns
TRD(7-0) hold time after CICLK↑	$t_{H(1a)}$	6.0			ns
TRD(7-0) hold time after PCLK↑	$t_{H(1b)}$	6.0			ns
TRD(7-0) hold time after LCLOCK↑	$t_{H(1c)}$	6.0			ns
TRD(7-0) hold time after $\overline{\text{CBWC}}$↓	$t_{H(1d)}$	11			ns

Note: $\overline{\text{TRWE}}$ output is high. All timing parameter values apply to both Microprocessor and Translation RAM read cycles.

Figure 34. Translation RAM Timing - Write to RAM



Parameter	Symbol	Min	Typ	Max	Unit
TRD(7-0) delay from tri-state after CICLK↑	$t_{D(1a)}$	4.0		16	ns
TRD(7-0) delay from tri-state after PCLK↑	$t_{D(1b)}$	4.0		16	ns
TRD(7-0) delay from tri-state after $\overline{\text{LCLOCK}}$↑	$t_{D(1c)}$	4.0		16	ns
TRD(7-0) delay from tri-state after $\overline{\text{CBWC}}$↓	$t_{D(1d)}$	4.0		21	ns
TRD(7-0) delay to tri-state after CICLK↑	$t_{Z(1a)}$	4.0		16	ns
TRD(7-0) delay to tri-state after PCLK↑	$t_{Z(1b)}$	4.0		16	ns
TRD(7-0) delay to tri-state after LCLOCK↑	$t_{Z(1c)}$	4.0		16	ns
TRD(7-0) delay to tri-state after $\overline{\text{CBWC}}$↓	$t_{Z(1d)}$	4.0		21	ns
TRA(17-0) delay after CICLK↑	$t_{D(2a)}$	4.0		16	ns
TRA(17-0) delay after PCLK↑	$t_{D(2b)}$	4.0		16	ns
TRA(17-0) delay after LCLOCK↑	$t_{D(2c)}$	4.0		16	ns
TRA(17-0) delay after $\overline{\text{CBWC}}$↓	$t_{D(2d)}$	4.0		21	ns
$\overline{\text{TRWE}}$ delay after CICLK↓	$t_{D(3a)}$	4.0		15	ns
$\overline{\text{TRWE}}$ delay after PCLK↓	$t_{D(3b)}$	4.0		14	ns
$\overline{\text{TRWE}}$ delay after LCLOCK↓	$t_{D(3c)}$	4.0		14	ns
$\overline{\text{TRWE}}$ delay after $\overline{\text{CBWC}}$↑	$t_{D(3d)}$	4.0		18	ns

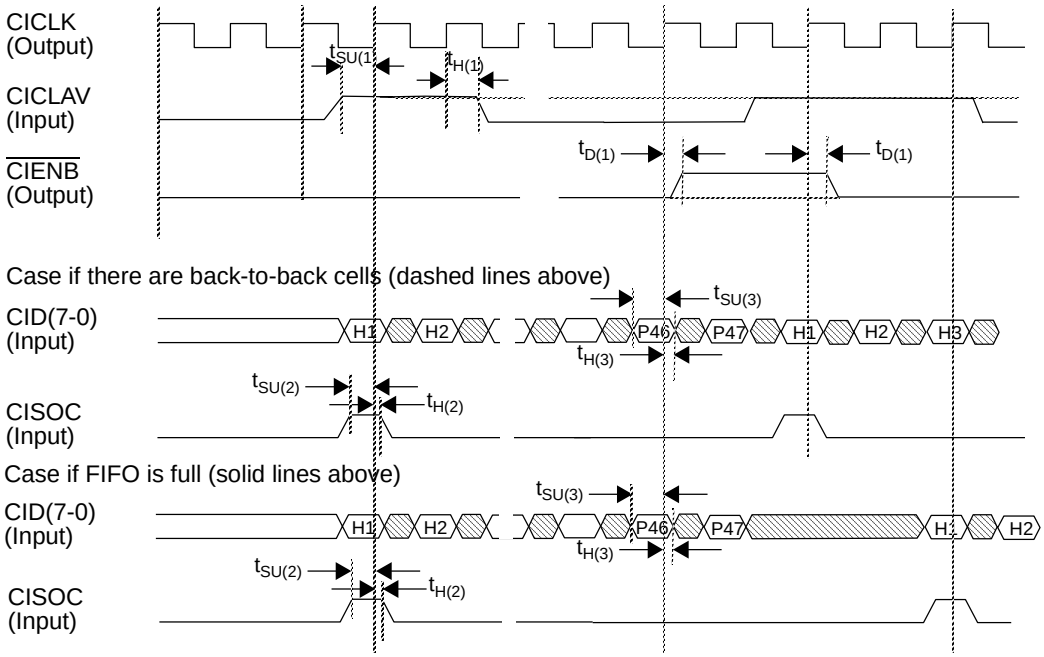
CELL INTERFACE

Note: For all cell interface timing diagrams, the 48 payload bytes of the cell are labelled as P0 through P47. This is consistent with Figures 10 and 13, which describe the byte/word ordering of the four cell interface modes.

Cell Inlet, UTOPIA Mode

ATM Layer Emulation Timing (Receive UTOPIA Interface Timing)

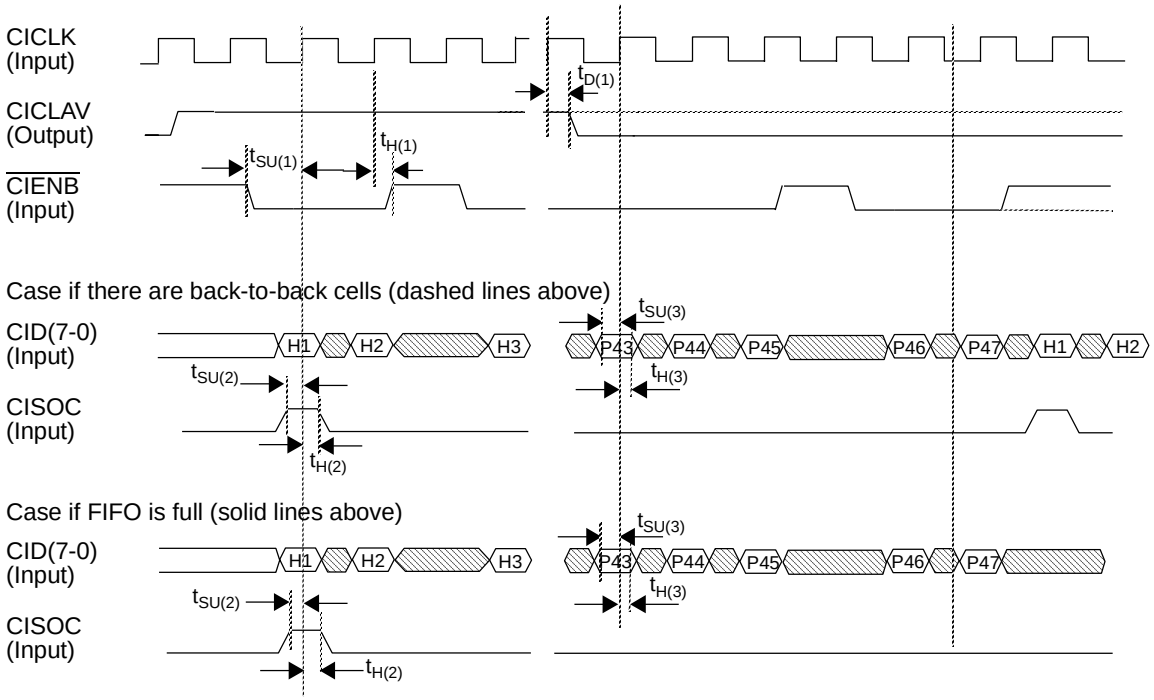
Figure 35. Timing of UTOPIA (ATM Layer Emulation) Cell Inlet Interface



Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	10.5			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	1.0			ns
$\overline{\text{CIENB}}$ delay after CICLK↑	$t_{D(1)}$	1.0		9.0	ns
CISOC setup time before CICLK↑	$t_{SU(2)}$	9.5			ns
CISOC hold time after CICLK↑	$t_{H(2)}$	1.0			ns
CID(7-0) setup time before CICLK↑	$t_{SU(3)}$	10.0			ns
CID(7-0) hold time after CICLK↑	$t_{H(3)}$	1.0			ns

PHY Layer Emulation Timing (Transmit UTOPIA Interface Timing)

Figure 36. Timing of UTOPIA (PHY Layer Emulation) Cell Inlet Interface

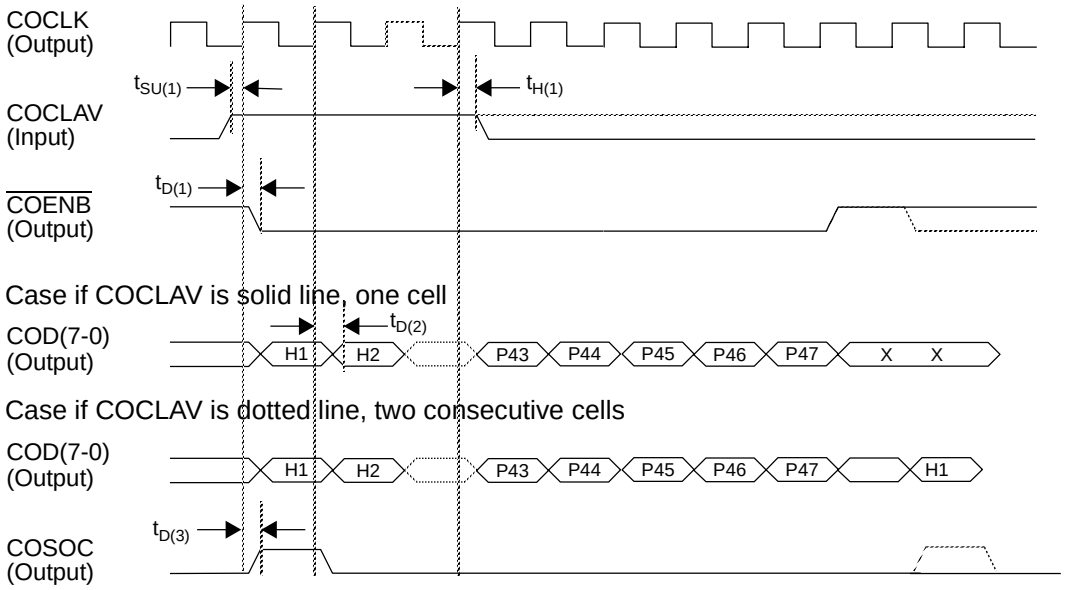


Parameter	Symbol	Min	Typ	Max	Unit
CICLAV delay from CICLK↑	$t_{D(1)}$	1.0		18	ns
$\overline{\text{CIENB}}$ setup time before CICLK↑	$t_{SU(1)}$	6.0			ns
$\overline{\text{CIENB}}$ hold time after CICLK↑	$t_{H(1)}$	0.0			ns
CISOC setup time before CICLK↑	$t_{SU(2)}$	6.0			ns
CISOC hold time after CICLK↑	$t_{H(2)}$	1.0			ns
CID(7-0) setup time before CICLK↑	$t_{SU(3)}$	6.0			ns
CID(7-0) hold time after CICLK↑	$t_{H(3)}$	1.0			ns

Cell Outlet, UTOPIA Mode

ATM Layer Emulation Timing (Transmit UTOPIA Interface Timing)

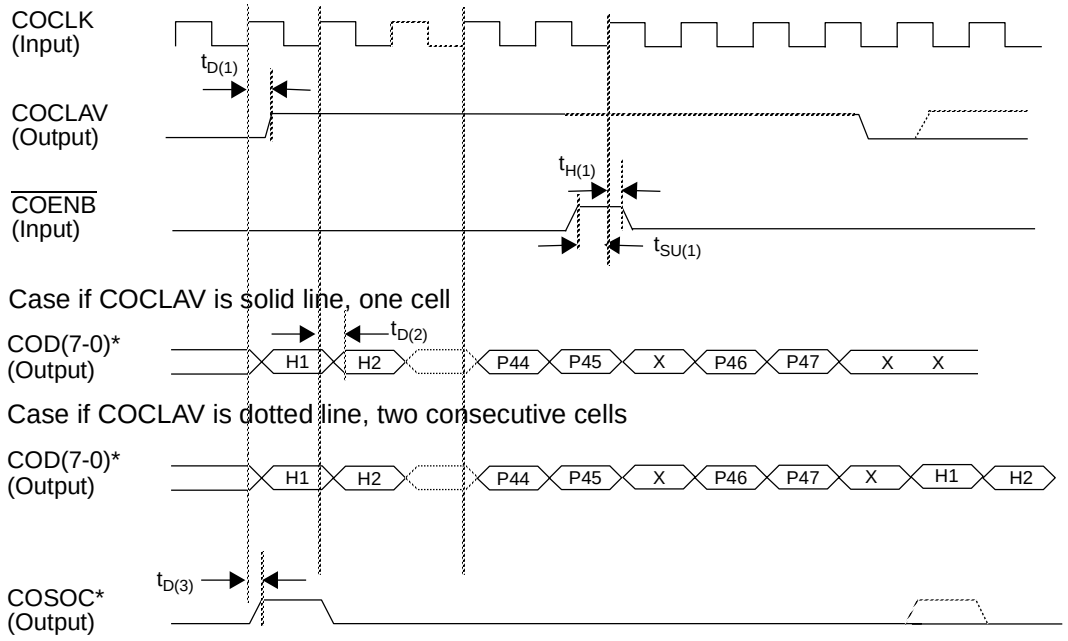
Figure 37. Timing of UTOPIA (ATM Layer Emulation) Cell Outlet Interface



Parameter	Symbol	Min	Typ	Max	Unit
COCLAV setup time before COCLK↑	$t_{SU(1)}$	6.0			ns
COCLAV hold time after COCLK↑	$t_{H(1)}$	1.0			ns
$\overline{\text{COENB}}$ delay after COCLK↑	$t_{D(1)}$	1.0		6.0	ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$	1.0		8.0	ns
COSOC delay after COCLK↑	$t_{D(3)}$	1.0		7.0	ns

PHY Layer Emulation Timing (Receive UTOPIA Interface Timing)

Figure 38. Timing of UTOPIA (PHY Layer Emulation) Cell Outlet Interface



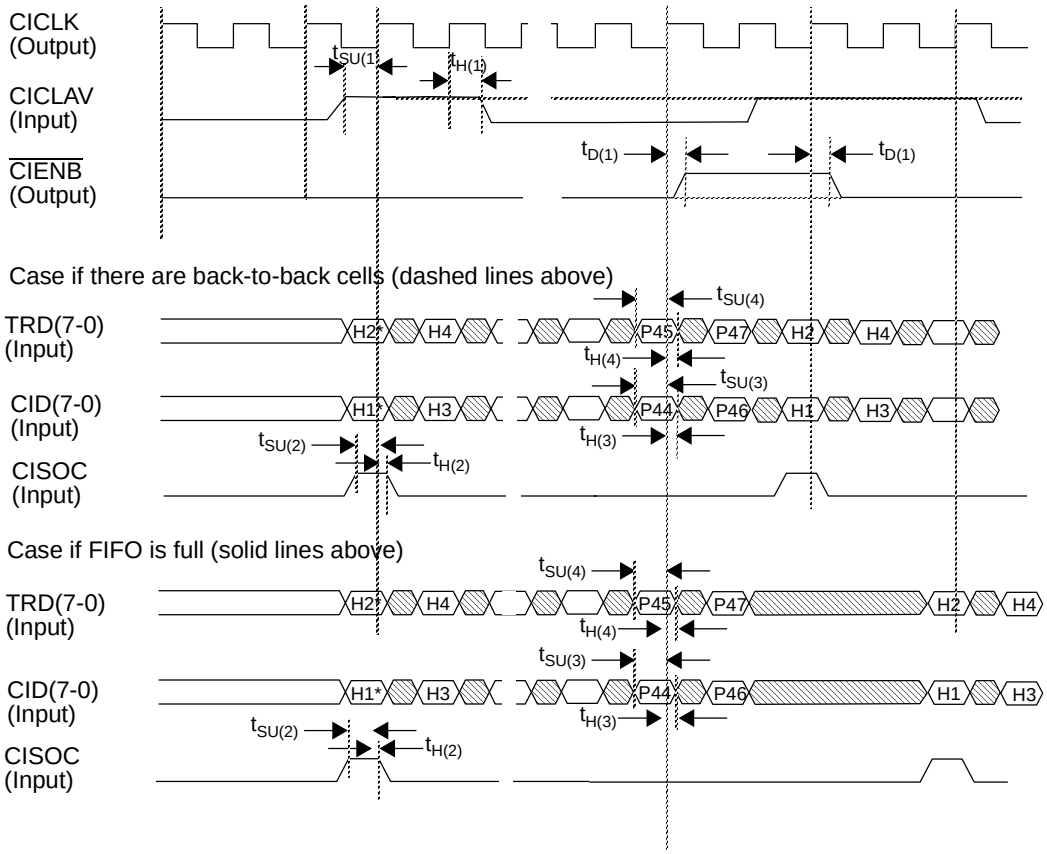
* Note: The COD(7-0) and COSOC outputs are tri-stated if the $\overline{\text{COENB}}$ input is changed to high.

Parameter	Symbol	Min	Typ	Max	Unit
COCLAV delay after COCLK↑	$t_{D(1)}$	1.0		12	ns
$\overline{\text{COENB}}$ setup time before COCLK↑	$t_{SU(1)}$	9.0			ns
$\overline{\text{COENB}}$ hold time after COCLK↑	$t_{H(1)}$	1.0			ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$	1.0		15	ns
COSOC delay after COCLK↑	$t_{D(3)}$	1.0		15	ns

Cell Inlet, 16-Bit Cell Interface Mode

ATM Layer Emulation Timing (Receive UTOPIA Interface Timing)

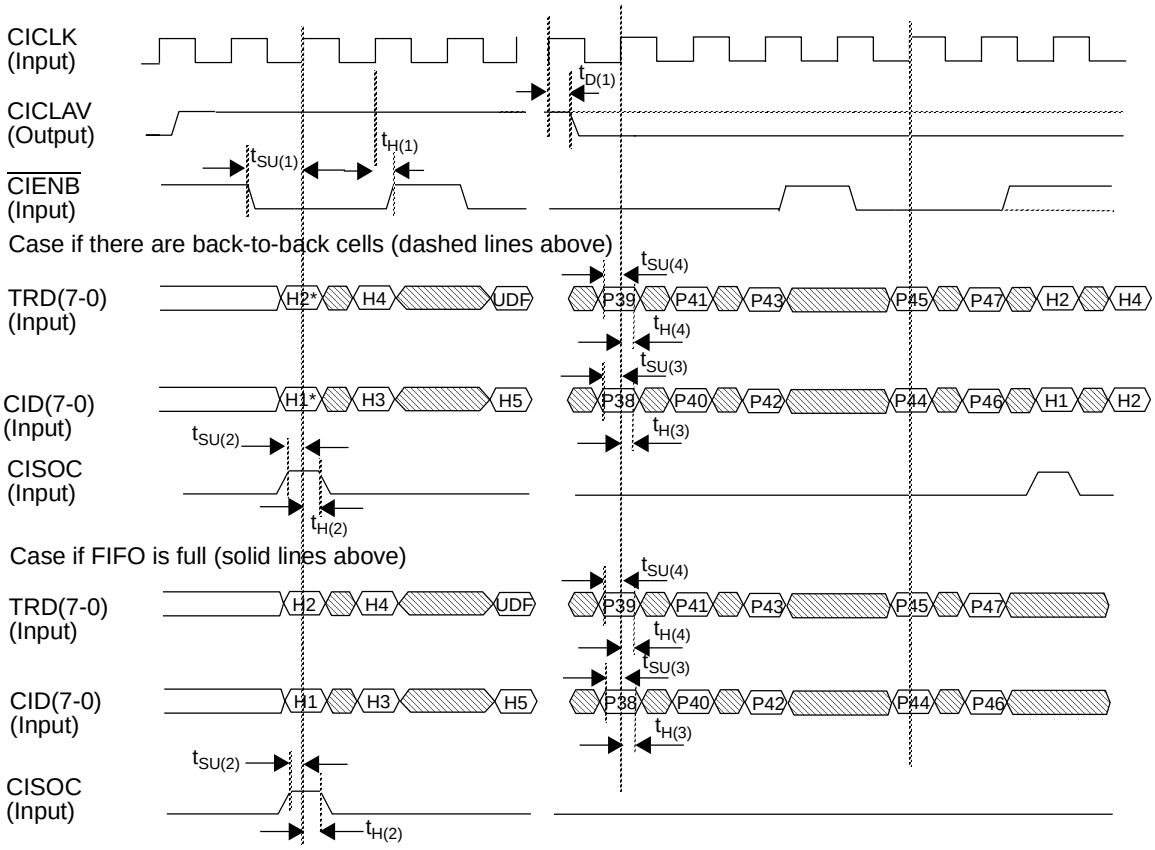
Figure 39. Timing of 16-Bit (ATM Layer Emulation) Cell Inlet Interface



Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	9.5			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	1.0			ns
$\overline{\text{CIENB}}$ delay after CICLK↑	$t_{D(1)}$	1.0		9.0	ns
CISOC setup time before CICLK↑	$t_{SU(2)}$	8.0			ns
CISOC hold time after CICLK↑	$t_{H(2)}$	1.0			ns
CID(7-0) setup time before CICLK↑	$t_{SU(3)}$	8.0			ns
CID(7-0) hold time after CICLK↑	$t_{H(3)}$	1.0			ns
TRD(7-0) setup time before CICLK↑	$t_{SU(4)}$	6.0			ns
TRD(7-0) hold time after CICLK↑	$t_{H(4)}$	1.0			ns

PHY Layer Emulation Timing (Transmit UTOPIA Interface Timing)

Figure 40. Timing of 16-Bit (PHY Layer Emulation) Cell Inlet Interface

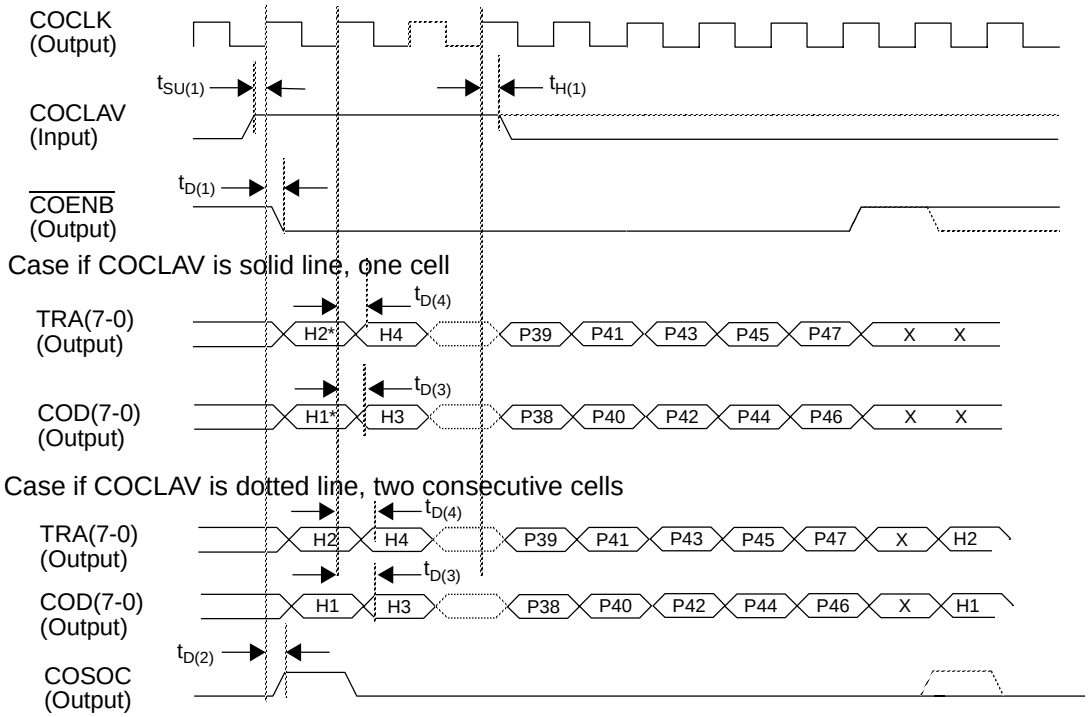


Parameter	Symbol	Min	Typ	Max	Unit
CICLAV delay from CICLK↑	$t_{D(1)}$	1.0		18	ns
$\overline{\text{CIENB}}$ setup time before CICLK↑	$t_{SU(1)}$	6.0			ns
$\overline{\text{CIENB}}$ hold time after CICLK↑	$t_{H(1)}$	0.0			ns
CISOC setup time before CICLK↑	$t_{SU(2)}$	6.0			ns
CISOC hold time after CICLK↑	$t_{H(2)}$	1.0			ns
CID(7-0) setup time before CICLK↑	$t_{SU(3)}$	6.0			ns
CID(7-0) hold time after CICLK↑	$t_{H(3)}$	1.0			ns
TRD(7-0) setup time before CICLK↑	$t_{SU(4)}$	6.0			ns
TRD(7-0) hold time after CICLK↑	$t_{H(4)}$	1.0			ns

Cell Outlet, 16-Bit Cell Interface Mode

ATM Layer Emulation Timing (Transmit UTOPIA Interface Timing)

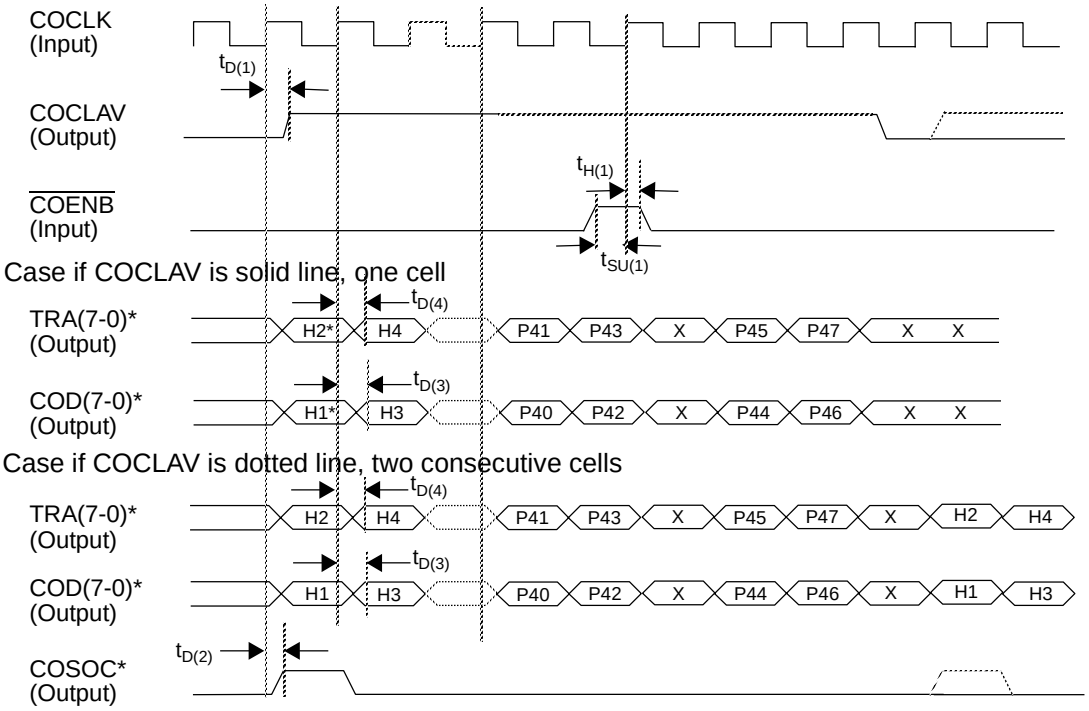
Figure 41. Timing of 16-Bit (ATM Layer Emulation) Cell Outlet Interface



Parameter	Symbol	Min	Typ	Max	Unit
COCLAV setup time before COCLK↑	$t_{SU(1)}$	6.0			ns
COCLAV hold time after COCLK↑	$t_{H(1)}$	1.0			ns
$\overline{\text{COENB}}$ delay after COCLK↑	$t_{D(1)}$	1.0		6.0	ns
COSOC delay after COCLK↑	$t_{D(2)}$	1.0		7.0	ns
COD(7-0) delay after COCLK↑	$t_{D(3)}$	1.0		8.0	ns
TRA(7-0) delay after COCLK↑	$t_{D(4)}$	1.0		7.0	ns

PHY Layer Emulation Timing (Receive UTOPIA Interface Timing)

Figure 42. Timing of 16-Bit (PHY Layer Emulation) Cell Outlet Interface

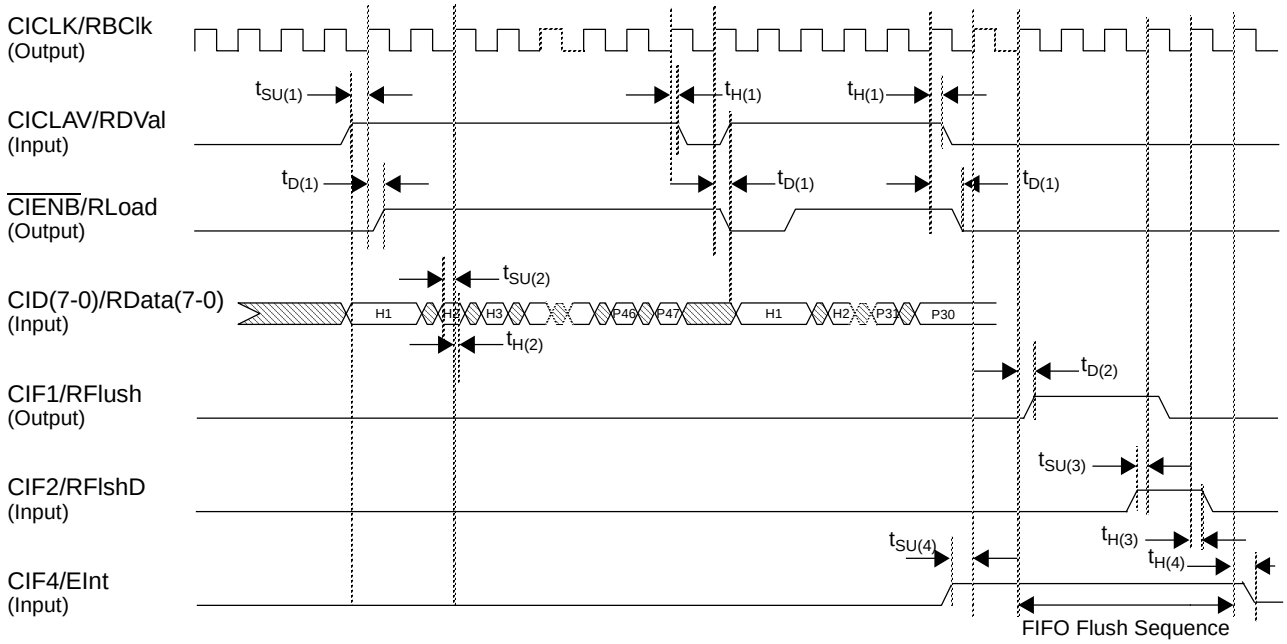


* Note: The TRA(7-0), COD(7-0) and COSOC outputs are tri-stated if the $\overline{\text{COENB}}$ input is changed to high.

Parameter	Symbol	Min	Typ	Max	Unit
COCLAV delay after COCLK↑	$t_{D(1)}$	1.0		12	ns
$\overline{\text{COENB}}$ setup time before COCLK↑	$t_{SU(1)}$	6.0			ns
$\overline{\text{COENB}}$ hold time after COCLK↑	$t_{H(1)}$	1.0			ns
COSOC delay after COCLK↑	$t_{D(2)}$	1.0		15	ns
COD(7-0) delay after COCLK↑	$t_{D(3)}$	1.0		16	ns
TRA(7-0) delay after COCLK↑	$t_{D(4)}$	1.0		15	ns

Cell Inlet, ALI-25 Mode

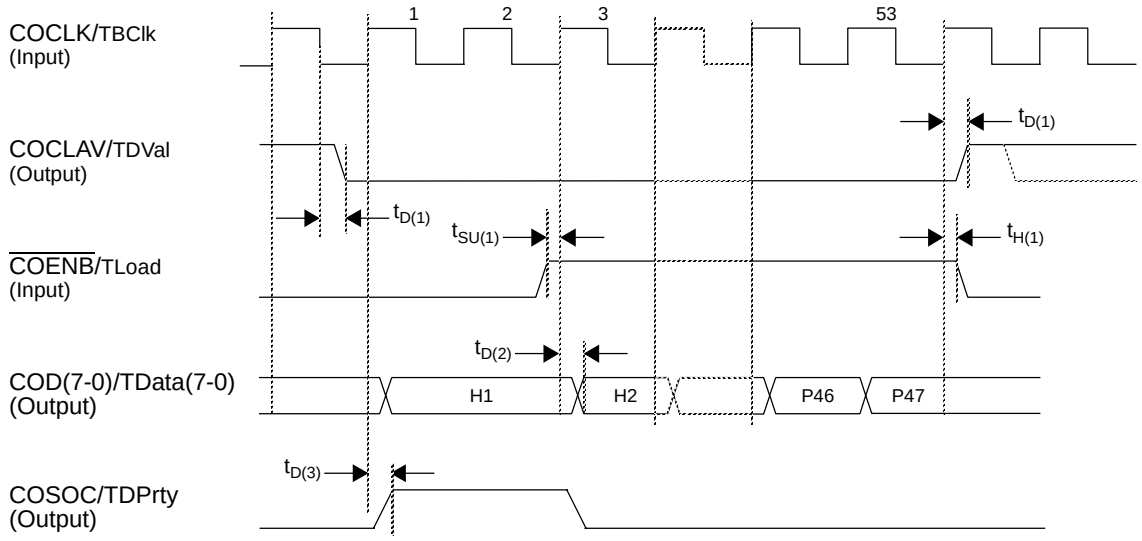
Figure 43. Timing of ALI-25 Cell Receive Interface



Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	12			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	0.0			ns
$\overline{\text{CIENB}}$ delay after CICLK↑	$t_{D(1)}$	1.0		9.0	ns
CID(7-0) setup time before CICLK↑	$t_{SU(2)}$	8.0			ns
CID(7-0) hold time after CICLK↑	$t_{H(2)}$	0.0			ns
CIF1 delay after CICLK↑	$t_{D(2)}$	1.0		21	ns
CIF2 setup time before CICLK↑	$t_{SU(3)}$	8.0			ns
CIF2 hold time after CICLK↑	$t_{H(3)}$	0.0			ns
CIF4 setup time before CICLK↑	$t_{SU(4)}$	10			ns
CIF4 hold time after CICLK↑	$t_{H(4)}$	0.0			ns

Cell Outlet, ALI-25 Mode

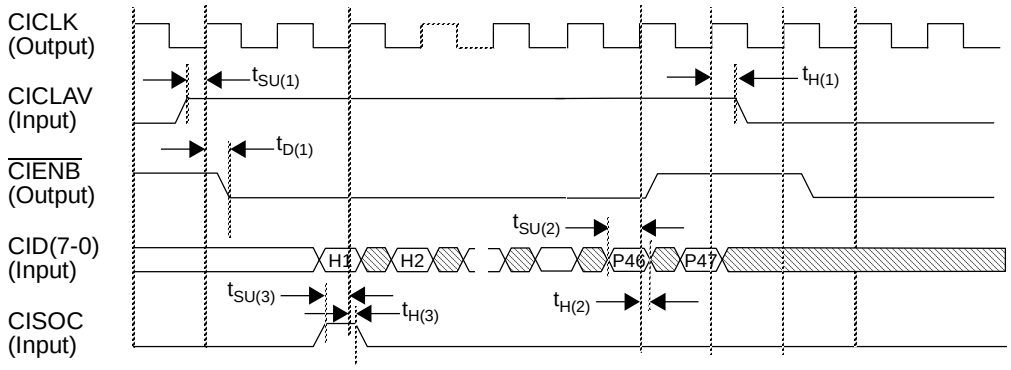
Figure 44. Timing of ALI-25 Cell Transmit Interface



Parameter	Symbol	Min	Typ	Max	Unit
COCLAV delay after COCLK↑	$t_{D(1)}$			13	ns
$\overline{\text{COENB}}$ setup time before COCLK↑	$t_{SU(1)}$	15			ns
$\overline{\text{COENB}}$ hold time after COCLK↑	$t_{H(1)}$	0.0			ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$	1.0		16	ns
COSOC delay after COCLK↑	$t_{D(3)}$	1.0		15	ns

Cell Inlet, Back-to-Back Mode

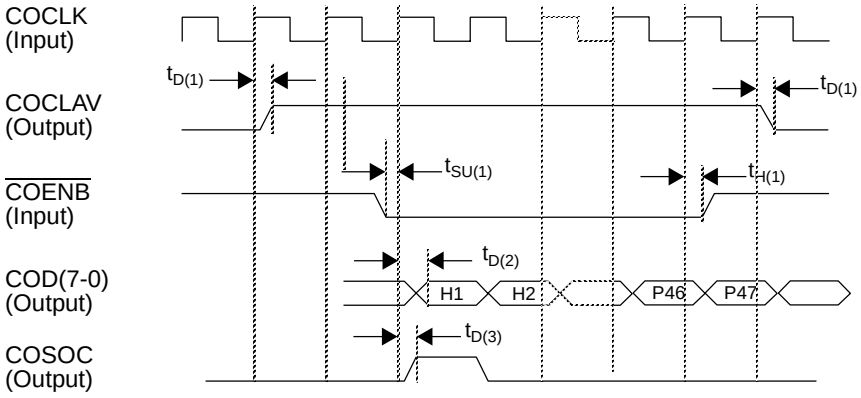
Figure 45. Timing of Back-to-Back Cell Receive Interface



Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	10			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	0.0			ns
$\overline{\text{CIENB}}$ delay after CICLK↑	$t_{D(1)}$	1.0		6.0	ns
CID(7-0) setup time before CICLK↑	$t_{SU(2)}$	9.0			ns
CID(7-0) hold time after CICLK↑	$t_{H(2)}$	0.0			ns
CISOC setup time before CICLK↑	$t_{SU(3)}$	9.0			ns
CISOC hold time after CICLK↑	$t_{H(3)}$	0.0			ns

Cell Outlet, Back-to-Back Mode

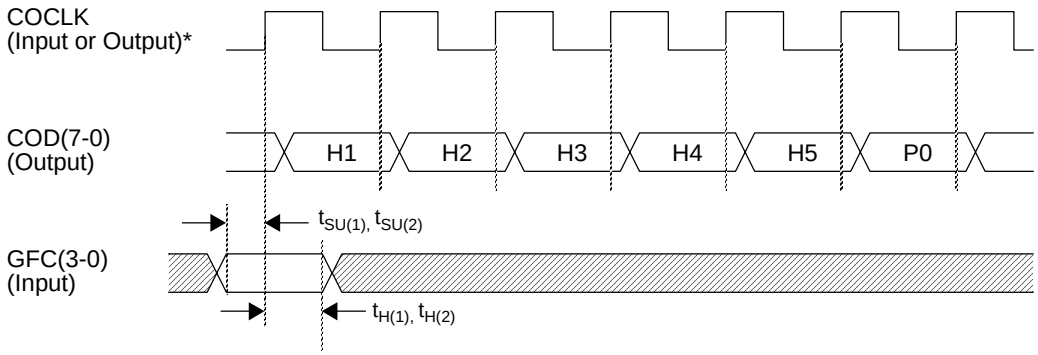
Figure 46. Timing of Back-to-Back Cell Transmit Interface



Parameter	Symbol	Min	Typ	Max	Unit
COCLAV delay after COCLK↑	$t_{D(1)}$			16	ns
$\overline{\text{COENB}}$ setup time before COCLK↑	$t_{SU(1)}$	18			ns
$\overline{\text{COENB}}$ hold time after COCLK↑	$t_{H(1)}$	0.0			ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$			15	ns
COSOC delay after COCLK↑	$t_{D(3)}$			15	ns

GFC Field Insertion

Figure 47. GFC Field Insertion Timing



* Note: Output signal for UTOPIA and 16-Bit ATM Layer emulation modes.
Input signal for UTOPIA and 16-Bit PHY Layer emulation modes, Back-to-Back mode and ALI-25 mode.

ATM Layer Emulation Mode

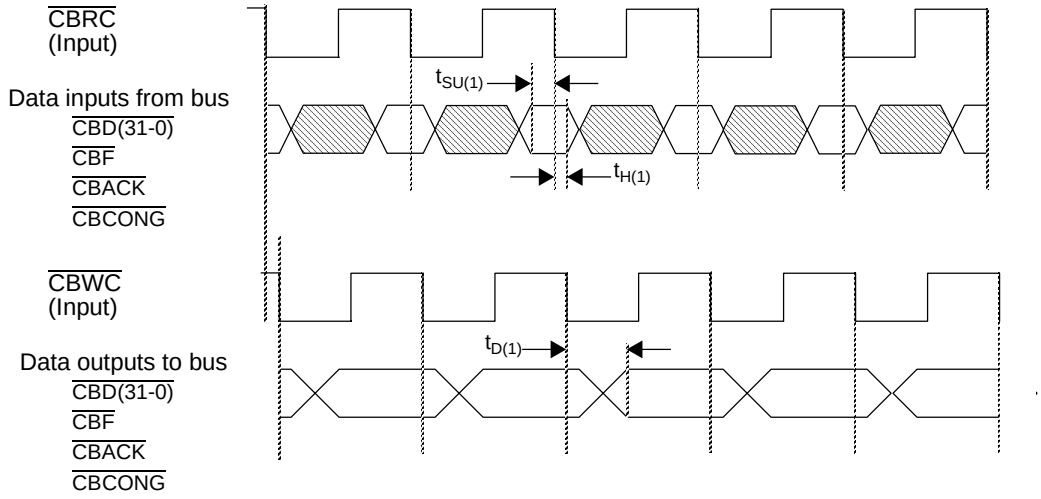
Parameter	Symbol	Min	Typ	Max	Unit
GFC(3-0) setup time before COCLK↑	$t_{SU(1)}$	4.0			ns
GFC(3-0) hold time after COCLK↑	$t_{H(1)}$	0.0			ns

PHY Layer Emulation, Back-to- Back and ALI-25 Modes

Parameter	Symbol	Min	Typ	Max	Unit
GFC(3-0) setup time before COCLK↑	$t_{SU(2)}$	0.0			ns
GFC(3-0) hold time after COCLK↑	$t_{H(2)}$	3.0			ns

CellBus Bus Port

Figure 48. *CellBus* Bus Timing



Parameter	Symbol	Min	Typ	Max	Unit
CellBus bus inputs setup time before $\overline{\text{CBRC}}\downarrow$	$t_{SU(1)}$	0.0			ns
CellBus bus inputs hold time after $\overline{\text{CBRC}}\downarrow$	$t_{H(1)}$	6.0			ns
CellBus bus outputs delay after $\overline{\text{CBWC}}\downarrow$	$t_{D(1)}$	6.0		See note	ns

Note:
The CUBIT-*Pro CellBus* write clock to *CellBus* data out time delay is complex and highly dependent on loading. The minimum value of delay $t_{D(1)}$ is the time after CBWC going low for which the old data output value does not change. This is shown in the table as 6 ns and is guaranteed by design inside the CUBIT-*Pro*. The maximum value (over voltage, temperature and process ranges) of $t_{D(1)}$ is 15.8 ns low-to-high, and 14.1 ns high-to-low for a minimum load consisting of a 50 ohm resistor to +1.2 volts and a 1.0 pF capacitor to ground. These output delay numbers have two components, internal delay and GTL output delay. With a real system load, the value of the GTL driver output delay of the CUBIT-*Pro* VLSI chip will depend on external circuitry: chip package effects, printed circuit boards at both ends, connectors, and backplane traces. The in-circuit value of delay then must be derived by adding the delays arising from these external effects to the internal delay.

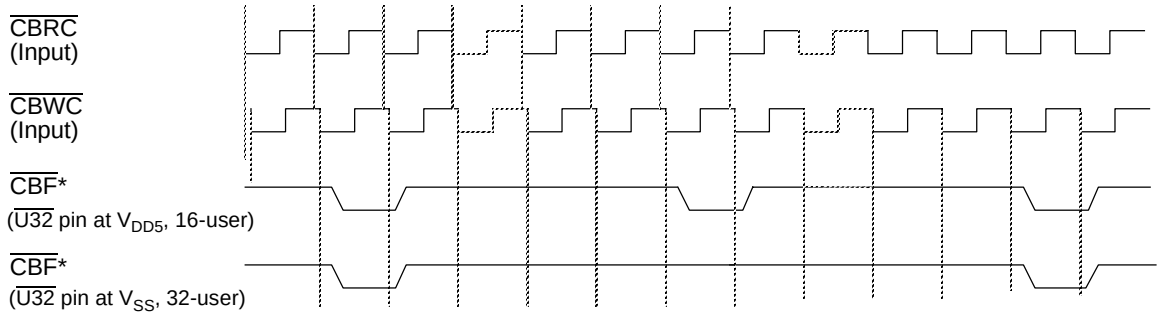
TranSwitch strongly recommends that all *CellBus* applications be analyzed by analog circuit simulation, using such tools as HSpice®. TranSwitch can provide the HSpice model of the CUBIT-*Pro* GTL transceiver. When doing such modeling, the CUBIT-*Pro* data delay time is divided into two parts: an internal delay time from the CBWC input to the (internal) GTL driver input, and the GTL driver delay. The minimum and maximum values of the CUBIT-*Pro* internal delay (up to the GTL driver) are 4.5 ns and 12 ns, respectively. In general, these simulations model timing from one CUBIT-*Pro*, through various levels of system interconnect, to another CUBIT-*Pro*. Models generally include the effects of the device package, printed circuit board and connectors, and back-plane. This level of simulation can very effectively model system performance. The actual value of delay from a CUBIT-*Pro* CBWC input to the point modeled in the simulation is the sum of the simulation delay and the CUBIT-*Pro* internal delay.

Applications with backplanes up to 17 inches wide and having clock speeds of no more than 25 MHz have proven to work well with good basic design. For the most part, this means keeping all of the significant copper wiring traces short: those from the back-plane connector to the CUBIT-*Pro*, and those from the *CellBus* bus ends to the pull-up resistors. Grounding is similarly important to performance, with the working assumption being that the backplane and all plug-in cards use full planes for power and ground, to maintain very low ground and supply inductance. The GTL clocks in this case are bussed across the backplane to all cards and driven at any point by a Texas Instruments SN74GTL1655, or equivalent. The clock line pull-ups are 27 ohms at each end. The delay from CBWC to CBRC is maintained, by an analog delay line at the clock source point, at a value between 2 and 4 ns.

Please contact the TranSwitch Applications Engineering Department for additional information and support.

HSpice is a registered trademark of Meta-Software, Inc.

Figure 49. *CellBus* Bus Frame Position, 16-User and 32-User Applications

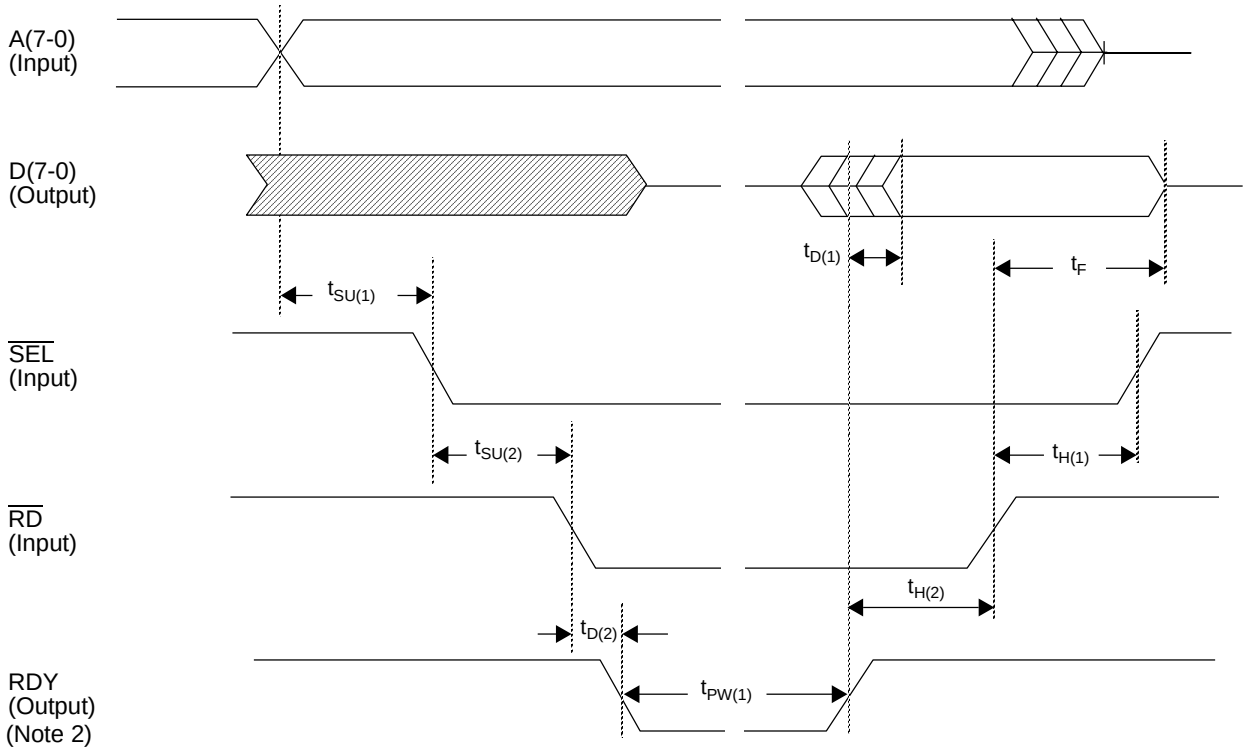


*Note: Output from the CUBIT-*Pro* that is selected to perform the bus arbitration function.
Input to all other CUBIT-Pros on the *CellBus* bus.

Microprocessor Interface

Intel Mode: Read Cycle

Figure 50. Intel Microprocessor Read Cycle Timing

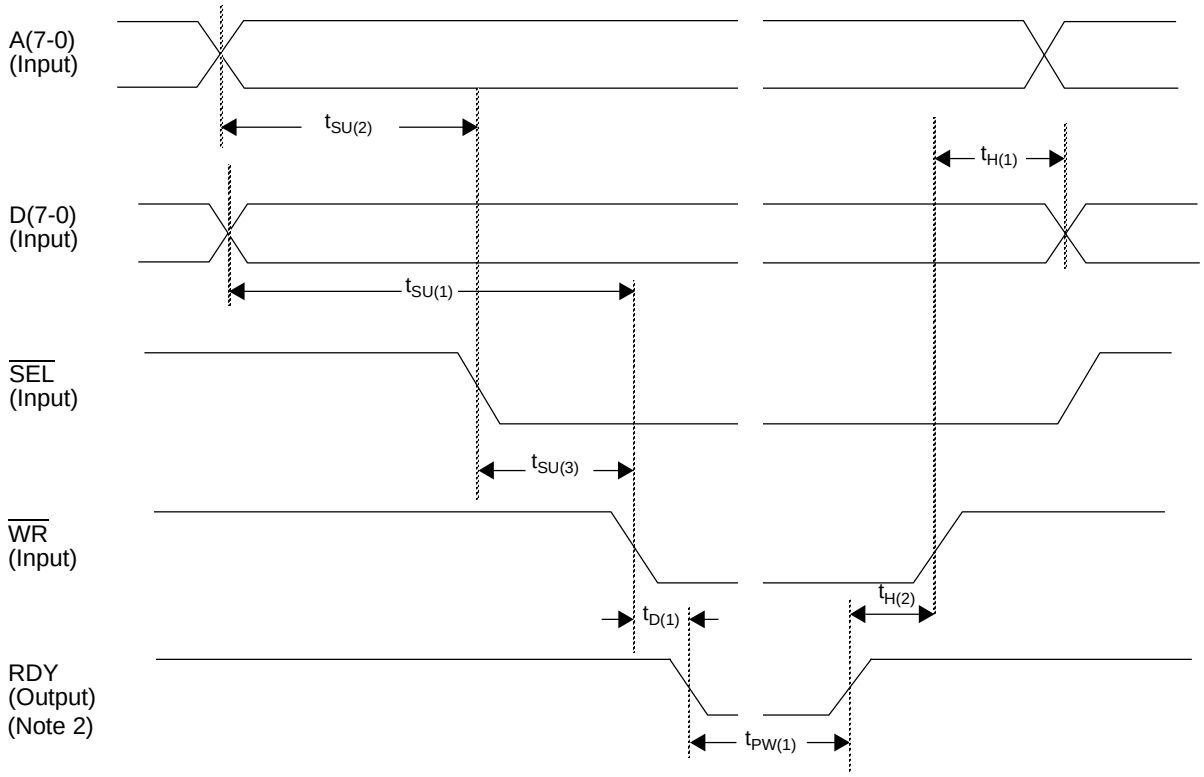


Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) valid delay after RDY$\uparrow$	$t_{D(1)}$	-10			ns
D(7-0) float time to tri-state after $\overline{RD}\uparrow$	t_F	1.0		5.0	ns
$\overline{SEL}$ setup time to $\overline{RD}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0.0			ns
$\overline{RD}$ hold time after $\overline{RDY}\uparrow$	$t_{H(2)}$	0.0			ns
RDY delay after $\overline{RD}\downarrow$	$t_{D(2)}$	0.0		12	ns
RDY pulse width	$t_{PW(1)}$	0.0		Note 1	ns

Notes:
1. The CUBIT-*Pro* will hold off the microprocessor for a period of up to 32 periods of the *CellBus* bus, LCLOCK or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 0BH). This occurs only during accesses to the external Translation RAM.
2. RDY is an open drain output signal pin that requires a pull-up resistor to V_{DD5} for proper operation.

Intel Mode: Write Cycle

Figure 51. Intel Microprocessor Write Cycle Timing

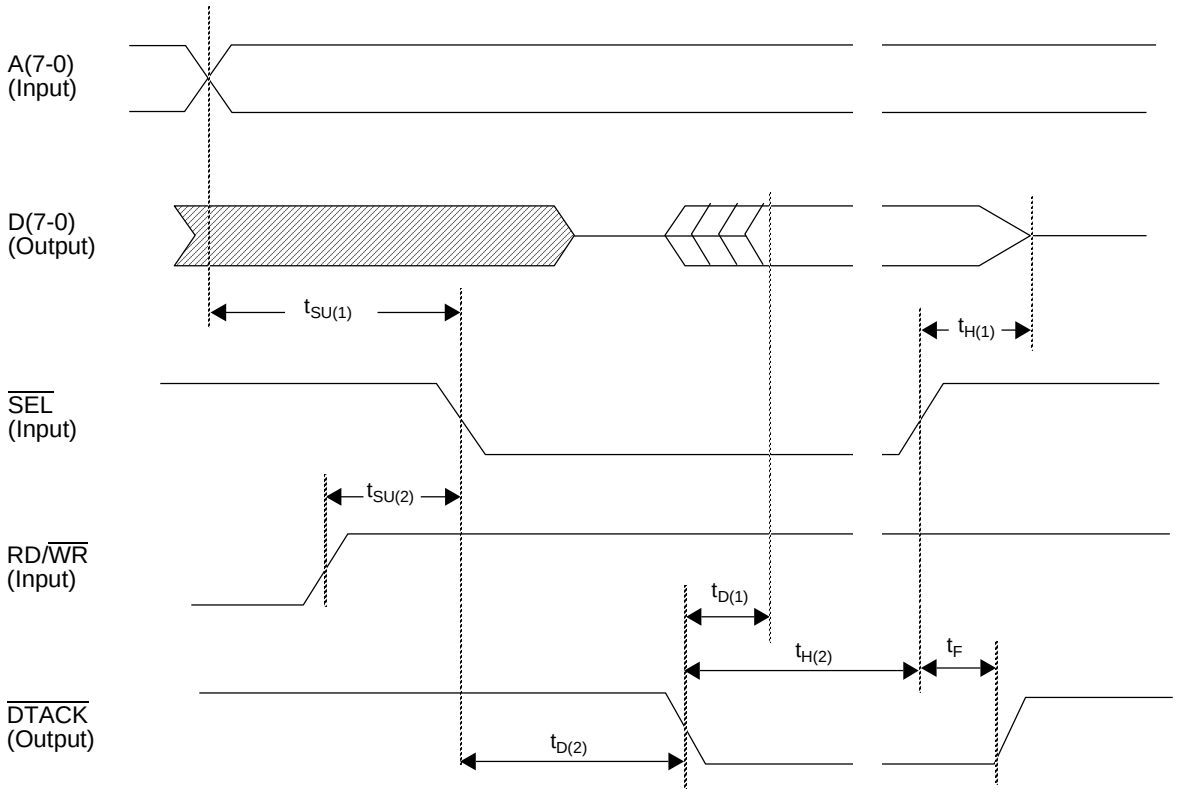


Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) setup time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
D(7-0) hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	5.0			ns
$\overline{WR}$ hold after RDY$\uparrow$	$t_{H(2)}$	0.0			ns
D(7-0) valid setup time to $\overline{WR}\downarrow$	$t_{SU(1)}$	0.0			ns
$\overline{SEL}$ setup time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
RDY delay after $\overline{WR}\downarrow$	$t_{D(1)}$	0.0		12	ns
RDY pulse width	$t_{PW(1)}$	0.0		Note 1	ns

Notes:
1. The CUBIT-*Pro* will hold off the microprocessor for a period of up to 32 periods of the *CellBus* bus, LCLOCK or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 0BH). This occurs only during accesses to the external Translation RAM.
2. RDY is an open drain output signal pin that requires a pull-up resistor to V_{DD5} for proper operation.

Motorola Mode: Read Cycle

Figure 52. Motorola Microprocessor Read Cycle Timing

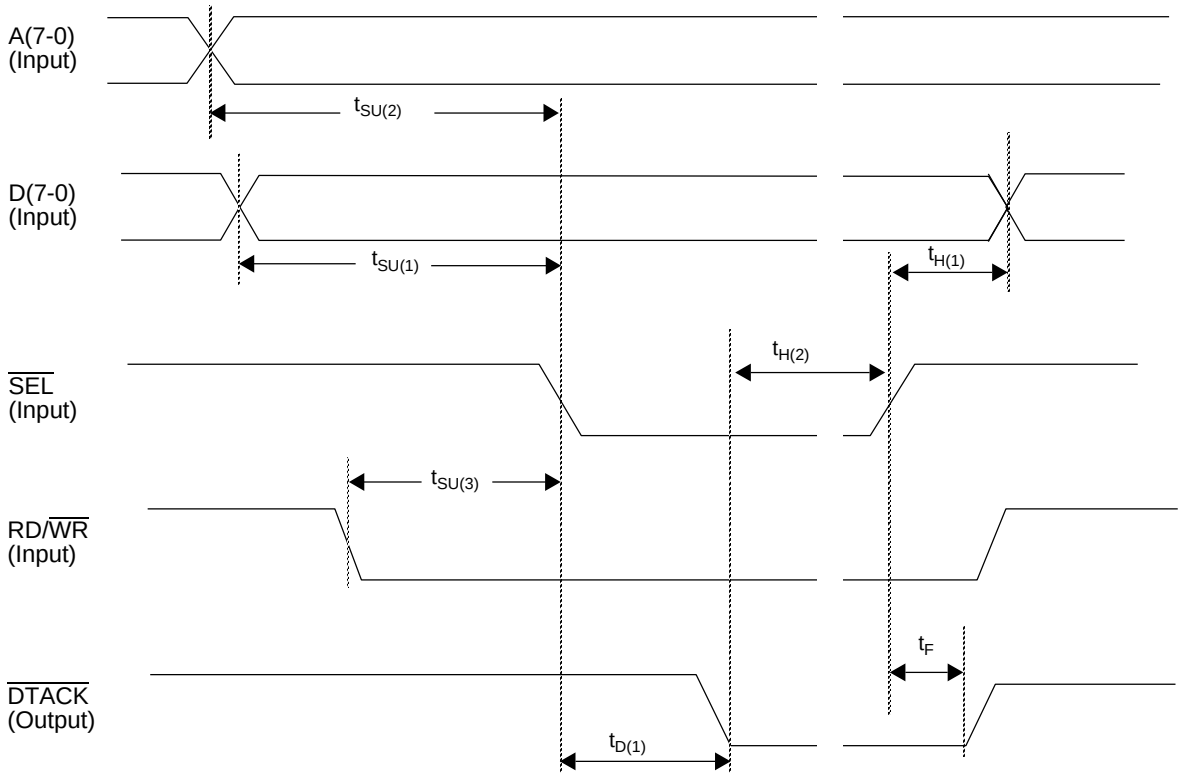


Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	1.0		5.0	ns
D(7-0) output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$			0.0	ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(2)}$	5.0			ns
RD/$\overline{WR}$ setup time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{DTACK}\downarrow$ delay time from $\overline{SEL}\downarrow$	$t_{D(2)}$	2*PCLK		Note 1	ns
$\overline{DTACK}\downarrow$ float time after $\overline{SEL}\uparrow$	t_F	1.0		10	ns

Note 1: The CUBIT-*Pro* will hold off the microprocessor for a period of up to 32 periods of the *CellBus* bus, LCLOCK or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 0BH). This occurs only during accesses to the external Translation RAM.

Motorola Mode: Write Cycle

Figure 53. Motorola Microprocessor Write Cycle Timing

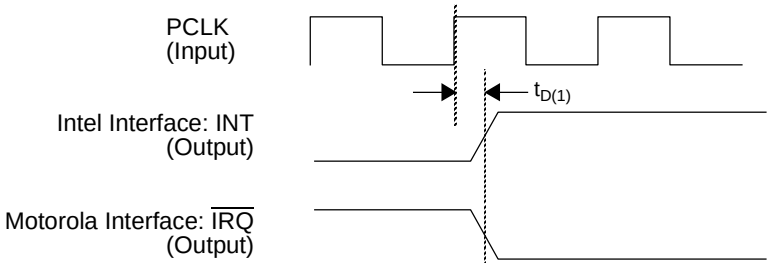


Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0.0			ns
D(7-0) valid setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
$\overline{D(7\text{-}0)}$ hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(2)}$	0.0			ns
RD/$\overline{WR}\downarrow$ setup time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{DTACK}$¦ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$	Note 1		Note 2	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	1.0		10	ns

Notes:
1. Two cycles of clock PCLK.
2. The CUBIT-*Pro* will hold off the microprocessor for a period of up to 32 periods of the *CellBus* bus, LCLOCK or PCLK clock selected by the settings of control bits CLKS1 and CLKS0 (bits 5 and 4 in register 0BH). This occurs only during accesses to the external Translation RAM.

Microprocessor Interrupt Generation

Figure 54. Microprocessor Interrupt Timing



Parameter	Symbol	Min	Typ	Max	Unit
INT/$\overline{IRQ}$ delay after PCLK$\uparrow$	$t_{D(1)}$	0.0		15	ns

MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	1	1	0	1	0	1	1	1
01	R	1	1	0	0	0	0	0	0
02	R	0	1	0	0	0	0	1	1
03	R	0	0	0	1	0	0	0	1
04	R	Mask Rev (0)	Mask Rev (0)	Mask Rev (0)	Mask Rev (1)	Reserved**			
05	RC	CTNAK	CTACK	Reserved**		BIP-8	CBLOF	CBLORC	CBLOWC
06	R/W	INTENA7	INTENA6	Reserved**		INTENA3	INTENA2	INTENA1	INTENA0
07	W	Reserved**							RESET
08	RC	CRCF	CRQOVF	CRQCAV	INSOC	CTSENT	NOGRT	Reserved**	OCOVF
09	R/W	INTEN7	INTEN6	INTEN5	INTEN4	INTEN3	INTEN2	Reserved**	INTEN0
0A	R/W	P1	P0	UNI	TRHENA	Reserved**		CTRDY	CRQSENT
0B	R/W	Reserved**		CLKS1	CLKS0	LINEDIV			
0C	R/W	ONLINE	TRHIZ	Reserved**		Reserved**	QM	GFCENA	IFECN
0D	R/W	Reserved**							MRCIN
0E	R/W	VRPS1	VRPS0	NOTIGN	CRC4I	CRC4EN	EBP	OAMRMEN	Reserved**
0F	R/W	TIME(7-0)							
10	R/W	0/X	CBRLEN(6-0)						
11	R/W	0/X	CBRLIMIT(6-0)						
12	R/W	0/X	VBRLIMIT(6-0)						
13	R/W	LBADDRL(7-0)							
14	R/W	Reserved**				LBADDRU(3-0)			
15	R/W	TRAL(7-0)							
16	R/W	TRAU(7-0)							
17	R/W	TRADATA(7-0)							

* R = Read-Only; W = Write-Only; RC = Read and Clear (individual bits remain set to 1 if their causative condition persists); R/W = Read/Write.

** Note: Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0.

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	Reg	DISCCTR(7-0)							
19	Reg	MRCCTR(7-0)							
1A	Reg	HECERCTR(7-0)							
1B	Reg	INCELLL(7-0) (Lower Byte)							
1C	Reg	INCELLM(7-0) (Middle Byte)							
1D	Reg	INCELLU(7-0) (Upper Byte)							
1E	R	16BMODE	32USER	MASTER	CUBIT-ID(4-0)				
1F	Reg	Reserved**							
20	R	MRCHEAD0(7-0)							
21	R	MRCHEAD1(7-0)							
22	R	MRCHEAD2(7-0)							
23	R	MRCHEAD3(7-0)							
24	R/W	Reserved**						TRAMSB(1-0)	
25-5F		Reserved**							
60	R	CRQ0(7-0)							
61-92	R	CRQ1(7-0) (61H) through CRQ50(7-0) (92H)							
93	R	CRQ51(7-0)							
94-9F		Reserved**							
A0	R/W	CTQ0(7-0)							
A1-D6	R/W	CTQ1(7-0) (A1H) through CTQ54(7-0) (D6H)							
D7	R/W	CTQ55(7-0)							
D8-DF		Reserved**							
E0	R/W	MCASTN00(7-0)							
E1-FE	R/W	MCASTN01(7-0) (E1H) through MCASTN1E(7-0) (FEH)							
FF	R/W	MCASTN1F(7-0)							

* R = Read-Only; R/W = Read/Write; Reg = Register.

** Note: Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0.

MEMORY MAP DESCRIPTIONS

DEVICE DESCRIPTOR AND RESET BITS

Address *	Bit	Symbol	Description
00-02 03	7-0 3-0	DEVID	Device identification code (28 bits).
03	7-4		Version number.
04	7-4		Mask revision level.
	3-0	--	Reserved bits.
07	7-1	--	Reserved bits.
	0	RESET	When set to 1, this bit clears the counters DISCCTR, MRCCTR, HECERCTR and INCELL (L, M and U) in addresses 18H through 1DH. This bit clears to 0 automatically.

* All addresses in memory map description tables are hexadecimal. Reserved addresses are not listed.

STATUS AND INTERRUPT-ENABLE BITS

Address	Bit	Symbol	Description
05	7	CTNAK	Bit is set to 1 if a microprocessor control cell sent by the CUBIT-*Pro* is not accepted at destination
	6	CTACK	Bit is set to 1 if a microprocessor control cell sent by the CUBIT-*Pro* is accepted at destination
	5,4	--	Reserved bits.
	3	BIP-8	Bit is set to 1 when a BIP-8 error is detected in the receiver. It will generate a microprocessor interrupt if bit 3 (INTENA3) is set to one in the interrupt enable location at address 06H.
	2	CBLOF	Bit is set to 1 if the *CellBus* bus frame pulse is not present for two consecutive frame pulse times ($\overline{U32}$ = low) or four consecutive frame pulse times ($\overline{U32}$ = high).
	1	CBLORC	Bit is set to 1 if the *CellBus* bus read clock is not present for more than the equivalent of 32 PCLK cycles.
	0	CBLOWC	Bit is set to 1 if the *CellBus* bus write clock is not present for more than the equivalent of 32 PCLK cycles.
06	7	INTENA7	Interrupt enabled for CTNAK, if = 1.
	6	INTENA6	Interrupt enabled for CTACK, if = 1.
	5, 4	--	Reserved bits.
	3	INTENA3	Interrupt enabled for BIP-8, if = 1.
	2	INTENA2	Interrupt enabled for CBLOF, if = 1.
	1	INTENA1	Interrupt enabled for CBLORC, if = 1.
	0	INTENA0	Interrupt enabled for CBLOWC, if = 1.

Address	Bit	Symbol	Description
08	7	CRCF	Bit is set to 1 to indicate a CRC check error on cell from *CellBus* bus.
	6	CRQOVF	Bit is set to 1 to indicate loss of an incoming control cell, due to overflow of the internal 4-cell control cell receive queue.
	5	CRQCAV	Bit is set to 1 to indicate that a control cell is present in the control cell receive queue, CRQ.
	4	INSOC	Bit is set to 1 to indicate a cell inlet Start-of-Cell error occurrence.
	3	CTSENT	Bit is set to 1 to indicate that a control cell has been sent to the *CellBus* bus from the control cell transmit buffer.
	2	NOGRT	Bit is set to 1 to indicate that no bus access grant has been received by the inlet side, after a bus access request, within a time established by register TIME.
	1	--	Reserved bit.
	0	OCOVF	Bit is set to 1 to indicate a cell discarded due to overflow of outlet FIFO.
09	7	INTEN7	Interrupt enabled for CRCF, if = 1.
	6	INTEN6	Interrupt enabled for CRQOVF, if = 1.
	5	INTEN5	Interrupt enabled for CRQCAV, if = 1.
	4	INTEN4	Interrupt enabled for INSOC, if = 1.
	3	INTEN3	Interrupt enabled for CTSENT, if = 1.
	2	INTEN2	Interrupt enabled for NOGRT, if = 1.
	1	--	Reserved bit.
	0	INTEN0	Interrupt enabled for OCOVF, if = 1.
1E	7	16BMODE	Bit is set to 1 if $\overline{\text{ABRENA}}$ is high. A 0 indicates that the CUBIT-*Pro* is operated in 16-Bit mode.
	6	32USER	Bit is set to 1 if $\overline{\text{U32}}$ is high. A 0 indicates that the CUBIT-*Pro* is operated in 32-user mode.
	5	MASTER	Bit is set to 1 if $\overline{\text{ENARB}}$ is high. A 0 indicates that the CUBIT-*Pro* is the master arbiter of the *CellBus* bus.
	4-0	CUBIT-ID (4-0)	Contains the address ID set at pins $\overline{\text{UA(4-0)}}$. These pin states are detected at power-up and if any of the $\overline{\text{UA(4-0)}}$ inputs change state. For example, CUBIT-ID is 1FH if the $\overline{\text{UA(4-0)}}$ pins are all high.

DEVICE MODE CONTROL BITS

Address	Bit	Symbol	Description
0A	7, 6	P1, P0	Set bus access priority of this CUBIT-*Pro* device. Possible values are: high-priority, P1=1, P0=1; medium-priority, P1=1, P0=0; low-priority, P1=0, P0=1; no request, P1=0, P0=0.
	5	UNI	If = 1, UNI operation, VPI filled width = 8 bits. If = 0, NNI operation, VPI filled width = 12 bits.
	4	TRHENA	Enable insertion of Tandem Routing Header during address translation.
	3, 2	--	Reserved bits.
	1	CTRDY	Set to 1 by microprocessor to indicate that a control cell is ready to be sent. Cleared by CUBIT-*Pro* when cell has been sent.
	0	CRQSENT	Set to 1 by the microprocessor to indicate that a control cell has been read from the CUBIT-*Pro*'s control cell receive buffer. Cleared to 0 automatically by CUBIT-*Pro*.
0B	7,6	--	Reserved bits.
	5	CLKS1	Clock source selection bit 1 for the cell inlet/outlet clock. This bit works in conjunction with CLKS0. The coding followed is: CLKS1, CLKS0 = 0,0: Cell interface clock = *CellBus* bus clock divided by $2^{LINEDIV}$ CLKS1, CLKS0 = 0,1: Cell interface clock = LCLOCK clock divided by $2^{LINEDIV}$ CLKS1, CLKS0 = 1,0: Cell interface clock = PCLK clock divided by $2^{LINEDIV}$ CLKS1, CLKS0 = 1,1: Reserved, do not use
	4	CLKS0	Clock source selection bit 0 for the cell inlet/outlet clock. This bit works in conjunction with CLKS1.
	3-0	LINEDIV	Cell inlet clock frequency control. Frequency will be equal to the frequency of the selected clock source, divided by 2-to-the-power-LINEDIV.
0C	7	ONLINE	Operational status. If = 1, the CUBIT-*Pro* is on-line and all functions are operating. If = 0, the CUBIT-*Pro* is off-line. In off-line condition, no cells are accepted from the cell inlet, the interface outputs are tri-stated, and only control and loopback cells are accepted from the *CellBus* bus.
	6	TRHIZ	Translation RAM interface tri-state bit. When set to 1 and the ONLINE bit is 0, the translation RAM interface is put in Hi-Z mode.
	5, 4, 3	--	Reserved bits.
	2	QM	Outlet cell queue structure. One single 123-cell queue if QM=0. Split queue (Control Data, CBR, VBR, ABR) if QM = 1.
	1	GFCENA	Enable insertion of the state of pins GFC(3-0) into the GFC field of outgoing cells if = 1. State of GFC(3-0) is sampled on the rising edge of COCLK that precedes the first byte of the ATM cell header (see Figure 47).
	0	IFECN	Enable insertion of FECN if = 1. The EFCI bit (middle bit of PT field) will be set =1 if the CBR or VBR FIFO length equals or exceeds the congestion limits, and IFECN = 1.

Address	Bit	Symbol	Description
0D	7-1	--	Reserved bits.
	0	MRCIN	Bit is set to 1 to indicate that a misrouted cell has been received. Cleared by a write operation.
0E	7	VRPS1	VCI Records per Page Selection bit 1. In conjunction with VRPS0, this bit selects the number of VCI records per page (VRP) to be either 256, 512, 1024 or 128. VRPS1,VRPS0= 0,0: VRP is 256 VRPS1,VRPS0= 0,1: VRP is 512 VRPS1,VRPS0= 1,0: VRP is 1024 VRPS1,VRPS0= 1,1: VRP is 128
	6	VRPS0	VCI Records per Page Selection bit 0. In conjunction with VRPS1, this bit selects the number of VCI records per page (VRP) to be either 256, 512, 1024 or 128.
	5	NOTIGN	Ignore translation record I-bit. When set to 1, connections marked as I-bit=1 in the translation records will be treated as if I-bit=0.
	4	CRC4I	CRC-4 calculation is inverted to produce an incorrect CRC-4 value for the *CellBus* Bus Routing Header. This bit is intended for test purposes.
	3	CRC4EN	When set to 1, this bit enables CUBIT-*Pro* to compute the CRC-4 field H3-H0 in the *CellBus* Bus Routing Header for all cells going into the cell inlet FIFO. If set to 0, then CRC-4 is computed only for loopback cells. The default at power-up is CRC4EN=0.
	2	EBP	If this bit is set to 1, the CONGOUT output signal is an indication of actual or impending congestion at the receiving CUBIT-*Pro*. If set to 0, $\overline{\text{CONGOUT}}$ is a GTL-to-CMOS translation of the *CellBus* bus signal $\overline{\text{CBCONG}}$. EBP must be set to 1 to enable the ACK and NACK functions of CIF1 and CIF3, respectively, when operating in UTOPIA or back-to-back modes. Also, EBP must be set to 1 in order to tri-state CONGOUT when ONLINE=0. The default at power-up is EBP=0.
	1	OAMRMEN	When set to 1, this bit enables the routing of OAM/RM and reserved VCs cells. If set to 0, the CUBIT-*Pro* TXC-05802 uses CUBIT TXC-05801 OAM routing. The default at power-up is OAMRMEN=0.
	0	--	Reserved bit.
0F	7-0	TIME	Time-out counter preset value for bus access watchdog timer. If timer expires after a request is made, and before a grant is received, alarm bit NOGRT is set. Each count represents one bus frame cycle.

OUTLET CELL FIFO SIZE AND LIMIT CONTROL REGISTERS

Address	Bit	Symbol	Description
10	6-0	CBRLEN	Length, in cells, of the CBR section of the cell outlet FIFO. Valid values are zero through 89.
11	6-0	CBRLIMIT	Congestion size for CBR FIFO. FECN may be set if CBR FIFO length is greater than or equal to this value and IFECN = 1.
12	6-0	VBRLIMIT	Congestion size for VBR FIFO. FECN may be set if VBR FIFO length is greater than or equal to this value and IFECN = 1.

LOOPBACK CONTROL ADDRESS REGISTER

Address	Bit	Symbol	Description
13	7-0	LBADDRL	8 LSB of Loopback Routing Header, bits 11-4 of *CellBus* Bus Routing Header (see Figure 31).
14	7-4	--	Reserved bits.
	3-0	LBADDRU	4 MSB of Loopback Routing Header, bits 15-12 of *CellBus* Bus Routing Header (see Figure 31).

TRANSLATION RAM READ/WRITE CONTROL

Address	Bit	Symbol	Description
15	7-0	TRAL	8 LSB of the translation RAM address [pins TRA(7-0)].
16	7-0	TRAU	Middle 8 bits of the translation RAM address [pins TRA(15-8)].
17	7-0	TRADATA	Data read from, or to be written into, the translation RAM at the address defined by pins TRA(17-0) [pins TRD(7-0)].
24	7-2	--	Reserved bits.
	1-0	TRAMSB	2 MSB of the translation RAM address [pins TRA(17-16)]

COUNTERS AND MISROUTED CELL HEADERS

Address	Bit	Symbol	Description
18	7-0	DISCCTR	Count of cells discarded at input to outlet-side FIFO. See Note 1.
19	7-0	MRCCTR	Count of cell inlet mis-routed cells received. See Note 1.
1A	7-0	HECERCTR	Count of cells at cell inlet having a HEC error indication. See Note 1.
1B	7-0	INCELLL	Bits 7-0 (8 LSB) of count of incoming cells. See Note 1.
1C	7-0	INCELLM	Bits 15-8 of count of incoming cells. See Note 1.
1D	7-0	INCELLU	Bits 23-16 (8 MSB) of count of incoming cells. See Note 1.
20	7-0	MRCHEAD0	First (least significant) byte of the header of the first misrouted cell received after this buffer was last cleared. This least significant byte of the ATM cell corresponds to VCI[3-0] (LSB), PT and CLP of the ATM cell header.
21	7-0	MRCHEAD1	Second byte of above header.
22	7-0	MRCHEAD2	Third byte of above header.
23	7-0	MRCHEAD3	Fourth (most significant) byte of above header.

Note 1: These registers are reset to 00H by the RESET bit in address 07H, bit 0.

CONTROL CELL SEND AND RECEIVE QUEUES

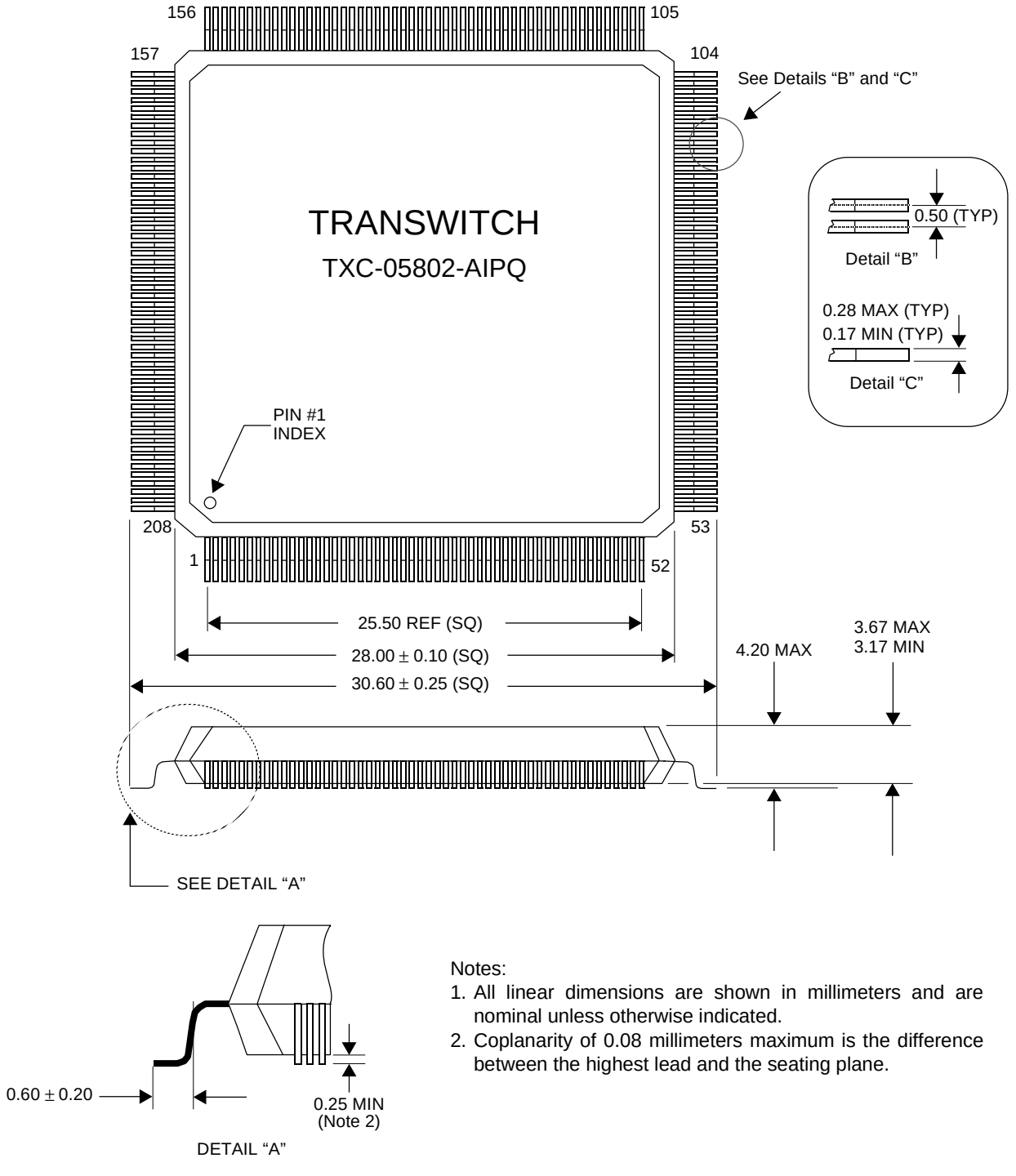
Address	Bit	Symbol	Description
60-93	7-0	CRQi	Control cell receive buffer, 52 bytes (i = 0 - 51).
A0-D7	7-0	CTQi	Control cell transmit buffer, 56 bytes (i = 0 - 55).

MULTICAST NUMBER MEMORY

Address	Bit	Symbol	Description
E0	7-0	MCASTN00	Multicast session RX enable bits, channels 7-0 (relative address zero decimal, bits 7-0).
E1-FE	7-0	MCASTN01-MCASTN1E	Multicast session RX enable bits for channels 15-8, 23-16, . . . , 247-240 (relative addresses 1 to 30 decimal, bits 7-0).
FF	7-0	MCASTN1F	Multicast session RX enable bits, channels 255-248 (relative address 31 decimal, bits 7-0).

PACKAGE INFORMATION

The CUBIT-*Pro* device is available in a 208-pin plastic quad flat package (PQFP) suitable for surface mounting, as shown in Figure 55.



Notes:
1. All linear dimensions are shown in millimeters and are nominal unless otherwise indicated.
2. Coplanarity of 0.08 millimeters maximum is the difference between the highest lead and the seating plane.

Figure 55. CUBIT-*Pro* TXC-05802 208-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-05802AIPQ 208-pin Plastic Quad Flat Package (PQFP)

RELATED PRODUCTS

Figure 56 illustrates typical applications of the CUBIT-*Pro* *CellBus* Bus Switch device in a generic architecture for ATM access switching. The other TranSwitch devices included in this diagram are briefly described below:

TXC-03003B, SOT-3 VLSI Device (STM-1, STS-3, STS-3c Overhead Terminator). This device performs all the functions for section, line and path overhead processing of STM-1, STS-3 or STS-3c signals, providing access to all overhead bytes. It performs pointer justification and payload tracking, alarm detection and generation, and performance monitoring.

TXC-03102, QDS1F VLSI Device (Quad DS1 Framer). A 4-channel DS1 (1.544 Mbit/s) framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device is not recommended for use in new designs, which should use QT1F-*Plus.*

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel DS1 (1.544 Mbit/s) framer designed with extended features for voice and data communications applications.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Extracts/inserts ATM cells from/to DS1, DS3, E1, STS-1, STS-3c or STM-1 line interface signals. Serial, byte and nibble interfaces operate from 1.544 to 155.52 Mbit/s.

TXC-05501 and TXC-05601, SARA-S and SARA-R VLSI Devices (Segmentation and Reassembly). A two-chip set for implementation of the ATM Adaptation Layers (AAL) 3, 4, and 5 at line rates from DS1 (1.544 Mbit/s) up to STS-3c/STM-1 (155.52 Mbit/s).

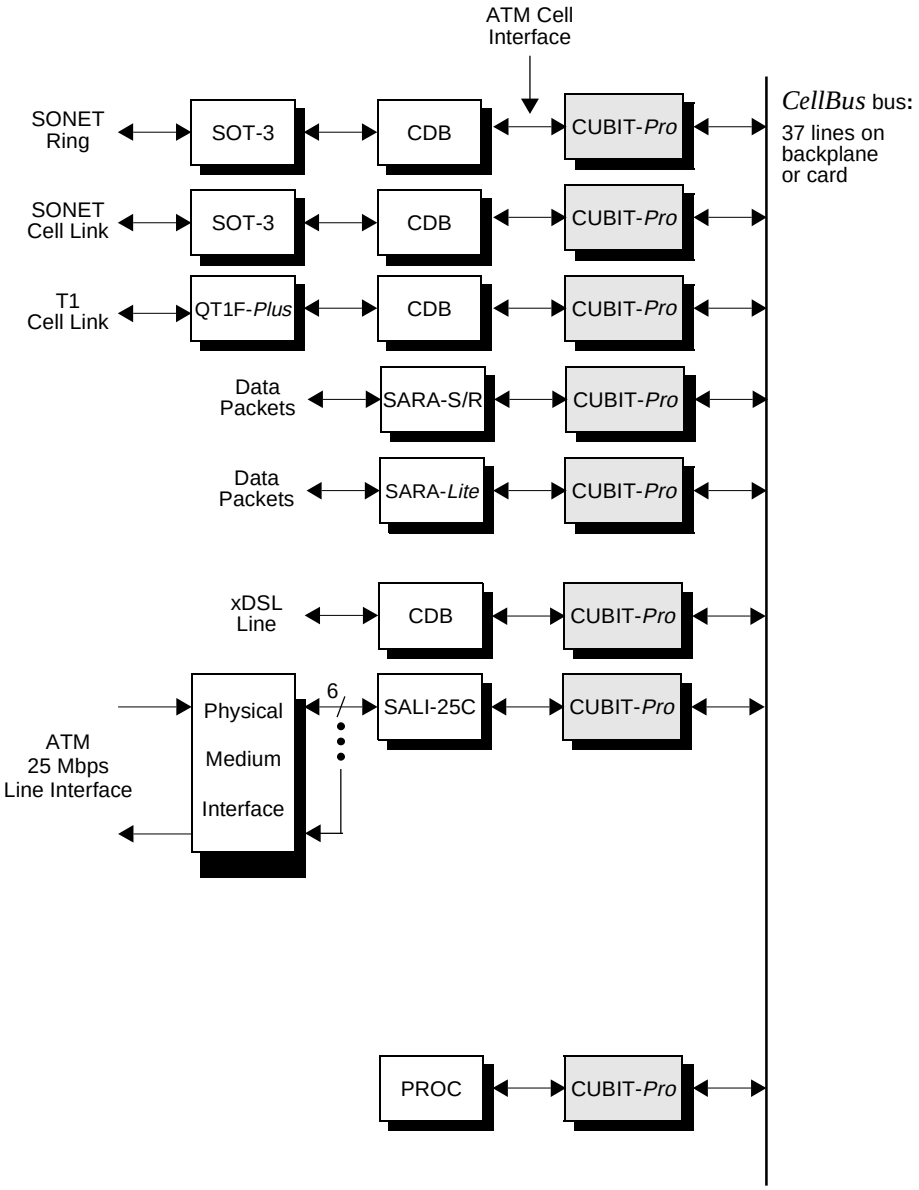
TXC-05551, SARA-2 ATM Cell Processing IC Device. Used with application-specific microcode to perform complete segmentation and reassembly (SAR) for implementing ATM adapter cards, legacy LAN to ATM hubs, and routers. PCI-based host interface. Supports CBR, VBR and UBR services. Integrated SONET/SDH framer.

TXC-05551/L, SARA-*Lite* ATM AAL0/5 Segmentation and Reassembly Product (combination of SARA-2 device and microcode that provides it with the SARA-*Lite* functionality)

TXC-05801, CUBIT Device (ATM *CellBus* Bus Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* bus architecture. A single-chip solution, the CUBIT has the ability to send and also receive cells for control purposes over the same *CellBus* bus. *CellBus* bus technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems. This device is not recommended for use in new designs, which should use CUBIT-*Pro.*

TXC-07625, SALI-25C VLSI Device (Six ATM Line Interface at 25 Mbit/s). Six channel 25.6 Mbit/s ATM transmission convergence function for twisted pair cable. Supports UTOPIA Level 1 and 2. Provides multicasting capability and 4 level priority queuing.

Figure 56. CUBIT-*Pro* TXC-05802 and Related Product Applications in ATM Access Switching



STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum:

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This list of changes identifies areas within this updated CUBIT-*Pro* TXC-05802 Data Sheet that have significant differences relative to the previous, and now superseded, CUBIT-*Pro* TXC-05802 Data Sheet:

Updated CUBIT-*Pro* TXC-05802 Data Sheet: Edition 3, November 1999

Previous CUBIT-*Pro* TXC-05802 Data Sheet: Edition 2B, September 1998

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Added a patent number and changed copyright year.
3	Changed page location for Figure 29.
36	Added Note at end of page.
40	Added Note 5 after the table.
44	Changed "1, 0" to "0,1" in last line of Name/Function column for Symbol LCLOCK.
59, 60	Interchanged the odd and even pulse number sequences (Pnn) between the TRD(7-0) and CID(7-0) signal waveform diagrams, making TRD odd and CID even.
61, 62	Interchanged the odd and even pulse number sequences (Pnn) between the TRA(7-0) and COD(7-0) signal waveform diagrams, making TRA odd and COD even.
67	Substituted two timing parameter tables, for different operating modes, for the one table common to all modes.
88	Replaced List of Data Sheet Changes.

- NOTES -

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