



# Evaluation Board For Fractional-N PLL Frequency Synthesizer

Evaluation Board Tech Note

**EVAL-ADF4154EB1**

## FEATURES

**Self-Contained Board Including Synthesizer, VCO and Loop Filter**

**Designed For PHS Application:**

**19.2 MHz PFD Frequency, 300 kHz Channel Spacing, 100 kHz Loop Bandwidth. Charge Pump Current 0.625mA for Fast Lock Operation**

**Accompanying Software Allows Complete Control of Synthesizer Functions from PC**

**Battery Operated: Choice of 3V or 5V Supplies**

**Typical Phase Noise Performance of -103 dBc/Hz @ 1 kHz Offset from Carrier**

## GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the ADF4154 Frequency Synthesizer for PLL's (Phase Locked Loops). The block diagram of the board is shown below. It contains the ADF4154 synthesizer, a pc connector, 19.2MHz TCXO for the reference input, SMA connectors for the power supplies and RF output. There is also a low pass loop filter (100kHz) and a VCO (Sirenza VCO190-1650T) on board. The evaluation board is set up for a 19.2MHz PFD comparison frequency. A cable is included with the board to connect to a pc printer port.

The package also contains windows software (2000 and XP compatible) to allow easy programming of the synthesizer.

## BLOCK DIAGRAM

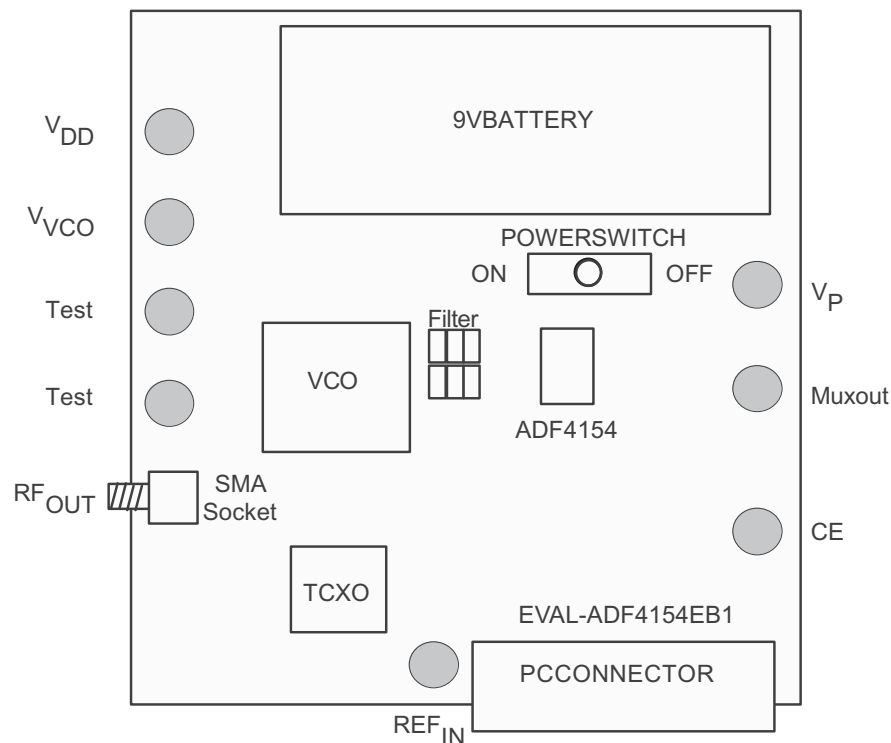


Figure 1.

## PR. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
 Tel: 781.329.4700 [www.analog.com](http://www.analog.com)  
 Fax: 781.326.8703 © 2004 Analog Devices, Inc. All rights reserved.

**TABLE OF CONTENTS**

<b>HARDWARE DESCRIPTION.....</b>	<b>3</b>	<b>SOFTWARE.....</b>	<b>7</b>
<i>OVERVIEW</i> .....	3	<i>Basic operation</i> .....	7
<i>POWER SUPPLIES</i> .....	3	<i>Fast Lock Operation</i> .....	8
<i>LOCAL OSCILLATOR COMPONENTS</i> .....	3	<b>PLL SIMULATIONS .....</b>	<b>11</b>
<i>SCHEMATICS</i> .....	4	<b>BILL OF MATERIALS .....</b>	<b>12</b>
<i>TEST SET UP</i> .....	6		

# HARDWARE DESCRIPTION

## OVERVIEW

The evaluation board comes with a cable for connecting to the printer port of a PC. The silk screen and cable diagram for the evaluation board are shown below. The board schematic is shown on pages 4 and 5.

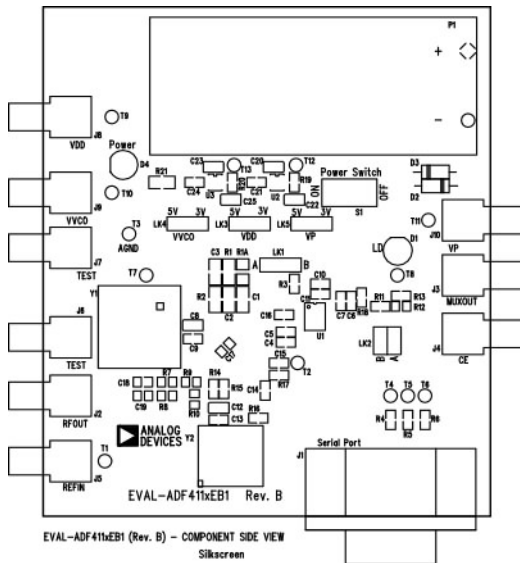


Figure 2. Evaluation Board Silk Screen

## POWER SUPPLIES

The board is powered from a single 9V battery. The power supply circuitry allows the user to choose 3V for the ADF4154  $V_{DD}$  and either 3V or 5V for the ADF4154  $V_P$  and for the VCO supply. The default settings are 3V for the ADF4154  $V_{DD}$  and 5V for the ADF4154  $V_P$  and for the VCO supply.

**It is very important to note that the ADF4154  $V_{DD}$  should never exceed the ADF4154  $V_P$ . This can cause damage to the device.**

If the user wishes, external power supplies may be used. In this case, you need to insert SMA connectors as shown on the silk screen and block diagram.

## LOCAL OSCILLATOR COMPONENTS

All components necessary for Local Oscillator (LO) generation are included on the board. The 19.2 MHz TCXO from Fox Electronics provides the necessary Reference Input. The PLL is made up of the ADF4154, a passive loop filter (100 kHz bandwidth), and the VCO190-1650T VCO from Sirenza Microdevices. The loop bandwidth has been set to 100kHz to meet typical PHS lock time requirements. The output is available at RFOUT through a standard SMA connector. Note that an external REFIN may be used if desired. In this case, an extra SMA needs to be inserted and the on-board TCXO disabled by removing R14, R16 and R18. If the external source has an output impedance of  $50 \Omega$ , then R17 (value  $50 \Omega$ ) should be inserted on the board for matching purposes.

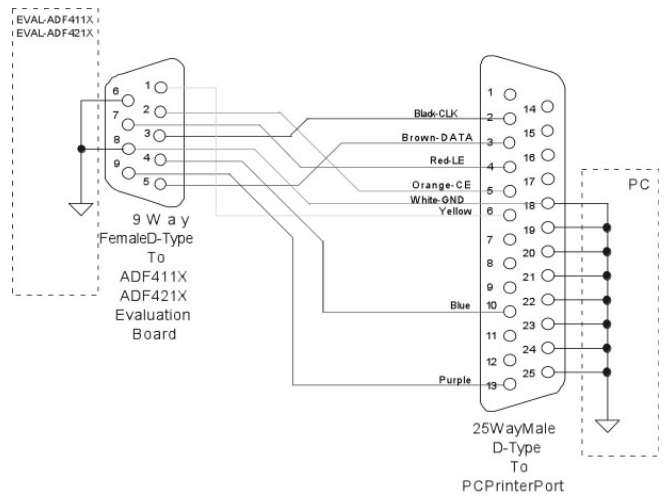


Figure 3. PC Cable Diagram

SCHEMATICS

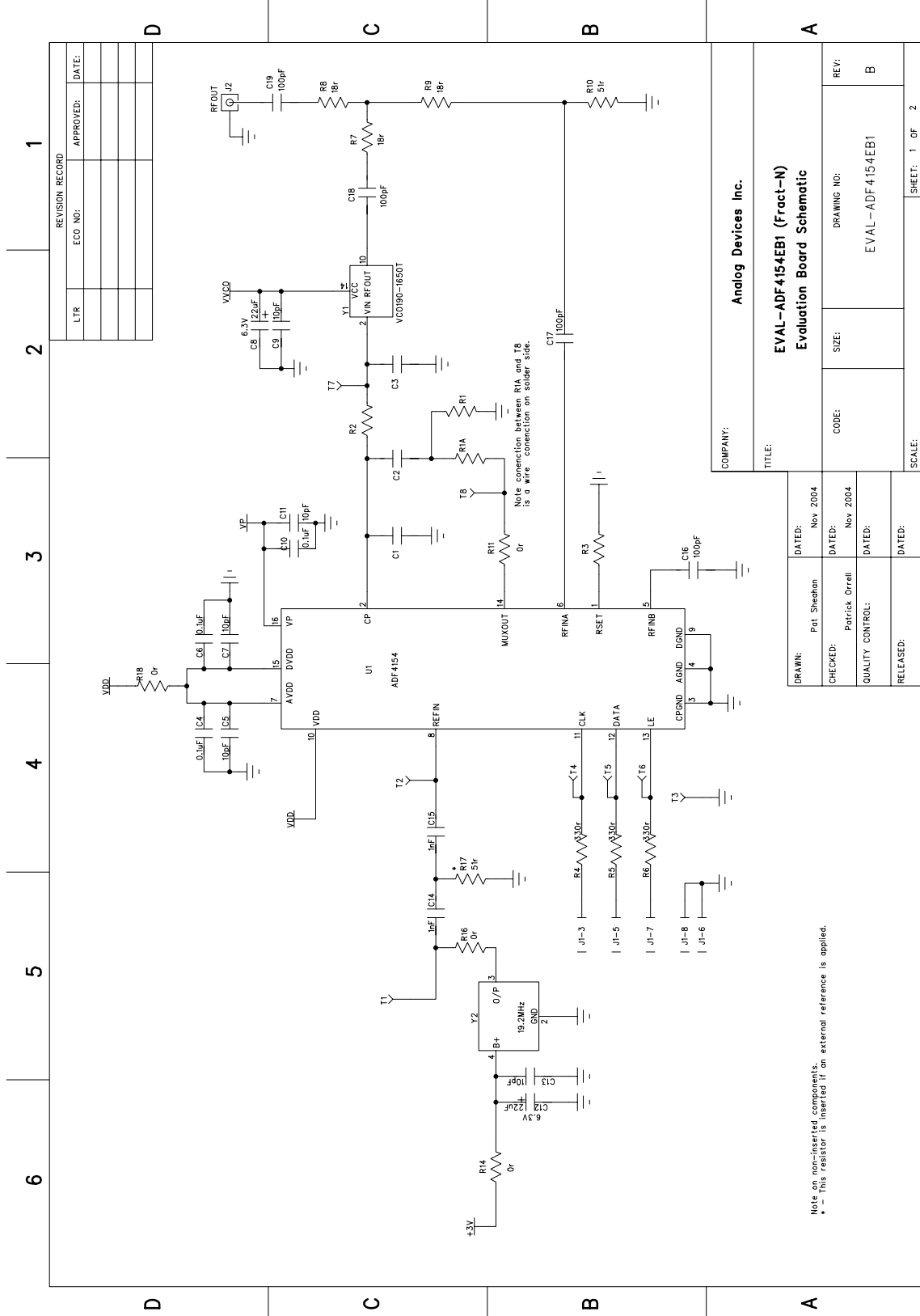
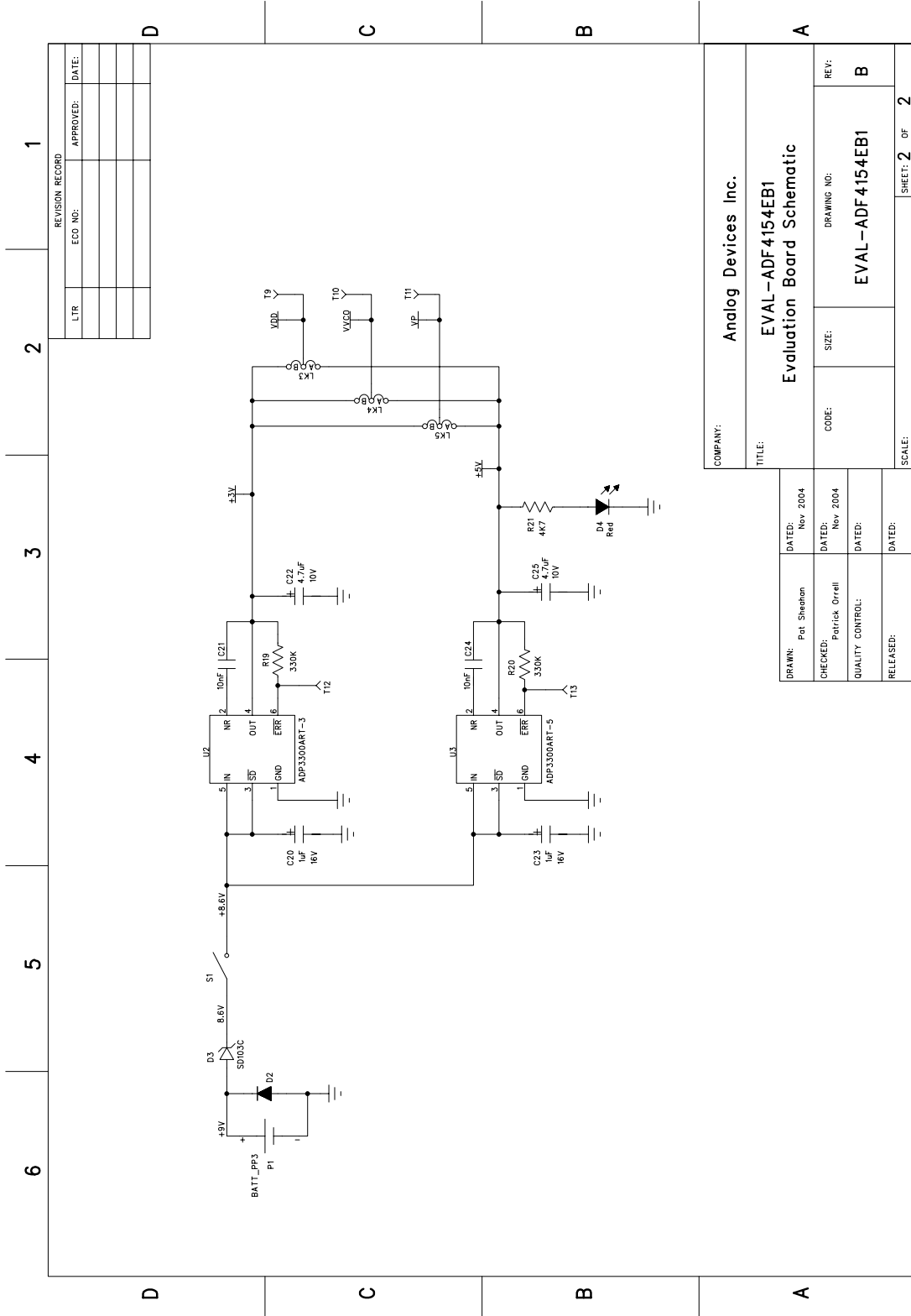


Figure 4. Evaluation Board Schematic (Page 1)



REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

COMPANY: Analog Devices Inc.			
TITLE: EVAL-ADF4154EB1 Evaluation Board Schematic			
DRAWN: Pat Sheehan	DATED: Nov 2004	CODE:	REV: B
CHECKED: Patrick Orrell	DATED: Nov 2004	SIZE:	DRAWING NO: EVAL-ADF4154EB1
QUALITY CONTROL:	DATED:	SCALE:	SHEET: 2 OF 2
RELEASED:	DATED:		

Figure 5. Evaluation Board Schematic (Page 2)

TEST SET UP

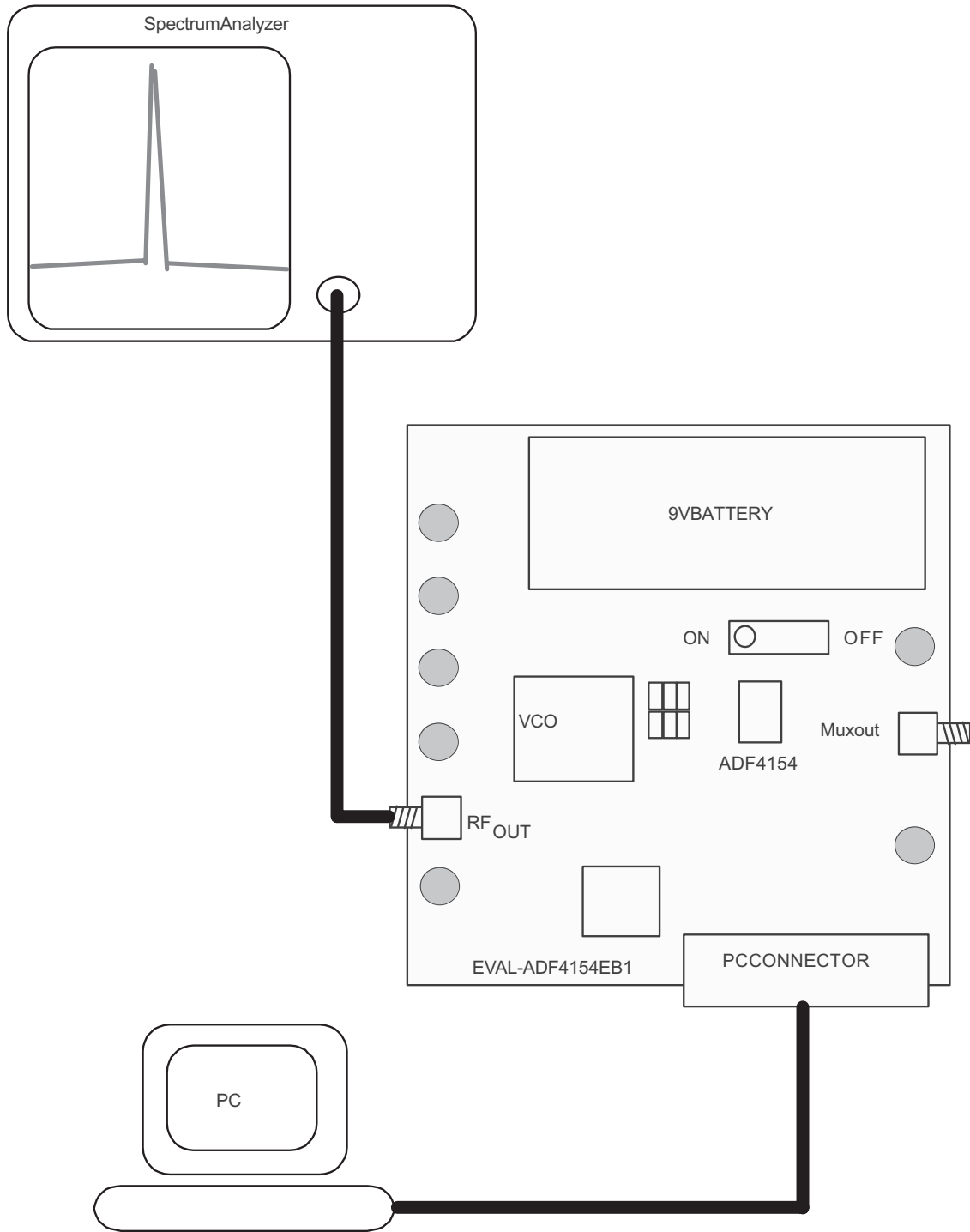


Figure 6. Test Set Up

# SOFTWARE

## BASIC OPERATION

The control software for EVAL-ADF4154EB1 is on the CD which accompanies the board. If the user clicks on “setup.exe”, then the install wizard guides the user through the install process. Simply follow the on-screen instructions. The software will be installed in a default directory call “C:/Program Files/Analog Devices/ADF\_Frac”. To run the software, click on ADF\_Frac\_\_exe.

Before the main software screen appears, the Device Window is shown. This will ask the user to choose which device is being evaluated. Choose ADF4154 and click OK.

The Main Interface Window will now appear (Figure 7). In the RF Section enter the PLL information as shown (Figure 8) and

Update R0 and R1 (Normal Mode). Now exit the window and the main interface will now appear again as in Figure 7

Click on “Update All Registers” and an RF spectrum should appear at the output. The data is now set up and other features can be examined by the user. Note that the charge pump current is 0.625mA to allow for current boosting in Fast lock Mode. To change the VCO output frequency and/or channel spacing, click on the text of the “RF VCO Output Frequency”. The output frequency window will appear and you can change this value. In addition frequency hopping and sweeping can now be performed

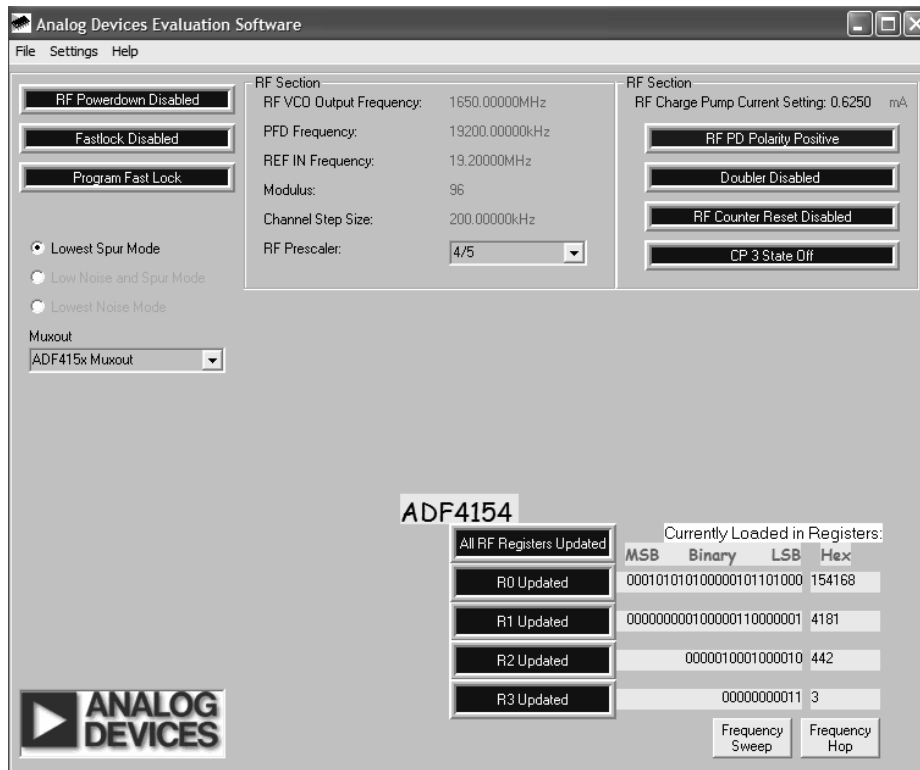


Figure 7. Software Front Panel

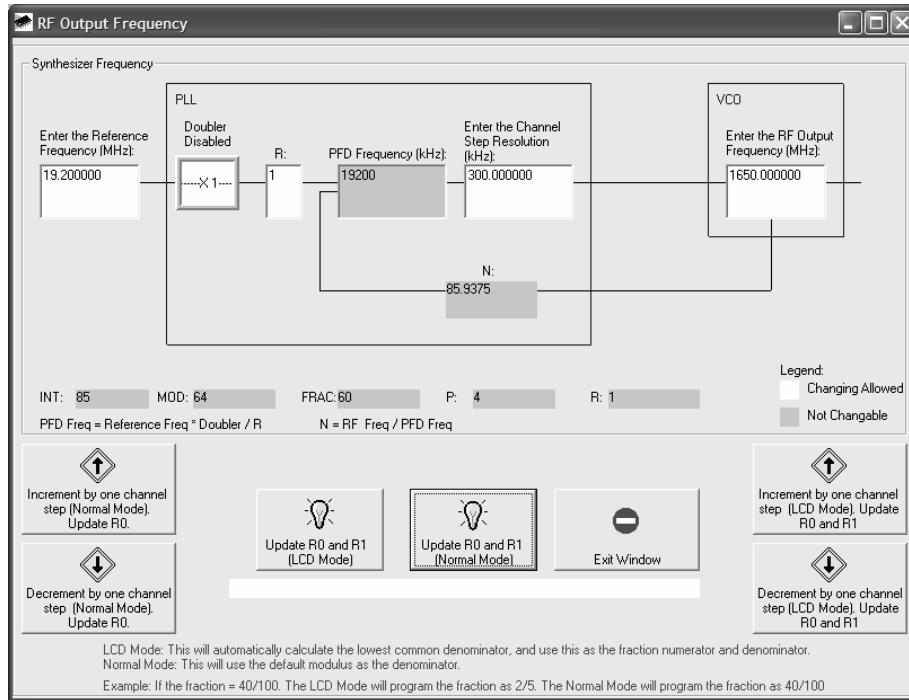


Figure 8. RF Front Panel

## FAST LOCK OPERATION

One of the main features of the ADF4154 is a built in timer that allows the PLL to lock faster than a traditional PLL. The ADF4154 can boost its bandwidth for a determined period of time to allow fast locking then switch back to its final loop bandwidth. The ADF4154 stores this timer value in the place of the Modulus if the correct bits are setup in the register. The following sequence describes how to use the FAST LOCK feature

Firstly, the FAST LOCK counter needs to be setup. Press “Program Fast Lock”, and the panel shown in Figure 9 should appear. In this panel the time period that the PLL will remain in FAST LOCK is programmed. Clearly this time period must be less than the lock time requirement eg If the lock time requirement was 20 $\mu$ s then a value of 30 $\mu$ s would not be suitable. A value needs to be chosen such that the wide bandwidth loop has settled.

The time in wide bandwidth = Timer Value/ PFD. In the example above the timer value is 150 and the PFD =19.2 MHz and hence the time in wide bandwidth is 7.8 $\mu$ s

Once the timer value has been selected Press “Load Now” and “Update R1”. Now the Fast lock must be enabled with the button above Fast Lock Programmed as shown in Figure 10. Now update R0

Finally, as Register 1 was used to store the timer value the Modulus Value need to be re-loaded to the part by entering a valid channel frequency, and press “Load R0 and R1” This is seen in Figure 11

Now the ADF4154 is ready for Fast Lock Operation. The part can “hop” between two channels by using the “Frequency Hop” button. Triggering for lock time measurements can be done by connecting to T6 on the evaluation board



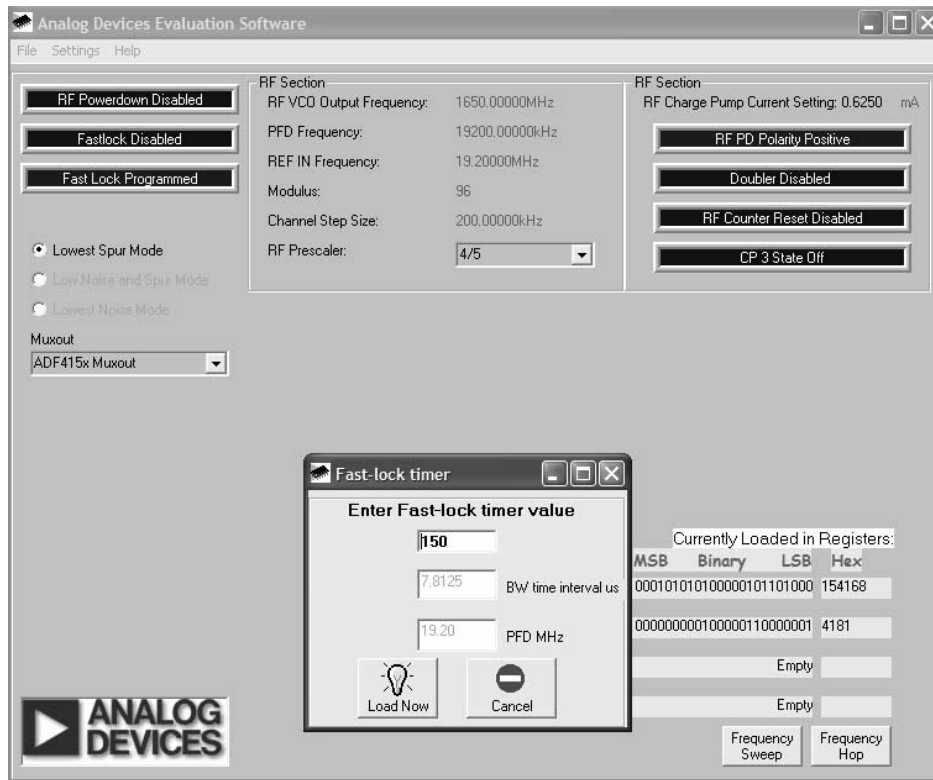


Figure 9. FAST LOCK timer set up

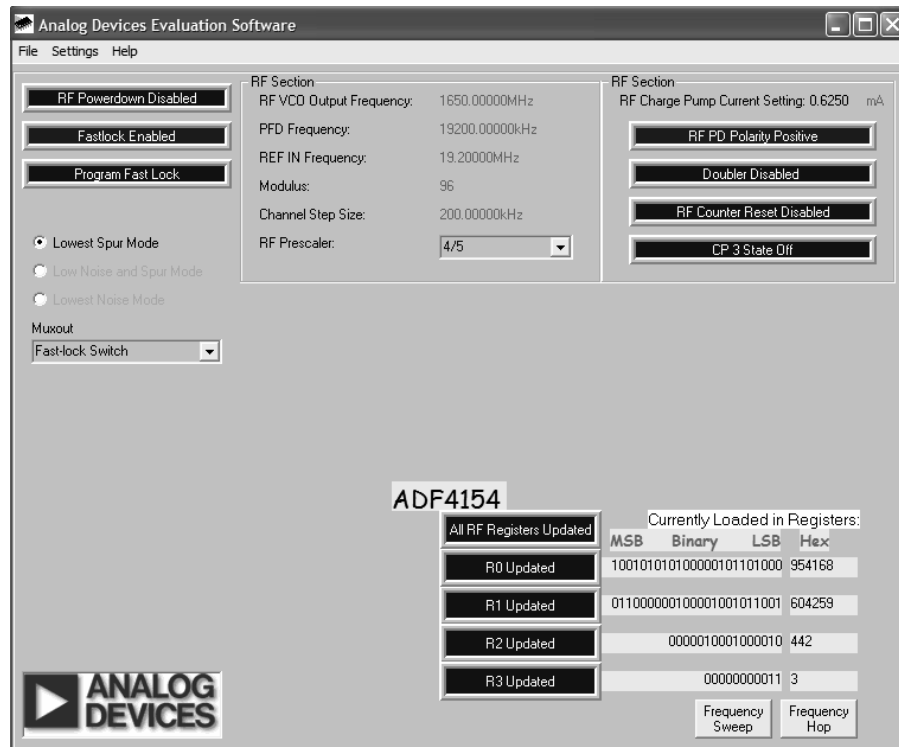


Figure 10. FAST LOCK Enable

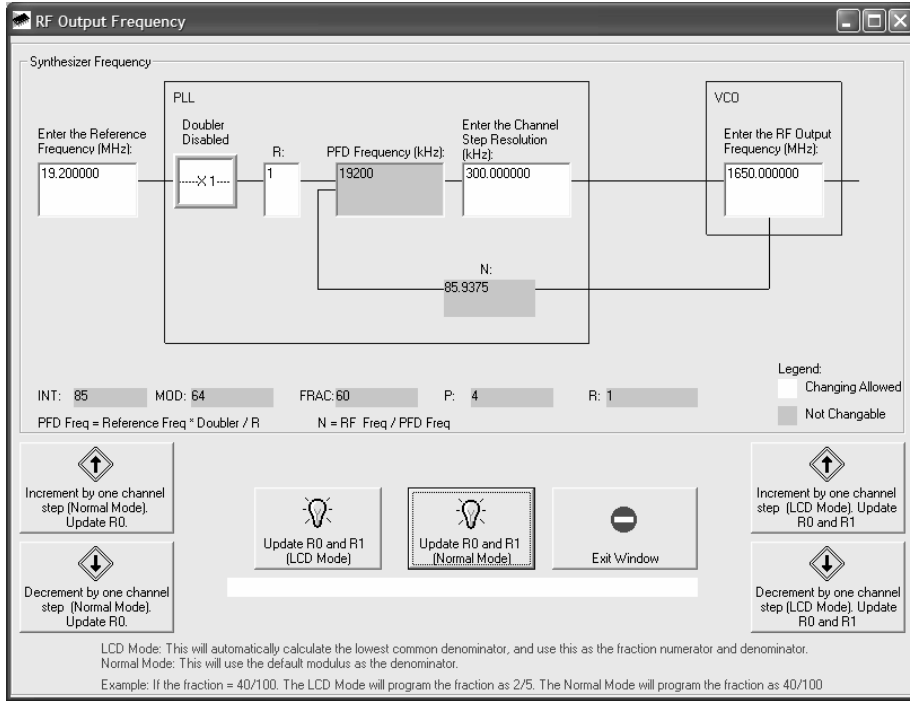
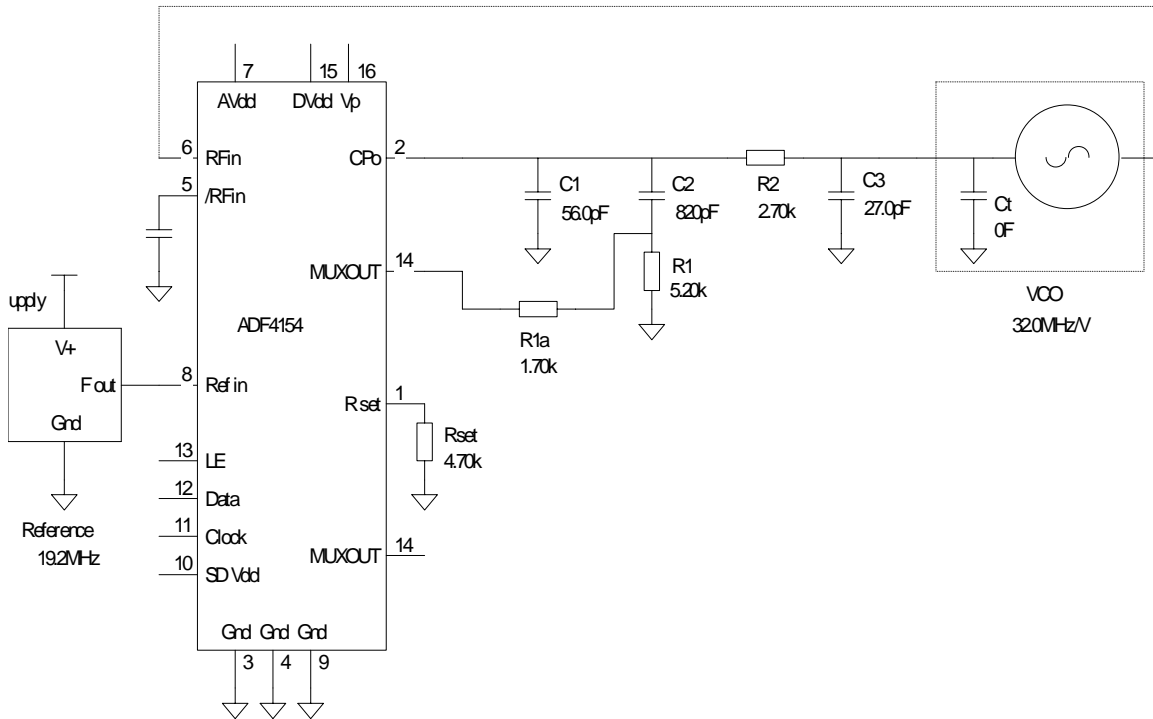
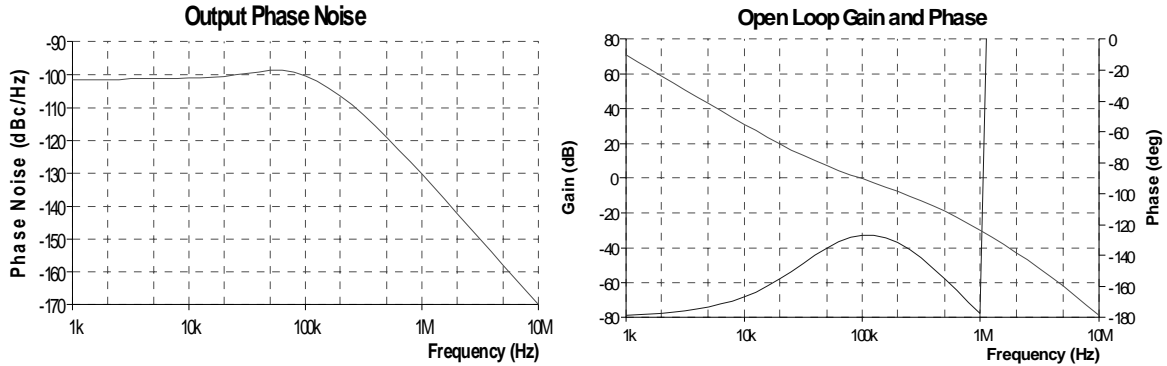


Figure 11 . Re-load the Modulus

# PLL SIMULATIONS

The ADF4154 performance can be simulated using ADI simPLL v2.5. The file has been provided on the CD that shows the performance of the evaluation board. The latest version of simPLL can be downloaded at [www.analog.com/pll](http://www.analog.com/pll)



- Notes:
1. TSSOP pin numbers shown
  2. AVdd Analog Power supply
  3. DVdd Digital Power Supply
  4. Vp Charge Pump power supply
  5. AVdd = DVdd, Vp >= DVdd/AVdd
  6. MUXOUT supports EITHER Fastlock OR Lock Detect functions
  6. Consult manufacturer's data sheet for full details

Figure 12. ADIsimPLL

BILL OF MATERIALS

Name	Part Type	Value	PCB Decal	Stock Code	SMD	Assemble
C1	CAP	56pF	0805		Yes	Yes
C2	CAP	820pF	0805		Yes	Yes
C3	CAP	27pF	0805		Yes	Yes
C4	CAP	0.1uF	0603	FEC 499-675	Yes	Yes
C5	CAP	10pF	0603	FEC 499-110	Yes	Yes
C6	CAP	0.1uF	0603	FEC 499-675	Yes	Yes
C7	CAP	10pF	0603	FEC 499-110	Yes	Yes
C8	CAP+	22uF 6.3V	CAP1TAJ_A	FEC 197-038	Yes	Yes
C9	CAP	10pF	0603	FEC 499-110	Yes	Yes
C10	CAP	0.1uF	0603	FEC 499-675	Yes	Yes
C11	CAP	10pF	0603	FEC 499-110	Yes	Yes
C12	CAP+	22uF 6.3V	CAP1TAJ_A	FEC 197-038	Yes	Yes
C13	CAP	10pF	0603	FEC 499-110	Yes	Yes
C14	CAP	1nF	0603	FEC 317-202	Yes	Yes
C15	CAP	1nF	0603	FEC 317-202	Yes	Yes
C16	CAP	100pF	0603	FEC 499-122	Yes	Yes
C17	CAP	100pF	0603	FEC 499-122	Yes	Yes
C18	CAP	100pF	0603	FEC 499-122	Yes	Yes
C19	CAP	100pF	0603	FEC 499-122	Yes	Yes
C20	CAP+	1uF	CAP1TAJ_A	FEC 498-701	Yes	Yes
C21	CAP	10nF	0603	FEC 499-146	Yes	Yes
C22	CAP+	4.7uF 10V	CAP1TAJ_A	FEC 498-658	Yes	Yes
C23	CAP+	1uF	CAP1TAJ_A	FEC 498-701	Yes	Yes
C24	CAP	10nF	0603	FEC 499-146	Yes	Yes
C25	CAP+	4.7uF 10V	CAP1TAJ_A	FEC 498-658	Yes	Yes
D1	LED	Green	LED		No	No
D2	DIODE		DO35	FEC 365-117	No	Yes
D3	SD103C	6.2V	DO35	SD103C	No	Yes
D4	LED	Red	LED	FEC 657-130	No	Yes
J1	CON-DB9HM		DB9-HM	FEC 150-750	No	Yes
J2	SMA		SMA_EDGE	Vitelec 142-0701-851	No	Yes
J3	SMA		SMA_EDGE	Digikey J658-ND	No	No
J4	SMA		SMA_EDGE		No	No
J5	SMA		SMA_EDGE		No	No
J6	SMA		SMA_EDGE		No	No
J7	SMA		SMA_EDGE		No	No
J8	SMA		SMA_EDGE		No	No
J9	SMA		SMA_EDGE		No	No
J10	SMA		SMA_EDGE		No	No
LK1	JUMPER2/SIP3		LINK-3P	FEC 512-047 & FEC 150-410	No	Yes
LK2	JUMPER-2		JUMPER_2	FEC 512-035 & FEC 150-410	No	Yes
LK3	JUMPER2/SIP3		LINK-3P	FEC 512-047 & FEC 150-410	No	Yes
LK4	JUMPER2/SIP3		LINK-3P	FEC 512-047 & FEC 150-410	No	Yes
LK5	JUMPER2/SIP3		LINK-3P	FEC 512-047 & FEC 150-410	No	Yes
P1	BATT_PP3		BATT_PP3	FEC 723-988	No	Yes
P1	9V PP3 Battery			FEC 908-526	No	Yes
R1A	RES	1.7k	0805		Yes	Yes
R1	RES	5.2k	0805		Yes	Yes
R2	RES	2.7K	0805		Yes	Yes
R3	RES	4k7	0603	FEC 911-318	Yes	Yes
R4	RES	330R	0603	FEC 911-143	Yes	Yes
R5	RES	330R	0603	FEC 911-143	Yes	Yes
R6	RES	330R	0603	FEC 911-143	Yes	Yes
R7	RES	18R	0603	FEC 911-021	Yes	Yes
R8	RES	18R	0603	FEC 911-021	Yes	Yes
R9	RES	18R	0603	FEC 911-021	Yes	Yes
R10	RES	51r	0603	Digikey 311-51GCT-ND	Yes	Yes
R11	RES	0r	0603	FEC 772-227	Yes	Yes
R12	RES	10K	0603		Yes	No
R13	RES	10K	0603		Yes	No
R14	RES	0r	0603	FEC 772-227	Yes	Yes
R15	RES	0r	0603		Yes	No
R16	RES	0r	0603	FEC 772-227	Yes	Yes
R17	RES	51r	0603		Yes	No
R18	RES	0r	0603	FEC 772-227	Yes	Yes
R19	RES	330K	0603	FEC 911-537	Yes	Yes
R20	RES	330K	0603	FEC 911-537	Yes	Yes
R21	RES	4K7	0805	FEC 911-318	Yes	Yes
S1	SW_POWER		SW_SIP-3P	FEC 150-559	No	Yes
T1	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T2	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T3	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T4	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T5	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T6	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T7	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T8	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T9	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T10	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T11	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T12	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
T13	TESTPOINT		TESTPOINT	FEC-240-345	No	Yes
U1	ADF411X		TSSOP-16	ADF4154BRU	Yes	Yes
U2	ADP3300		SOT23-6	ADP3300ART-3	Yes	Yes
U3	ADP3300		SOT23-6	ADP3300ART-5	Yes	Yes
Y1	VCO190-1750T		VCO190-1650T	Var-L VCO190-1650T	Yes	Yes
Y2	OSC_TCXO	19.2MHz	OSC_TCXO	Fox 801BE	Yes	Yes
Insert wire link from R1a (end near LK1 A jumper) to R11 (end near T5)						
Corners						
	Rubber Stick-On Feet x4			FEC 148-922		
	Bare PCB			Eval-ADF411xEB1 Rev. B1		
	RF Eval Board Cable			Aragorn Services		
	CD & Sleeve			ADI Issue		
	Barcode Label			Eval-ADF4154EB1		
	Eval Board Box			Europaks K-645/1		
	Anti-Static Bag			FEC 522-764		
	Anti-Static Bubble Wrap					



**NOTES**

## NOTES