National Semiconductor

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LMH6555
Low Distortion 1.2 GHz Differential Driver

General Description

The LMH6555 is an ultra high speed differential line driver with 53 dB SFDR at 750 MHz. The LMH6555 features a fixed gain of 13.7 dB. An input to the device allows the output common mode voltage to be set independent of the input common mode voltage in order to simplify the interface to high speed differential input ADCs. A unique architecture allows the device to operate as a fully differential driver or as a single-ended to differential converter.

The outstanding linearity and drive capability (100Ω differential load) of this device are a perfect match for driving high speed analog-to-digital converters. When combined with the ADC081000/ ADC081500 (single or dual ADC), the LMH6555 forms an excellent 8-bit data acquisition system with analog bandwidths exceeding 750 MHz.

The LMH6555 is offered in a space saving 16-pin LLP package.

Features

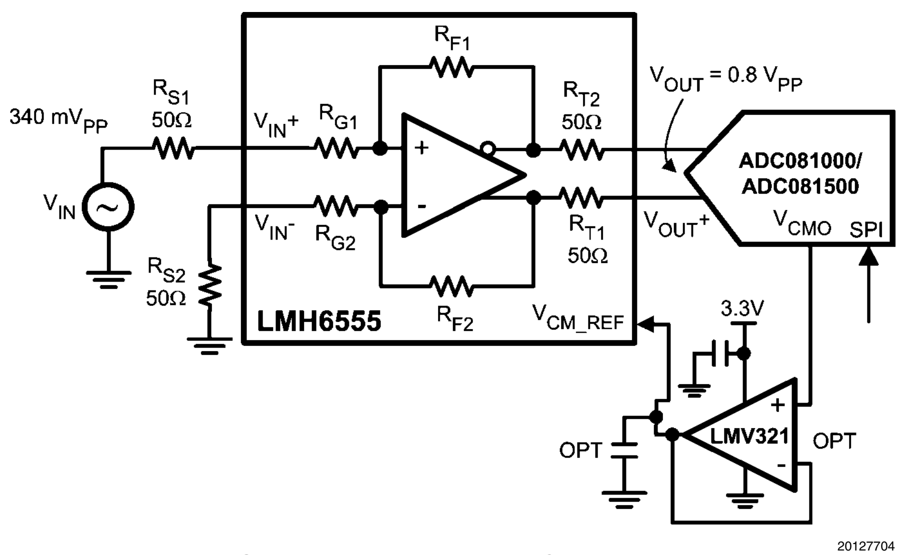
Typical values unless otherwise specified.

- −3 dB bandwidth (V_{OUT} = 0.80 V_{PP}) — 1.2 GHz
- ±0.5 dB gain flatness (V_{OUT} = 0.80 V_{PP}) — 330 MHz
- Slew rate — 1300 V/μs
- 2nd/3rd Harmonics (750 MHz) — −53/−54 dBc
- Fixed gain — 13.7 dB
- Supply current — 120 mA
- Single supply operation — 3.3V ±10%
- Adjustable common-mode output voltage

Applications

- Differential ADC driver
- National Semiconductor ADC081500/ ADC081000 (single or dual) driver
- Single ended to differential converter
- Intermediate frequency (IF) amplifier
- Communication receivers
- Oscilloscope front end

Typical Application



Single Ended to Differential Conversion

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V
V_S	4.2V
Output Short Circuit Duration (one pin to ground)	Infinite
Common Mode Input Voltage	−0.4V to 3V
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 4)	−40°C to +85°C
Supply Voltage Range	+3.3V ±10%
Package Thermal Resistance (θ_{JA})(Note 4)	
16-Pin LLP	65°C/W

3.3V Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A= 25°C, V_{CM_REF} = 1.2V, both inputs tied to 0.3V through 50Ω (R_{S1} & R_{S2}) each (Note 11), V_S = 3.3V, R_L = 100Ω differential, V_{OUT} = 0.8 V_{PP}. See the Definition of Terms and Specification section for definition of terms used throughout the datasheet. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
AC/DC Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		1200		MHz
LSBW		V_{OUT} = 0.8 V_{PP}		1200		
Peak	Peaking	V_{OUT} = 0.8 V_{PP}		1.4		dB
GF_0.1 dB	Gain Flatness	±0.1 dB		180		MHz
GF_0.5 dB		±0.5 dB		330		
Ph_Delta	Phase Delta	Output Differential Phase Difference f ≤ 1.2 GHz		< ±0.8		deg
Lin_Ph	Linear Phase Deviation	Each Output f ≤ 2 GHz		< ±30		deg
GD	Group Delay	Each Output f ≤ 2 GHz		0.75		ns
P_1 dB	1 dB Compression	1 GHz		1		V_{PP}
TRS/TRL	Rise/ Fall Time	V_{OUT} = 0.2 V_{PP} Each Output		320		pS
OS	Overshoot	V_{OUT} = 0.2 V_{PP} Each Output		14		%
SR	Slew Rate	0.8V Step, 10% to 90%,(Note 6)		1300		V/µs
t_s	Settling Time	±1%		2.2		ns
A_{V_DIFF}	Insertion Gain (IS_{21}I)	DC, $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	13.2 **13.1**	13.7	14.0 **14.1**	dB
TC A_{V_DIFF}	Temperature Coefficient of Insertion Gain			−0.9		mdB/°C
ΔA_{V_DIFF1}	Insertion Gain Variation with V_{CM_REF}	V_{CM_REF} Input Varied from 0.95V to 1.45, V_{OUT} = 0.8 V_{PP}		−0.04	±0.50 **±0.58**	dB
ΔA_{V_DIFF2}	Insertion Gain Variation with V_{I_CM}	$-0.3 \le V_{I\_CM} \le 2.0V$		±0.03	±0.48 **±0.55**	dB
Distortion And Noise Response						
HD2_L	2nd Harmonic Distortion	250 MHz (Note 12)		−60		dBc
HD2_M		500 MHz (Note 12)		−62		
HD2_H		750 MHz (Note 12)		−53		
HD3_L	3rd Harmonic Distortion	250 MHz (Note 12)		−67		dBc
HD3_M		500 MHz (Note 12)		−61		
HD3_H		750 MHz (Note 12)		−54		

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
OIP3	Output 3rd Order Intermodulation Intercept	f = 1 GHz P_{OUT} (Each Tone) ≤ 8.5 dBm (Notes 12, 13)		27.5		dBm
OIM3	3rd Order Intermodulation Distortion	f = 1 GHz P_{OUT} (Each Tone) = −6 dBm (Notes 12, 13)		−67		dBc
e_{no}	Output Referred Voltage Noise	≥1 MHz		19		$nV/\sqrt{Hz}$
NF	Noise Figure	Relative to a Differential Input ≥10 MHz		15.0		dB
Input Characteristics						
R_{IN}	CM Input Resistance	Each Input to Ground	45	50	55	Ω
R_{IN_DIFF}	Differential Input Resistance	Differential	66	78	100	Ω
C_{IN}	Input Capacitance	Each Input to GND		0.3		pF
CMRR	Common Mode Rejection Ratio	−0.3 ≤ CMVR ≤ 2.0V	40 **36**	68		dB
Output Characteristics						
V_{OOS}	Output Offset Voltage	Differential Mode		15	±50 **±55**	mV
TCV_{OOS}	Output Offset Voltage Average Drift	(Note 9)		±100		μV/°C
R_O	Output Resistance	R_{T1} and R_{T2}	43	50	53	Ω
BAL_Error_DC	Output Gain Balance Error	DC, $\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$		−57	−38	dB
BAL_Error_AC		f = 750 MHz, $\frac{V_{O\_CM}}{V_{OUT}}$		−48		
BAL_Error_AC_ Phase	Output Phase Balance Error	f = 750 MHz, V_{OUT+} - V_{OUT-} Phase		±0.6		deg
$\lvert\Delta V_{O\_CM}/\Delta V_{I\_CM}\rvert$	Output Common Mode Gain	DC		−26	−22 **−21**	dB
V_{CM_REF} Characteristics						
V_{OS_CM}	Output CM Offset Voltage	$V_{OS\_CM} = V_{O\_CM} - V_{CM\_REF}$		−4	±60 **±85**	mV
TC_V_{OS_CM}	CM Offset Voltage Temp Coefficient			−0.2		mV/°C
I_{B_CM}	V_{CM_REF} Bias Current	0.95V ≤ V_{CM_REF} ≤ 1.45V (Note 10)		−25	±390 **±415**	μA
R_{IN_CM}	V_{CM_REF} Input Resistance		3.5	5.8		kΩ
Gain_V_{CM_REF}	V_{CM_REF} Input Gain to Output	$\Delta V_{O\_CM}/\Delta V_{CM\_REF}$	0.97	0.99	1.00	V/V
Power Supply						
I_S	Supply Current	R_{S1} & R_{S2} Open (Note 3)		120	150 **156**	mA
PSRR	Differential Power Supply Rejection Ratio	DC, ΔV_S = ±0.3V, $\Delta V_{OUT}/\Delta V_S$	−27 **−25**	−44		dB
PSRR_CM	Common Mode PSRR	DC, ΔV_S = ±0.3V, $\Delta V_{O\_CM}/\Delta V_S$	−29 **−27**	−39		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: Total supply current is affected by the input voltages connected through R_{S1} and R_{S2}. Supply current tested with input removed.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D= (T_{J(MAX)} — T_A)/ \theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow. Package should be soldered unto a 6.8 mm^2 copper area as shown in the “recommended land pattern” shown in the package drawing.

Note 5: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)
Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 8: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 10: Positive current is current flowing into the device.

Note 11: Quiescent device common mode input voltage is 0.3V.

Note 12: Distortion data taken under single ended input condition.

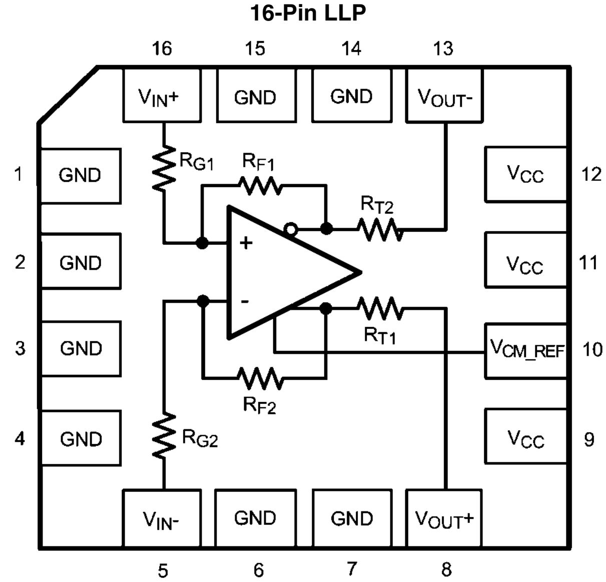
Note 13: 0 dBm = 894 mV_{PP} across 100Ω differential load

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin LLP	LMH6555SQ	L6555SQ	1k Units Tape and Reel	SQA16A
	LMH6555SQE		250 Units Tape and Reel	
	LMH6555SQX		4.5k Units Tape and Reel	

Connection Diagram

16-Pin LLP



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Definition of Terms and Specifications (Alphabetical Order)

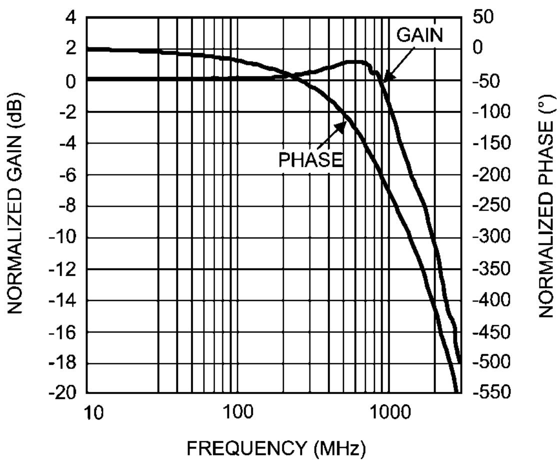
Unless otherwise specified, V_{CM_REF} = 1.2V

1.	A_{V_CM} (dB)	Change in the differential output voltage (ΔV_{OUT}) with respect to the change in input common mode voltage (ΔV_{I_CM})
2.	A_{V_DIFF} (dB)	Insertion gain from a single ended 50Ω (or 100Ω differential) source to the differential output (ΔV_{OUT})
3.	ΔA_{V_DIFF} (dB)	Variation in insertion gain (A_{V_DIFF})
4.	BAL_ERR_DC & BAL_ERR_AC	Balance Error. See $\left(\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}\right)$
5.	CM	Common Mode
6.	CMRR (dB)	Common Mode rejection defined as: A_{V_DIFF} (dB) - A_{V_CM} (dB)
7.	CMVR (V)	Range of input common mode voltage (V_{I_CM})
8.	Gain_V_{CM_REF} (V/V)	Variation in output common mode voltage (ΔV_{O_CM}) with respect to change in V_{CM_REF} input (ΔV_{CM_REF}) with maximum differential output
9.	PSRR (dB)	Differential output change (ΔV_{OUT}) with respect to the power supply voltage change (ΔV_S) with nominal differential output
10.	PSRR_CM (dB)	Output common mode voltage change (ΔV_{O_CM}) with respect to the change in the power supply voltage (ΔV_S)
11.	R_{IN} (Ω)	Single ended input impedance to ground
12.	R_{IN_DIFF} (Ω)	Differential input impedance
13.	R_L (Ω)	Differential output load
14.	R_O (Ω)	Device output impedance equivalent to R_{T1} & R_{T2}
15.	R_{S1}, R_{S2} (Ω)	Source impedance to V_{IN+} and V_{IN-} respectively
16.	R_{T1}, R_{T2} (Ω)	Output impedance looking into each output
17.	V_{CM_REF} (V)	Device input pin which controls output common mode
18.	ΔV_{CM_REF} (V)	Change in the V_{CM_REF} input
19.	V_{I_CM} (V)	DC average of the inputs (V_{IN+}, V_{IN-}) or the common mode signal at those same input pins
20.	ΔV_{I_CM} (V)	Variation in input common mode voltage (V_{I_CM})
21.	V_{IN+}, V_{IN-} (V)	Device input pin voltages
22.	ΔV_{IN} (V)	Terminated (50Ω for single ended and 100Ω for differential) generator voltage
23.	V_{O_CM} (V)	Output common mode voltage (DC average of V_{OUT+} and V_{OUT-})
24.	ΔV_{O_CM} (V)	Variation in output common mode voltage (V_{O_CM})
25.	$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$ (dB)	Balance Error. Measure of the output swing balance of V_{OUT+} and V_{OUT-}, as reflected on the output common mode voltage (V_{O_CM}), relative to the differential output swing (V_{OUT}). Calculated as output common mode voltage change (ΔV_{O_CM}) divided into the output differential voltage change (ΔV_{OUT} which is nominally around 800 mV_{PP})
26.	$\frac{V_{O\_CM}}{V_{OUT}}$ (dB)	AC version of the DC balance error $\left(\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}\right)$ test
27.	V_{OOS} (V)	DC Offset Voltage. Differential output voltage measured with both inputs grounded through 50Ω
28.	V_{OS_CM} (V)	Difference between the output common mode voltage (V_{O_CM}) and the voltage on the V_{CM_REF} input, for the allowable V_{CM_REF} range
29.	V_{OUT} (V)	Differential Output Voltage (V_{OUT+} - V_{OUT-}) (Corrected for DC offset (V_{OOS}))
30.	ΔV_{OUT} (V)	Change in the differential output voltage (Corrected for DC offset (V_{OOS}))
31.	V_{OUT+}, V_{OUT-} (V)	Device output pin voltages
32.	V_S (V)	Supply Voltage (V^+ - V^-)
33.	ΔV_S (V)	Change in V_{CC} supply voltage

Typical Performance Characteristics

Unless otherwise specified, $R_{S1} = R_{S2} = 50\Omega$, $V_S = 3.3V$, $R_L = 100\Omega$ differential, $V_{OUT} = 0.8\ V_{PP}$. See the Definition of Terms and Conditions section for definition of terms used throughout the datasheet.

Frequency Response



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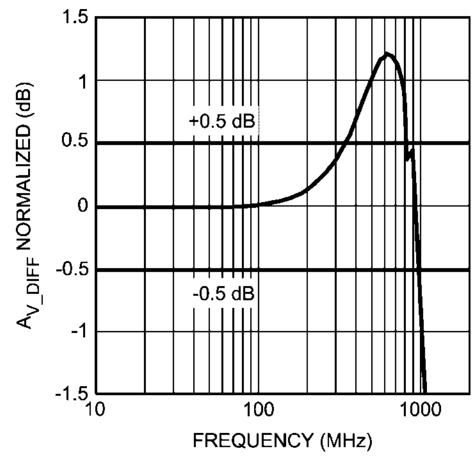
±0.5 dB Gain Flatness



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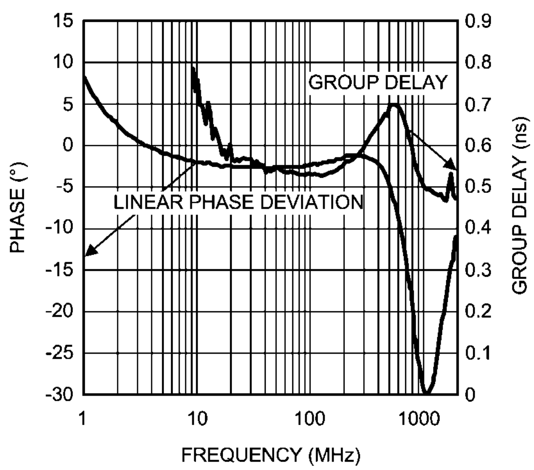
Linear Phase Deviation & Group Delay



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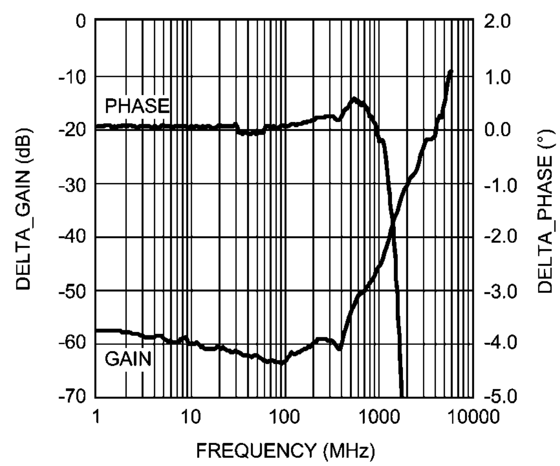
Bal_Error vs. Frequency



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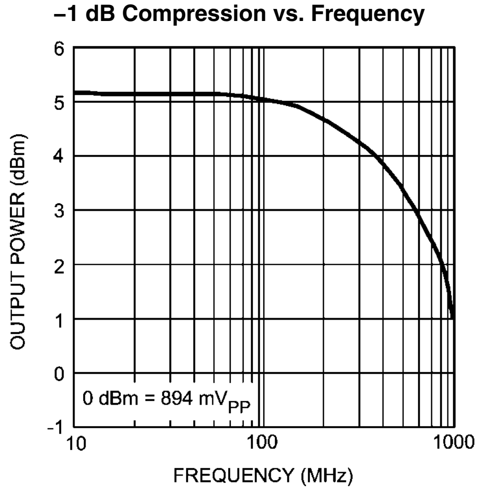
−1 dB Compression vs. Frequency



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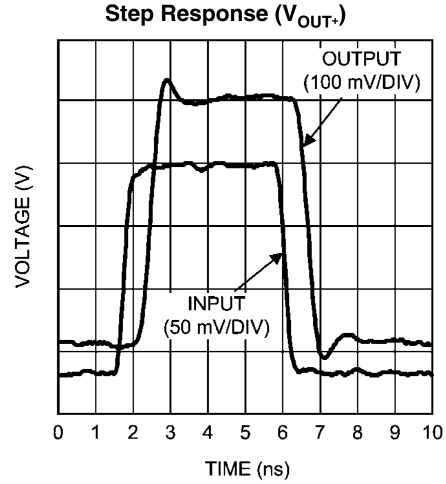
Step Response (V_{OUT+})



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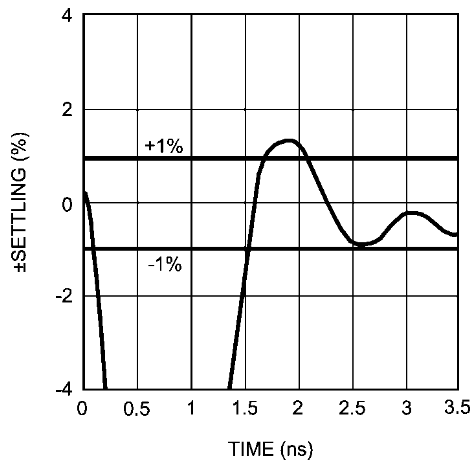
Step Response Settling Time



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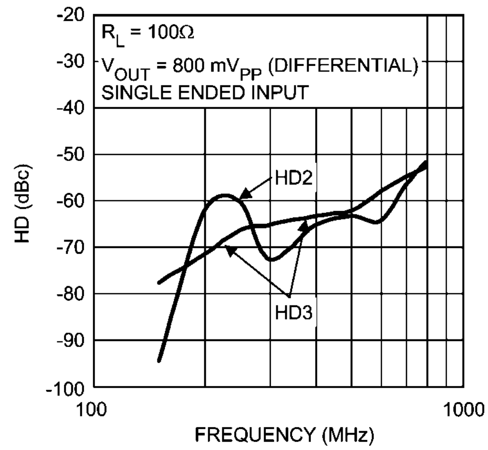
Harmonic Distortion vs. Frequency



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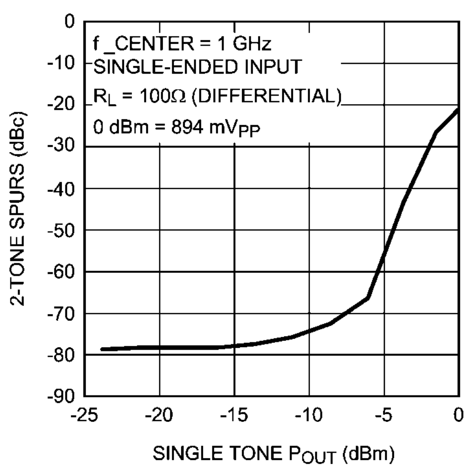
3rd Order Intermodulation Distortion



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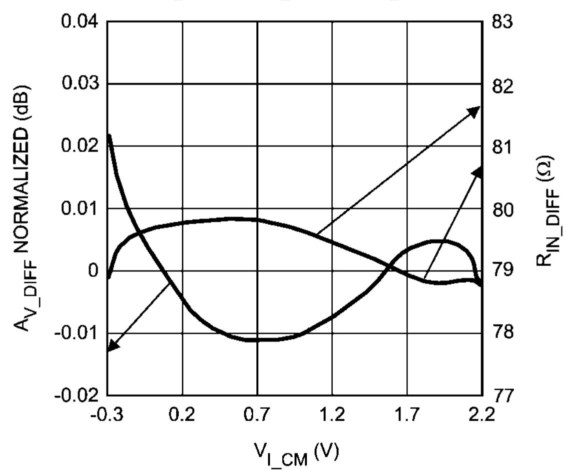
A_{V_DIFF} & R_{IN_DIFF} vs. V_{I_CM}



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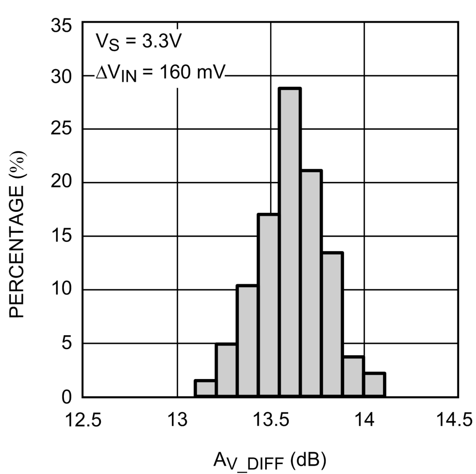
Insertion Gain Distribution



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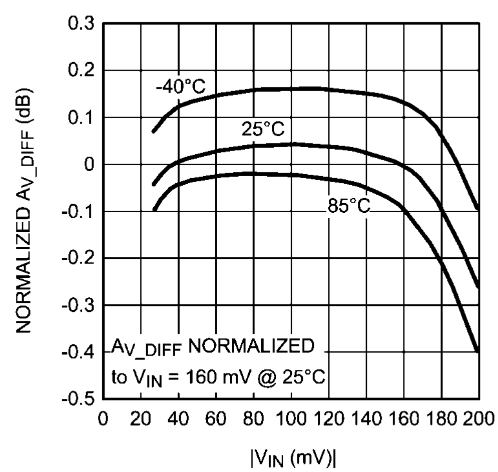
Insertion Gain Variation vs. Input Amplitude



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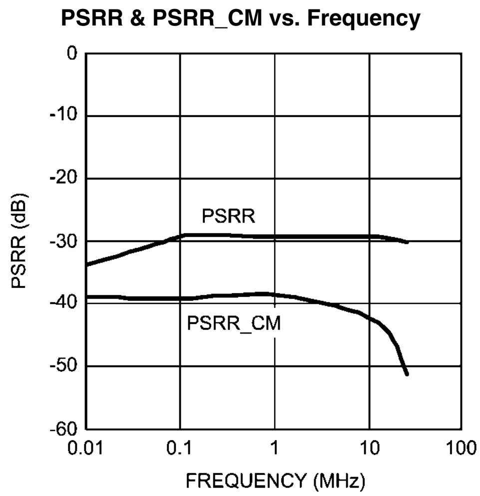

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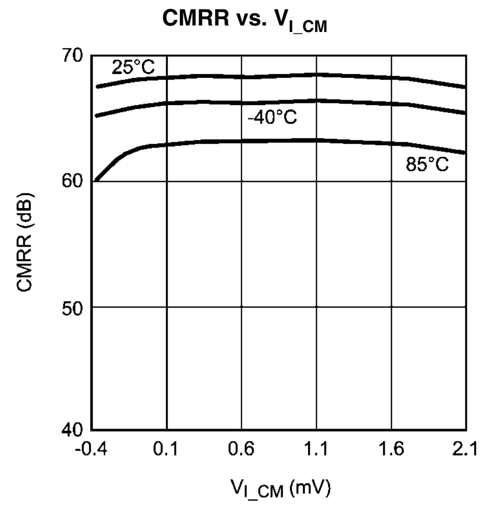

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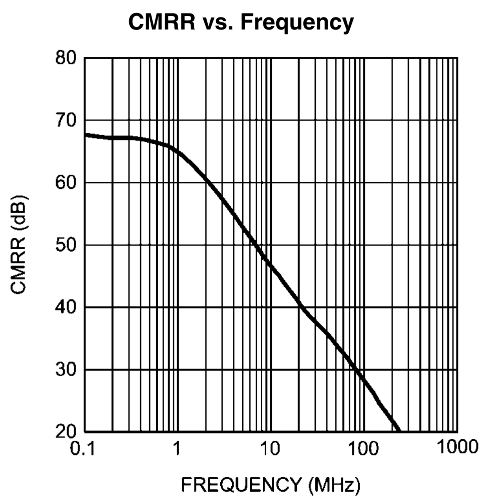

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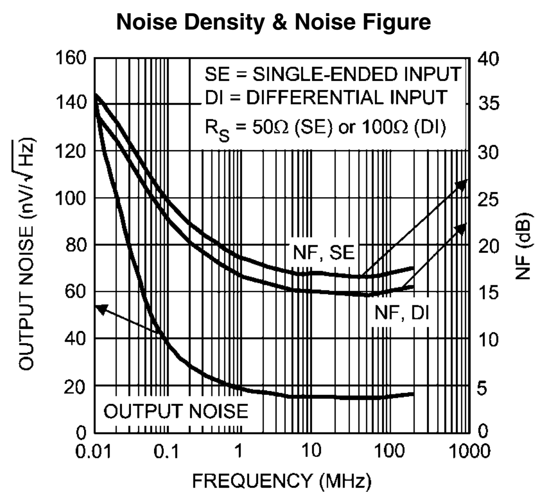

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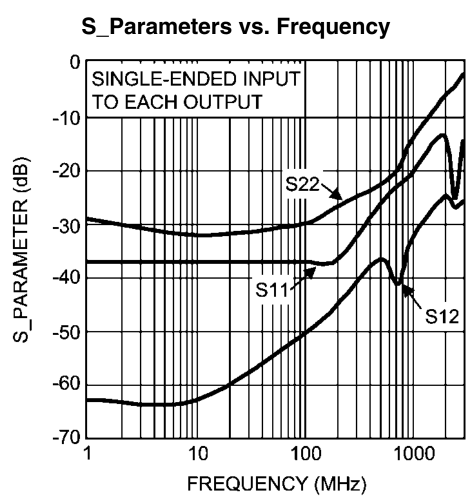

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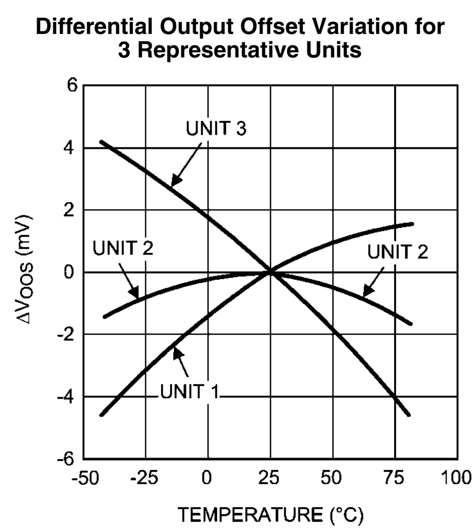

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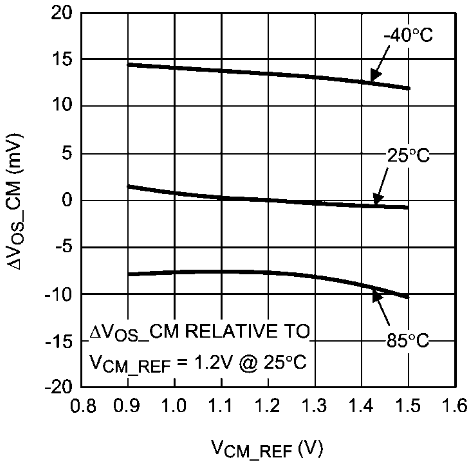
Common Mode Offset Voltage Variation vs. V_{CM_REF}



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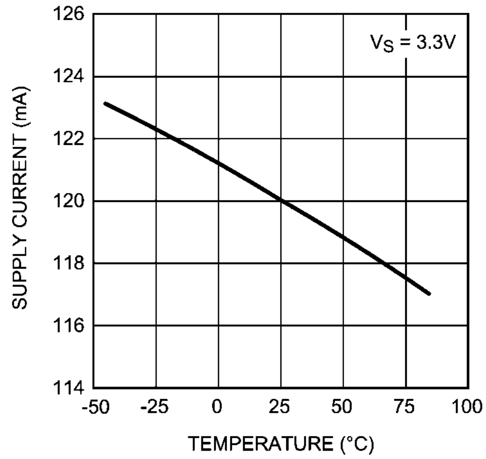
Supply Current vs. Temperature



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Application Information

See the Definition of Terms and Conditions section for definition of terms used.

GENERAL

The LMH6555 consists of three individual amplifiers: The V_{OUT+} driver, V_{OUT-} driver, and the common mode amplifier. Being a differential amplifier, the LMH6555 will not respond to the common mode input (as long as it is within its input common mode range) and instead the output common mode is forced by the built-in common mode amplifier with V_{CM_REF} as its input. As shown, in *Figure 1* below, the V_{CMO} output of most differential high speed ADC's is tied to the V_{CM_REF} input of the LMH6555 for direct output common mode control. In some cases, the output drive capability of the ADC V_{CMO} output may need an external buffer, as shown, to increase its current capability in order to drive the V_{CM_REF} pin. The LMH6555 Electrical Characteristics table shows the gain (Gain_V_{CM_REF}) and the offset (V_{OS_CM}) from the V_{CM_REF} to the device output common mode.

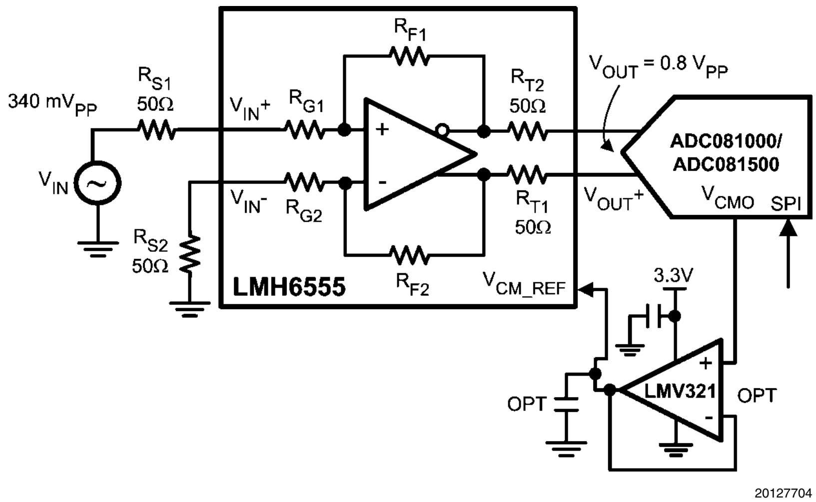


FIGURE 1. Single Ended to Differential Conversion

The single ended input and output impedances of the LMH6555 I/O pins are close to 50Ω as specified in the Electrical Characteristics table (R_{IN} and R_O). With differential input drive, the differential input impedance (R_{IN_DIFF}) is close to 78Ω.

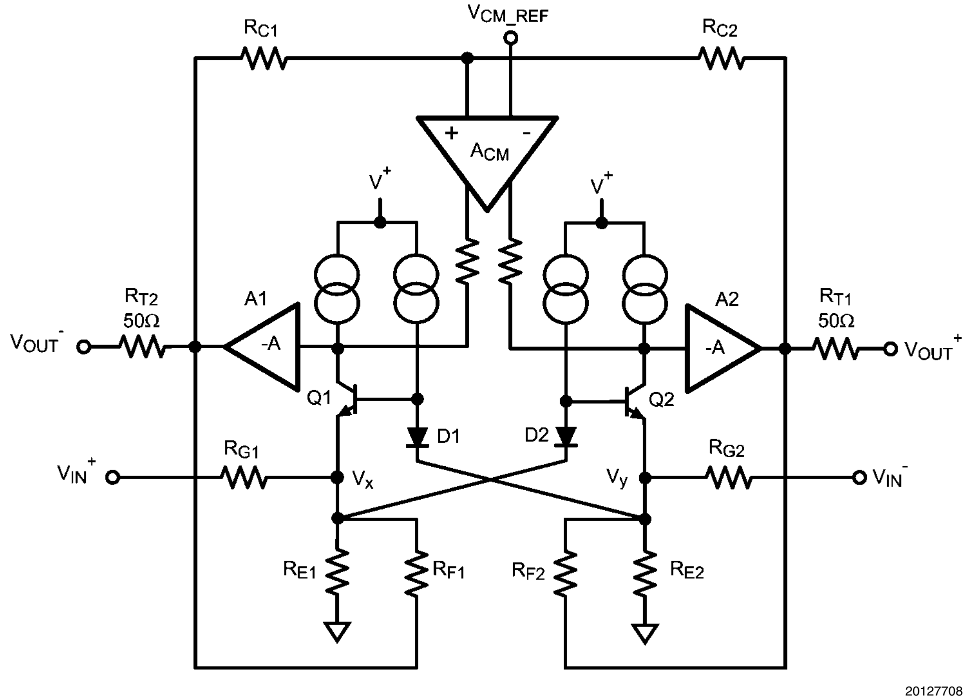
The device nominal input common mode voltage (V_{I_CM}) is close to 0.3V when R_{S1} and R_{S2} of *Figure 1* are open. Thus, the input source will experience a DC current with 0V input. Because of this, the differential output offset voltage is influenced by the matching between R_{S1} and R_{S2}. So, in a single ended input condition, if the signal source is AC coupled to one input, the undriven input needs to also be AC coupled in order to cancel the output offset voltage (V_{OOS}).

In applications where low output offset is required, it is possible to inject some current to the appropriate input (V_{IN+} or V_{IN-}) as an effective method of trimming the output offset voltage of the LMH6555. This is explained later in this document. The nominal value of R_{S1} and R_{S2} will also affect the insertion gain (A_{V_DIFF}). The LMH6555 can also be used with the input AC coupled through equal valued DC blocking capacitors (C) in series with V_{IN+} and V_{IN-}. In this case, the coupling capacitors need to be large enough to not block the low frequency content. The lower cutoff frequency will be $1/(\pi R_{EQ}C)$Hz with $R_{EQ} = R_{S1} + R_{S2} + R_{IN\_DIFF}$ where $R_{IN\_DIFF} \approx 78\Omega$.

The single ended output impedance of the LMH6555 is 50Ω. The LMH6555 Electrical Characteristics shows the device performance with 100Ω differential output load, as would be the case if a device such as the ADC081000/ ADC081500 (single/ dual ADC) were being driven.

CIRCUIT ANALYSIS

Figure 2 shows the block diagram of the LMH6555.



$R_{G1} = R_{G2} = R_G = 39\Omega$
$R_{E1} = R_{E2} = R_E = 25\Omega$
$R_{F1} = R_{F2} = R_F = 430\Omega$
$I_{CQ1} = I_{CQ2} = 12.6$ mA

FIGURE 2. Block Diagram

The differential input stage consists of cross-coupled common base bipolar NPN stages, Q1 and Q2. These stages give the device its differential input characteristic. The internal loop gain from V_x and V_y internal nodes (Q1 and Q2 emitters) to the output is large, such that these nodes act as a virtual ground. The cross-coupling will ensure that these nodes are at the same voltage as long as the amplifier is operating within its normal range. Output common mode voltage is enforced through the action of "A_{CM}" which servos the output common mode to the "V_{CM_REF}" input voltage.

The discussion that follows, provides the formulas needed to analyze single ended and differential input applications. For a more detailed explanation including derivations, please see the Appendix at the end of the datasheet.

SINGLE-ENDED INPUT

The following is the procedure for determining the device operating conditions for single ended input applications. This example will use the schematic shown in *Figure 3*.

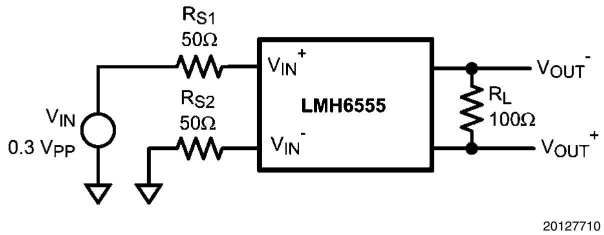


FIGURE 3. Single-Ended Input Drive

1. Determine the driven input's (V_{IN}+ or V_{IN}–) swing knowing that each input common mode impedance to ground (R_{IN}) is 50Ω:

   $$\mathbf{V_{IN}+ \text{ (or } V_{IN}-) = V_{IN} \cdot R_{IN}/(R_{IN} + R_S)}$$

   For *Figure 3*

   $V_{IN}+ = 0.3\ V_{PP} \cdot 50/(50+50) = 0.15\ V_{PP}$

2. Calculate V_{OUT} knowing the Insertion Gain (A_{V_DIFF}):

   $$\mathbf{V_{OUT} = (V_{IN}/2) \cdot A_{V\_DIFF}}$$

   $$\mathbf{A_{V\_DIFF} = 2 \cdot R_F/ (2R_S + R_{IN\_DIFF})}$$

   where $R_F = 430\Omega$ & $R_{IN\_DIFF} = 78\Omega$

   For *Figure 3*

   $R_S = 50\Omega \rightarrow A_{V\_DIFF} = 4.83$ V/V

   $V_{OUT} = (0.3\ V_{PP}/2) \cdot 4.83\ \text{V/V} = 724.5\ mV_{PP}$

3. Determine the peak-to-peak differential current (I_{IN_DIFF}) through the device's differential input impedance (R_{IN_DIFF}) which would result in the V_{OUT} calculated in step 2:

   $$\mathbf{I_{IN\_DIFF} = V_{OUT}/ R_F}$$

   For *Figure 3*

   $I_{IN\_DIFF} = 724.5\ mV_{PP}/ 430\Omega = 1.685\ mA_{PP}$

4. Determine the swing across the input terminals (V_{IN_DIFF}) which would give rise to the I_{IN_DIFF} calculated in step 3 above.

   $$\mathbf{V_{IN\_DIFF} = I_{IN\_DIFF} \cdot R_{IN\_DIFF}}$$

   For *Figure 3*

   $V_{IN\_DIFF} = 1.685\ mA_{PP} \cdot 78\Omega = 131.4\ mV_{PP}$

5. Calculate the undriven input's swing, based on V_{IN_DIFF} determined in step 4 and V_{IN}+ calculated in step 1:

   $$\mathbf{V_{IN}- = V_{IN}+ - V_{IN\_DIFF}}$$

   For *Figure 3*

   $V_{IN}- = 150\ mV_{PP} - 131.4\ mV_{PP} = 18.6\ mV_{PP}$

6. Determine the DC average of the two inputs (V_{I_CM}) by using the following expression:

   $$\mathbf{V_{I\_CM} = 12.6\ mA \cdot R_E \cdot R_S / (R_S + R_G + R_E)}$$

   where $R_E = 25\Omega$ & $R_G = 39\Omega$ (both internal to the LMH6555)

   For *Figure 3*

   $$\mathbf{R_S = 50\Omega \rightarrow V_{I\_CM} = 15.75 / (R_S + 64)}$$

   $V_{I\_CM} = 15.75/ (50+64) = 138.2$ mV

The values determined with the procedure outlined here are shown in *Figure 4*.

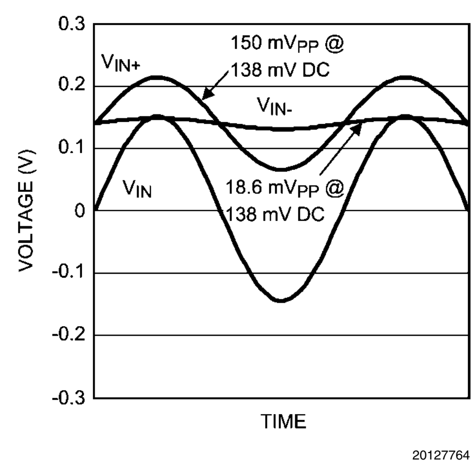
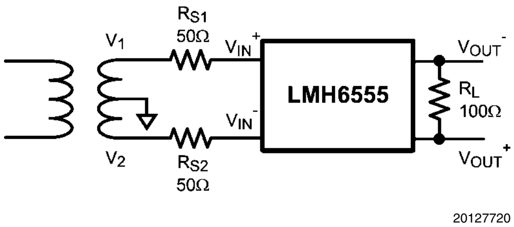


FIGURE 4. Input Voltage for *Figure 3* Schematic

DIFFERENTIAL INPUT

The following is the procedure for determining the device operating conditions for differential input applications using the *Figure 5* schematic as an example.



Assuming transformer secondary, V_{IN}, of 300 mV_{PP}

FIGURE 5. Differential Input Drive

1. Calculate the swing across the input terminals (V_{IN_DIFF}) by considering the voltage division from the differential source (V_{IN}) to the LMH6555 input terminals with differential input impedance R_{IN_DIFF}:

   $$\mathbf{V_{IN\_DIFF} = V_{IN} \cdot R_{IN\_DIFF} / (2R_S + R_{IN\_DIFF})}$$

   For *Figure 5*

   V_{IN_DIFF} = 300 mV_{PP} · 78 / (100 + 78) = 131.5 mV_{PP}

2. Calculate each input pin swing to be ½ the swing determined in step 1:

   $$\mathbf{V_{IN}+ = V_{IN}- = V_{IN\_DIFF} / 2}$$

   For *Figure 5*

   $V_{IN}+ = V_{IN}-$ = 131.5 mV_{PP}/ 2 = 65.7 mV_{PP}

3. Determine the DC average of the two inputs (V_{I_CM}) by using the following expression:

   $$\mathbf{V_{I\_CM} = 12.6\ mA \cdot R_E \cdot R_S / (R_S + R_G + R_E)}$$

   where R_E = 25Ω & R_G = 39Ω (both internal to the LMH6555)

   For *Figure 5*

   $$\mathbf{R_S = 50\Omega \rightarrow V_{I\_CM} = 15.75 / (R_S + 64)}$$

   V_{I_CM} = 15.75/ (50+64) = 138.2 mV

4. Calculate V_{OUT} knowing the Insertion Gain (A_{V_DIFF}):

   $$\mathbf{V_{OUT} = (V_{IN} \cdot / 2) \cdot A_{V\_DIFF}}$$

   $$\mathbf{A_{V\_DIFF} = 2 \cdot R_F / (2R_S + R_{IN\_DIFF})}$$

   where R_F= 430Ω & R_{IN_DIFF} = 78Ω

   For *Figure 5*

   $R_S = 50\Omega \rightarrow A_{V\_DIFF}$ = 4.83 V/V

   V_{OUT} = (0.3 V_{PP}/2) · 4.83 V/V= 724.5 mV_{PP}

The values determined with the procedure outlined here are shown in *Figure 6*.

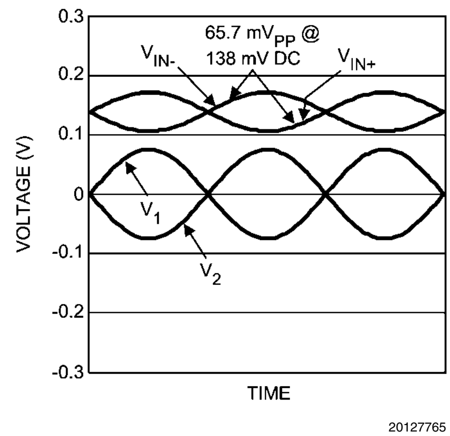


FIGURE 6. Input Voltage for *Figure 5* Schematic

SOURCE IMPEDANCE(S) AND THEIR EFFECT ON GAIN AND OFFSET

The source impedances R_{S1} and R_{S2}, as shown in *Figure 3* or *Figure 5*, affect gain and output offset. The datasheet tables and typical performance graphs are generated with equal valued source impedances R_{S1} and R_{S2}, unless otherwise specified. Any mismatch between the values of these two impedances would alter the gain and offset voltage.

OUTPUT OFFSET CONTROL AND ADJUSTMENT

There are applications which require that the LMH6555 differential output voltage be set by the user. An example of such an application is a unipolar signal which is converted to a differential output by the LMH6555. In order to utilize the full scale range of the ADC input, it is beneficial to shift the LMH6555 outputs to the limits of the ADC analog input range under minimal signal condition. That is, one LMH6555 output is shifted close to the negative limit of the ADC analog input and the other close to the positive limit of the ADC analog input. Then, under maximum signal condition, with proper gain, the full scale range of the ADC input can be traversed and the ADC input dynamic range is properly utilized. If this forced offset were not imposed, the ADC output codes would be reduced to half of what the ADC is capable of producing, resulting in a significant reduction in ENOB. The choice of the direction of this shift is determined by the polarity of the expected signal.

Another scenario where it may be necessary to shift the LMH6555 output offset voltage is in applications where it is necessary to improve the specified Output Offset Voltage (differential mode), "V_{OOS}". Some ADC's, including the ADC081000/ ADC081500 (and their dual counterparts), have internal registers to correct for the driver's (LMH6555) V_{OOS}. If the LMH6555 V_{OOS} rating exceeds the maximum value allowed into this register, then shifting the output is required for maximum ADC performance.

It is possible to affect output offset voltage by manipulating the value of one input resistance relative to the other (e.g. R_{S1} relative to R_{S2} or vice versa). However, this will also alter the gain. Assuming that the source is applied to the V_{IN+} side through R_{S1}, *Figure 7(A)* shows the effect of varying R_{S1} on the overall gain and output offset voltage. *Figure 7(B)* shows the same effects but this time for when the undriven side impedance, R_{S2}, is varied.

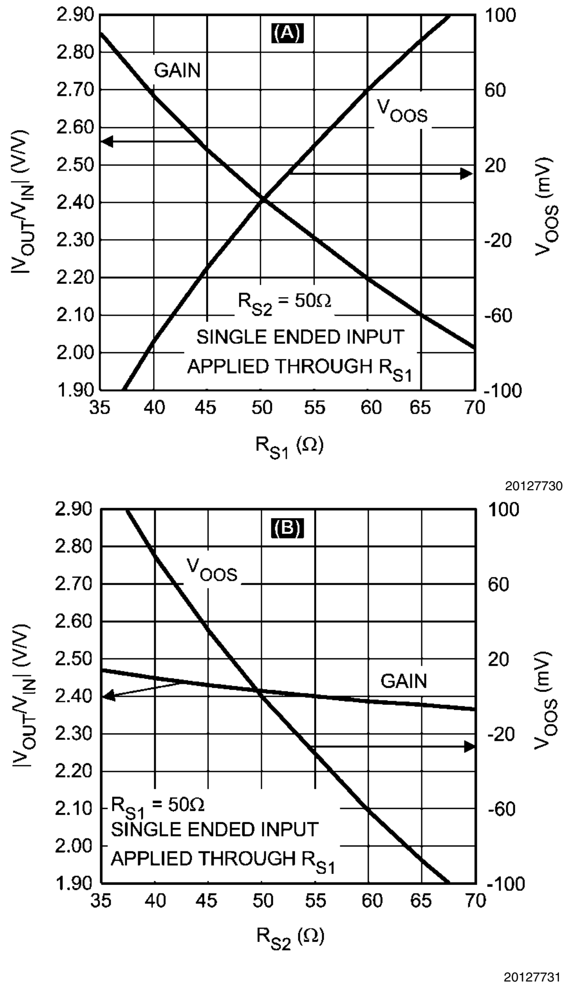


FIGURE 7. Gain & Output Offset Voltage vs. Source Impedance Shift for Single Ended Input Drive

As can be seen in *Figure 7*, the source impedance of the input side being driven has a bigger effect on gain than the undriven source impedance. R_{S1} and R_{S2} affect the output offset in opposite directions. Manipulating the value of R_{S2} for offset control has another advantage over doing the same to R_{S1} and that is the signal input termination is not affected by it. This is especially important in applications where the signal is applied to the LMH6555 through a transmission line which needs to be terminated in its characteristic impedance for minimum reflection.

For reference, *Figure 8* shows the effect of source impedance misbalance on overall gain and output offset voltage with differential input drive.

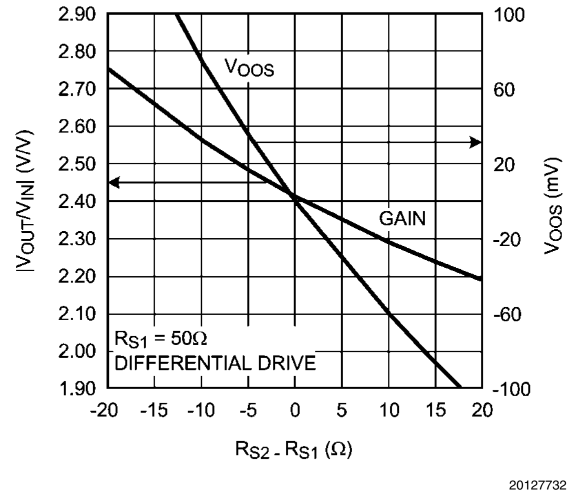


FIGURE 8. Gain & Output Offset Voltage vs. Source Impedance Shift for Differential Input Drive

It is possible to manipulate output offset with little or no effect on source resistance balance, gain, and, cable termination.

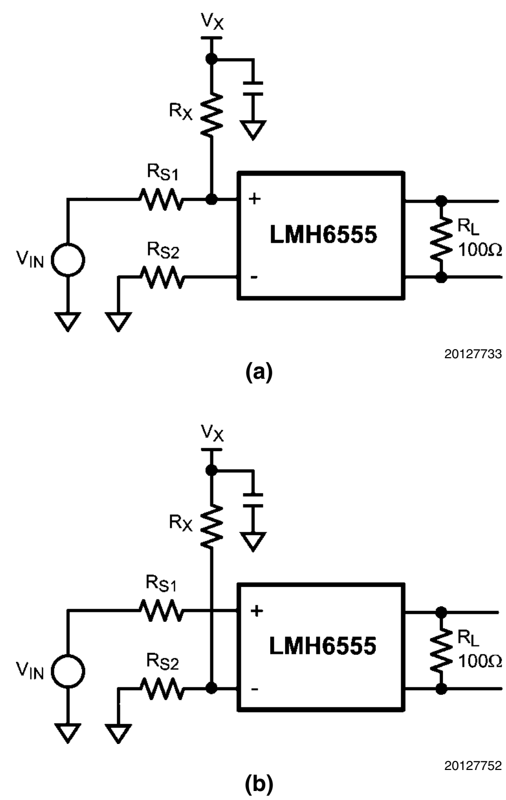


FIGURE 9. Differential Output Shift Circuits

R_X, shown in *Figure 9(a)* and *Figure 9(b)*, injects current into the input to achieve the required output shift. For a positive shift, positive current would need to be injected into the V_{IN+} terminal (*Figure 9(a)*) and for a negative shift, to the V_{IN-} terminal (*Figure 9(b)*). *Figure 10* shows the effect of R_X on the output with V_X = 3.3V or 5V, and $R_{S1} = R_{S2}$ = 50Ω.

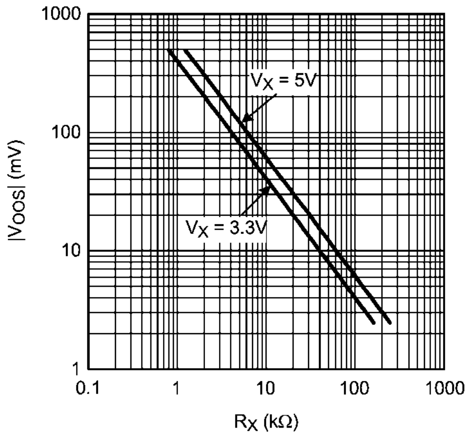


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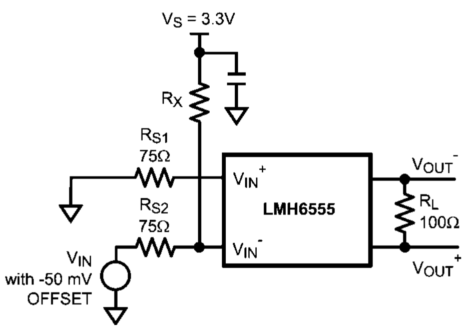
FIGURE 10. LMH6555 Differential Output Shift Due to R_X in *Figure 9*

To shift the LMH6555 differential output negative by about 100 mV, referring to the plot in *Figure 10*, R_X would be chosen to be around 3.9 kΩ in the schematic of *Figure 9(b)* (using $V_X = V_S = 3.3V$).

In applications where V_{IN} has a built-in non-zero offset voltage, or when R_{S1} and R_{S2} are not 50Ω, the *Figure 10* plot cannot be used to estimate the required value for R_X.

Consider the case of a more general offset correction application, shown in *Figure 11(a)*, where $R_{S1} = R_{S2} = 75\Omega$ and V_{IN} has a built-in offset of −50 mV. It is necessary to shift the differential output offset voltage of the LMH6555 to 0 mV. *Figure 11(b)* is the Thevenin equivalent of the circuit in *Figure 11(a)* assuming $R_X >> R_{S2}$.



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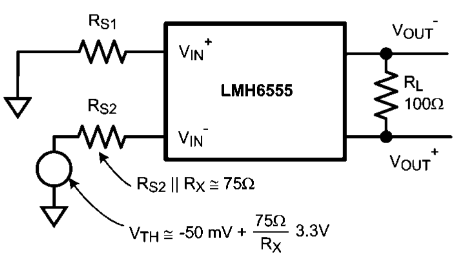
(a)



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(b)

FIGURE 11. Offset Correction Example ($R_S = 75\Omega$)

From the gain expression in *Equation 4* (see Appendix) (but with opposite polarity because V_{TH} is applied to V_{IN-} instead):

$$\frac{V_{OUT}}{V_{TH}} = \frac{-R_F}{2R_S + 78} \Rightarrow$$

$$V_{OUT} = \frac{-430\Omega}{(150 + 78)\Omega} \times \left(-50\text{ mV} + \frac{75}{R_X} 3.3V\right) \quad (1)$$

The expression derived for V_{OUT} in *Equation 1* can be set equal to zero to solve for R_X resulting in $R_X = 4.95$ kΩ. If the differential output offset voltage, V_{OOS}, is also known, V_{OUT} could be set to a value equal to $-V_{OOS}$. For example, if the V_{OOS} for the particular LMH6555 is +30 mV, then the following nulls the differential output:

$$V_{OUT} = -30\text{ mV} = (-1.89)\left(-50\text{ mV} + \frac{248}{R_X}\right)$$

$$\Rightarrow R_X = 3.76\text{ k}\Omega \quad (2)$$

$R_X >> R_{S2}$ confirming the assumption made in the derivation. Note that *Equation 2*, which is derived based on the configuration in *Figure 9(b)*, will yield a real solution for R_X if and only if:

$$V_{OOS} \geq (V_{IN\_OFFSET} \times 1.89)$$
(for *Figure 11(b)* and with $R_S = 75\Omega$) (3)

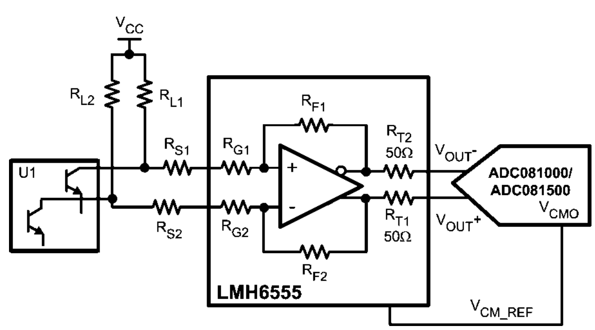
where V_{IN_OFFSET} is the source offset shown as −50 mV in *Figure 11(a)*.

If *Equation 3* were not satisfied, then *Figure 9(a)* offset correction, where R_X is tied to the V_{IN+} side, should be employed instead.

Alternatively, replace the V_X and R_X combination with a discrete current source or current sink. Because of a current source's high output impedance, there will be less gain imbalance. However, a current source might have a relatively large output capacitance which could degrade high frequency performance.

INTERFACE DESIGN EXAMPLE

As shown in *Figure 12* below, the LMH6555 can be used to interface an open collector output device (U1) to a high speed ADC. In this application, the LMH6555 performs the task of amplifying and driving the 100Ω differential input impedance of the ADC.



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V_{CM_REF} buffer not shown

FIGURE 12. Differential Amplification and ADC Drive

For applications similar to the one shown in *Figure 12*, the following conditions should be maintained:

1. The LMH6555 differential output voltage has to comply with the ADC full scale voltage (800 mV_{PP} in this case).
2. The LMH6555 input Common Mode Voltage Range is observed. "CMVR", as specified in the Electrical Characteristics table, is to be between –0.3V and 2.0V for the specified CMRR.
3. U1 collector voltage swing must to be observed so that the U1 output transistors do not saturate. The expected operating range of these output transistors is defined by the specifications and operating conditions of U1.

Consider a numerical example (R_L refers to R_{L1} & R_{L2}, R_S refers to R_{S1} & R_{S2}).

Assume:

V_{CC} = 10V, U1 peak-to-peak collector current (I_{PP}) = 15 mA_{PP} with 10 mA quiescent (I_{cQ}), and minimum operational U1 collector voltage = 6V.

Here are the series of steps to take in order to carry out this design:

a. Select the R_L value which allows compliance with the U1 collector voltage (6V in this case) with 1V extra as margin because of LMH6555 loading.

R_L = [10 - (6+1)] V / (10+ 7.5) mA = 171Ω

Choose 169Ω, 1% resistors for R_L

b. Find the value of R_S to get the proper swing at the output (800 mV_{PP}). To do so, convert the input stage into its Norton equivalent as shown in *Figure 13*.

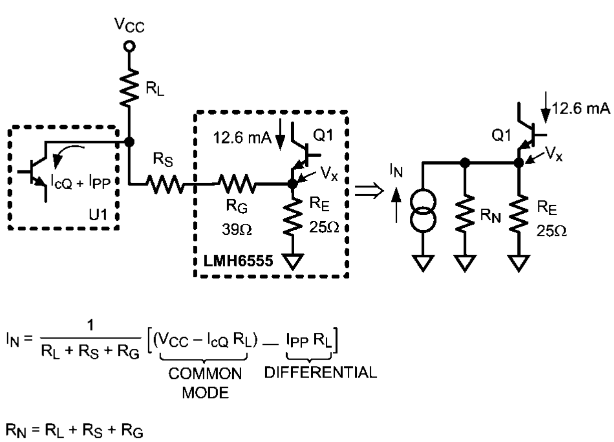

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FIGURE 13. Norton Equivalent of the Input Circuitry Tied to Q1 within the LMH6555 in *Figure 12*

I_N = I_N (common mode) + I_N (differential)

I_N (common mode) = (V_{CC} – I_{cQ} * R_L) / (R_L + R_S + R_G)

I_N (differential) = I_{PP} * R_L / (R_L + R_S + R_G)

The entirety of the Norton source differential component will flow through the feedback resistors within the LMH6555 and generate an output. Therefore:

I_N (differential) * R_F = 800 mV_{PP}

→ R_S = (R_L* I_{PP} * R_F/ 0.8) – R_G – R_L where R_F = 430Ω, R_G = 39Ω (R_F and R_G are internal LMH6555 resistances).

So, in this case:

R_S = (169 * 15 mA_{PP} * 430/ 0.8) – 39 – 169 = 1154Ω

Choose 1.15 kΩ, 1% resistors for R_S.

c. With R_L and R_S defined, ensure that the U1 collector voltage(s) minimum is not violated due to the loading effect of the LMH6555 through R_S. Also, it is important to ensure that the LMH6555's CMVR is also not violated.

The "V_x" node voltage within the LMH6555 (see *Figure 13*) would need to be calculated. Use the Common Mode component of the Norton equivalent source from above, and write the KCL at the V_x node as follows:

V_x / R_E + V_x / R_N = 12.6 mA + I_N (common mode); with R_E = 25Ω.

V_x / R_E + V_x / R_N = 12.6 mA + (V_{CC} – I_{cQ} R_L)/ (R_L + R_S + R_G)

→V_x = 0.4595V

With V_x calculated, both the input voltage range (high and low) and the low end of the U1 collector voltage (V_C) can be derived to be within the acceptable range. If necessary, steps "a" through "c" would have to be repeated to readjust these values.

V_C = V_X R_L / R_N + I_N (R_S + R_G)

I_N_High = 7.05 mA, I_N_Low = 5.19 mA (based on the values derived)

→V_C_High = 0.4595 * 169 / 1358 + 7.05 mA (1150 + 39) = 8.44V

→V_C_Low = 0.4595 * 169 / 1358 + 5.19 mA (1150 + 39) = 6.22V

V_{IN} = V_X (R_N – R_G) / R_N + I_N R_G

→V_{IN}_High = 0.4595 * (1358- 39) / 1358 + 7.05 mA * 39 = 0.721V

→V_{IN}_Low = 0.4595 * (1358- 39) / 1358 + 5.19 mA * 39 = 0.649V

Figure 14 shows the complete solution using the values derived above, with the node voltages marked on the schematic for reference.

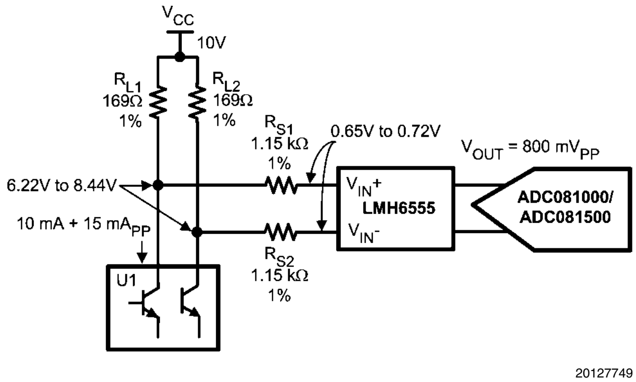


FIGURE 14. Implementation #1 of *Figure 12* Design Example

It is important to note that the matching of the resistors on either input side of the LMH6555 (R_{S1} to R_{S2} and R_{L1} to R_{L2}) is very important for output offset voltage and gain balance. This is particularly true with values of R_S higher than the nominal 50Ω. Therefore, in this example, 1% or better resistor values are specified.

If the U1 collector voltage turns out to be too low due to the loading of the LMH6555, lower R_L. Lower values of R_L result in lower R_S which in turn increases the LMH6555's V_{I_CM} because of increased pull up action towards V_{CC}. The upper limit on V_{I_CM} is 2V. *Figure 15* shows the 2nd implementation of this same application with lowered values of R_L and R_S. Notice that the lower end of U1's collector voltage and the upper end of LMH6555's V_{I_CM} have both increased compared to the 1st implementation.

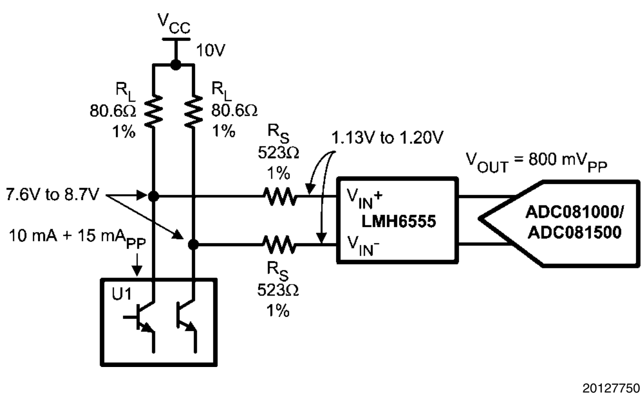


FIGURE 15. Implementation #2 of *Figure 12* Design Example

An alternative would be to AC couple the LMH6555 inputs. With this approach, the design steps would be very similar to the ones outlined except that there would be no common mode interaction between the LMH6555 and U1 and this results in fewer design constraints:

$V_x / R_E = 12.6\text{ mA} \rightarrow V_x = 0.3150\text{V}$

For the component values shown in *Figure 15* use:

$V_{C\_}High = V_{CC} – R_L (I_{cQ} + I_{PP} / 2 - I_N \text{ (differential) } /2)$

$V_{C\_}Low = V_{CC} – R_L (I_{cQ} - I_{PP} / 2 + I_N \text{ (differential) } /2)$

I_N (differential) = $I_{PP} * R_L / (R_L + R_S + R_G)$ = 1.88 mA (based on the values used.)

$\rightarrow V_{C\_}High = 10 – 80.6 (10 + 15 / 2 – 1.88 /2) \text{ mA} = 8.67\text{V}$

$\rightarrow V_{C\_}Low = 10 – 80.6 (10 – 15 / 2 + 1.88 /2) \text{ mA} = 9.72\text{V}$

$V_{IN} = V_X \pm R_G \cdot I_N \text{ (differential) } /2$

$\rightarrow V_{IN\_}High = 0.3150 + 39 * 1.88 \text{ mA} /2 = 0.3517\text{V}$

$\rightarrow V_{IN\_}Low = 0.3150 - 39 * 1.88 \text{ mA} /2 = 0.2783\text{V}$

Figure 16 shows the AC coupled implementation of the *Figure 15* schematic along with the node voltages marked to demonstrate the reduced V_{I_CM} of the LMH6555 and the increase in the U1 collector voltage minimum.

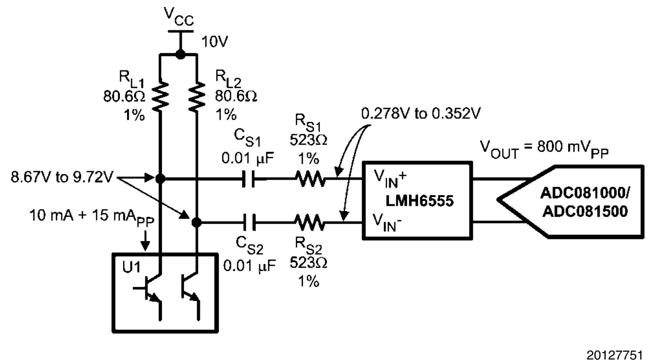


FIGURE 16. AC Coupled Version of *Figure 15*

Note that the lower cut-off frequency is:

f_cut-off = 1 / ($\pi ReqC_S$) where Req = R_{S1}+ R_{S2} + R_{IN_DIFF} where $R_{IN\_DIFF} \approx 78\Omega$

So, for the component values shown (C_S = 0.01 µF and R_{S1} = R_{S2} = 523Ω):

f_cut-off = 28.2 kHz

DATA ACQUISITION APPLICATIONS

Figure 17 shows the LMH6555 used as the differential driver to the National Semiconductor ADC081500 running at 1.5G samples/second.

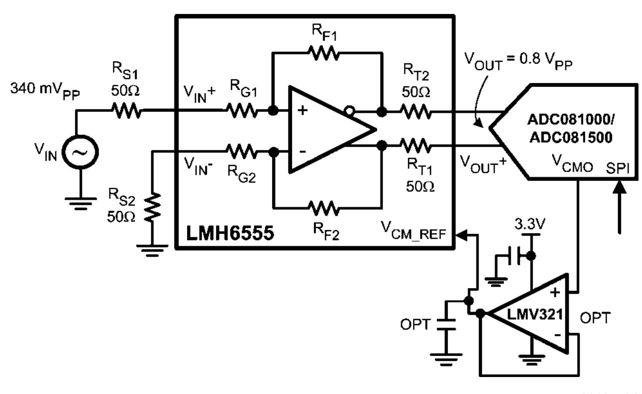


FIGURE 17. Schematic of the LMH6555 Interfaced to the ADC081500

In the schematic of *Figure 17*, the LMH6555 converts a single ended input into a differential output for direct interface to the ADC's 100Ω differential input. An alternative approach to using the LMH6555 for this purpose, would have been to use a balun transformer, as shown in *Figure 18*.

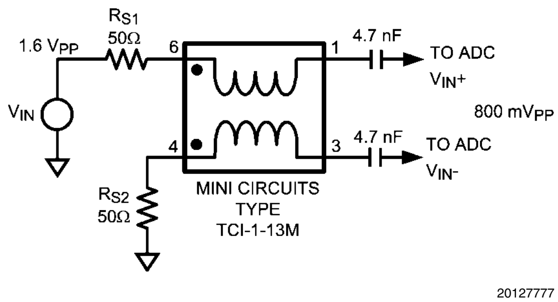


FIGURE 18. Single Ended to Differential Conversion (AC only) with a Balun Transformer

In the circuit of *Figure 18*, the ADC will see a 100Ω differential driver which will swing the required 800 mV_{PP} when V_{IN} is 1.6 V_{PP}. The source (V_{IN}) will see an overall impedance of 200Ω for the frequency range that the transformer is specified to operate. Note that with this scheme, the signal to the ADC must be AC coupled, because of the transformer's minimum operating frequency which would prevent DC coupling. For the transformer specified, the lower operating frequency is around 4.5 MHz and the input high pass filter's −3 dB bandwidth is around 340 kHz for the values shown (or $(1/\pi R_{EQ}C)$ Hz where R_{EQ} = 200Ω).

Table 1 compares the LMH6555 solution (*Figure 17*) vs. that of the balun transformer coupling (*Figure 18*) for various categories.

TABLE 1. ADC Input Coupling Schemes Compared

Category	Preferred Solution	
	LMH6555	Balun Transformer
Lower Power Consumption		✓
Lower Distortion		✓
Wider Dynamic Range	✓	
DC Coupling & Broadband Applications	✓	
Highest Gain & Phase Balance	✓	
Input/ Output Broadband Impedance Matching (Highest Return Loss)	✓	
Additional Gain	✓	
ADC Input Protection against Overdrive	✓	
Highest SNR	✓	
Ability to Control Gain Flatness	✓ (see below)	

GAIN FLATNESS

In applications where the full 1.2 GHz bandwidth of the LMH6555 is not necessary, it is possible to improve the gain flatness frequency at the expense of bandwidth. *Figure 19* shows C_O placed across the LMH6555 output terminals to reduce the frequency response gain peaking and thereby to increase the ±0.5 dB gain flatness frequency.

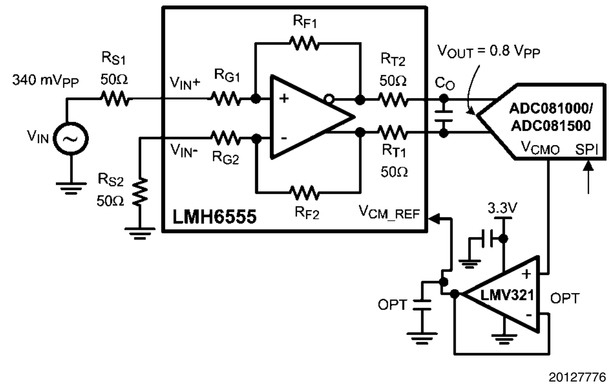


FIGURE 19. Increasing ±0.5 dB Gain Flatness using External Output Capacitance, C_O

Figures 20, *21* and *Figure 22* show the FFT analysis results with the setup shown in *Figure 17*.

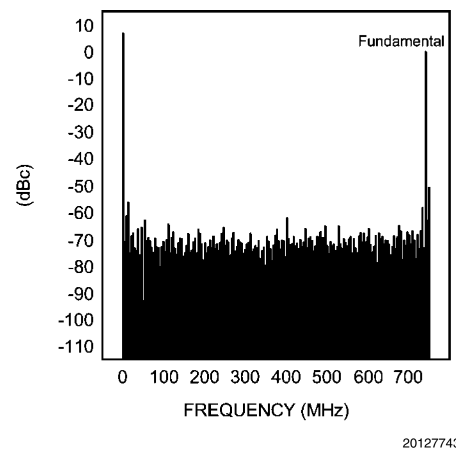


FIGURE 20. LMH6555 FFT Result When Used as the Differential Driver to ADC081500

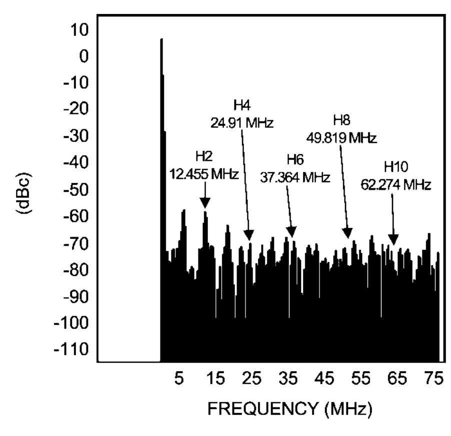


FIGURE 21. LMH6555 FFT Result When Used as the Differential Driver to ADC081500 (Lower Fs/2 Region Magnified)

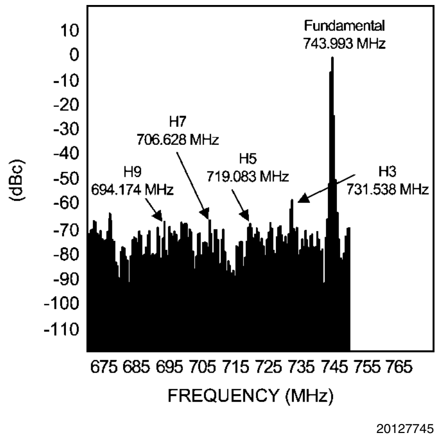


FIGURE 22. LMH6555 FFT Result When Used as the Differential Driver to ADC081500 (Upper Fs/2 Region Magnified)

Figures 20, *21*, and *Figure 22* information summary:

• Fundamental Test Frequency	744 MHz
• LMH6555 Output	0.8 V_{PP}
• Sampling Rate:	1.5G samples/ second
• 2nd Harmonic	–59 dBc @ ~ 12 MHz or l1.5 GHz*1– 744 MHz*2l
• 3rd Harmonic	–57 dBc @ ~ 732 MHz or l1.5 GHz*1- 744 MHz *3l
• 4th Harmonic	–71 dBc @ ~ 24 MHz or l1.5 GHz*2 – 744 MHz *4l
• 5th Harmonic	–68 dBc @ ~ 720 MHz or l1.5 GHz*2- 744 MHz*5l
• 6th Harmonic	–68 dBc @ ~ 36 MHz or l1.5 GHz*3- 744 MHz*6l
• THD	–51.8 dBc
• SNR	43.4 dB
• Spurious Free Dynamic Range (SFDR):	57 dB
• SINAD	42.8 dB
• ENOB	6.8 bits

The LMH6555 is capable of driving a variety of National Semiconductor Analog to Digital Converters. This is shown in *Table 2*, which offers a complete list of possible signal path ADC+ Amplifier combinations. The use of the LMH6555 to drive an ADC is determined by the application and the desired sampling process (Nyquist operation, sub-sampling or over-sampling). See application note (AN-236) for more details on the sampling processes and application note (AN-1393) for details on “Using High Speed Differential Amplifiers to Drive ADCs”. For more information regarding a particular ADC, refer to the particular ADC datasheet for details.

TABLE 2. Differential Input ADC’s Compatible with the LMH6555 Driver

ADC Part Number	Resolution (bits)	Single/ Dual	Speed (MSPS)
ADC08D500	8	S	500
ADC081000	8	S	1000
ADC08D1000	8	D	1000
ADC08D1020	8	D	1000
ADC081500	8	S	1500
ADC08D1500	8	D	1500
ADC08D1520	8	D	1500
ADC083000	8	S	3000
ADC08B3000	8	S	3000

EXPOSED PAD LLP PACKAGE

The LMH6555 is in a thermally enhanced package. The exposed pad (device bottom) is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. The thermal dissipation of the device is largely dependent on the connection of this pad. The exposed pad should be attached to as much copper on the circuit board as possible, preferably external copper. However, it is very important to maintain good high speed layout practices when designing a system board.

Here is a link to more information on the National 16-pin LLP package:

http://www.national.com/packaging/folders/sqa16a.html

EVALUATION BOARD

National Semiconductor suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization.

Device	Package	Evaluation Board Ordering ID
LMH6555	16-Pin LLP	LMH6555EVAL

The evaluation board can be ordered when a device sample request is placed with National Semiconductor.

Appendix

Here is a more detailed analysis of the LMH6555, including the derivation of the expressions used throughout the Application Information.

INPUT STAGE

Because of the input stage cross-coupling, if the instantaneous values of the input node voltages (V_{IN+} and V_{IN-}) and current values are required, use the circuit of *Figure 23* as the equivalent input stage for each input (V_{IN+} and V_{IN-}).

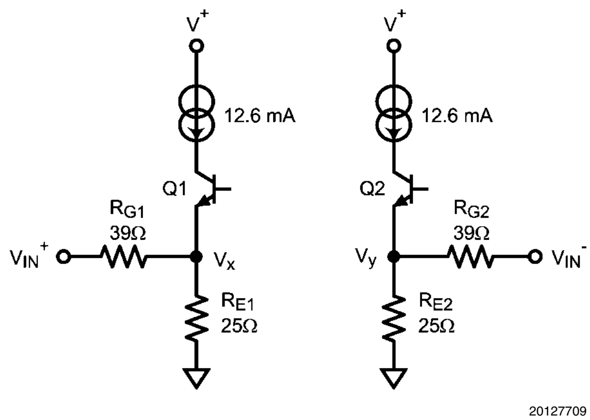


FIGURE 23. Equivalent Input Stage

Using this simplified circuit, one can assume a constant collector current, to simplify the analysis. This is a valid approximation as the large open loop gain of the device will keep the two collector currents relatively constant. First derive Q1 and Q2 emitter voltages. From there, derive the voltages at V_{IN+} and V_{IN-}.

With the component values shown, it is possible to analyze the input circuits of *Figure 23* in order to determine Q1 and Q2 emitter voltages. This will result in a first order estimate of Q1 and Q2 emitter voltages. Since Q1 and Q2 emitters are cross-coupled, the voltages derived would have to be equal. With the action of the common mode amplifier, "A_{CM}", shown in *Figure 2*, these two emitters will be equalized. So, one other iteration can be performed whereby both emitters are set to be equal to the average of the 1st derived emitter voltages. Using this new emitter voltage, one could recalculate V_{IN+} and V_{IN-} voltages. The values derived in this fashion will be within ±10% of the measured values.

Single Ended Input Analysis

Here is an actual example to further clarify the procedure.

Consider the case where the LMH6555 is used as a single ended to differential converter shown in *Figure 24*.

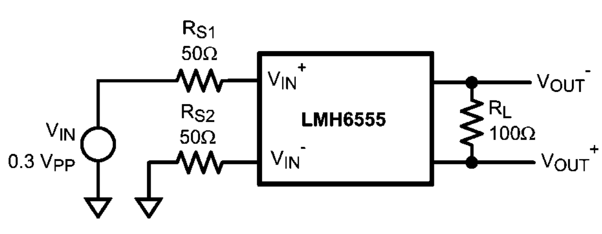


FIGURE 24. Single Ended Input Drive

The first task would be to derive the internal transistor emitter voltages based on the schematic of *Figure 23* (assuming that there is no interaction between the stages.) Here is the derivation of V_X and V_y:

$$\frac{Vx}{25} + \frac{Vx \mp 0.15}{89} = 12.6\text{ mA} \Rightarrow Vx = \begin{cases} 0.279V \\ 0.213V \end{cases}$$

$$\frac{Vy}{25} + \frac{Vy}{89} = 12.6\text{ mA} \Rightarrow Vy = 0.246V$$

V_X varies with V_{IN+} (0.213V with negative V_{IN} swing and 0.279V with positive.) The values derived above assume that the two halves of the input circuit do not interact with each other. They do through the common mode amplifier and the input stage cross-coupling. V_x and V_y are equal to the average of V_y with either end of the swing of V_X. This is calculated below along with the derivation of V_{IN+} and V_{IN-} based on this new average emitter voltage (the average of V_X and V_y.)

$$\frac{Vx + Vy}{2} = \begin{cases} \dfrac{0.279 + 0.246}{2} = 0.262V \\ \dfrac{0.213 + 0.246}{2} = 0.229V \end{cases} = \text{Emitter Voltage Swing}$$

$$V_{IN}^{+} = \pm 0.15V - 50\,\frac{\pm 0.15V - \begin{cases} 0.262V \\ 0.229V \end{cases}}{89}$$

$$V_{IN}^{+} = \begin{cases} 0.213V \\ 63.2\text{ mV} \end{cases};\quad V_{IN}^{-} = \frac{50}{89} \times \begin{cases} 0.262V \\ 0.229V \end{cases}$$

$$V_{IN}^{-} = \begin{cases} 0.147V \\ 0.129V \end{cases}$$

With 0.3 V_{PP} V_{IN}, V_{IN+} experiences 150 mV_{PP} (213 mV - 63.2 mV) of swing and V_{IN-} will swing by about 18.6 mV_{PP} in the process (147 mV – 129 mV). The input voltages are shown in *Figure 25*.

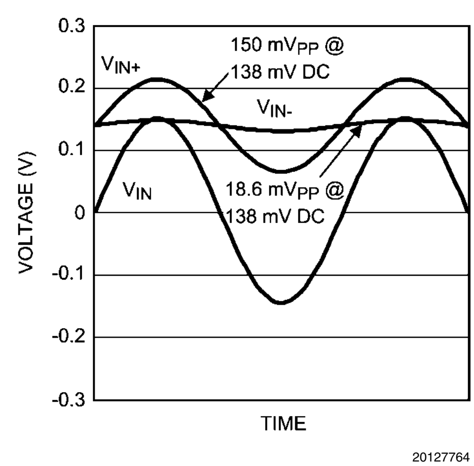


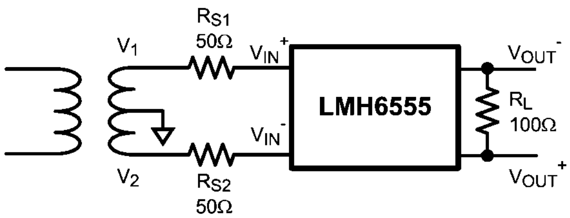
FIGURE 25. Input Voltages for *Figure 24* Schematic

Using the calculated swing on V_{IN+} with known V_{IN}, one can estimate the input impedance, R_{IN} as follows:

$$R_{IN} = \frac{\Delta V_{IN}^{+}}{\Delta I_{IN}^{+}} = \frac{150\ \text{mV}}{(-1.26 + 4.26)\ \text{mA}} = 50\Omega$$

Differential Input Analysis

Assume that the LMH6555 is used as a differential amplifier with a transformer with its Center Tap at ground as shown in *Figure 26*:



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Assuming transformer secondary, V_{IN}, of 300 mV_{PP}

FIGURE 26. Differential Input Drive

The input voltages (V_{IN+} and V_{IN-}) can be derived using the technique explained previously. Assuming no transformer output and referring to the schematic of *Figure 23*:

$$\frac{Vx}{25} + \frac{Vx}{50 + 39} = 12.6\ \text{mA} \Rightarrow Vx = Vy = 0.246\text{V}$$

$$V_{IN}^{+} = \frac{50}{50 + 39} \times 0.246 \Rightarrow V_{IN}^{+} = V_{IN}^{-} = 0.138\text{V}$$

The peak V_{IN+} and V_{IN-} voltages can be determined using the transformer output voltage. Assuming there is 0.3 V_{PP} of signal across the transformer secondary, ½ of that, or 0.15 V_{PP} (±75 mV peak), would appear at each input side (V_1 or V_2 in *Figure 26*). Here is the derivation of the LMH6555 input terminal's peak voltages.

$$\frac{Vx}{25} + \frac{Vx \pm 0.075}{89} = 12.6\ \text{mA} \Rightarrow Vx = \begin{cases} 262.4\ \text{mV} \\ 229.5\ \text{mV} \end{cases}$$

When V_1 swings positive, V_2 will go negative by the same value, and vice versa. Therefore, the values derived above for V_x can be used to determine the average emitter voltage, as described earlier:

$$\frac{Vx + Vy}{2} = \frac{262.4\ \text{mV} + 229.5\ \text{mV}}{2} = 245.9\ \text{mV} = \text{Emitter Voltage}$$

$$V_{IN}^{+} = \pm 75\ \text{mV} - 50\ \frac{\pm 75\ \text{mV} - 245.9\ \text{mV}}{89}$$

$$V_{IN}^{+} = \begin{cases} 171.0\ \text{mV} \\ 105.3\ \text{mV} \end{cases} \text{ and by symmetry: } V_{IN}^{-} = \begin{cases} 105.3\ \text{mV} \\ 171.0\ \text{mV} \end{cases}$$

With the transformer voltage of 0.3 V_{PP}, each input (V_{IN+} and V_{IN-}) swings from 105.3 mV to 171.0 mV or about 65.7 mV_{PP}. The input voltages are shown in *Figure 27*.

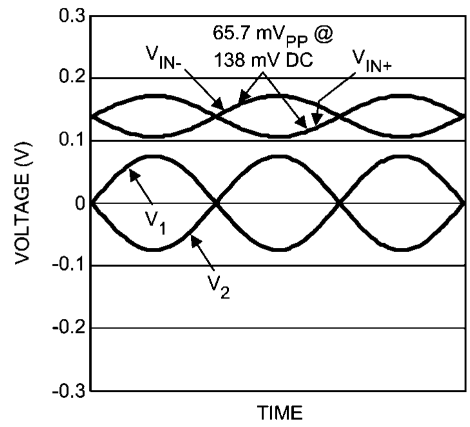

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FIGURE 27. Input Voltages for *Figure 26* Schematic

Knowing the device input terminal voltages, one can estimate the differential input impedance as follows:

$$\frac{R_{IN\_DIFF}}{R_{IN\_DIFF} + 100} = \frac{0.131\ V_{PP}}{0.3\ V_{PP}} \Rightarrow R_{IN\_DIFF} = 78\Omega$$

This is comparable to R_{IN_DIFF} found in the Electrical Characteristic table.

OUTPUT STAGE AND GAIN ANALYSIS

Differential gain is determined by the differential current flow through the feedback resistors R_{F1} and R_{F2} as shown in *Figure 2*. Current through R_{F1} (or R_{F2}) sets the V_{OUT-} (or V_{OUT+}) swing. The nominal value of these resistors is close to 430Ω.

The LMH6555 output stage consists of two bipolar common emitter amplifiers with built in output resistances, R_{T1} and R_{T2}, of 50Ω, as shown in *Figure 28*.

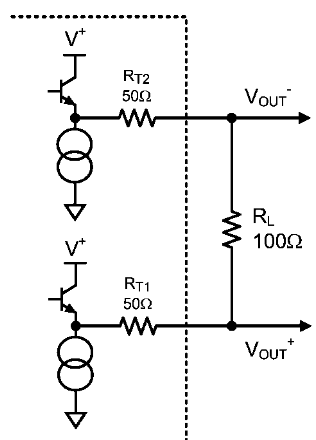

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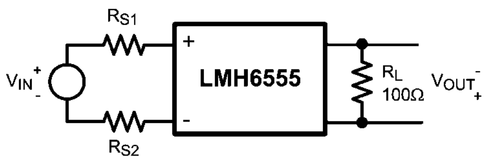
FIGURE 28. Output Stage Including External Load R_L

With an output differential load, R_L, of 100Ω, half the differential swing between the output emitters appears at the LMH6555 output terminals as V_{OUT}.

With good matching between the input source impedances, R_{S1} and R_{S2} shown in *Figure 24* and *Figure 26*, it is possible to infer the gain and output swing by inspection. The differential input impedance of the LMH6555, R_{IN_DIFF}, is close to 78Ω.

In differential input drive applications, there is a balanced swing across the input terminals of the LMH6555, V_{IN+} and V_{IN-}. So, by using the R_{IN_DIFF} value, one determines the differential current flow through the input terminals and from that the output swing and gain.



$$V_{OUT} = \frac{V_{IN} \times R_F}{2R_S + R_{IN\_DIFF}}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F}{2R_S + 78\Omega} = \frac{430\Omega}{2R_S + 78\Omega} \quad (4)$$

For the special case where $R_{S1} = R_{S2} = R_S = 50\Omega$ we have:

$$\text{for } R_S = 50\Omega \Rightarrow \frac{V_{OUT}}{V_{IN}} = \frac{430}{178} = 2.42 \text{ V/V}$$

The following is the expression for the Insertion Gain, A_{V_DIFF}:

$$A_{V\_DIFF} = \frac{V_{OUT}}{V_{IN} \times \frac{100\Omega}{2R_S + 100}}$$

$$= \frac{V_{OUT}/V_{IN}}{100/200} = 2\ V_{OUT}/V_{IN} = 4.83 \text{ V/V}$$

$$= 13.7 \text{ dB}$$

The expressions above apply equally to the single ended input drive case as well, as long as $R_{S1} = R_{S2} = 50\Omega$. For the case of the single ended input drive:

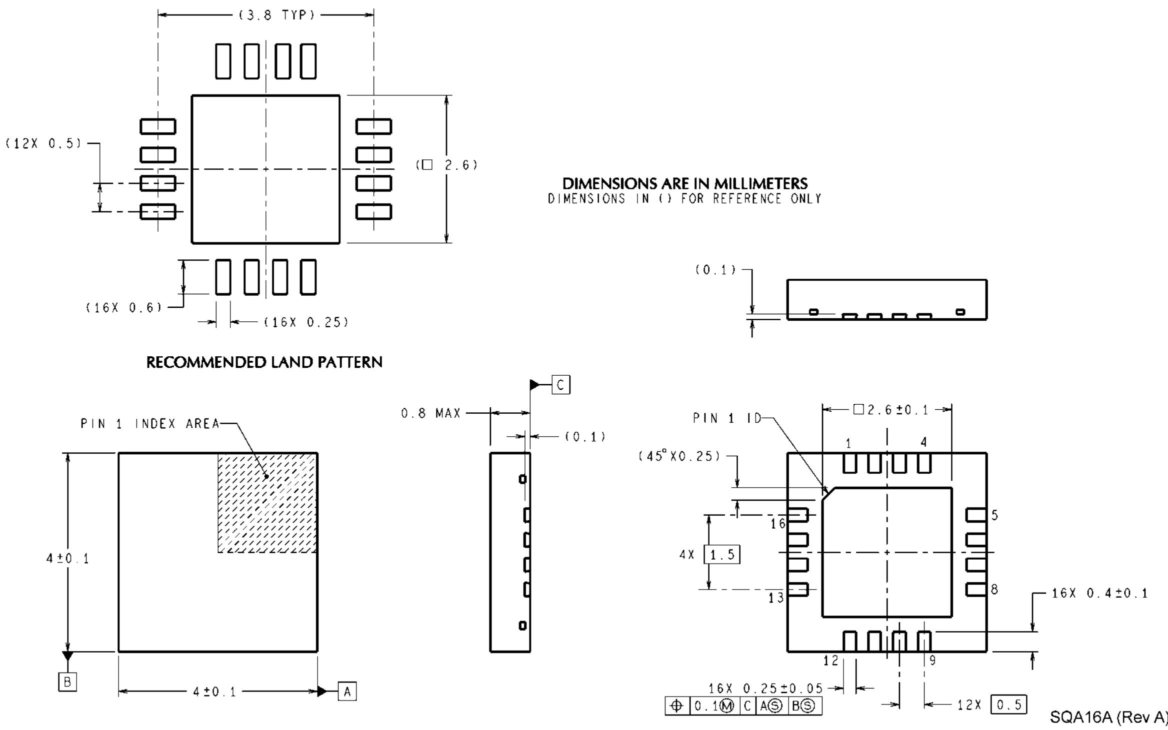
$$A_{V\_DIFF} = \frac{V_{OUT}}{V_{IN} \times \frac{50}{R_S + 50}}$$

$$= \frac{V_{OUT}/V_{IN}}{50/100} = 2\ V_{OUT}/V_{IN} = 4.83 \text{ V/V}$$

$$= 13.7 \text{ dB}$$

This is comparable to A_{V_DIFF} found in the Electrical Characteristic table.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Pin LLP
NS Package Number SQA16A

Notes

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