P-Channel JFETs

2N5460 SST5460
2N5461 SST5461
2N5462 SST5462

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_{DSS} Min (mA)
2N/SST5460	0.75 to 6	40	1	–1
2N/SST5461	1 to 7.5	40	1.5	–2
2N/SST5462	1.8 to 9	40	2	–4

FEATURES

- High Input Impedance
- Very Low Noise
- High Gain: A_V = 80 @ 20 μA
- Low Capacitance: 1.2 pF Typical

BENEFITS

- Low Signal Loss/System Error
- High System Sensitivity
- High-Quality Low-Level Signal Amplification

APPLICATIONS

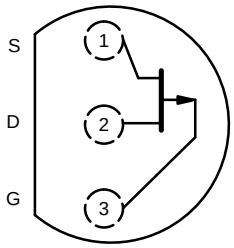
- Low-Current, Low-Voltage Amplifiers
- High-Side Switching
- Ultrahigh Input Impedance Pre-Amplifiers

DESCRIPTION

The 2N/SST5460 series are p-channel JFETs designed to provide all-around performance in a wide range of amplifier and analog switch applications.

The 2N series, TO-226AA (TO-92), and SST series, TO-236 (SOT-23), plastic packages provide low cost options, and are available in tape-and-reel for automated assembly, (see Packaging Information).

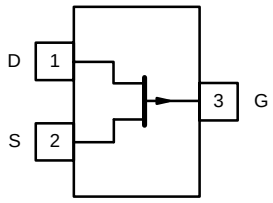
TO-226AA
(TO-92)



2N5460
2N5461
2N5462

Top View

TO-236
(SOT-23)



SST5460 (B0)*
SST5461 (B1)*
SST5462 (B2)*

*Marking Code for TO-236

Top View

ABSOLUTE MAXIMUM RATINGS

Gate-Drain Voltage . . . . . 40 V
Gate-Source Voltage . . . . . 40 V
Gate Current . . . . . –10 mA
Storage Temperature . . . . . –65 to 150°C
Operating Junction Temperature . . . . . –55 to 150°C

Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Power Dissipation[a] . . . . . 350 mW

Notes
a. Derate 2.8 mW/°C above 25°C

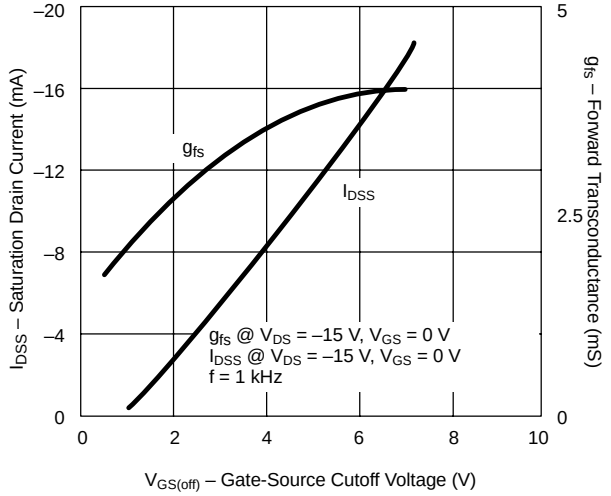
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions		Typ[a]	Limits 2N/SST5460 Min	2N/SST5460 Max	2N/SST5461 Min	2N/SST5461 Max	2N/SST5462 Min	2N/SST5462 Max	Unit
Static											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 10 μA , V_{DS} = 0 V		55	40		40		40		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –15 V, I_D = –1 μA			0.75	6	1	7.5	1.8	9	
Saturation Drain Current[b]	I_{DSS}	V_{DS} = –15 V, V_{GS} = 0 V			–1	–5	–2	–9	–4	–16	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V		0.003		5		5		5	nA
			T_A = 100°C	0.0003		1		1		1	μA
Gate Operating Current	I_G	V_{DG} = –20 V, I_D = –0.1 mA		3							pA
Drain Cutoff Current	$I_{D(off)}$	V_{DS} = –15 V, V_{GS} = 10 V		–5							
Gate-Source Voltage	V_{GS}	V_{DS} = –15 V	I_D = –0.1 mA	1.3	0.5	4					V
			I_D = –0.2 mA	2.3			0.8	4.5			
			I_D = –0.4 mA	3.8					1.5	6	
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = –1 mA , V_{DS} = 0 V		–0.7							
Dynamic											
Common-Source Forward Transconductance	g_{fs}	V_{DS} = –15 V, V_{GS} = 0 V f = 1 kHz			1	4	1.5	5	2	6	mS
Common-Source Output Conductance	g_{os}					75		75		75	μS
Common-Source Reverse Transfer Capacitance	C_{iss}	V_{DS} = –15 V, V_{GS} = 0 V f = 1 MHz	2N	4.5		7		7		7	pF
			SST	4.5							
Common-Source Reverse Transfer Capacitance	C_{rss}			1.2							
Common-Source Output Capacitance	C_{oss}		2N	1.5		2		2		2	
			SST	1.5							
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = –15 V, V_{GS} = 0 V f = 100 Hz	2N	15		115		115		115	nV/√Hz
			SST	15							
Noise Figure	NF	V_{DS} = –15 V, V_{GS} = 0 V f = 100 Hz, R_G = 1 MΩ BW = 1 Hz	2N	0.2		2.5		2.5		2.5	dB
			SST	0.2							

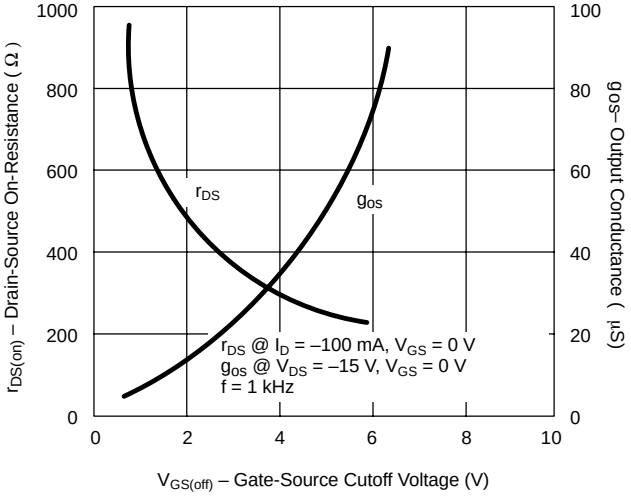
Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. PSCIB
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

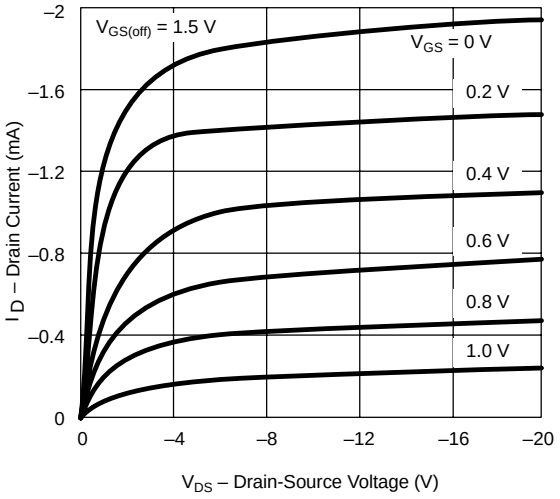
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



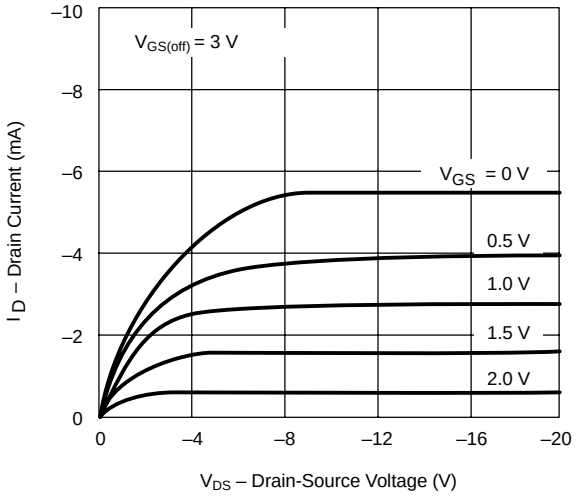
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



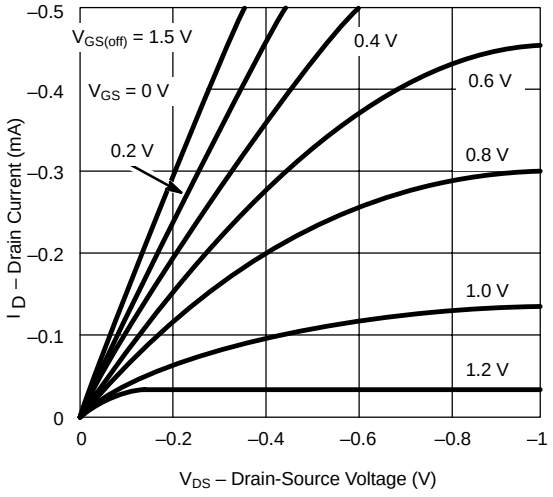
Output Characteristics



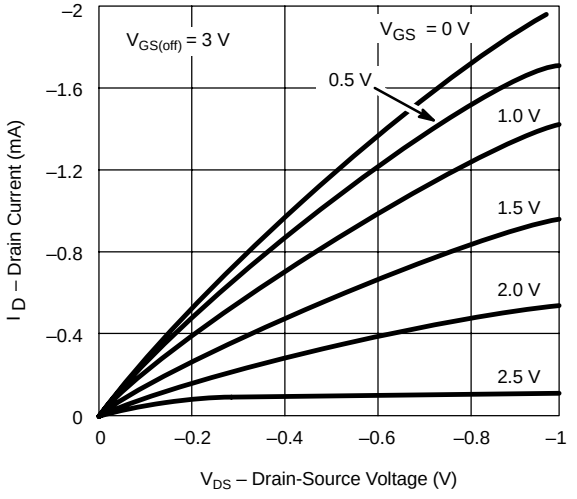
Output Characteristics



Output Characteristics

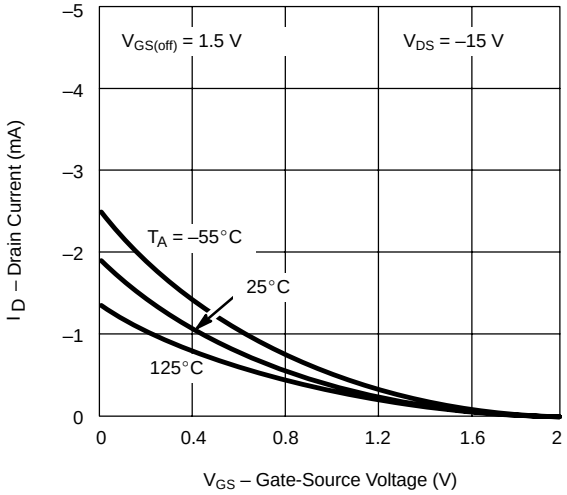


Output Characteristics

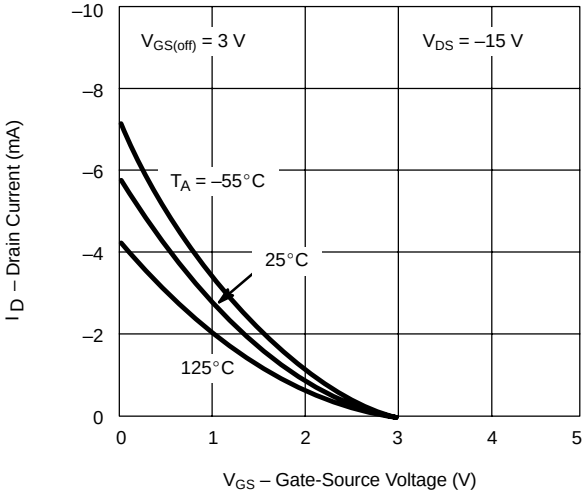


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

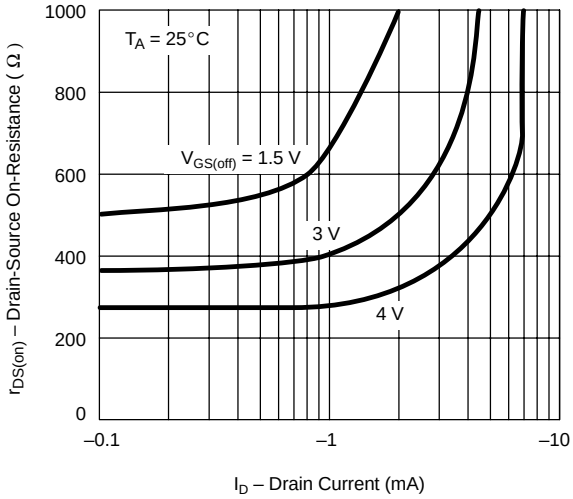
Transfer Characteristics



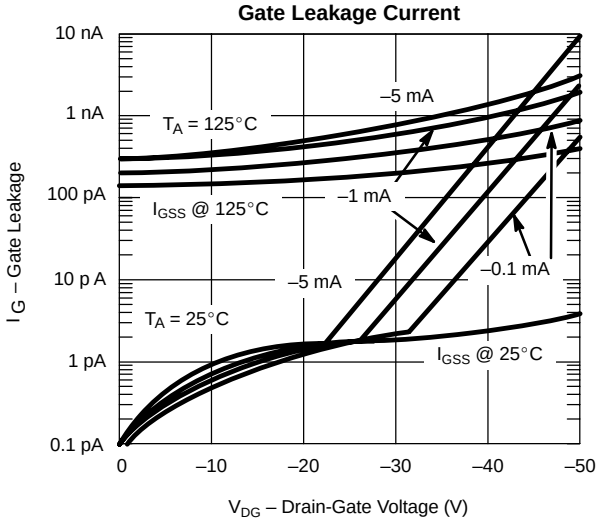
Transfer Characteristics



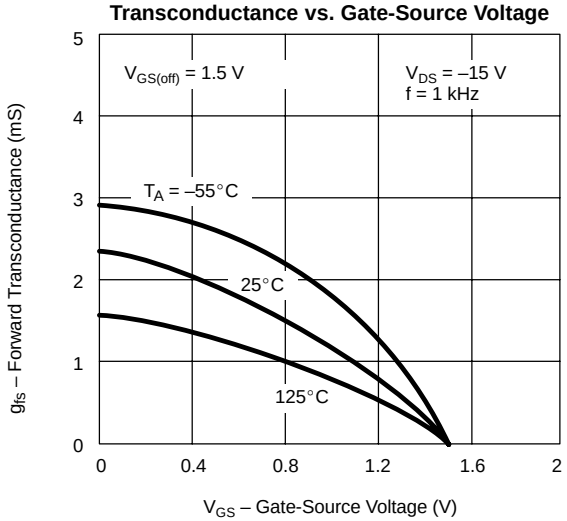
On-Resistance vs. Drain Current



Gate Leakage Current



Transconductance vs. Gate-Source Voltage



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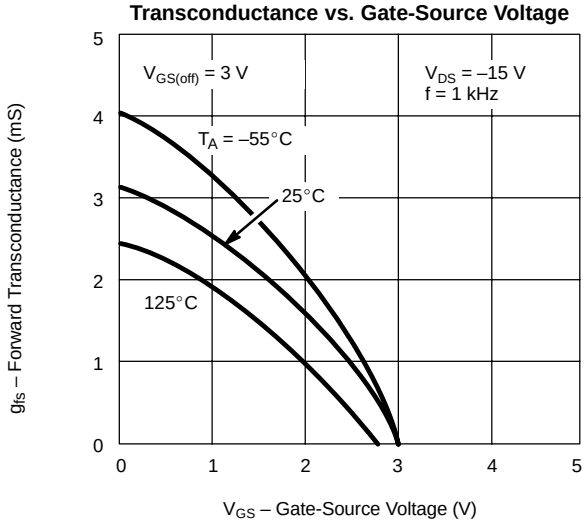
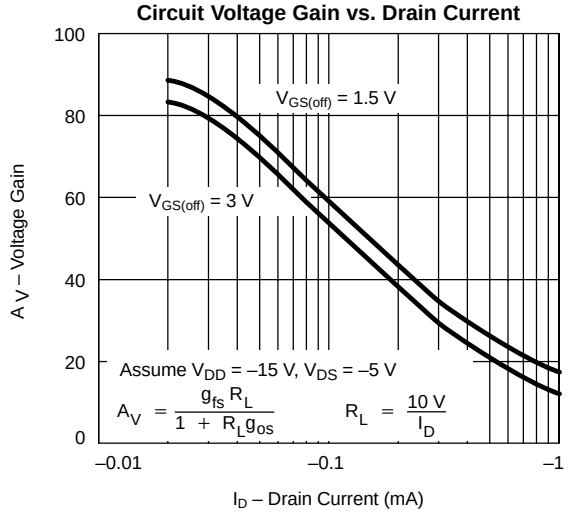
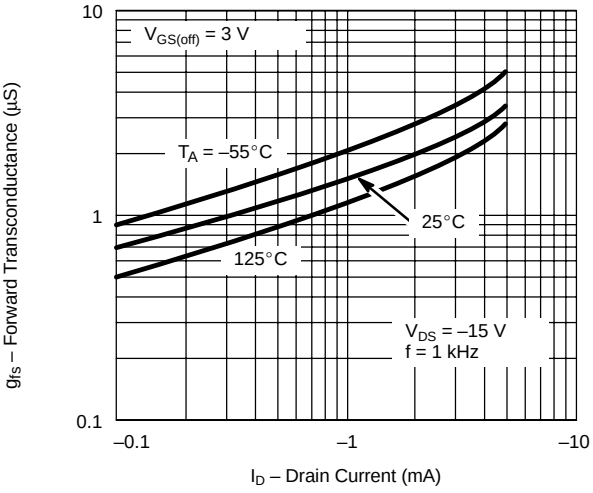


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

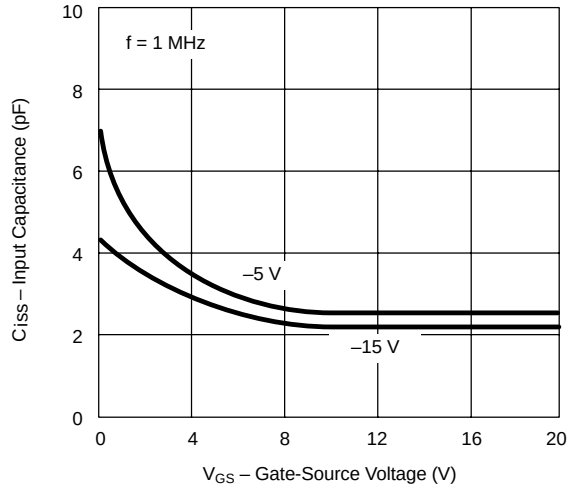
Circuit Voltage Gain vs. Drain Current



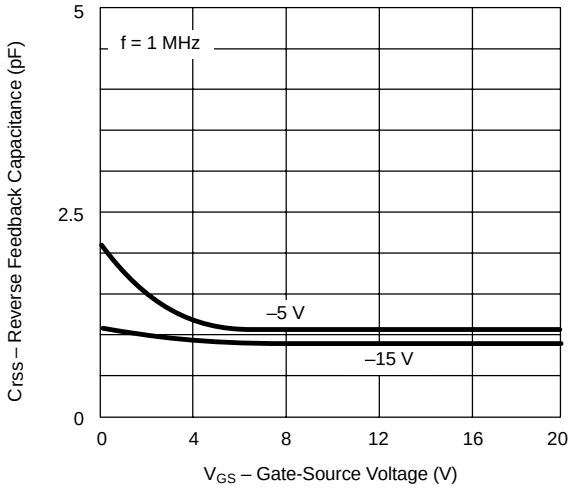
Common-Source Forward Transconductance vs. Drain Current



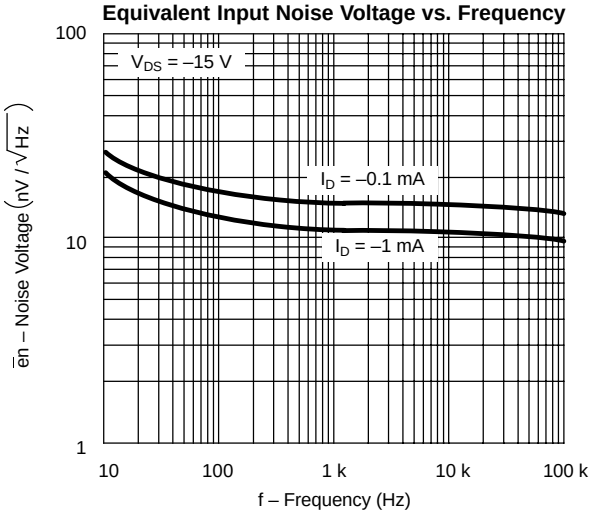
Common-Source Input Capacitance vs. Gate-Source Voltage



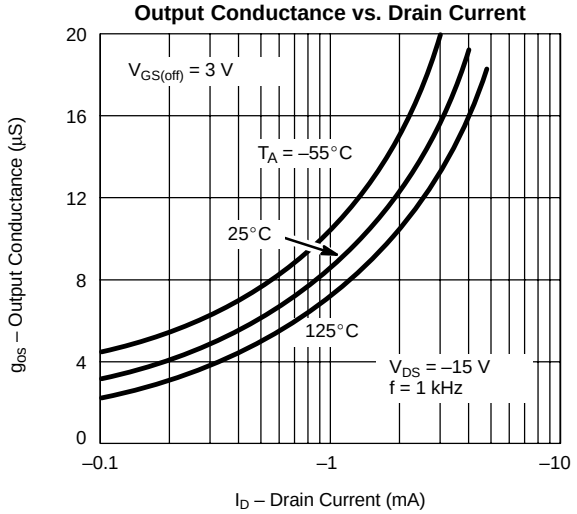
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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