

## N-Channel JFETs

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$r_{DS(on)}$ Max ( $\Omega$ )	$I_{D(off)}$ Typ (pA)	$t_{ON}$ Typ (ns)
J105	-4.5 to -10	3	10	14
J106	-2 to -6	6	10	14
J107	-0.5 to -4.5	8	10	14

### FEATURES

- Low On-Resistance: J105 < 3  $\Omega$
- Fast Switching— $t_{ON}$ : 14 ns
- Low Leakage: 10 pA
- Low Capacitance: 20 pF
- Low Insertion Loss

### BENEFITS

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error,” Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

### APPLICATIONS

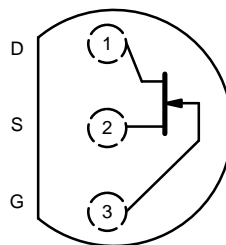
- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters

### DESCRIPTION

The J105/106/107 are high-performance JFET analog switches designed to offer low on-resistance and fast switching.  $r_{DS(on)} < 3 \Omega$  is guaranteed for the J105 making this device the lowest of any commercially available JFET.

The low cost TO-226AA (TO-92) plastic package is available in a wide range of tape-and-reel options (see Packaging Information). For similar products in TO-206AC (TO-52) packaging, see the U290/291 data sheet.

TO-226AA  
(TO-92)



Top View

### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage ..... -25 V  
 Gate Current ..... 50 mA  
 Storage Temperature ..... -55 to 150°C  
 Operating Junction Temperature ..... -55 to 150°C

Power Dissipation<sup>a</sup> ..... 350 mW

Notes  
 a. Derate 2.8 mW/°C above 25°C

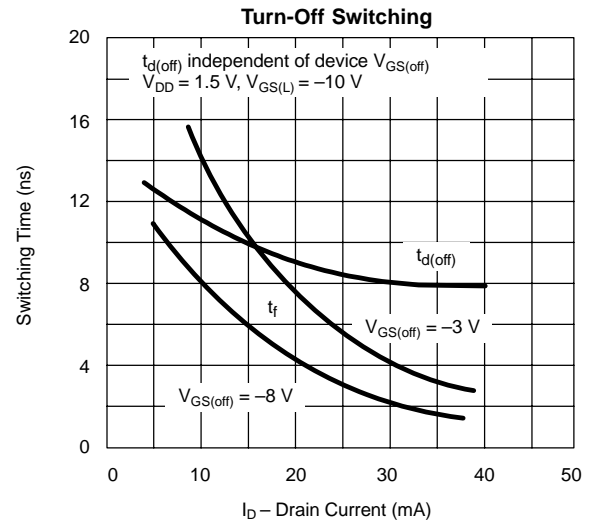
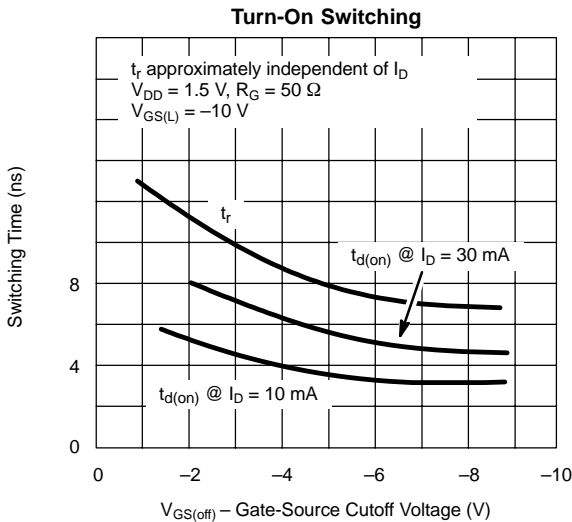
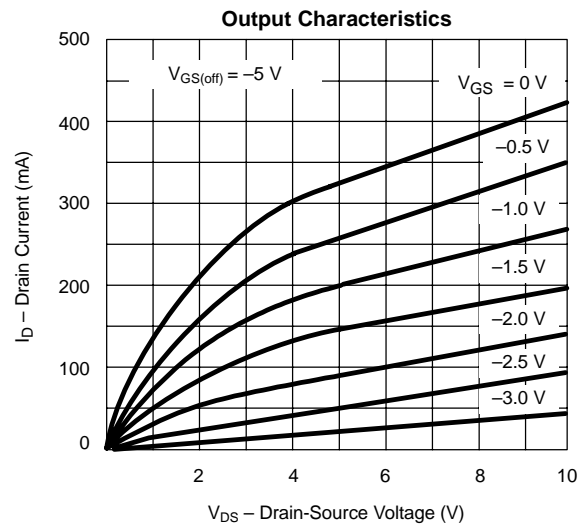
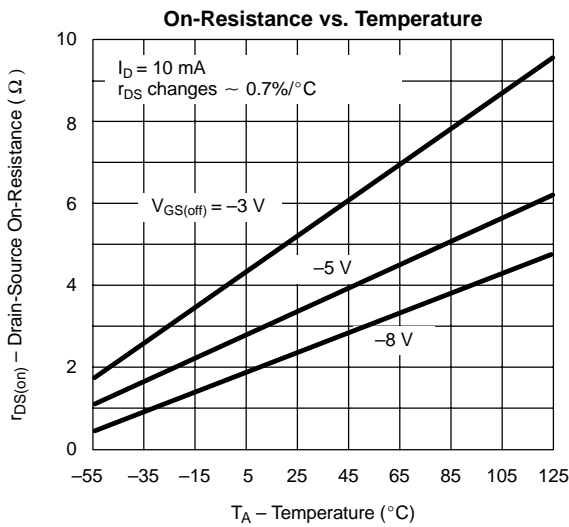
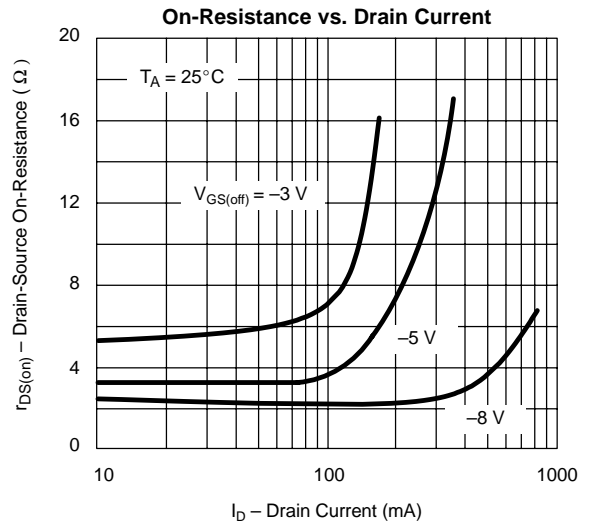
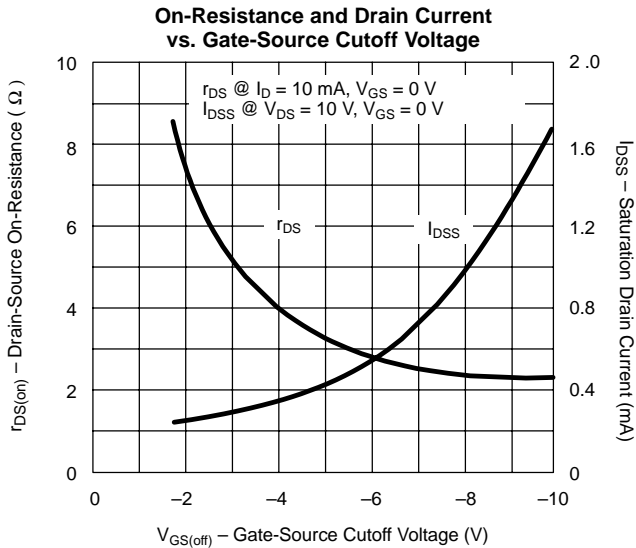
SPECIFICATIONS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ <sup>a</sup>	Limits						Unit
				J105		J106		J107		
				Min	Max	Min	Max	Min	Max	
<b>Static</b>										
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 1 μA		-4.5	-10	-2	-6	-0.5	-4.5	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V		500		200		100		mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0 V								nA
			T <sub>A</sub> = 125 °C	-10						
Gate Operating Current <sup>b</sup>	I <sub>G</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 25 mA	-0.01							nA
Drain Cutoff Current	I <sub>D(off)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = -10 V								nA
			T <sub>A</sub> = 125 °C	0.01		3		3		
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA			3		6		8	Ω
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = 1 mA, V <sub>DS</sub> = 0 V	0.7							V
<b>Dynamic</b>										
Common-Source Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 25 mA f = 1 kHz	55							mS
			5							
Common-Source Output Conductance <sup>b</sup>	g <sub>os</sub>									
Drain-Source On-Resistance	r <sub>ds(on)</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 0 mA f = 1 kHz			3		6		8	Ω
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 0 V f = 1 MHz	120		160		160		160	pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -10 V f = 1 MHz	20		35		35		35	
Equivalent Input Noise Voltage	e <sub>n</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 25 mA f = 1 kHz	3							nV/ √Hz
<b>Switching</b>										
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 1.5 V, V <sub>GS(H)</sub> = 0 V See Switching Diagram	6							ns
	t <sub>r</sub>		8							
Turn-Off Time	t <sub>d(off)</sub>		5							
	t <sub>f</sub>		9							

Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

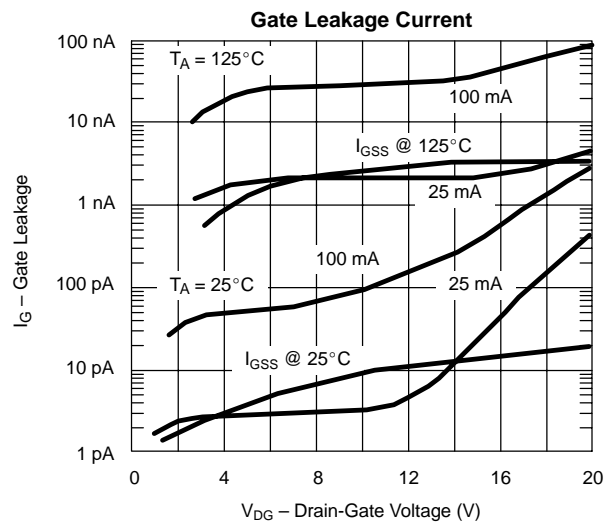
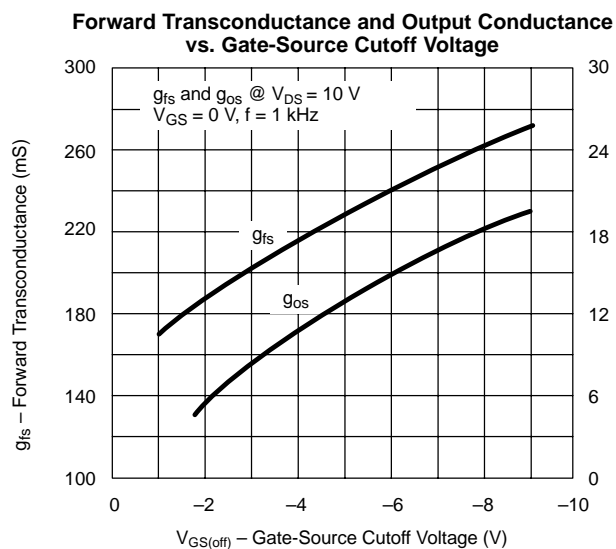
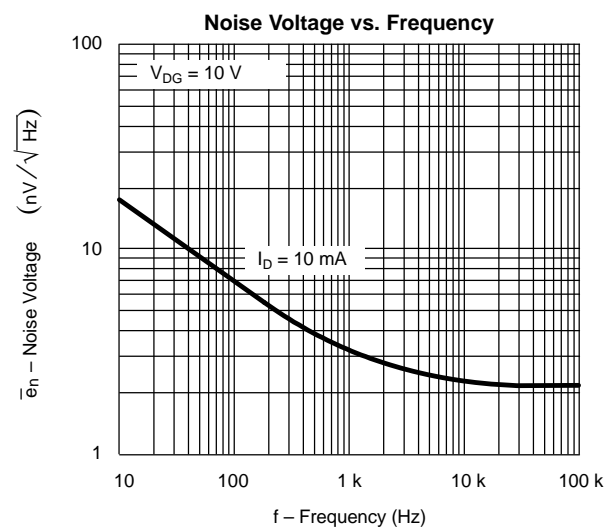
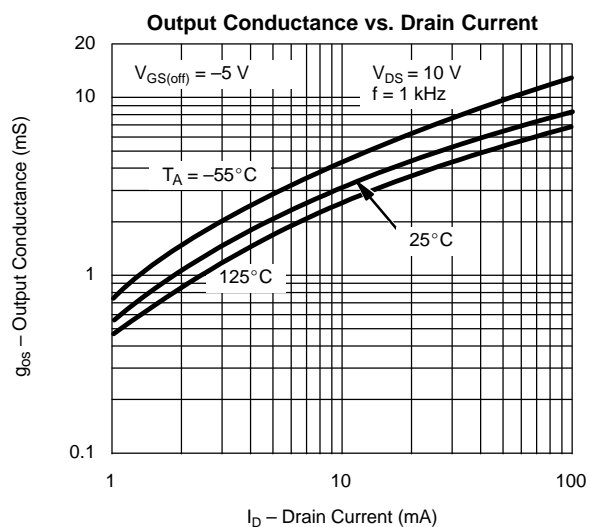
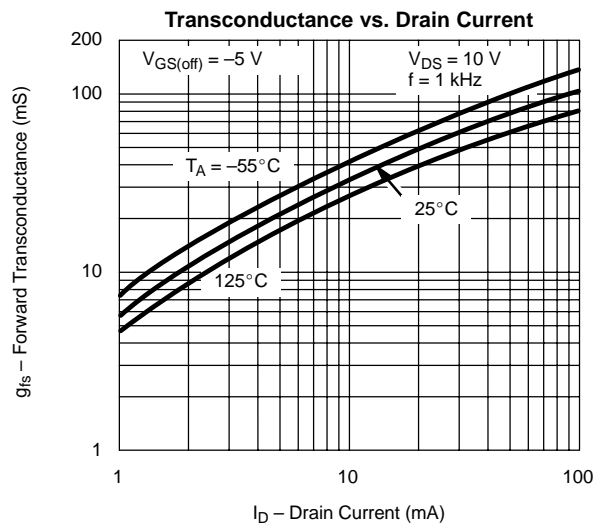
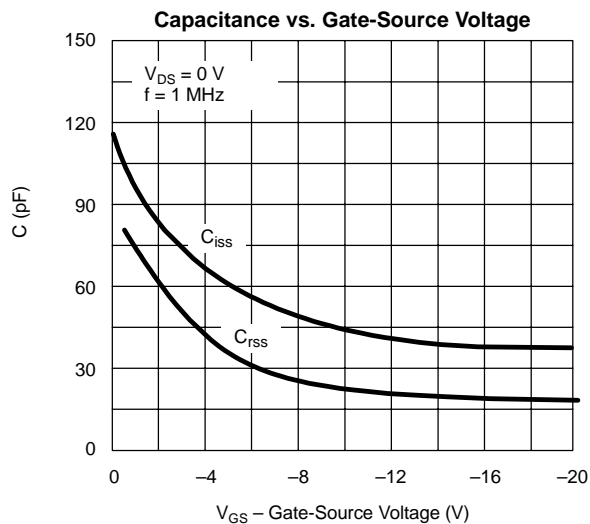
NVA

**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)**





### TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



<b>SWITCHING TIME TEST CIRCUIT</b>			
	<b>J105</b>	<b>J106</b>	<b>J107</b>
$V_{GS(L)}$	-12V	-7V	-5V
$R_L^*$	50 $\Omega$	50 $\Omega$	50 $\Omega$
$I_{D(on)}$	28 mA	27 mA	26 mA

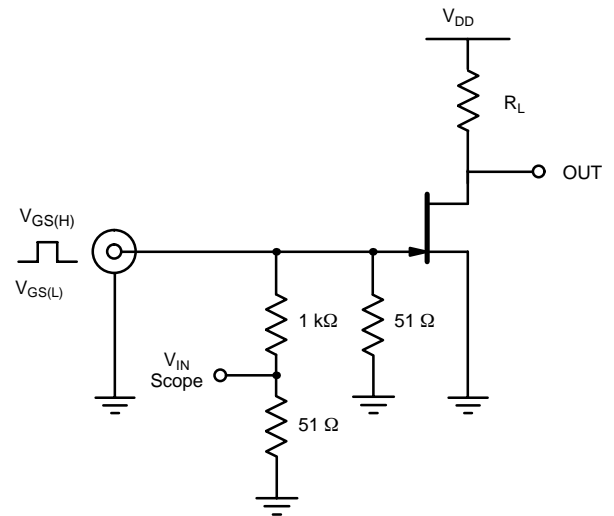
\*Non-inductive

**Input Pulse**

Rise Time < 1 ns  
 Fall Time < 1 ns  
 Pulse Width 100 ns  
 PRF 1 MHz

**Sampling Scope**

Rise Time 0.4 ns  
 Input Resistance 10 M $\Omega$   
 Input Capacitance 1.5 pF





## Disclaimer

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